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(NASA-Case-ERC-10285) PHASE CONTROL CIRCUITS USING FREQUENCY MULTIPLICATIONS FOR PHASED ARRAY ANTENNAS Patent (NASA) 13 p CSCL 09C 00/10 Unclas 52690

REPLY TO ATTN OF: GP

TO: KSI/Scientific & Technical Information Division
Attention: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General Counsel for Patent Matters

SUBJECT: Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U.S. Patent No. : 3,710,329

Government or Corporate Employee : U.S. Government

Supplementary Corporate Source (if applicable) :

NASA Patent Case No. : ERC-10285

NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

Yes ☐ No ☒

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 1 of the Specification, following the words ". . . with respect to an invention of . . ."

Elizabeth A. Carter

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Enclosure
Copy of Patent cited above

United States Patent [19]

Mailloux et al.

[11] **3,710,329**

[45] **Jan. 9, 1973**

[54] PHASE CONTROL CIRCUITS USING FREQUENCY MULTIPLICATION FOR PHASED ARRAY ANTENNAS

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[22] Filed: **July 16, 1970**

[21] Appl. No.: **55,333**

[52] **U.S. Cl.** .....**343/100 SA**, 331/45, 343/100 R, 343/853

[51] **Int. Cl.**.....**H01q 3/26**

[58] **Field of Search** .....343/100 R, 100 SA, 853; 331/45

[56] **References Cited**

UNITED STATES PATENTS

2,920,284	1/1960	Beagles et al.	331/45
3,501,764	3/1970	Mailloux et al.	343/100 R

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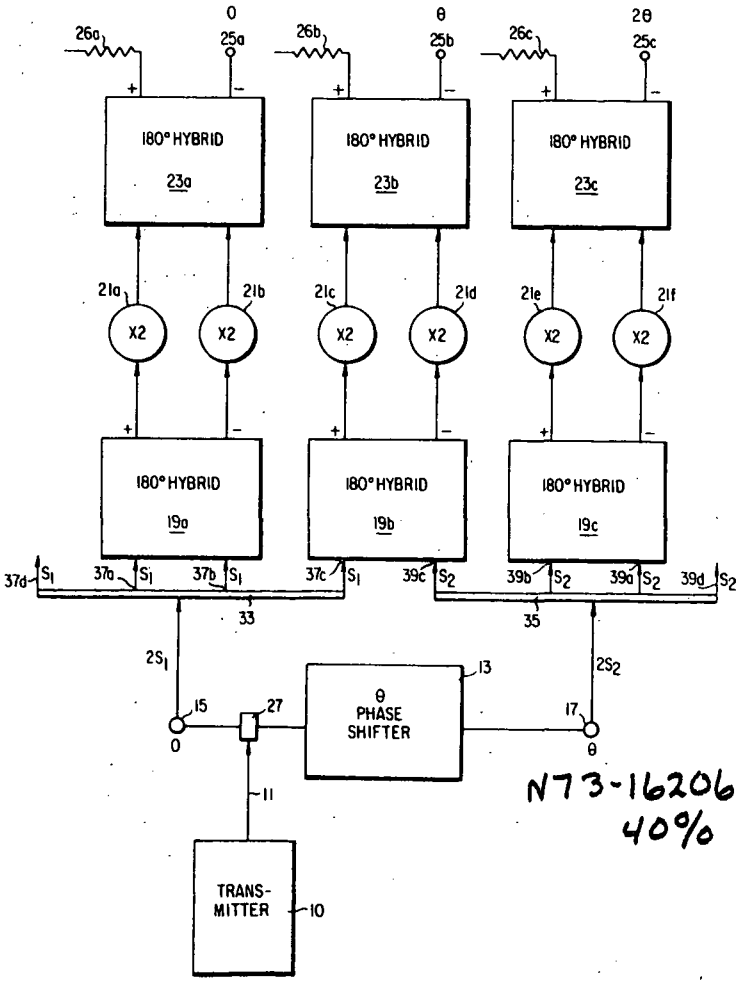
[57] **ABSTRACT**

The disclosure describes a phase control coupling circuit for use with a phased array antenna. The coupling circuit includes a combining circuit which is coupled to a transmission line, a frequency multiplier circuit which is coupled to the combining circuit, and a recombining circuit which is coupled between the frequency multiplier circuit and phased array antenna elements. In a "doubler" embodiment, the frequency multiplier circuit comprises frequency doublers and the combining and recombining circuits comprise four-port hybrid power dividers. In a generalized embodiment, the multiplier circuit comprises frequency multiplier elements which multiply to the *N*th power, the combining circuit comprises four-port hybrid power dividers, and the recombining circuit comprises summing circuits. In a quadrupler embodiment, the multiplier circuit comprises frequency quadrupler elements, the combining circuit comprises four-port hybrid power dividers and the recombining circuit comprises two levels of four-port hybrid power dividers.

13 Claims, 5 Drawing Figures



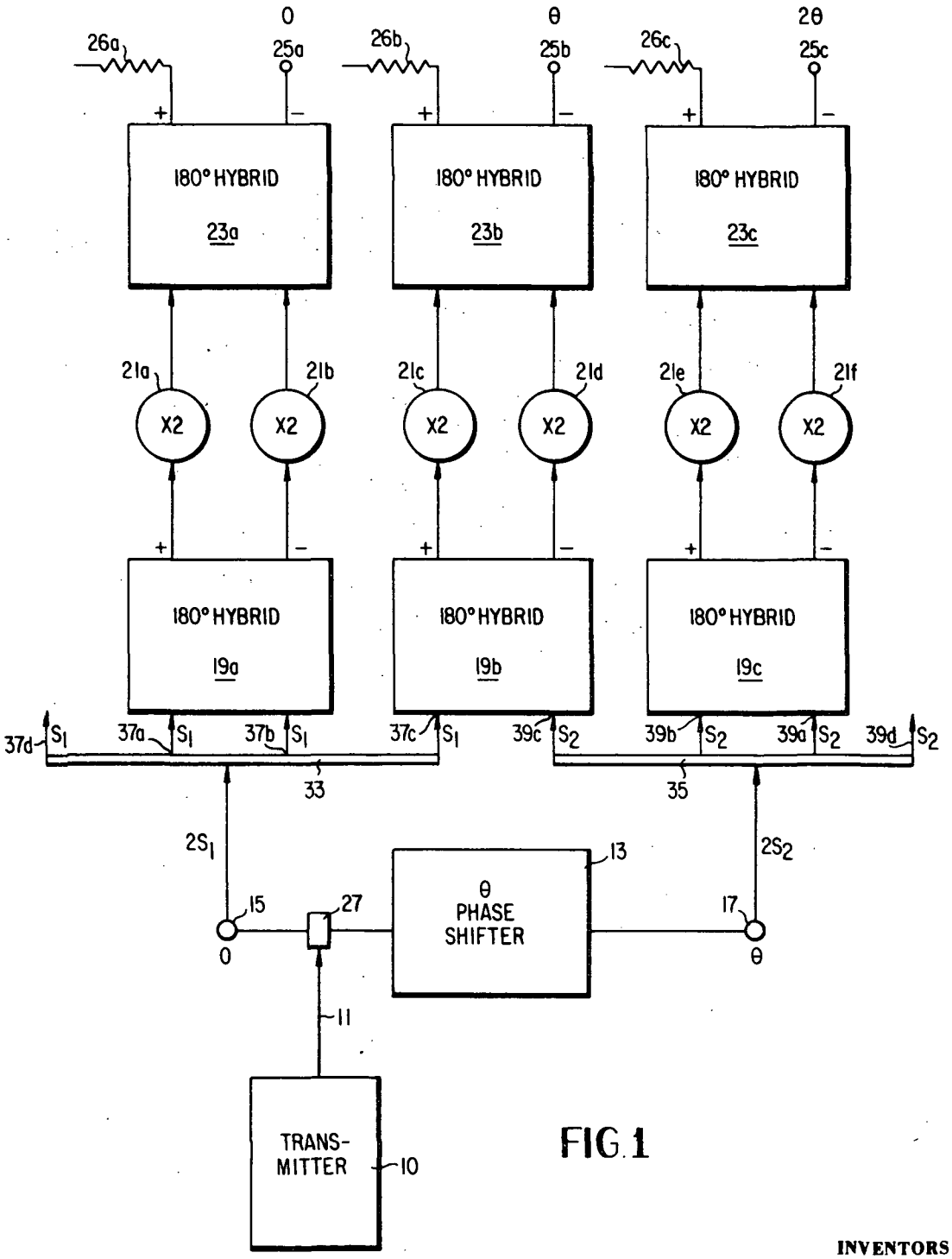


FIG. 1

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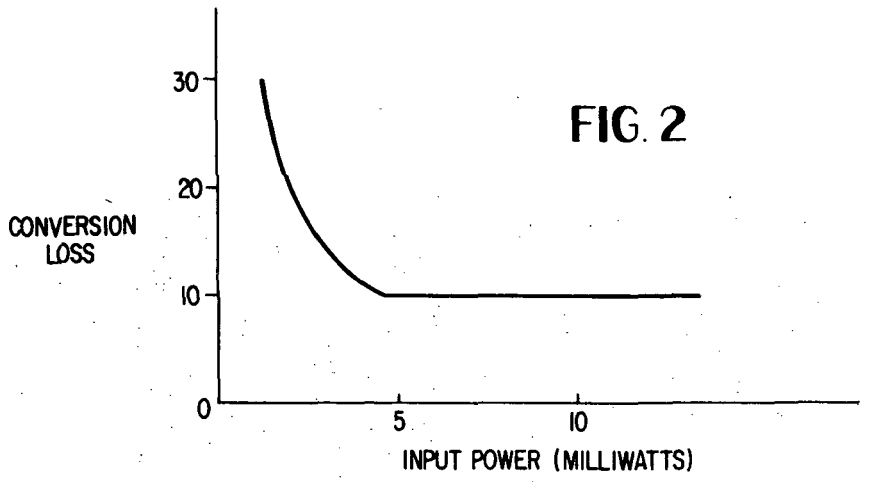
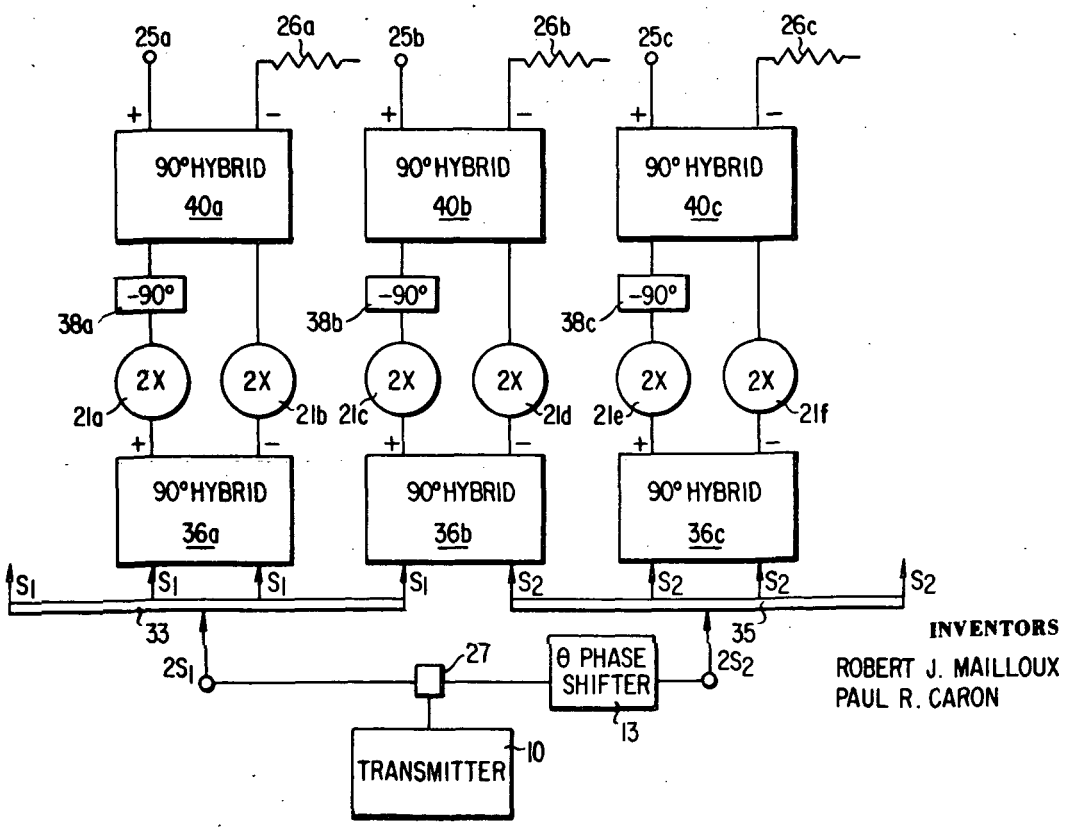


FIG. 2

FIG. 3



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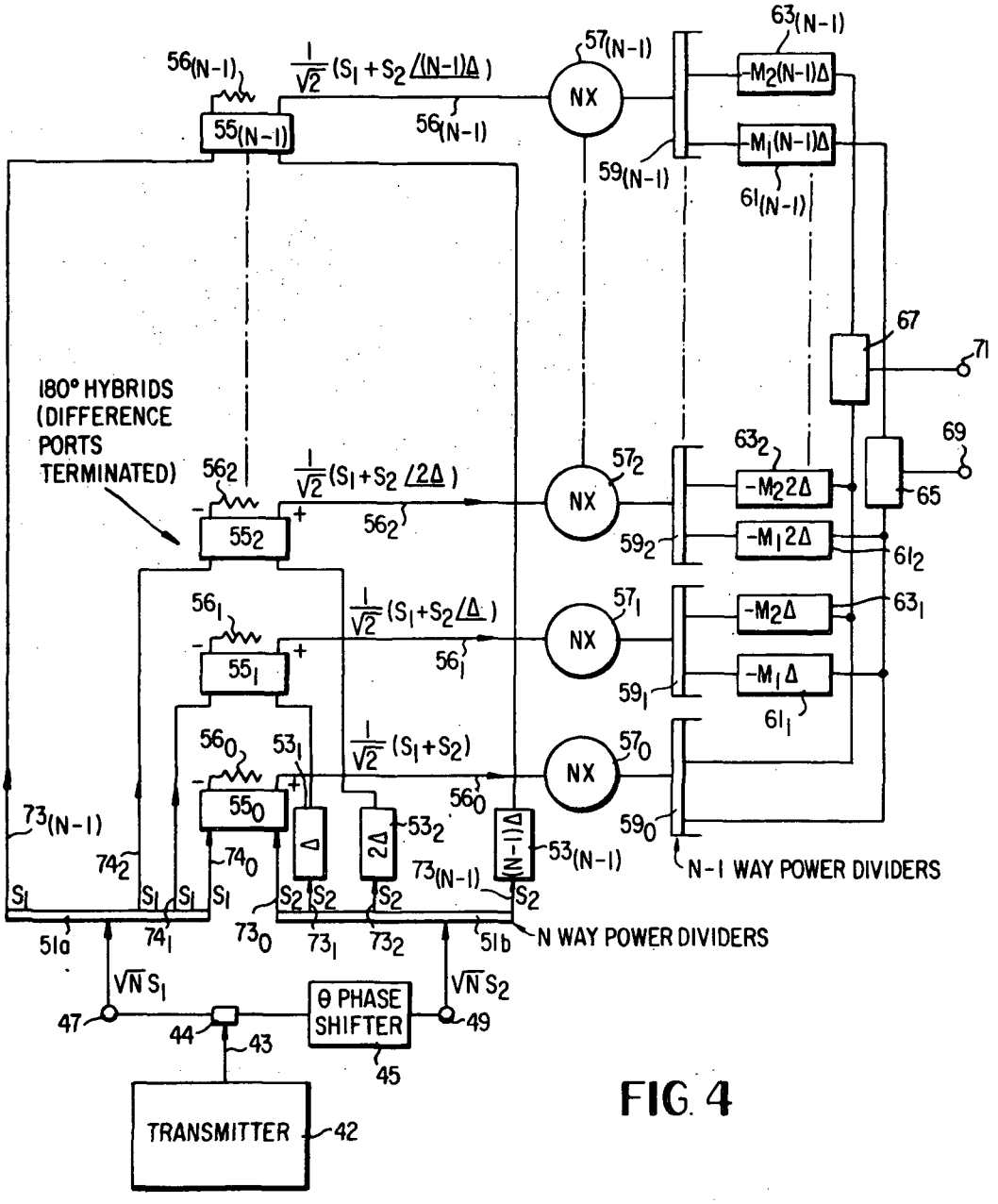

FIG. 4

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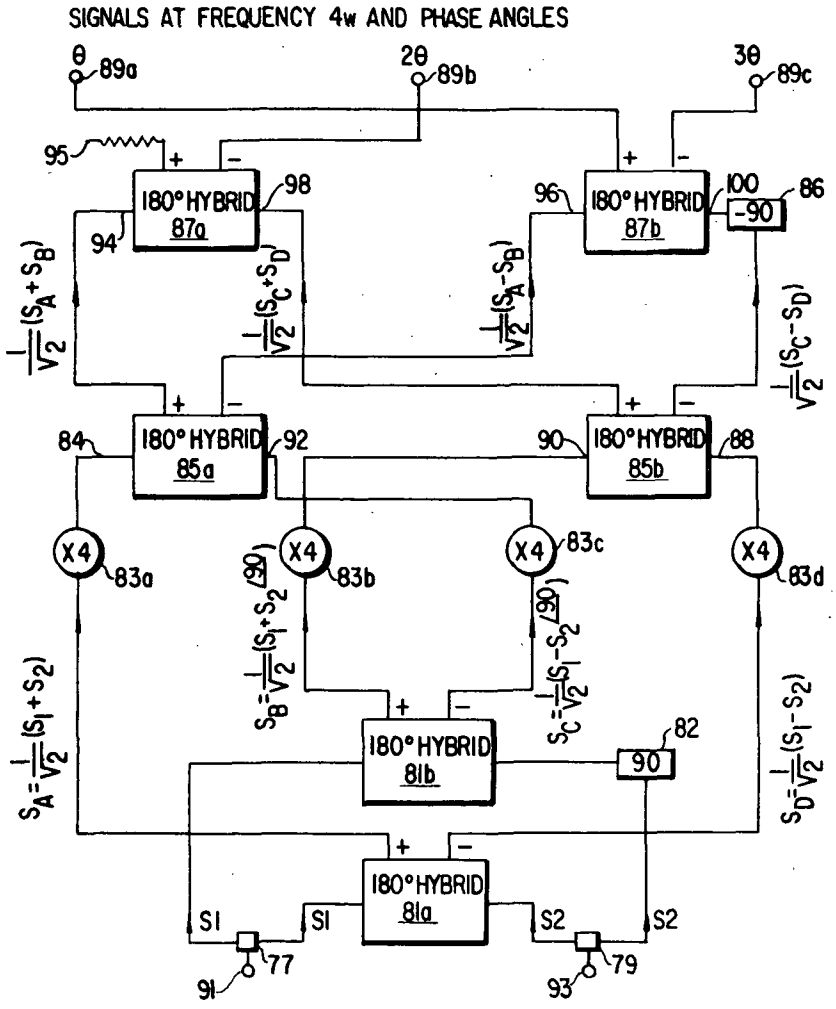

FIG. 5

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PHASE CONTROL CIRCUITS USING FREQUENCY MULTIPLICATION FOR PHASED ARRAY ANTENNAS

ORIGIN OF THE INVENTION

BACKGROUND OF THE INVENTION

This invention relates generally to the art of coupling circuits used for phasing signals. More particularly, this invention relates to the art of phase control coupling circuits for phased array antennas.

In recent years, phased array antennas have been used with increasing frequency, particularly phased array antennas employing high frequency antenna elements such as slot antenna elements. A phased array antenna normally comprises a matrix of antenna elements which are arranged according to a pattern; for example, some phased array antenna elements are arranged in crossed columns to form a square. Each antenna element in a phased array antenna usually handles a signal which is phase shifted from the signals handled by other antenna elements in the array. The reason for this is that a combined radiation field developed by a phased array antenna at a distant point is the vector sum of radiation fields produced by individual antenna elements in the phased array. By properly controlling the respective phases of signals handled by phased array antenna elements, it is possible to concentrate a combined radiation field very strongly in a desired direction. To do this, however, requires high accuracy of phase control between individual antenna elements.

Phase control of a phased array antenna is normally accomplished by an antenna coupling circuit. That is, a transmitter or a receiver, depending on whether the system is transmitting or receiving, is coupled to the antenna elements of the phased array antenna through a power dividing chain which has phase shifting elements connected at some point or points in it. Many prior art phase controllers employ phase shifters connected at the ends of power dividing chains, prior to their connections with the antenna elements. An example of such a phase control coupling circuit is disclosed in U.S. Pat. No. 3,480,958 to Tcheditch. Other prior art phase controllers involve phase shifters connected in series along power dividing chains. An example of this type phase controller is found in U.S. Pat. No. 3,255,450 to Butler. The major difficulty with such phase control coupling circuits is that they are not accurate enough. When a phase shifter is connected at each antenna element, the phase shifter must be coordinated with other phase shifters to achieve the proper phase coordination between the antenna elements. When phase shifters are connected in series in power dividing chains, there is an additional problem in that errors are cumulative as signals travel along the power dividing chains.

Some sophisticated phase control circuits provide relatively accurate phase control, such as the system described by Johnson in an article "Phased-Array Beam Steering by Multiplex Sampling," Proceedings of the IEEE, Vol. 56, No. 11, pp. 1,801–1,811, November 1968. The difficulty with most such systems is that they require relatively expensive and generally "nonstandarized" components.

It is therefore an object of this invention to provide a novel phase control coupling circuit suitable for use with a phased array antenna.

It is a further object of this invention to provide a phase control coupling circuit which is accurate.

It is still a further object of this invention to provide a phase control coupling circuit which is relatively inexpensive.

It is yet another object of this invention to provide a phase control coupling circuit which is relatively uncomplicated and is generally composed of standardized components.

SUMMARY OF THE INVENTION

In accordance with the principles of this invention, a phase control coupling circuit suitable for use with a phased array antenna is provided. The antenna may be operating in either a transmitting or receiving mode. The phase control coupling circuit of the invention employs frequency multiplying elements to create multiplied signals (assuming the system is transmitting). The phase control coupling circuit then separates out, from these multiplied signals, antenna element signals which have desirable phase angles and respectively feeds them to the antenna elements of the phased array antenna.

More particularly, the phase control coupling circuit of the invention employs a first combining circuit which receives two signals (one signal having a zero phase angle and the other signal having a θ phase angle) from a transmission line (assuming the system is transmitting), subdivides these signals into two groups of smaller signals, and combines the smaller signals in various ways so as to create a plurality of combined signals. Frequency multiplying elements respectively multiply each of the combined signals by a multiple N thereby creating a plurality of the combined signals. A recombining circuit recombines the "multiplied combined signals" in such a manner as to separate out signals which have phase angles equal to integers of N times θ. Thus, a phase control coupling circuit employing the principles of this invention receives two signals separated by a phase angle and emits more than two signals which are separated from one another by highly accurate incremental phase angles.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of this invention will become more apparent from the following more particular description of the preferred embodiments of the invention illustrated in the accompanying drawings wherein:

FIG. 1 is a block diagram of an antenna system which utilizes a doubler phase control circuit employing the principles of this invention;

FIG. 2 is a graphical representation of a conversion loss characteristic similar to conversion loss characteristics of many commercially available doublers;

FIG. 3 is a block diagram of an antenna system which utilizes another doubler phase control circuit employing the principles of this invention;

FIG. 4 is a block diagram of an antenna system which utilizes a generalized phase control circuit employing the principles of this invention; and,

FIG. 5 is a block diagram of an antenna system which utilizes a quadrupler phase control circuit employing the principles of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

For clarity and convenience of description, the invention is firstly described below in a relatively uncomplicated embodiment (doubler phase control circuit), secondly in a more generalized embodiment (generalized phase control circuit), and thirdly, in a particularized embodiment (quadrupler phase control circuit). Also, throughout the following description, it is assumed, for ease of description, that the phase control circuits are used to couple "transmitters" to phased array antennas; however, it should be understood that phase control circuits employing the principles of this invention can be used to couple "receivers" to phased array antennas as well as transmitters.

DOUBLER PHASE CONTROL CIRCUIT

FIG. **1** illustrates a "doubler" phase control circuit employing the principles of this invention. Essentially, the doubler phase control circuit shown in FIG. **1** receives two phase shifted transmitter signals and emits three phase shifted antenna element signals (assuming the phase control circuit shown is being used with a transmitting system). The phase control circuit accomplishes this by combining the two transmitter signals in various ways, doubling the combined signals, and then separating out, from the doubled combined signals, signals having the desired phase angles.

Referring now to FIG. **1**, there is shown a transmitter circuit comprising: a transmitter **10**; a two-way power divider **27**; and a θ phase shifter **13**. The transmitter circuit feeds a doubler phase control coupling circuit which comprises: left and right multi-output power dividers **33** and **35**; three combining **180°** hybrids **19***a–c;* six frequency doublers **21***a–f;* and three recombining 180° hybrids **23***a–c*. The recombining 180° hybrids **23***a–c*, respectively feed antenna elements **25***a–c*.

A signal applied by the transmitter **10** on transmitter line **11** passes through the two-way power divider **27** and a θ phase shifter **13** to a right terminal **17** and through the two-way power divider **27** to a left terminal **15**. Thus, a signal $2S_1$ which has a zero relative phase shift appears on the left terminal **15**, and a signal $2S_2$ which has a θ relative phase shift appears on the right terminal **17**. The signals, $2S_1$ and $2S_2$, are fed into the left and right multi-output dividers **33** and **35** and these power dividers respectively provide outputs S_1 and S_2. In the embodiment illustrated in FIG. **1**, the multi-output power dividers **33** and **35** are four-way power dividers and their input to output amplitude ratios are **2**, i.e., $\sqrt{4}$; thus, their input signals are designated as $2S_1$, $2S_2$ and their output signals are designated as S_1, S_2. Signals S_1 appearing at first, second and third outputs **37***a–c* of the left multi-output power divider **33** are respectively connected to first and second inputs of a first combining 180° hybrid **19***a* and to a first input of a second combining 180° hybrid **19***b*. Signals S_2 appearing at first, second and third outputs **39***a–c* of the right multi-output power divider **35** are respectively connected to first and second inputs of a third combining 180° hybrid **19***c* and to a second input of the second combining 180° hybrid **19***b*. Signals appearing at a fourth output **37***d* of the left multi-output power divider **33** and a fourth output **39***d* of the right multi-output power divider **35** are used to feed additional output signals S_1 and S_2 to additional combining hybrids which, for simplicity, are not shown.

The combining 180° hybrids **19***a–c* each have a sum port, which are represented in FIG. **1** by "plus" symbols, and a difference port, which are represented in FIG. **1** by "minus" symbols. The output signals appearing at the sum and difference ports of the first combining 180° hybrid **19***a* are respectively connected, through first and second frequency doublers **21***a* and **21***b* to separate inputs of a first recombining 180° hybrid **23***a*. The output signals appearing at the sum and difference ports of the second combining 180° hybrid **19***b* are respectively connected, through third and fourth frequency doublers **21***c* and **21***d*, to separate inputs of a second recombining 180° hybrid **23***b*. The output signals appearing at sum and difference ports of the third combining 180° hybrid **19***c* are respectively connected, through fifth and sixth frequency doublers **21***e* and **21***f*, to separate inputs of a third recombining 180° hybrid **32***c*. The difference ports of the three recombining 180° hybrids **23***a–c* respectively feed active antenna elements **25***a–c*. The sum ports of the recombining 180° hybrids **23***a–c* are applied to terminating resistors **26***a–c*.

Effectively, the doubler phase control circuit receives two signals, $2S_1$ and $2S_2$, $2S_2$ being separated from $2S_1$ by a phase angle of θ; subdivides these signals, $2S_1$ and $2S_2$ into two groups of smaller signals S_1 and S_2; combines these smaller signals in various ways (i.e., by summing and subtracting) in the combining 180° hybrids **19***a–c;* doubles the combined signals using the frequency doublers **21***a–f;* recombines the doubled-combined signals in the recombining 180° hybrids **23***a–c* and thereby separates out three signals, one each at the respective antenna elements **25***a–c*, the first having a zero phase angle, the second a θ phase angle and the third a 2θ phase angle.

The theory involved in the operation of the doubler phase control circuit shown in FIG. **1** is hereinafter described. For ease of understanding, sine waves are used to trace the signals through the phase control circuit. Thus, equations which represent the signals from the outputs of the left and right four-way power dividers **33** and **35** are respectively expressed as:

$$S_1 = \cos \omega t \tag{1}$$

$$S_2 = \cos (\omega t + \theta) \tag{2}$$

where θ is the angular velocity of the signals S_1 and S_2 and θ is the angle by which S_2 leads S_1.

At the respective sum and difference ports of the combining 180° hybrid **19***b*, the signals are expressed by the following equations:

$$\text{sum signal} = (1/\sqrt{2})(S_1 + S_2) \quad (3)$$

$$\text{difference signal} = (1/\sqrt{2})(S_1 - S_2) \quad (4)$$

If the doublers are ideal, then the respective outputs of doublers **21***c* and **21***d* are proportional to the squares of the inputs or are proportional to $\frac{1}{2}(S_1 + S_2)^2$ and $\frac{1}{2}(S_1 - S_2)^2$. The difference term at the output of the recombining 180° hybrid **23***b* (which goes to the antenna element **25***b*) is similarly proportional to:

$$\sqrt{2}\, S_1 S_2 \quad (5)$$

The corresponding signal having a frequency of $2\omega t$ is expressed as follows:

$$(1/\sqrt{2})\cos(2\omega t + \theta). \quad (6)$$

The outputs of the difference ports for the recombining 180° hybrids feeding antenna elements **23***a* and **23***b* can be shown respectively to be:

$$(1/\sqrt{2})\cos(2\omega t) \text{ and} \quad (7)$$

$$(1/\sqrt{2})\cos(2\omega t + 2\theta) \quad (8)$$

Thus the doubler phase control coupler circuit shown in FIG. **1** provides three outputs, one each on the antenna elements **25***a–c*. Each of the signals has a frequency of $2\Phi t$, which is double the frequency of the input signals S_1 and S_2. The signal appearing at antenna element **25***a* has a zero relative phase shift, the signal appearing at antenna element **25***b* has a θ relative phase shift, and the signal appearing at antenna element **25***c* has a 2θ relative phase shift.

Generally, each of the combining 180° hybrids **19***a–c* combines two signals. Each of the frequency doublers **21***a–f* respectively doubles a combined signal, and each of the recombining 180° hybrids **23***a–c* respectively separate out a desired signal to be applied to an antenna element **25***a–c*.

Thus, the doubler phase control circuit shown in FIG. **1** provides phase shifted signals which are shifted one from the other by highly accurate increments. Further, this circuit employs standard interchangeable components and is relatively uncomplicated to construct.

A unique feature of the "doubler" phase control circuit of the invention is that it may be used even when the frequency doubler conversion loss is a variable function of power input. Many commercially available doublers have conversion loss characteristics similar to those shown in FIG. **2**. FIG. **2** is a plot of conversion loss vs. input power of a doubler. It can be seen in FIG. **2** that as input power drops below 5 milliwatts the conversion loss varies greatly. Normally, this conversion loss characteristic is important because when the relative phase angle θ between S_1 and S_2 is zero, all of the signal arrives at the sum port of the combining 180° hybrid **19***b* and no signal arrives at its difference port. Similarly, when θ equals 180°, all of the signal arrives at the difference port and none at the sum port. The power appearing at each doubler **21***c* and **21***d* is, therefore, a function of the phase angle θ. From this it appears that the conversion loss characteristics of the doublers **21***c* and *d* would cause a phase error and amplitude modulation of their output signals as a function of the phase angle between signals S_1 and S_2 when the power input is below 5 milliwatts. However, this is not so.

The foregoing advantage of the doubler phase control circuit of the invention will be better understood by the following technical analysis; assuming that the doublers are identical and have phase shift characteristics independent of power, the output signal of any of the doublers **21***a–f* whose input signal is S (where $S = |S| \cos(\omega t + \theta_s)$ and θ_s is the relative phase shift of S) can be expressed as:

$$S^2 A(|S|) \quad (9)$$

where $A(|S|)$ is a transmission factor for a doubler. Referring to FIG. **1** and plugging in the sum and difference signals obtained from the 180° hybrid **19***b*, the output from doubler **21***c* is therefore:

$$\tfrac{1}{2}(S_1+S_2)^2 A\left(\left|\frac{S_1+S_2}{\sqrt{2}}\right|\right) \quad (10)$$

and the output from doubler **21***d* is:

$$1/2(S_1-S_2)^2 A\left(\left|\frac{S_1-S_2}{\sqrt{2}}\right|\right) \quad (11)$$

The signal appearing at the antenna element **25***b* is 1/2 times the first of these minus the second. Combining these terms and writing the frequency components at 2ω, the following output signal is obtained:

$$\frac{1}{4\sqrt{2}}\left\{\left[A\left(\left|\frac{S_1+S_2}{\sqrt{2}}\right|\right) - A\left(\left|\frac{S_1-S_2}{\sqrt{2}}\right|\right)\right]\cos 2\omega t + \left[A\left(\left|\frac{S_1+S_2}{\sqrt{2}}\right|\right) - A\left(\left|\frac{S_1-S_2}{\sqrt{2}}\right|\right)\right]\cos(2\omega t + 2\theta) + 2\left[A\left(\left|\frac{S_1+S_2}{\sqrt{2}}\right|\right) + A\left(\left|\frac{S_1-S_2}{\sqrt{2}}\right|\right)\right]\cos(2\omega t + \theta)\right\} \quad (12)$$

The third term of this expression is the only term with a phase angle of θ, however, the resultant phase angle of the first two term is also θ because the bracketed portions of both these terms are identical. Moreover, it can be shown that the resultant signal of the first two terms varies as a function of power in such a manner as to substantially cancel out variations in the third term as a function of power input into the doublers. Thus, the output signal indicated above can be written as:

$$1/\sqrt{2}A(|r|)\cos(2\omega t + \theta) \quad (13)$$

where r varies between a maximum of 1.414 and a minimum of 1.0 (assuming that the input signals S_1 and S_2 have been normalized to 1.0). Hence, even if the signals S_1 and S_2 are in the range of saturation in the curve of FIG. **2**, the doubler phase control circuit will operate with essentially no phase error and only 3db of amplitude modulation even though the doublers' conversion losses differ considerably for changes in input power.

Another interesting feature of the doubler phase control circuit, as well as of all phase control circuits employing the principles of this invention, is that it "up-converts" a signal's frequency. That is, the phase control circuit receives a signal from a transmitter having a frequency of ω and emits signals at antenna elements **25***a–c* having frequencies of 2ω. Normally, the phase control circuits of this invention multiply the frequency of a signal coming from a transmitter by the multiple of a multiplying element before they deliver signals to antenna elements. For example, in the doubler phase control circuit shown in FIG. **1** the transmitter signal frequency is doubled before it is delivered to the antenna elements **25***a–c*.

FIG. 3 shows another "doubler" phase control circuit employing the principles of this invention which is quite similar to the embodiment shown in FIG. 1. The doubler phase control circuits shown in FIGS. 1 and 3 differ from one another in that the FIG. 3 embodiment employs: 90° hybrids rather than 180° hybrids as in the FIG. 1 embodiment; 90° phase delay elements connected in series to sum port frequency doublers; and antenna elements which are connected to sum ports of recombining 90° hybrids rather than to difference ports, as in the FIG. 1 embodiment. Otherwise, the FIG. 3 embodiment functions essentially the same as the FIG. 1 embodiment. That is, it receives two signals S_1 and S_2 separated by an angle θ, and emits three signals having respective phase angles of zero phase shift, θ phase shift and 2θ phase shift. Also, the circuit shown in FIG. 3 has the same "conversion loss" feature described above for the circuit shown in FIG. 1.

More particularly FIG. 3 shows a transmitter circuit comprising: a transmitter **10**; a two-way power divider **27**; and a θ phase shifter **13**. The transmitter circuit feeds a doubler phase control coupling circuit which comprises: left and right multi-output power dividers **33** and **35**; three combining 90° hybrids **36***a–c*; six frequency doublers **21***a–f*; three 90° phase delay elements **38***a–c*; and three recombining 90° hybrids **40***a–c*. The recombining 90° hybrids **40***a–c* feed antenna elements **25***a–c*.

The transmitter **10** is coupled to the two-way power divider **27**, and one output of the two-way power divider **27** is coupled directly to the left multi-output power divider **33** while the other output is connected through the θ phase shifter **13** to the right multi-output power divider **35**. First and second outputs of the left multi-output power divider **33** are respectively coupled to first and second inputs of a first combining 90° hybrid **36***a*, and a third output of the left multi-output power divider **33** is coupled to a first input of a second combining 90° hybrid **36***b*. First and second outputs of the right multi-output power divider **35** are respectively coupled to first and second inputs of a third combining 90° hybrid **36***c*, and a third output of the right multi-output power divider **35** is coupled to a second input of the second combining 90° hybrid **36***b*.

The sum port of the first combining 90° hybrid **36***a* is coupled through the first doubler **21***a* and a first phase delay element **38***a* to a first input of a first recombining 90° hybrid **40***a*; and the difference port of the first combining 90° hybrid **36***a* is coupled through the second doubler **21***b* to a second input of the first recombining 90° hybrid **40***a*. The sum port of the second combining 90° hybrid **36***b* is coupled through the third doubler **21***c* and a second phase delay element **38***b* to a first input of a second recombining 90° hybrid **40***b*; and the difference port of the second combining 90° hybrid **36***b* is coupled through the fourth doubler **21***d* to a second input of the second recombining 90° hybrid **40***b*. The sum port of the third combining 90° hybrid **36***c* is coupled through the fifth doubler **21***e* and a third phase delay element **38***c* to a first input of a third recombining 90° hybrid **40***c*; and the difference port of the third combining 90° hybrid **36***c* is coupled through the sixth doubler **21***f* to a second input of the third recombining 90° hybrid **40***c*.

The sum ports of the three recombining 90° hybrids **40***a–c* are respectively coupled to active antenna elements **25***a–c*. The difference ports of the recombining 90° hybrids **40***a–c* are terminated at terminating resistors **26***a–c*.

As is mentioned above, the 90° hybrid doubler phase control circuit functions similarly to the 180° hybrid doubler phase control circuit described in detail above, hence, its operation will not be further described here.

GENERALIZED PHASE CONTROL CIRCUIT

A generalized phase control circuit, shown in FIG. 4, employs the same principles as the doubler phase control circuits shown in FIGS. 1 and 3. However, it uses a higher order of multiplication and produces more output phase shifted signals than the doubler phase control circuits of FIGS. 1 and 3.

The doubler phase control circuits of FIGS. 1 and 3 accomplish their function by combining two phase shifted input signals, doubling the combined signal and separating out of the doubled-combined signal an integral phase shift signal of the highest phase shift in the system. In the doubler circuits there is only one integral phase shift, namely, θ. This is because θ is the only one integral between zero and the highest phase shift of the system 2θ. In the system shown in FIG. 4, essentially what is done is two signals, which are out of phase by angle θ, are subdivided into two groups of smaller signals and the smaller signals are combined to produce various combined signals; each combined signal is multiplied by N. Then the combined signals are recombined and thereby separated into $N-1$ phase shifted integral signals, each being phase shifted from a zero reference by a multiple of θ times an integral integer M of N, covering a range of M from 1 to $N-1$.

Referring now to FIG. 4, there is shown a transmitter circuit comprising: a transmitter **42**; a two-way power divider **44**; and a θ phase shifter **45**. The transmitter circuit feeds a generalized phase control coupling circuit which comprises: left and right N-way power dividers **51***a* and *b*; phase shifters 53_1–$53_{(N-1)}$; combining 180°-hybrids 55_0–$55_{(N-1)}$; frequency multipliers 57_0–$57_{(N-1)}$; $(N-1)$-way power dividers 59_0–$59_{(N-1)}$; N−1 phase delay elements 61_1–$61_{(N-1)}$; N−1 phase delay elements 63_1–$63_{n31)}$; an M_1 summing circuit **65**; and an M_2 summing circuit **67**. The summing circuits **65**, **67** respectively feed antenna elements **69**, **71**.

A signal applied by the transmitter **42** on a transmitter line **43** passes through the two-way power divider **44** and θ phase shifter **45** to a right terminal **49** and through the two-way power divider **44** to a left terminal **47**. Signals appearing at the left and right terminals **47** and **49** are respectively fed into left and right N-way power dividers **51***a* and **51***b*. The input to output amplitude ratios for the left and right N-way power dividers **51***a* and **51***b* are $\sqrt{N}$; thus, their input signals are designated as $\sqrt{N}\,S_1$, $\sqrt{N}\,S2$ and their output signals are designated as S_1, S_2.

Except for a first output 73_0 of the right N-way power divider **51***b*, each output of the right N-way power divider **51***b* is connected to a separate phase shifter 53_1–$53_{n31)}$. First phase shifter 53_1 shifts its signal, S_2, Δ degrees forward where $\Delta = (2\pi)/N$; second phase shifter 53_2 shifts its signal, S_2, 2Δ degrees forward; and so on up to the phase shifter $53_{(N-1)}$ which shifts its signal, S_2, $(N-1)\Delta$ degrees forward.

The signal S_2 coming from the first output 73_0 of the right N-way power divider **51***b*, is combined with a signal S_1 coming from a first output 74_0 of the left N-way power divider **51***a* in a first combining 180° hybrid 55_0. A signal S_2 coming from a second output **73**, of the right N-way power divider **51***b*, after passing through a phase shifter **53**, is combined with a signal S_2 coming from a second output 74_1 of the left N-way power divider **51***a* in a second combining 180° hybrid 51_1. In a similar manner, signals S_2 coming from outputs 73_2–$73_{(N-1)}$ of the right N-way power divider **51***b* are respectively combined with signals S_1 coming from outputs 74_2–$74_{n31)}$ of the left N-way power divider **51***a* in combining 180° hybrids 55_2–$55_{(N-1)}$.

The difference ports of the combining 180° hybrids 55_0–$55_{n31)}$ are terminated into resistors 56_0–$56_{(N-1)}$.

The sum ports of the hybrids 55_0–$55_{(N-1)}$ are connected through lines 56_0–$56_{(N-1)}$ to separate frequency multipliers 57_0–$57_{(N-1)}$, each of which multiplies its input signal by N.

Frequency multipliers 57_0–$57_{(N-1)}$ respectively feed their multiplied signals into separate $(N-1)$-way power dividers 59_0–$59_{(N-1)}$.

Each of the $N-1$ outputs of a second $(N-1)$-way power divider 59_1 respectively feeds a separate phase delay element 61_1–63_1, etc., with only two being shown for clarity. Each of these phase delay elements delays its input signal by an amount equal to the forward phase shift caused by the series connected phased shifter **53**, multiplied by an integral integer M of N; e.g., the phase delay element 63_1 is in series with a phase shifter 53_1 having a forward phase shift of Δ. Therefore, the phase delay caused by 63_1 is Δ times M_2. Similarly each of the $N-1$ outputs of a third $(N-1)$-way power divider 59_2 respectively feeds a separate phase delay element 61_2, 63_2, etc., with only two being shown for clarity. As for the phase delay elements of the $(N-1)$-way power divider 59_1, each of these delay elements delays a signal by an amount equal to the forward phase shift caused by the series connected phase shifter 53_2 multiplied by an integral integer M of N. For example, the phase delay element 63_2 is in series with a phase shifter 53_2 having a forward phase shift of $2\ \Delta$. Therefore, the phase delay caused by 63_2 is $2\ \Delta$ times M_2. A similar description is applicable for all of the phase delay elements attached to the outputs of the $(N-1)$-way power dividers 59_0–$59_{(N-1)}$. The $(N-1)$-way power divider 59_0 does not have phase delay elements connected to its outputs because it is not in series with a phase shifter 53_1–$53_{(N-1)}$.

Each of the $(N-1)$-way power dividers 59_0–$59_{(N-1)}$ has $N-1$ phase delay elements **61**, **63**, etc., connected to its respective outputs, and the M integral integers of N utilized by the phase delay elements of each one of the $(N-1)$-way power dividers 59_0–$59_{(N-1)}$ covers the range of from 1 to $N-1$. It can be seen in FIG. **4** that the phase delay elements 61_1–$61_{(N-1)}$ are connected in parallel to a M_1 summing circuit **65**. In this regard, all of the phase delay elements 61_1–$61_{(N-1)}$ have a phase delay which is a multiple of the integral integer M_1. Further, all of the phase delay elements 63_1–$63_{(N-1)}$ are connected in parallel to a M_2 summing circuit **67**. In this regard, all of the phase delay elements 63_1–$63_{(N-1)}$ delay the phase by an angle which is a multiple of the integral integer M_2. Similarly, there are phase delay elements feeding $N-1$ summing circuits (only combining elements **65** and **67** are shown for clarity), with the phase delay elements feeding each summing circuit being a multiple of an integral integer M of N, covering the range from $M=M_1=1$ to $M=M_{(N-1)}=N-1$.

The signals coming from the phase delay elements 61_1–$61_{n31)}$ are combined at the M_1 summing circuit **65** and feed into an antenna element **69** and the signals coming from the phase delay elements 63_1–$63_{(N-1)}$ are combined at the M_2 summing circuit **67** and feed into an antenna element **71**. Similarly, there are $N-1$ antenna elements, each being fed by a summing circuit, however, only two antenna elements are shown for clarity.

Effectively, the generalized phase control circuit shown in FIG. **4** receives two phase shifted signals, one shifted from the other by an angle θ, and converts them into $N-1$ signals, each being phase shifted from a reference signal by an integral integer M of the number N times θ. That is, the output signals are respectively shifted from a reference signal by angle θ, 2θ, 3θ . . . $(N-1)$. The general theory behind the operation of this circuit is as follows:

The input signals S_1 and S_2 are expressed by the equations:

$$S_1 = \cos \omega t \tag{14}$$

$$S_2 = \cos(\omega t + \theta) \tag{15}$$

Similarly, the signals emitted from the sum ports of the combining 180° hybrids 55_0–55_{N-1} (the difference ports are terminated as previously mentioned above) onto their respective lines 56_0–$56_{(N-1)}$ are expressed by the equations:

$$S_{56_0} = (1/\sqrt{2})(S_1 + S_2) \tag{16}$$

$$S_{56_1} = (1/\sqrt{2})(S_1 + S_2/\Delta) \tag{17}$$

$$S_{56_2} = (1/\sqrt{2})(S_1 + S_2/2\Delta) \tag{18}$$

$$S_{56(N-1)} = (1/\sqrt{2})(S_1 + S_2/(N-1)\Delta) \tag{19}$$

where the notation $S_2/p\ \Delta = \cos(\omega t + \theta + p\Delta)$, with p = integral integers of N covering the range from 1 to $N-1$; and $\Delta = (2\pi)/N$. These signals are fed into the frequency multipliers 57_0–$57_{(N-1)}$ of the order N. The multipliers 57_0–$57_{(N-1)}$, respectively, raise the signals $S_{56_0} - S_{56(n-1)}$ to the power N and filter out all components except those at frequency $N\omega$. It can be shown from binomial expansion that the term in each $(S_{56})^N$ which has its phase angle equal to some general integral integer M of N times θ is

$$[N(N-1)(N-2)\ldots(N-M+L)/M](S_1)^{(N-M)}\cos(\omega t + \theta + p\Delta)^M \tag{20}$$

Apart from the amplitude factor which is common to each $(S_{56})^2$, the component of this expression which emerges from each of the multipliers 57_0–$57_{(N-1)}$ at the frequency $N\omega$ is expressed as

$$\cos(N\omega t + M\theta + Mp\Delta) \tag{21}$$

It can be shown that the following mathematical relationship exists:

$$\sum_{P=0}^{P=(N-1)} n \cos [N\omega t + M\theta + p\Delta(M-K)] \quad (22)$$
$$= \begin{cases} 0 \text{ at } K \neq M \\ N \cos (N\omega t + M\theta) \text{ at } K = M \end{cases}$$

It is desirable to obtain a final output expressed as $N \cos (N\omega t + M\theta)$ which is a multiple of an angle θ by an integral integer of N. To separate out this term with a phase angle of $M\theta$, it is necessary to subtract, or delay, a phase angle $Mp\,\Delta$ from each of the signals $(S_{56})^N$ coming from the multipliers 57_0–$57_{(N-1)}$ and then add all of the difference signals together. The notation $(S_{56})^N/-Mp\,\Delta$ is used to indicate that an angle $Mp\,\Delta$ is subtracted from each of the signals $(S_{56})^N$ coming from the doublers 57_0–$57_{(N-1)}$. The sum of these signals is then expressed as $N \cos (N\omega t + M\theta)$. To get this result using the circuit shown in FIG. 4, each signal $(S_{56})^N$ is divided into $N-1$ parts (using the power dividers 59_0–$59_{(N-1)}$) and the appropriate phase delay elements, for example phase delay elements 61_1–$61_{(N-1)}$, have a phase delay of $M_1 p\,\Delta$ and are respectively inserted between the power dividers 59_1–$59_{(N-1)}$ and the summing circuit 65. In this case the sum of the signals which are combined by the summing circuit, and therefore appear on the antenna element 69, is expressed as $N \cos (N\omega t + M_1\theta)$. This summing operation is similarly carried out for all values of M as follows:

$M_1 = 1$
$M_2 = 2$
$M_3 = 3$
.
.
.
$M_{(N-1)} = N-1$

The summing operations for each of these values of M can be generally expressed as:

$$\Sigma(M\theta) = \frac{1}{\sqrt{N-1}} \sum_{p=0}^{p=(N-1)} (S_{56})^N/-Mp\Delta \quad (23)$$

Each of the sums is respectively free of all terms at phase angles other than $M_1\theta$, $M_2\theta \ldots M_{(N-1)}\theta$, as the case may be. The generalized phase control circuit has therefore yielded a set of signals with phase angles of θ, $2\theta \ldots (N-1)\theta$ which lie equally spaced between the extreme phases 0 and $N\theta$.

Thus, this circuit has converted two phase shifted signals into many phase shifted signals, each phase shifted from the others by highly accurate increments. Again, the circuit uses standardized interchangeable components which makes it economical and relatively uncomplicated.

Unlike the doubler phase control circuit described above, the generalized phase control circuit does not exhibit the same invariance to multiplier power sensitivity. Indeed, it can be shown that if the multiplier parameters do vary with power, then both amplitude modulation and phase error are evident at the antenna elements 69, 71, etc.

The generalized phase control circuits also "up-convert" the input signals' frequencies from lower transmitter frequencies to higher broadcasting frequencies at the antenna elements 69, 71, etc., as do the doubler phase control circuits.

Another feature of importance with regard to generalized phase control circuits is that the various antenna signals are of different amplitude for $N > 3$. This arises because of the binomial coefficient amplitude factor multiplying the various terms is a multiplier extension $(S_{56})^N$. This factor limits the practical upper boundary to the order of multiplication. Beyond the order 5, the amplitude ratio of a center signal, $(N\theta/2$ for N even, or $(N-1)\theta/2$ for N odd) to those at the angle θ and $(N-1)\theta$, exceeds 2.0. Beyond the order of 10 this ratio exceeds 25.0. Directional couplers, attenuators or limitors may be used to equalize the signals, but when the difference in signal amplitude becomes too great, this too becomes impractical.

QUADRUPLER PHASE CONTROL CIRCUIT

FIG. 5 illustrates a "guadrulpler phase control circuit" employing the principles of this invention. Essentially, the quadrupler phase control circuit shown in FIG. 5 receives two phase shifted transmitter signals, a first at zero phase shift and a second at θ phase shift, and emits three phase shifted antenna element signals; a first at θ phase shift, and a second at 2θ phase shift, and a third at 3θ phase shift. The quadrupler phase control circuit accomplishes this by subdividing the two received signals into two groups of smaller signals, combining the smaller signals, in various ways, doubling the combined signals, and then recombining twice the combined signals so as to separate out, from the doubled combined signals, signals having the desired phase angles.

Referring now to FIG. 5, there is shown a quadrupler phase control coupling circuit which comprises: left and right two-way power dividers 77 and 79; two combining 180° hybrids 81*a* and 81*b*; a 90° forward phase shifter 82; four frequency quadruplers 83*a–d*; two recombining 180° hybrids 85*a* and 85*b*; a 90° phase delay element 86 and two re-recombining 180° hybrids 87*a* and 87*b*. The re-recombining 180° hybrids 87*a* and 87*b* feed three antenna elements 89*a–c*. A transmitter circuit is not shown in FIG. 5, however it should be understood that the quadrupler phase control circuit is normally fed by a transmitter circuit similar to the transmitter circuits shown in FIGS. 1, 3 and 4 and described in conjunction therewith.

More particularly, a transmitter circuit, not shown, feeds a zero phase angle signal to input 91 of the left two-way power divider 77 and a θ phase angle signal to input 93 of the right two-way power divider 79. First and second outputs of the left two-way power divider 77 are respectively coupled to first inputs of first and second combining 180° hybrids 81*a* and 81*b*. A first output of the right two-way power divider 79 is coupled to a second input of the first combining 180° hybrid 81*a*. A second output of the right two-way power divider 79 is coupled through the 90° forward phase shifter 82 to a second input of the second combining 180° hybrid 81*b*.

The sum port of the first combining 180° hybrid 81*a* is coupled through a first frequency quadrupler 83*a* to a first input 84 of a first recombining 180° hybrid 85*a*. The difference port of the first combining 180° hybrid 81*a* is coupled through a fourth frequency quadrupler 83*d* to a second input 88 of a second recombining 180° hybrid 85*b*. The sum port of the second combining 180°

hybrid **81***b* is coupled through a second frequency quadrupler **83***b* to a first input **90** of the second recombining 180° hybrid **85***b*. The difference port of the second combining 180° hybrid **81***b* is connected through a third frequency quadrupler **83***c* to a second input **92** of the first recombining 180° hybrid **85***a*.

The sum and difference ports of the first recombining 180° hybrid **85***a* are respectively connected to first inputs **94**, **96** of first and second re-recombining 180° hybrids **87***a* and **87***b*. The sum port of the second combining 180° hybrid **85***b* is coupled to a second input **98** of the first re-recombining 180° hybrid **87***a* and the difference port of the second recombining 180° hybrid **85***b* is coupled through the phase delay element **86** to a second input **100** of the second re-recombining 180° hybrid **87***b*.

The sum port of the first re-recombining 180° hybrid **87***a* is terminated into a resistor **95** and the difference port of the first re-recombining 180° hybrid **87***a* is coupled to a second antenna element **89***b*. The sum port of the second re-recombining 180° hybrid **87***b* is coupled to a first antenna element **89***a* and the difference port of the second re-recombining 180° hybrid **87***b* is coupled to a third antenna element **89***c*.

Effectively, the quadrupler phase control circuit receives two input signals which are separated from one another by a phase angle θ; divides each of the input signals into two S_1 signals and two S_2 signals; combines the S_1 signals and the S_2 signals in various ways (i.e, by summing and subtracting) in the two combining 180° hybrids **81***a* and **81***b;* quadruples the combined signals using the frequency quadruplers **83***a–d;* recombines the quadrupled-combined signals in the recombining 180° hybrids **85***a* and **85***b;* re-recombines the recombined-quadrupled-combined signals in the re-recombining 180° hybrids **87***a* and **87***b* and thereby separates out three signals, one each at the three antenna elements **89***a–c*. The signal appearing at the first antenna element **89***a* has a relative phase angle of θ, the signal appearing at the second antenna element **89***b* has a relative phase angle of 2θ, and the signal appearing at the third antenna element **89***c* has a relative phase angle of 3θ.

Equations which express the signals appearing on various lines in the quadrupler phase control circuit are included in FIG. **5**.

It will be appreciated by those skilled in the art that the phase control array antenna circuits specifically disclosed in this application offer advantages of lack of complexity and accuracy over prior art phase control array antenna coupling circuits. However, it will be appreciated that various changes in form and detail may be made in the specifically disclosed embodiments without departing from the spirit and scope of the invention.

What is claimed is:

1. A phased array antenna coupling circuit of the type used for coupling a transmission circuit with a plurality of more than two phased array antenna elements comprising:

a multiplier circuit, means for multiplying the frequencies of at least two signals supplied thereto;

combining circuit means for interconnecting said transmission circuit and said multiplier circuit means, said combining circuit means being adapted to combine in a preselected manner at least two signals which are separated by a phase angle; and,

a recombining circuit means for interconnecting said multiplier circuit means and said more than two phased array antenna elements.

2. A phased array antenna coupling circuit as claimed in claim **1** wherein:

said combining circuit means includes phase shifting means connected to said transmission circuit first and second input terminal means, each of which handles a signal which is separated by a phase angle from the signal handled by the other.

3. A phased array antenna coupling circuit as claimed in claim **2** wherein:

said multiplier circuit comprises a plurality of frequency multiplier elements each being connected between said combining and recombining circuits; and,

said combining circuit comprises first and second multi-output power dividers, said first multi-output power divider being connected to said first input terminal means and said second multi-output power divider being connected to said second input terminal means.

4. A phased array antenna coupling circuit as claimed in claim **3** wherein said combining circuit and said recombining circuit each combine at least two signals which are separated from one another by a phase angle.

5. A phased array antenna coupling circuit as claimed in claim **4** wherein:

said combining circuit includes a four port hybrid power divider which is connected to both said first and said second multi-output power dividers and is further connected to two of said frequency multiplier elements;

said frequency multiplier elements are frequency doublers; and,

said recombining circuit includes a four port hybrid power divider which is connected between at least two of said frequency doublers and at least one of said antenna elements.

6. A phased array antenna coupling circuit as claimed in claim **4** wherein:

there are three four port hybrid power dividers in said combining circuit, a first of which has two inputs connected to said first multi-output power divider, a second of which has a first input connected to said first multi-output power divider and a second input connected to said second multi-output power divider, and a third of which has two inputs connected to said second multi-output power divider;

there are six doublers, a pair of said doublers being attached to each of said three four port hybrid power dividers in said combining circuit; and,

there are three four port hybrid power dividers in said recombining circuit, each one being attached to a separate pair of said doublers.

7. A phased array antenna coupling circuit as claimed in claim **6** wherein:

said four port hybrid power dividers in said combining circuit and said recombining circuit are 90° hybrids; and,

there is further included three 90° delay elements which are respectively connected between one frequency doubler in each frequency doubler pair and a four port hybrid in said recombining circuit.

8. A phased array antenna coupling circuit as claimed in claim **4** wherein:

said combining circuit includes a 180° four port hybrid power divider which is connected to both said first and said second multi-output power dividers and is further connected to two said frequency multiplier elements;

said frequency multiplier elements are frequency doublers; and,

said recombining circuit includes a 180° four port hybrid power divider which is connected between at least two of said frequency doublers and at least one of said antenna elements.

9. A phased array antenna coupling circuit as claimed in claim **4** wherein:

said frequency multiplier elements each multiply signals to the Nth power; and,

said combining circuit includes *N* four port hybrid power dividers which are respectively connected to both said first and said second multi-output power dividers and which are respectively further connected to separate ones of said multiplier elements.

10. A phased array antenna coupling circuit as claimed in claim **9** wherein:

said multi-output power dividers are N-way power dividers, each having *N* outputs;

there are *N*−1 phase shifting elements, each connected between a separate output of one of said *N*-way power dividers and a separate one of said *N* four port hybrid power dividers;

there are N multiplying elements, each one connected to a separate four port hybrid power divider in said combining circuit;

there are (*N*−1)-way power dividers connected between each said multiplier element and said recombining circuit; and,

phase delay elements are connected between the outputs of all but one of said (*N*−1)-way power dividers and said recombining circuit.

11. A phased array antenna coupling circuit as claimed in claim **4** wherein:

said frequency multiplier elements each multiply signals to the Nth power;

said multi-output power dividers each have *N* outputs; and wherein is further included (*N*−1)-way power dividers each having *N*−1 outputs and each being connected between a separate multiplier element and said recombining circuit means.

12. A phased array antenna coupling circuit as claimed in claim **4** wherein;

said multiplier elements are quadruplers.

13. A phased array antenna coupling circuit as claimed in claim **12** wherein:

said first and second multi-output power dividers are two-way power dividers each having first and second outputs;

said combining circuit further comprises a 90° phase shifter;

said combining circuit further includes a first and a second combining 180° hybrid each having sum and difference parts, said first combining 180° hybrid having a first input connected to said first output of said first two-way power divider and a second input connected to said first output of said second two-way power divider, and said second combining 180° hybrid having a first input connected to said second output of said first two-way power divider and a second input connected through said 90° phase shifter to said second output of said second two-way power divider;

said recombining circuit comprises first and second recombining 180° hybrids each having first and second inputs and sum and difference ports, and first and second recombining 180° hybrids each having first and second inputs and sum and difference ports;

said sum port of said first combining 180° hybrid is connected through a quadrupler to said first input of said first recombining 180° hybrid;

said difference port of said first combining 180° hybrid is connected through a quadrupler to said second input of said second recombining 180° hybrid;

said sum port of said second combining 180° hybrid is connected through a quadrupler to said first input of said second recombining 180° hybrid;

said difference port of said second combining 180° hybrid is connected through a quadrupler to said second input of said first recombining circuit further comprises a 90° phase delay element;

said sum port of said first recombining 180° hybrid is connected to said first input of said first re-recombining 180° hybrid;

said difference port of said first recombining 180° hybrid is connected to said first input of said second re-recombining 180° hybrid;

said sum port of said second recombining 180° hybrid is connected to said second input of said first re-recombining 180° hybrid;

said difference port of said second recombining 180° hybrid is connected through said 90° phase delay element to said 90° phase delay element to said second input of said second rerecombining 180° hybrid; and,

said difference port of said first re-recombining 180° hybrid and said sum and difference ports of said second re-recombining 180° hybrid are each connected to one of said phased array antenna elements.

* * * * *