Phase Noise in Frequency Divider Circuits

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***Abstract*— We identify limitations of the models for phase noise in frequency dividers by Egan and by Phillips and present a new model applicable to both high frequency and low power frequency divider design. Further, we design both synchronous and asynchronous frequency divider test chips that allow us to observe experimentally the effects of noise accumulation, sampling frequency and biasing conditions on the total phase noise performance of frequency dividers. We use our measurements to validate the simulated values obtained by time domain phase noise analysis offered by the commercial simulator Spectre RF. The measured data show good agreement with the simulation results.**

I. Introduction

Low power consumption and high performance are often contradictory requirements and this constitutes a design trade-off. In particular, achieving a low phase noise in the phase locked loop (PLL) of frequency synthesizers is one of the most stringent requirements. Normally, the current trend towards lower power consumption degrades phase noise performance. Therefore, we need to define an appropriate way of optimizing towards low power consumption without sacrificing the phase noise performance of the PLL. To comprehend in depth this design trade-off, one should identify the internal phase noise mechanisms intrinsic to each block constituting a PLL.

We choose the frequency dividers (FD) as the focus of this work. The phase noise generated by a FD affects the synthesizer noise performance within the PLL band, especially if a high division factor is used. Additionally, the digital FD is in general responsible for a significant portion of the total power consumption of the PLL. However, a decrease in the power consumption of the divider degrades its phase noise performance.

Therefore, we need, first, to identify the fundamental trade-off between noise and power consumption in this particular block and, second, to have a robust and reliable way of simulating phase noise of "sample and hold" based circuits such as a digital FD. Section II addresses the former problem. We identify the limitations in the FD phase noise models suggested by Phillips [1] and by Egan [2] and propose a new model that captures the power and phase noise trade-off for a fixed operating frequency. In Section III, we present the divider architectures and test chips that are used for measurements. In the same section, measurements are compared against simulations, and deviations from theory are identified and explained. Finally, Section IV concludes this paper.

II. Models of Phase Noise in frequency dividers

Several models for classifying and describing the phase noise of digital FDs are available [1]–[3]. Levantino et al. in [3] present a physical derivation of phase noise in a source-coupled logic Dlatch. However, they do not quantify the total divider-by-N phase noise. Phillips and Egan in [1] and [2] attempt to model the phase noise of digital FD architectures. However, they make certain assumptions that limit the design space at which their model is applicable. In the following, we identify the limitations of the existing models and extend Phillip's model to include noise sources and effects that occur in a generic divider architecture.

A. Phillips' and Extended Phillips' model

The total divider output phase noise according to Phillips' model is

$$\phi_{out}^2 = \left(\frac{\phi_{in}}{N}\right)^2 + \left(\frac{v_n}{K_p}\right)^2 \frac{2H}{N} + \phi_{p,1}^2 + \phi_{p,2}^2 + ... + \phi_{p,M}^2, \quad (1)$$

where ϕ_{in} is the narrow-band "input phase noise", v_n models driving source noise, as well as device input noise in between divider interstages, H is the maximum significant harmonic, N is the division ratio, K_p is the zero crossing slope measured in $volts/radian$, and $\phi_{p,n}^2$ is the "propagation-delay noise" of the n^{th} gate [1].

In the first term on the right hand side of equation (1), the $1/N^2-$dependence is derived from FM theory. The second term represents the equivalent input phase noise power (from input noise voltages) $2v_n^2/K_p^2$, divided by N^2 also according to FM theory and simultaneously multiplied by HN to incorporate the "sampling effect" (sampling results into a replication (aliasing) of the wide-band noise spectrum at a rate αf_{out}, where f_{out} is the output frequency of the divider stage and α equals 2 or 1 for sampling once or twice per cycle, respectively). In the following, we prefer to formulate the "sampling effect" in a different way. As Fig. 1 shows, the bandwidth BW of the divider stage determines how many of the replicated spectra (due to sampling) contribute to the total noise. The aliased spectra are responsible for the extra gain factor of $\alpha BW/f_{out}$, and thus one needs to multiply $2v_n^2/(K_pN)^2$ by this factor. This factor equals N only under the condition that $BW = Nf_{out} = f_{in}$ which yields the minimum bandwidth for which correct division can be sustained.

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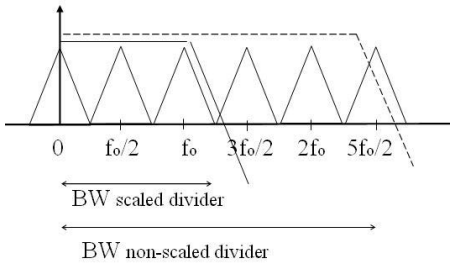

Fig. 1. The smaller bandwidth of a down-scaled divider reduces the amount of aliased spectra and therefore its contribution to the total noise.

Phillips assumes that a total of M gates contribute to the total propagation delay $\phi_{p,1}^2+\phi_{p,2}^2+...+\phi_{p,M}^2$ of a synchronous divider stage. This does not include the case of asynchronous stages. In the case of M asynchronous divider stages, the total propagation-delay noise at the output of the M-th stage is

$$\frac{\phi_{p,1}^2}{(N_2N_3...N_M)^2}+\frac{\phi_{p,2}^2}{(N_3...N_M)^2}+...+\phi_{p,M}^2, \qquad (2)$$

where N_i is the division ratio of the i-th asynchronous divider stage.

Finally, similarly to Egan, Phillips assumes that the only point where an AM to PM noise transformation occurs is at the input of the total divider structure. This is true if and only if the signals driving the divider inter-stages are resembling square waves which is unrealistic at higher frequencies.

Despite these limitations, Phillips' model can be easily made into a model that, first, takes into account the sampling effect for all wide-band noise sources; second, does not assume square-like driving signals; and third, concerns a generic divider structure consisting of both synchronous and asynchronous stages.

We start by modifying eq. (1) so as to incorporate the sampling effect into the model. For a synchronous divider-by-N, one may write

$$\phi_{out}^2=\left(\frac{\phi_{in}}{N}\right)^2+\alpha\frac{BW}{f_{out}}\left(\left(\frac{v_n}{K_p}\right)^2\frac{2}{N^2}\right)+\phi_p^2. \qquad (3)$$

Here, the aliasing of the additive input voltage noise is accounted for by multiplying this noise types by $\alpha BW/f_{out}$.

To obtain the general form of Phillips' model, we consider two stages of synchronous dividers coupled in an asynchronous fashion as depicted in Fig. 2. The first syn-

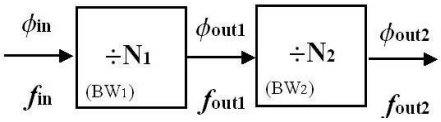

Fig. 2. Two stages of synchronous dividers, coupled asynchronously.

chronous divider realizes a division-by-N_1 and the second one a division-by-N_2. The total division is, thus, N_1N_2. We apply eq. (3) on each divider stage to obtain the total noise at the output of the first- and second-asynchronous stages,

$$\phi_{out,1}^2=\left(\frac{\phi_{in}}{N_1}\right)^2+\alpha\frac{BW_1}{f_{out,1}}\left(\left(\frac{v_{n,1}}{K_{p,1}}\right)^2\frac{2}{N_1^2}\right)+\phi_{p,1}^2, \quad (4)$$

$$\phi_{out,2}^2=\left(\frac{\phi_{out,1}}{N_2}\right)^2+\alpha\frac{BW_2}{f_{out,2}}\left(\left(\frac{v_{n,2}}{K_{p,2}}\right)^2\frac{2}{N_2^2}\right)+\phi_{p,2}^2. \quad (5)$$

Substituting eq. (4) in eq. (5), we obtain the expression for the total output phase noise power,

$$\phi_{out,2}^2=\left(\frac{\phi_{in}}{N_1N_2}\right)^2+\left(\frac{\phi_{p,1}^2}{N_2^2}+\phi_{p,2}^2\right)+\alpha\left(\left(\frac{v_{n,1}}{K_{p,1}}\right)^2\frac{2}{N_1^2N_2^2}\frac{BW_1}{f_{out,1}}+\left(\frac{v_{n,2}}{K_{p,2}}\right)^2\frac{2}{N_2^2}\frac{BW_2}{f_{out,2}}\right).$$

Here, $K_{p,i}$ is the zero crossing slope of the driving signal, $2v_{n,i}^2$ is the noise power in rms values within the Nyquist band, and $\phi_{p,i}$ represents the propagation delay noise of the i^{th} component.

Note that the parameters determining the bandwidth BW influence the value of K_p which drives the subsequent divider stage. We identify here one design trade-off: (a) BW should be as small as possible to decrease the gain due to sampling while (b) BW should be as large as possible to increase K_p. Additionally, the extended model covers cases where the synchronous division ratios N_1 and N_2 are unequal and larger than or equal to 2, as well as cases where the driving signals between divider stages are not square-like. The first enhances the generic character of the model. The latter models the additive phase noise in between divider-stages. Finally, ϕ_i and $v_{n,i}$ are phase noise parameters intrinsic to the unit elements of each divider stage and hence, are treated as an independent modeling procedure. Such a model is presented by Levantino et al. in [3].

Understanding the impact that design parameters, such as BW, division number N, and number of asynchronous stages, have on the total output phase noise, helps us choose their values. However, we are still missing a reliable way of predicting the phase noise values of a FD. In the following, we will evaluate the "time domain" (strobed) phase noise analysis offered by the commercial simulator Spectre RF.

III. Test chips for measurements

To verify the accuracy of the "strobed" phase noise analysis against measured values, we layout two different designs under test (DUT), namely a synchronous and an asynchronous divider-by-4 architecture. Fig. 3 shows their block diagrams.

To ensure sufficient reliability of the measurements, one must isolate the DUT from any external noise source. We use the typical I/Q measurement setup [2]. Two identical dividers ($DUT1$ and $DUT2$) are driven by the same signal generated by an on-wafer input amplifier used to convert the single-ended source input to a differential one at the clock inputs. $DUT2$ is preset to be 90^o out of phase with respect to $DUT1$ (this is the proper condition for operation of a balanced-mixer phase detector). The I and Q signals are fed into the mixer, which is

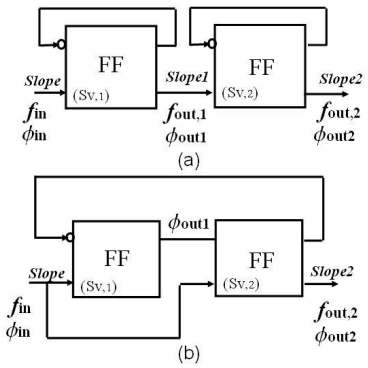

Fig. 3. The asynchronous (a) and synchronous (b) divider-by-4 architectures.

internal to the phase noise measurement equipment, see Fig. 5. Half of the measured noise power is ascribed to each of the two FDs. Since both dividers have a common input, phase noise from the source and from the input amplifier (which is correlated noise in the I/Q paths) tends to cancel.

A. Divider-by-2 cell

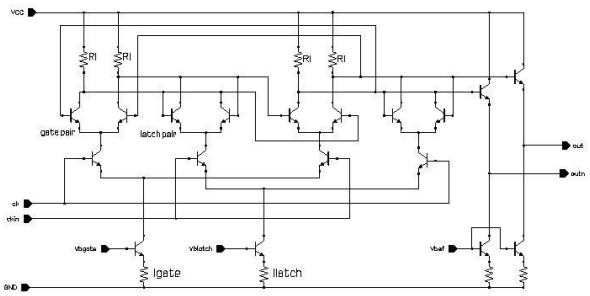

Fig. 4. Schematic view of the divider-by-2 cell.

The divider-by-2 cells, that are used in each DUT, are the state-of-the-art adaptive FD cells [4], see Fig. 4. We recall that, in the adaptive architecture, the cross-coupled stage and the amplifier stage in each Dlatch are biased independently. By biasing the cross-coupled pair I_{latch} with lower current than the one in the amplifier stage I_{gate}, we extend the frequency of operation.

B. Measurement set-up

Calibration of the measurement set-up (depicted in Fig. 5 excluding the test chip in its path) shows that its noise floor is $L(2MHz) = -155$dBc/Hz at $f_{out} = 5$GHz. The high $1/f$ noise present in GaAs low noise amplifiers ($LNAs$) restricts our experiment only within the white noise region. Unfortunately, we cannot eliminate these $LNAs$, since amplification of the output I/Q signals is necessary.

C. Simulations versus measurements

To measure the phase noise generated by our DUT, we perform "phase noise without a PLL" measurements, involving the calibration of the phase detector constant which determines the absolute noise floor of the system. Table I shows the measured and simulated phase noise results at $f_m = 2$ MHz. These results were obtained under different input frequencies, cross-coupled pair current biasing and divider architectures. We mark as N/A the set of conditions for which division was impossible. Simulations match the measurements within 1 dB.

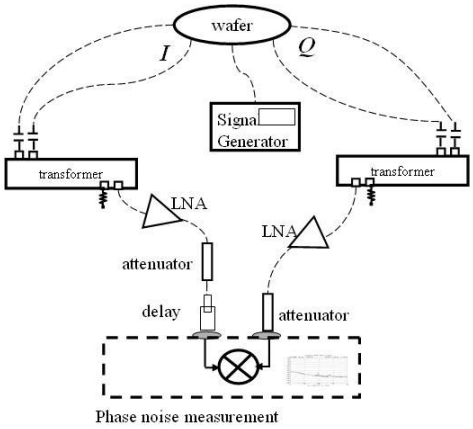

Fig. 5. Setup for phase noise measurements.

TABLE I
MEASURED AND SIMULATED DIVIDER PHASE NOISE AT $f_m = 2$MHz.

Measured divider phase noise at $f_m = 2$MHz.		
$I_{gate} = 2I_{latch}$	**Div-4 Synchr**	**Div-4 Asynchr**
10 GHz	-152.5 dBc/Hz	-152 dBc/Hz
20 GHz	N/A	-148.5 dBc/Hz
$I_{gate} = I_{latch}$	**Div-4 Synchr**	**Div-4 Asynchr**
10 GHz	-154.5 dBc/Hz	-153.5 dBc/Hz
20 GHz	N/A	-147.5 dBc/Hz
Simulated divider phase noise at $f_m = 2$MHz.		
$I_{gate} = 2I_{latch}$	**Div-4 Synchr**	**Div-4 Asynchr**
10 GHz	-153 dBc/Hz	-152 dBc/Hz
20 GHz	N/A	-149 dBc/Hz
$I_{gate} = I_{latch}$	**Div-4 Synchr**	**Div-4 Asynchr**
10 GHz	-155 dBc/Hz	-153.5 dBc/Hz
20 GHz	N/A	-148.5 dBc/Hz

D. Theory versus measurements

Since theory only models the various effects qualitatively and not quantitatively, we can only compare relative theoretical values. In particular, we focus on replacing an asynchronous by a synchronous architecture (accumulation effect), doubling the input frequency (sampling effect) and decreasing the biasing current in the cross-coupled pair.

1) Asynchronous against Synchronous: Theoretically, the asynchronous divider-by-4 contributes 3 dB more phase noise than its synchronous divider-by-4 equivalent. The total phase noise at the output node of the asynchronous architectures is

$$S_{\phi,asyn}(f_m) = (2\pi f_{out,1})^2 \frac{S_{v,1}(f_m)}{2Slope_1^2} + (2\pi f_{out,2})^2 \frac{S_{v,2}(f_m)}{Slope_2^2},$$

where $f_{out,x}$, $S_{v,x}$ and $Slope_x$ denote the frequency, the spectrum of the noise (in V^2/Hz) and the slope of the driving signal at node x, see Fig. 3. Since $f_{out,1} = 2f_{out,2}$, $S_{v,1} = S_{v,2}/2$ and $Slope_1 = Slope_2$, $S_{\phi,asyn}(f_m)$ becomes

$$S_{\phi,asyn}(f_m) = 2(2\pi f_{out,2})^2 \frac{S_{v,2}(f_m)}{Slope_2^2}. \quad (6)$$

For the synchronous divider-by-4 architecture, only the second divider stage is important,

$$S_{\phi,sync}(f_m) = (2\pi f_{out,2})^2 \frac{S_{v,2}(f_m)}{Slope_2^2}. \quad (7)$$

Subtracting eq. (7) from eq. (6) (reexpressed in dB units), we obtain $S_{\phi,async}(f_m) - S_{\phi,sync}(f_m) = 3$ dB, which deviates from the simulated and measured 1 dB value. We recall that input and output slope values are equal in both divider stages in our theoretical calculations. However, $Slope_2$ may be deteriorated with respect to $Slope_1$, since the loading conditions for each of the divider-by-2 stages are unequal, and hence, the percentage of total phase noise attributed to the second divider stage increases.

2) Sampling effect: We perform phase noise measurements at $f_{in} = 10$ GHz and $f_{in} = 20$ GHz and observe an increase of 3.5 dB. Theoretical calculations show that doubling the input frequency f_{in} increases the output phase noise by 3dB. For the asynchronous architecture, we calculate

$$S_{\phi,fin}(f_m) = (2\pi f_{out,2new})^2 \frac{S_{v,2new}(f_m)}{Slope_{new}^2}. \quad (8)$$

Fig. 6 assists us in extracting a set of relations. Since

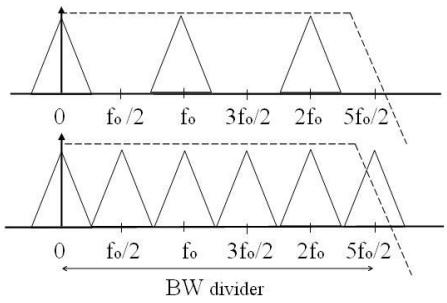

Fig. 6. Replicated spectra at the output of a divider when doubling f_{in}.

$f_{in,new} = 2f_{in}$, it holds that $f_{out,2new} = 2f_{out,2}$, $S_{v,2new} = S_{v,2}/2$ and $Slope_{new} = Slope$. Then, eq. (8) becomes

$$S_{\phi,2f_{in}}(f_m) = 2(2\pi f_{out,2})^2 \frac{S_{v,2}(f_m)}{Slope^2}. \quad (9)$$

Subtracting eq. (8) from eq. (9) (reexpressed in dB units), we obtain $S_{\phi,2f_{in}}(f_m) - S_{\phi,fin}(f_m) = 3$ dB. The theoretical calculations validate the measurements with the precondition that the value of $Slope$ at the output of the divider stages is analogous to BW. As we show subsequently, this assumption is under certain conditions invalid.

3) Biasing conditions: We recall the "adaptive frequency" divider architecture depicted in Fig. 4 and its feature of extending the maximum frequency of operation by decreasing the biasing current at the cross-coupled pair [4]. During our measurements, we observe that the improvement in maximum frequency of operation does not come at the cost of an increased phase noise performance. To the contrary, phase noise measurements performed with $I_{latch} = I_{gate}/2$ prove equally or less noisy than under $I_{latch} = I_{gate}$. The shot noise, which in great extent defines $S_v(f_m)$, decreases with I_{latch}. At moderate frequencies $f < f_o$, $Slope$ follows BW; hence, a higher I_{latch} means a higher $Slope$ value, Fig. 7. However, for

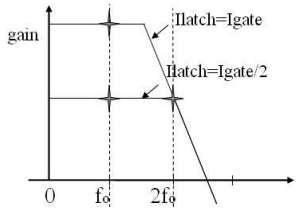

Fig. 7. Gain versus frequency at different biasing condition.

high frequencies $f \geq 2f_o$, where the gain is limited, the $Slope$ does not depend on BW any more, see Fig. 7. Therefore, phase noise becomes solely a function of $S_v(f_m)$ at these frequencies.

IV. Conclusions

We extended Phillips' model to include noise sources and effects occurring in a generic divider architecture. We also changed the model to include high frequency effects (such as AM to PM transformation in the divider interstages) as well as design parameters such as bandwidth of each synchronous divider stage BW_i, the number of asynchronous divider stages, and the division ratios N_i, that are better suited to our design objectives (high frequency, low phase noise and low power).

The measurements on the taped-out test-structures, at different biasing and frequency conditions, allowed us to observe the accumulation and sampling effects on the phase noise performance of the FD. We also observed that lowering the biasing current of the cross-coupled pair degrades the phase noise performance at moderate frequencies while it improves it at higher frequencies. Measurements and simulations match within 1 dB. Therefore, the "time domain" phase noise simulations of Spectre RF estimate accurately the phase noise in all cases considered in this paper.

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