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Phase-Shifted Energy Balance Control for Multilevel Inverters in Grid-Connected PV Systems

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Abstract: Cascaded multilevel converters are promising candidates for grid-connected PV systems, but low-frequency ripples may exist in a DC link. Such ripples are not just inherent; they can occur due to environmental factors, such as variations in a certain range of irradiance of the PV. To address this issue, this article proposes a clock phase-shifted (CPS) energy balance control method for grid-connected cascaded multilevel inverters for photovoltaic (PV) systems. The proposed control scheme can prevent the low-frequency ripple of the DC link propagating to the power grid. Furthermore, it is feasible in principle and no adjustment of the control parameters is needed. The simulation and experimental results verify the effectiveness and feasibility of the proposed approach.

Keywords: PV grid-connected inverter; energy conservation principle; cascaded multilevel converter

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1. Introduction

Motivated by environmental concerns, the promotion of distributed generation (DG) from renewable resources in power grids, such as solar and wind, is rapidly increasing [1,2]. As the cost per watt of PV systems has continuously reduced, the installed capacity of grid-connected solar PV energy conversion systems has increased substantially in recent years [3]. Thus, multilevel inverters are being investigated as an interesting option for grid-connected PV systems. Among the available multilevel converter topologies [4], the cascaded multilevel topology—in particular, the novel CSD multilevel topology proposed in [5]—is particularly attractive for grid-connected PV applications for the following reasons. 1. The required output voltage level can be achieved without a transformer. 2. The DC link voltages can be independently controlled, which is more suitable for the PV modules operate under mismatching conditions such as in the case of partial shadowing. 3. Compared to other cascaded multilevel inverter topologies [6–8], the novel CSD multilevel topology proposed in [5] can produce the same voltage levels with a lower number of switches and remove the high-voltage spikes by adding a spike remove switch.

However, the cascaded topology tends to require more rigorous control methods, particularly working in situations that accommodate for the motor drives in PV systems. The conventional phase-shifted PWM (PS-PWM), whose ability to suppress low-frequency fluctuations on the input side is weak, will undoubtedly lead to low-order harmonics pollution in the power grid, which causes distortions of the grid currents [9,10]. To resolve this problem, the most direct way is to increase the value of the capacitor of the DC link or add a passive filter [11,12], which will lead to a reduction in the system reliability. Active filtering methods have been proposed based on power electronic devices, which suppress low-frequency ripples by adding DC active power filters in the DC port of each cascaded unit [13,14]. Additionally, DC–DC converters have also been introduced between the DC link and each cascaded unit. By using specific control methods, the intermediate capacitance is forced to take almost all the double-frequency power, thus achieving the goal of

the ripple suppression of low-frequency input currents [15,16]. However, these methods present certain disadvantages related to the volume of the whole system, cost or structural complexity. In medium-voltage (MV) motor drives, the low-frequency pulsating power is reduced by replacing the half-bridge submodules (SMs) with full-bridge submodules. However, this undoubtedly increases the number of switches [17]. A new control strategy based on model predictive control (MPC) was proposed in [18]; using this strategy, the capacitor voltage ripple can be suppressed. In [19], combined with the intercross control structure, wherein the d-q currents are controlled by the feedforward decoupling control structure, the low-frequency voltage ripple can be suppressed in cascaded H-bridge (CHB) multilevel converters for large-scale grid-connected PV systems.

This work aimed to eliminate the low-frequency harmonic interferences caused by the low-frequency harmonic voltage ripples in the DC link. Thus, the proposed control method is useful as it helps to avoid sensitivity to environmental factors, such as light, temperature, etc. This is especially true for the PV system. This article is a conference extended version of [20] and includes a more detailed theoretical analysis of the proposed control method based on the energy balance, a more advanced (17-level) simulation and experimental verification of the proposed control scheme. The remainder of this article is organized as follows. Section 2 introduces the CSD multilevel topology. And based on the CSD topology, the control equation of the proposed control method is analyzed. The design and implementation of the proposed CPS energy balance control method are illustrated in Section 3. Sections 4 and 5 present the simulation and experimental results. Conclusions are provided in Section 6.

2. Deriving the Control Equation Based on the CSD Multilevel Topology

Figure 1 shows the block diagram of the PV CSD multilevel inverter with the proposed CPS energy balance control method. In Figure 1, the PV panels carry out the task of maximum power point tracking (MPPT). Because the goal of this research was to present a novel control method for the inverter, the MPPT stage was not implemented but emulated by DC sources with fluctuations, reflecting the low-harmonic voltage ripple.

As shown in Figure 1, the CSD topology comprises an n cascaded switched-diode converter, a spike removal switch S_g and a full-bridge inverter, where n is the number of cascaded basic units. The basic unit 1 shown in Figure 1 consists of a PV string and a capacitor, which are emulated by a DC voltage source with fluctuations, a switch S_{11} with its internal reverse diode and a diode D_{11}. Then, u_{o1} of the basic unit 1 will be one of two values, i.e., u_{c1} when S_{11} conducts and 0 when S_{11} is turned off. The spike-removal switch S_g provides a path for the reverse load current. It is connected between unit 2 and unit n and occurs when S_{11} is on and the other switches are off.

Table 1 shows the switch states of the second stage. As shown in Table 1, the positive and negative halves of output waveforms are detected during the second stage of the multilevel inverter by comparing the reference current i_{gref} with zero. Thus, the proposed CPS energy balance control method is designed for just the first stage, which only considers the positive state. The main principle of the proposed control method is to force the grid current to be equal to a desired value.

Table 1. Values of i_g with respect to switch states of the second stage [20].

State	Switches States				u_o	Condition
	S_1	S_2	S_3	S_4		
1	on	off	off	on	i_g	$i_{gref} \geqslant 0$
2	off	on	on	off	$-i_g$	$i_{gref} < 0$

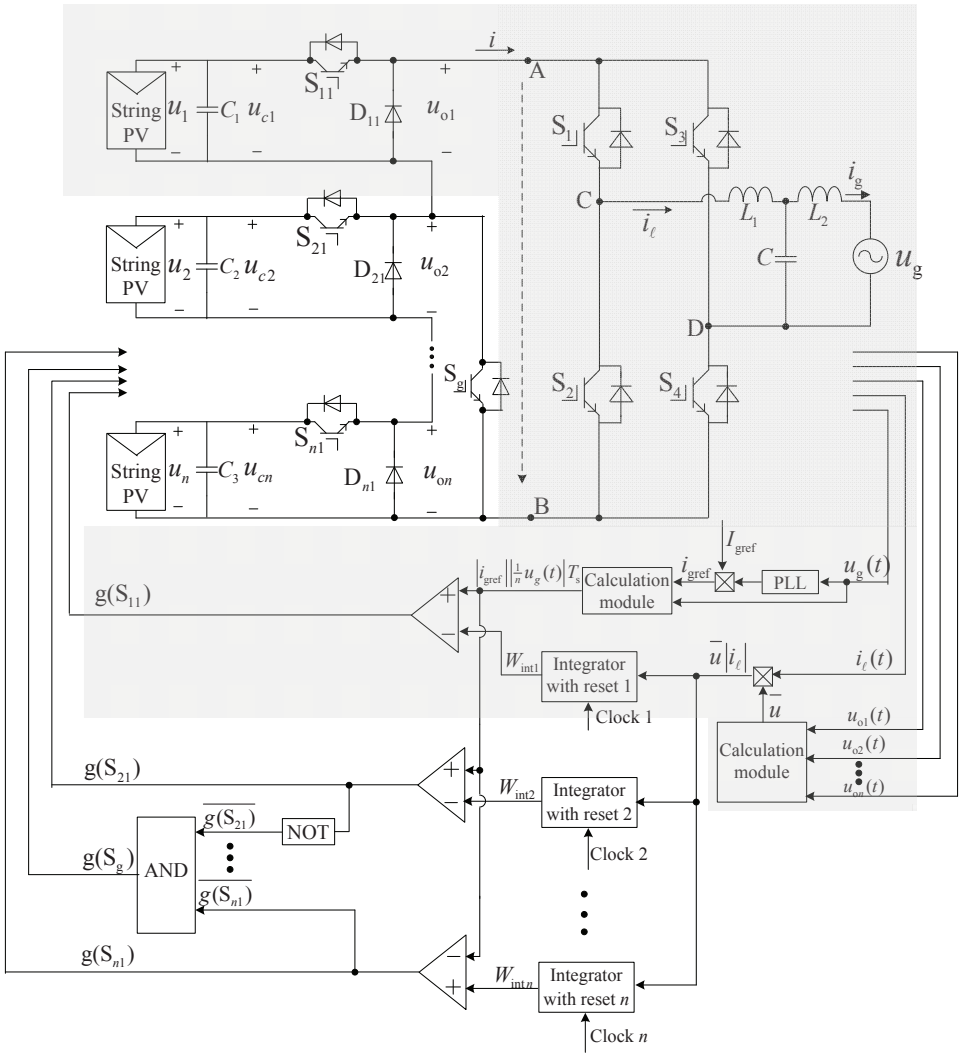

Figure 1. PV CSD multilevel inverter with the proposed CPS energy balance control method [20].

The following control equation is based on cascaded unit 1, as shown in Figure 2, which is the shaded part in Figure 1. For cascaded unit 1, the energy balance means that, during the n^{th} switching cycle $[(n-1)T_\text{s}, nT_\text{s})$, where T_s represents the switching cycle, the energy injected into the circuit is kept equal to the sum of the energy fed into the grid $W_{\text{g1}}(n)$, the stored energy of L_1 and L_2 as $\Delta W_\ell(n)$ and that of the capacitor C as $\Delta W_\text{c}(n)$:

$$W_{\text{in1}}(n) = W_{\text{g1}}(n) + \Delta W_\ell(n) + \Delta W_\text{c}(n) \quad (n = 1, 2, \cdots) \tag{1}$$

The circuit in Figure 2 can be seen as a buck converter, where u_{c1} emulates the PV panels. As a buck converter, during the n^{th} switching cycle, cascaded unit 1 operates in two states:

State 1: $-$ S_{11} is on for duration $t_{\text{on1}}(n)$ and, in this switching state, the energy is injected into the circuit and i_ℓ flows through the loop ($u_{\text{c1}} \rightarrow \text{S}_{11} \rightarrow \text{L}_1 \rightarrow \text{C} \parallel \text{L}_2$ and $u_\text{g} \rightarrow u_{\text{c1}}$). L_1 and L_2 are charged, the grid is fed energy and u_{o1} is derived using (2):

$$u_{\text{o1}}(t) = u_{\text{c1}} \quad (t \in [(n-1)T_\text{s}, (n-1)T_\text{s} + t_{\text{on1}}(n)) \tag{2}$$

State 2: $-$ S_{11} is off for duration $t_{\text{off1}}(n)$ and, in this switching state, no energy is fed into the circuit; however, i_ℓ flows through the loop ($\text{D}_{11} \rightarrow \text{L} \rightarrow \text{C} \parallel \text{R} \rightarrow \text{D}_{11}$). L_1 and L_2 are discharged, the grid is fed energy and u_{o1} is obtained using

$$u_{\text{o1}}(t) = 0 \quad (t \in [(n-1)T_\text{s} + t_{\text{on1}}(n), nT_\text{s}) \tag{3}$$

According to the above state analysis, the values of $W_{in1}(n)$, $W_{grid1}(n)$ during the n^{th} switching cycle can be obtained as follows:

$$W_{in1}(n) = \int_{(n-1)T_s}^{(n-1)T_s+t_{on1}(n)} u_{o1}(t)i(t)dt \tag{4}$$

substituting $i = |i_\ell(t)|$ into (4) results in:

$$W_{in1}(n) = \int_{(n-1)T_s}^{(n-1)T_s+t_{on1}(n)} u_{c1}(t)|i_\ell(t)|dt \tag{5}$$

$$W_{g1}(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} |\frac{1}{n}u_g(t)||i_{gref}(t)|dt \tag{6}$$

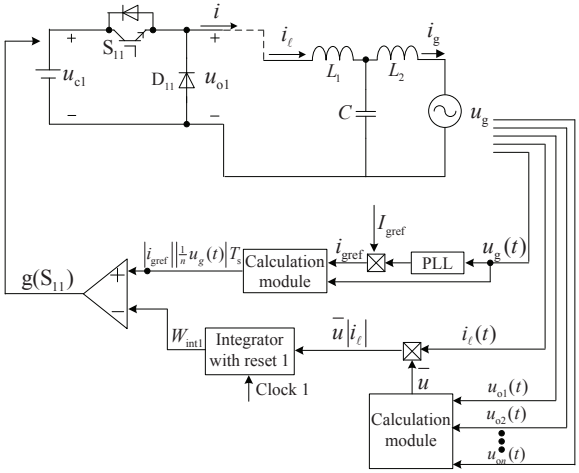

Figure 2. Cascaded unit 1 with the proposed CPS energy balance control method [20].

Additionally, the purpose of this control mechanism is to ensure that the grid current $i_g(n)$ is equal to the reference grid current i_{gref}; thus, i_g can be substituted by i_{gref}, which is regarded as a constant value in a switching cycle. Then, $u_{\ell 2}$ can be calculated as follows:

$$u_{\ell 2} = L\frac{di_g}{dt} = L\frac{di_{gref}}{dt} = 0 \tag{7}$$

Then, u_c is calculated as follows:

$$u_c = u_{\ell 2} + u_g = u_g \tag{8}$$

where u_g is the grid voltage, which can also be regarded as a constant value in a switching cycle; thus, i_c can be obtained in the following way:

$$i_c = C\frac{du_c}{dt} = C\frac{du_g}{dt} = 0 \tag{9}$$

Then, $i_{\ell 1}$ is calculated as follows:

$$i_{\ell 1} = i_c + i_g = i_g \tag{10}$$

From (10), it can be seen that $i_{\ell 1}$ is also regarded as a constant value since i_g can be substituted by i_{gref} as mentioned above. Then, $u_{\ell 1}$ can be obtained as follows:

$$u_{\ell 1} = L\frac{di_{\ell 1}}{dt} = 0 \tag{11}$$

In a buck converter, the inductors work in the entire cycle during each switching cycle n; as a result, the stored energy of the inductor is calculated using (12):

$$\begin{aligned}\Delta W_\ell(t) &= \Delta W_{\ell 1} + \Delta W_{\ell 2} \\ &= \int_{(n-1)T_s}^{(n-1)T_s+T_s} u_{\ell 1} i_{\ell 1} dt + \int_{(n-1)T_s}^{(n-1)T_s+T_s} u_{\ell 2} i_{\ell 2} dt\end{aligned} \tag{12}$$

By substituting (7) and (11) into (12), $\Delta W_\ell(n)$ can be derived as follows:

$$\Delta W_\ell(n) = 0 \tag{13}$$

Similarly, $\Delta W_c(n)$ can be obtained as $\Delta W_c(n) = 0$.

Thus, $\Delta W_\ell(n)$ and $\Delta W_c(n)$ in (1) can be ignored and, combining the aforementioned state analysis, the energy conservation in the circuit can be realized by controlling u_{o1}, which is expressed in (14):

$$\int_{(n-1)T_s}^{nT_s} u_{o1}(t)|i_\ell(t)|dt = |u_g||i_{gref}(t)|T_s \quad (n = 1, 2, \cdots) \tag{14}$$

3. The Design and Implementation of the Proposed CPS Energy Balance Control Method

The control Equation (14) can be implemented using comparison and integration, as shown in Figure 2. The control implementation for cascaded unit 1 is described as follows: at the beginning of a switching cycle, when the pulse of clock 1 arrives, S_{11} is turned on and the integrator starts working, whose value $W_{int1}(k)$ increases from its initial value. $W_{int1}(t)$ is compared with the control reference W_{g1} instantaneously. At the instant when $W_{int1}(t)$ reaches W_{g1}, the output of the comparator changes to a low level, which turns off S_{11}. Then, S_{11} is switched from the on state to the off state. S_{11} is switched off until the arrival of the next clock pulse, which resets the integrator and starts the $(n+1)^{th}$ switching cycle.

As shown in Figure 1, u_{o1} can be replaced by $\overline{u}$, which is the average value of all the values of the DC link (u_{c1}, $\cdots$, u_{c1}, u_{cn}); then, (14) can be rewritten as follows:

$$\int_{(n-1)T_s}^{nT_s} \overline{u}(t)|i_\ell(t)|dt = |u_g||i_{gref}(t)|T_s \quad (n = 1, 2, \cdots) \tag{15}$$

Thus, the input value of all the reset integrators can be obtained using (15). Additionally, the controls of the other cascaded units are similar to that of cascaded unit 1, but with a phase-shift for T_s/n of the clock pulse. Furthermore, the spike removal switch S_g, which is connected between unit 2 and unit n, is controlled by operations when S_{11} is on and S_{21} to S_{n1} is off.

4. Simulation Results

In order to verify the feasibility and performances of the proposed control method, a 5-level and a 17-level CSD topology were developed using MATLAB/Simulink. During the simulation, the MPPT stage was not implemented but simulated by DC sources with fluctuations. A comparative study using a conventional PS-PWM control method is presented to evaluate the performances of the proposed method. The PS-PWM grid-connected system was designed using the SISO tool of MATLAB with phase and amplitude margins of 32.7° and 7.61 dB, respectively.

4.1. Simulation Results of the 5-Level Topology

The diagram of a 5-level CSD topology is shown in Figure 3. It comprises a two-cascaded switched-diode converter, a spike removal switch S_g and a full-bridge inverter.

The spike removal switch S_g is connected between E and F and operates when S_{11} is on and S_{21} is off. The circuit parameters are listed in Table 2.

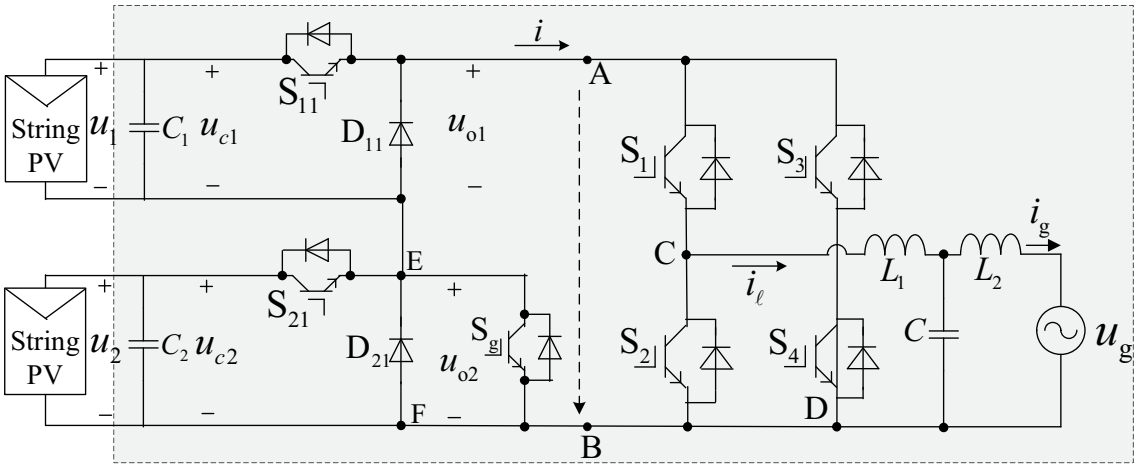

Figure 3. The diagram of a 5-level CSD topology.

Table 2. Circuit parameters of the 5-level CSD topology.

$u_{c1} = u_{c2}$	L_1	L_2	C	u_g	f_c
50 V	4 mH	2 mH	2.2 μF	80 V	2500 Hz

Where 80 V is the amplitude of u_g, and its frequency is 50 Hz.

Figures 4 and 5 show the simulation results of the operation of the PV cascaded multilevel grid-connected inverter with the proposed control method. From Figure 4, it can be observed that, as the sum of the output value of all the cascaded units, u_{AB} and the current i of the first-stage have zero and positive values. Figure 5 shows the waveform of u_{CD}, which is a 5-level stepped waveform. The waveform of i_g in Figure 5 illustrates that, after the $L - C - L$ filter, it is sinusoidal and in phase with the grid voltage.

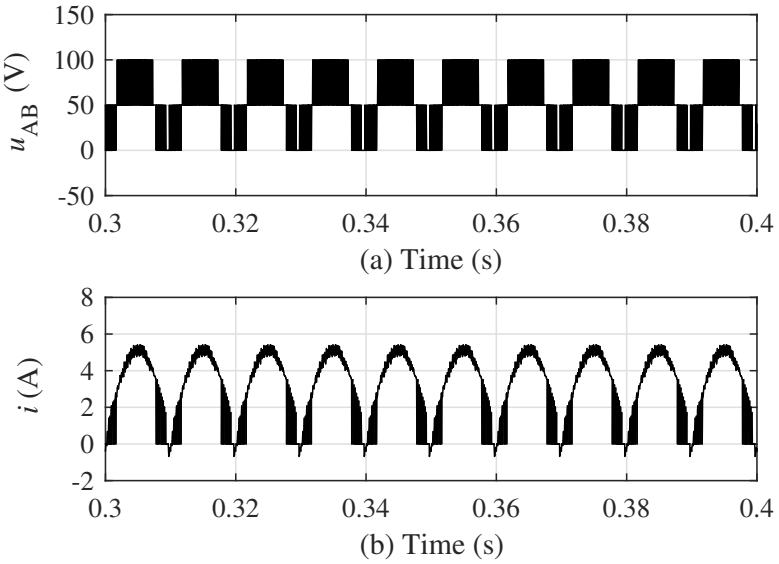

Figure 4. The 5-level simulation results of the first stage. (**a**) u_{AB}; (**b**) i.

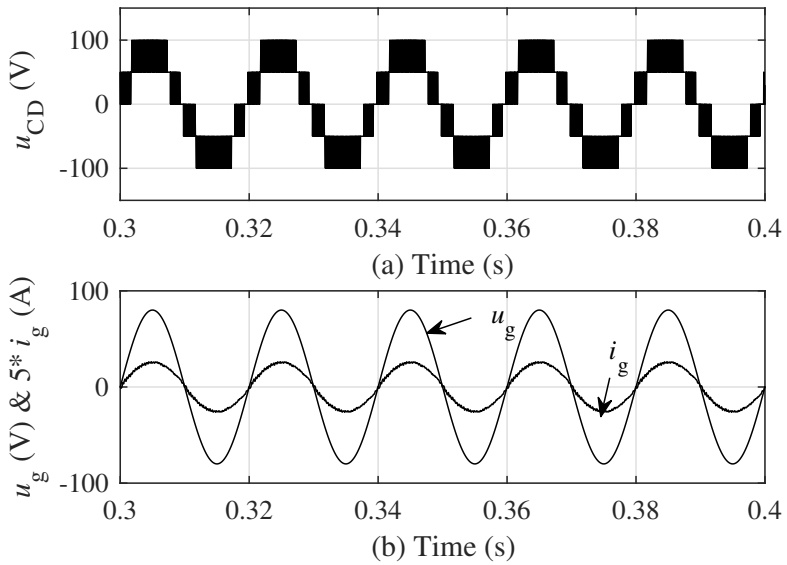

Figure 5. The 5-level simulation results of the stepped voltage, the grid voltage and current. (**a**) u_{CD}; (**b**) u_g and i_g after filter.

The THD of the stepped output voltage waveform u_{CD} of the 5-level multilevel inverter is 38.39%, as shown in Figure 6. The frequencies of the main harmonics are twice the switching frequency (2500 Hz) and its multiples. After the $L-C-L$ filter, the THD of i_g is 3.09%, as shown in Figure 7. Additionally, the calculation result of the power factor is 99.98%, which means that the power factor is almost unity.

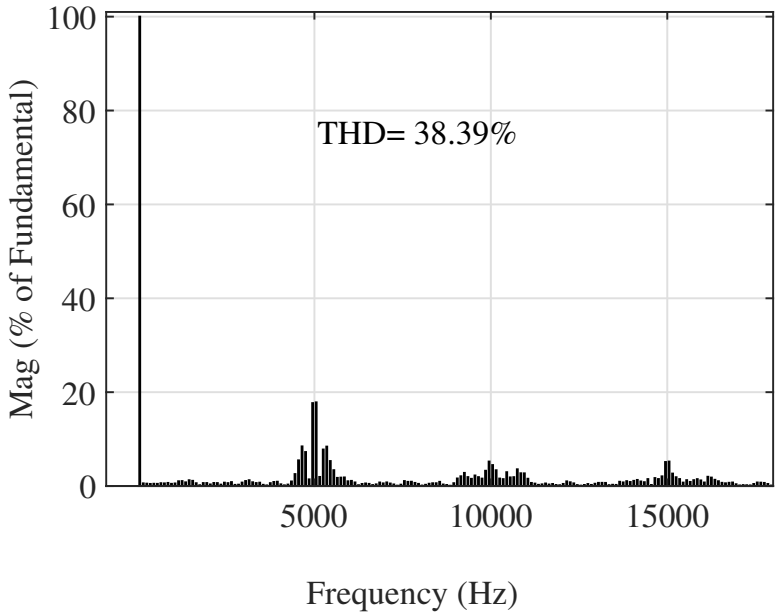

Figure 6. The FFT analysis result of the simulation result of u_{CD} [20].

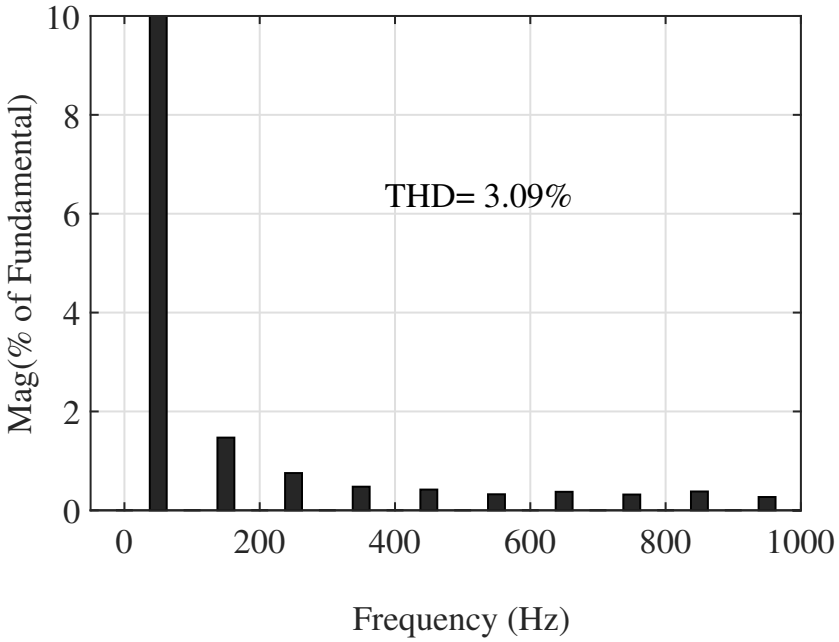

Figure 7. The FFT analysis result of the simulation result of u_g [20].

From these results, it is clear that the proposed CPS energy balance control method is feasible for the CSD multilevel inverter for the grid-connected PV system.

Figure 8 show the 5-level simulation results of the suppression ability against second-order harmonics in a DC link, which is realized by adding second-frequency harmonic ripples into the DC link voltages of each cascaded unit. Figure 8 illustrates the results under the case where the DC link is added with a second-harmonic voltage ripple, which has an amplitude of 8 V. Although the distortion caused by this harmonic is not obvious from the waveform, the FFT analysis of Figures 9 and 10 illustrate that i_g using PS-PWM contains corresponding harmonics to those of the DC link voltage, whose THD has increased to 4.17%. In contrast, the THD of i_g using the proposed control method is 3.17%, with a slight increase.

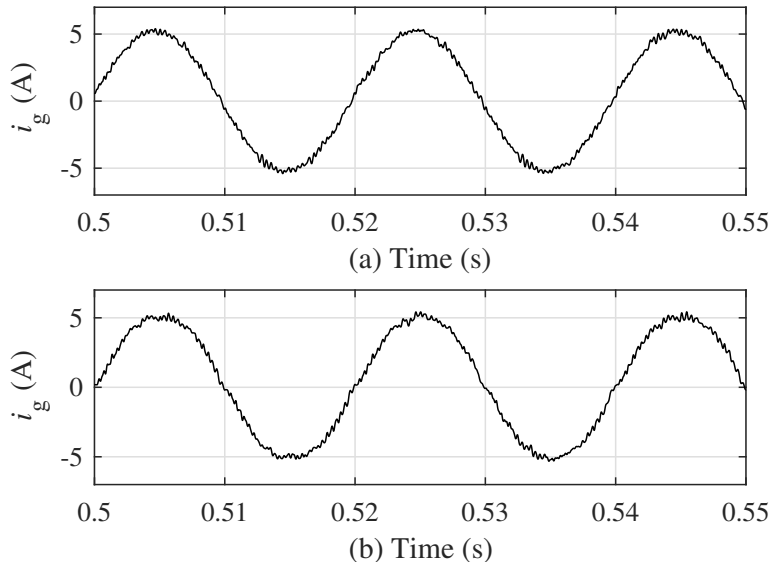

Figure 8. The 5-level simulation results for the DC link, including the second-harmonic ripple. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM [20].

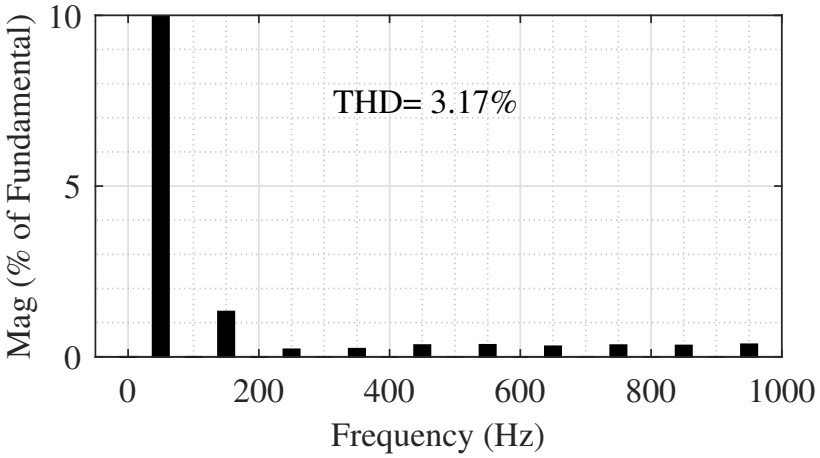

Figure 9. The 5-level FFT analysis result with the proposed controller under DC link, including second-harmonic ripple [20].

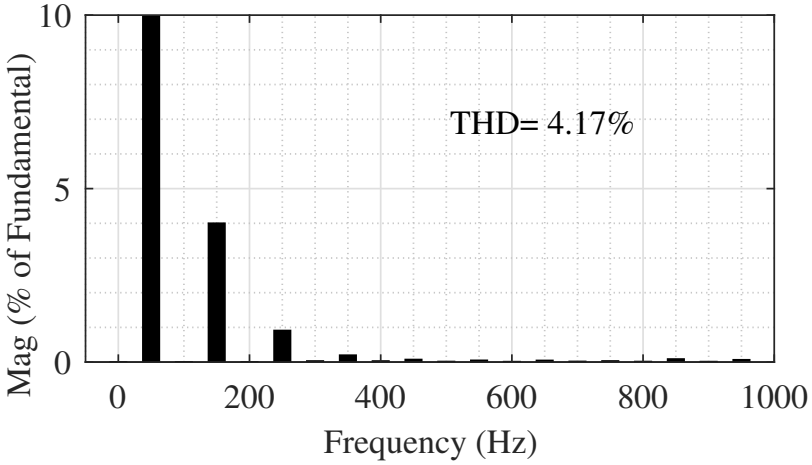

Figure 10. The 5-level FFT analysis result with the PS-PWM under DC link, including second-harmonic ripple [20].

Although the harmonics that the PV system may contain are mainly the second-harmonic voltage ripples, other low-frequency harmonics may also be caused by environmental factors; for example, the irradiance level varies in a certain range. Thus, third-harmonic voltage ripples with an amplitude of 8 V are added in DC links of the 5-level topology. The simulation results are shown in Figure 11. From the waveform in Figure 11a, it can be seen that, using the proposed control method, i_g remains a consistent output, and the FFT analysis of Figure 12 illustrates that the THD is 3.18%, with a slight increase. In contrast, the waveform when using the PS-PWM control method is distorted obviously, as shown in Figure 11b. Additionally, from the FFT analysis of Figure 13, it can be observed that the corresponding harmonics propagate from the DC link to the power grid, leading the THD to increase to 5.17%.

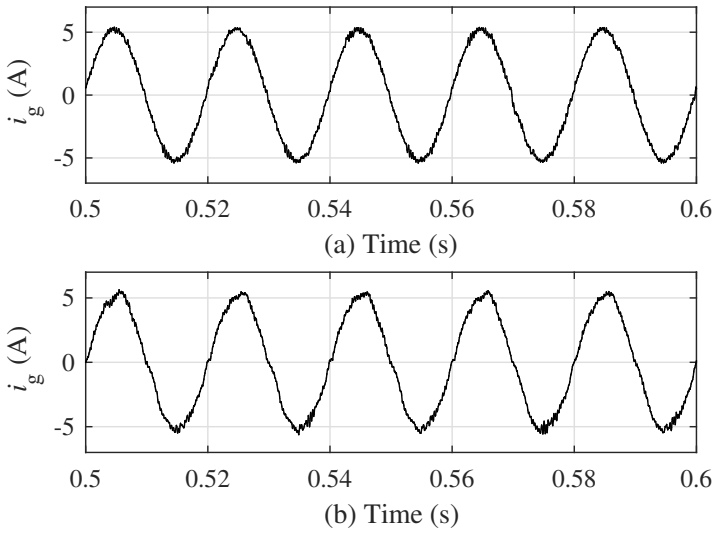

Figure 11. The 5-level simulation results in the DC link, including the third-harmonic ripple. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM [20].

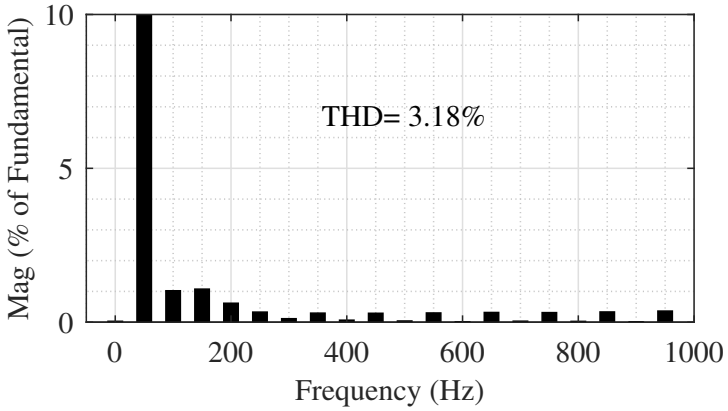

Figure 12. The 5-level FFT analysis result with the proposed controller under DC link, including third-harmonic ripple.

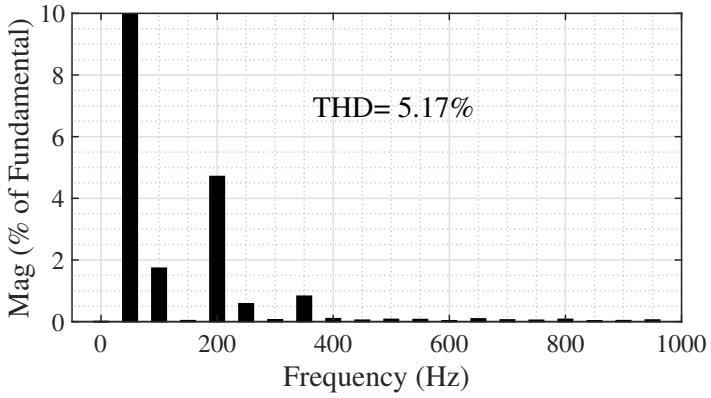

Figure 13. The 5-level FFT analysis result with the PS-PWM under DC link, including second-harmonic ripple.

4.2. Simulation Results of the 17-Level Topology

The 17-level CSD topology is similar to that of the 5-level topology shown in Figure 3. However, it comprises an eight-cascaded switched-diode converter, a spike removal switch S_g and a full-bridge inverter. The spike removal switch S_g is connected between unit 2 and

8 and works when S_{11} is on and all the other switches are off. The circuit parameters are listed in Table 3.

Table 3. Circuit parameters of 17-level CSD topology.

$u_{c1} = u_{c2} = ... = u_{c8}$	L_1	L_2	C	u_g	f_c
50 V	1.6 mH	0.8 mH	1.1 μF	360 V	2500 Hz

Where 360 V is the amplitude of u_g, and its frequency is 50 Hz.

Figures 14 and 15 show the simulation results of the operation of the 17-level CSD cascaded multilevel grid-connected inverter with the proposed control method. From Figure 14, it can be observed that, as the sum of the output value of all the cascaded units, u_{AB} and the current i of the first stage has zero and positive values. Additionally, Figure 15 shows the waveform of u_{CD}, which is a 17-level stepped waveform. The waveform of i_g in Figure 15 illustrates that, after the $L - C - L$ filter, it is sinusoidal and in phase with the grid voltage.

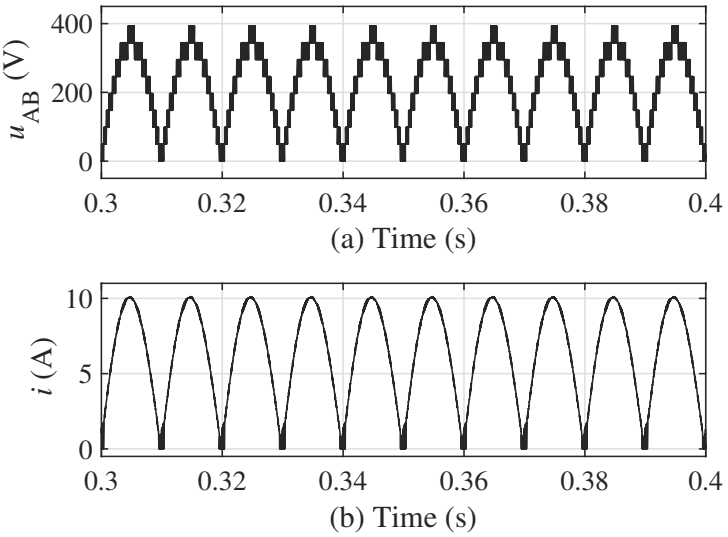

Figure 14. The 17-level simulation results of the first stage. (**a**) u_{AB}; (**b**) i.

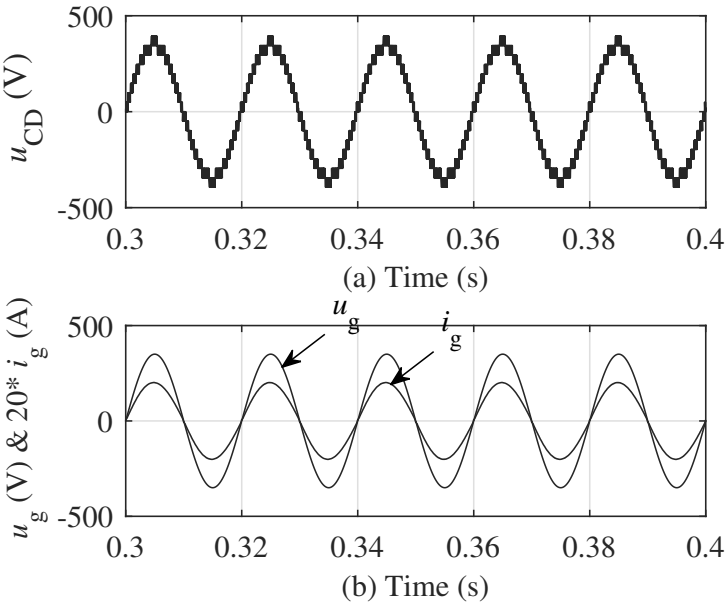

Figure 15. The 17-level simulation results of the stepped voltage, the grid voltage and current. (**a**) u_{CD}; (**b**) u_g and i_g after filter.

The THD of the stepped output voltage waveform u_{CD} of the 17-level multilevel inverter is 7.88%, as shown in Figure 16. The frequencies of the main harmonics are eight times the switching frequency (2500 Hz) and its multiples. Compared with the THD of u_{CD} of the 5-level multilevel inverter, the THD is lower and the frequencies that the main harmonics focus on move backward. Figure 17 shows the THD of i_g, which is 1.36%. Additionally, the calculation result of the power factor is 99.982%, which means that the power factor is close to unity.

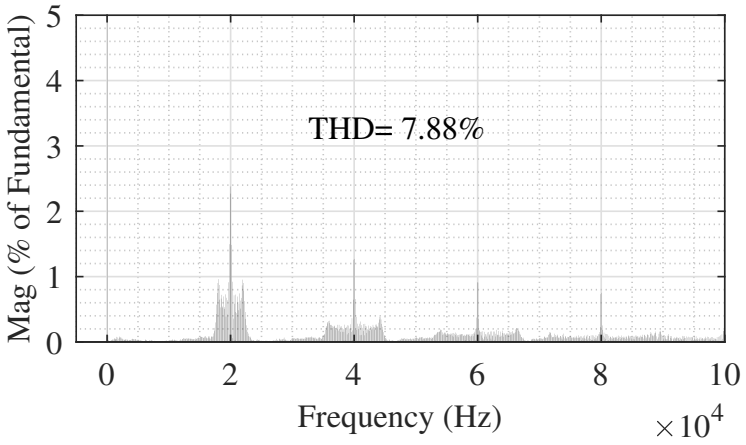

Figure 16. The 17-level FFT analysis result of the simulation result of u_{CD}.

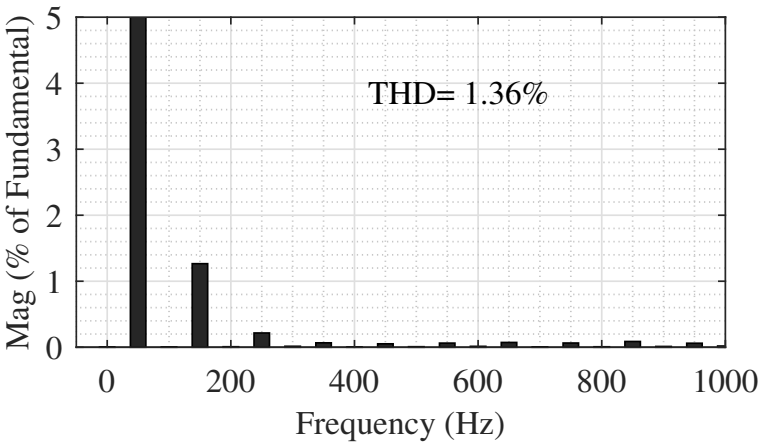

Figure 17. The 17-level FFT analysis result of the simulation result of i_g.

From these results, it is clear that the proposed CPS energy balance control method is feasible for the CSD multilevel inverter for the grid-connected PV system.

Figure 18 illustrates the results of the case where the DC link is added with a second-harmonic voltage ripple, which has an amplitude of 8 V. Although the distortion caused by this harmonic is not obvious, as shown in the waveforms, the FFT analysis of Figures 19 and 20 illustrates that i_g using PS-PWM contains corresponding harmonics to those of the DC link voltage, for which the THD increased to 2.92%. In contrast, the THD of i_g using the proposed control method is 1.49%, with a slight increase.

Figure 21 illustrates the results of the case where the DC link is added with a third-harmonic voltage ripple, which has an amplitude of 8 V. From the waveform in Figure 21a, it can be seen that, using the proposed control method, i_g is a consistent output, and the FFT analysis of Figure 22 illustrates that the THD is 1.41%, with a slight increase. In contrast, the waveform when using the PS-PWM control method is distorted clearly, as shown in Figure 21b. Additionally, from the FFT analysis of Figure 23, it can be observed that corresponding harmonics propagate from the DC link to the power grid, leading to the THD increasing to 4.25%.

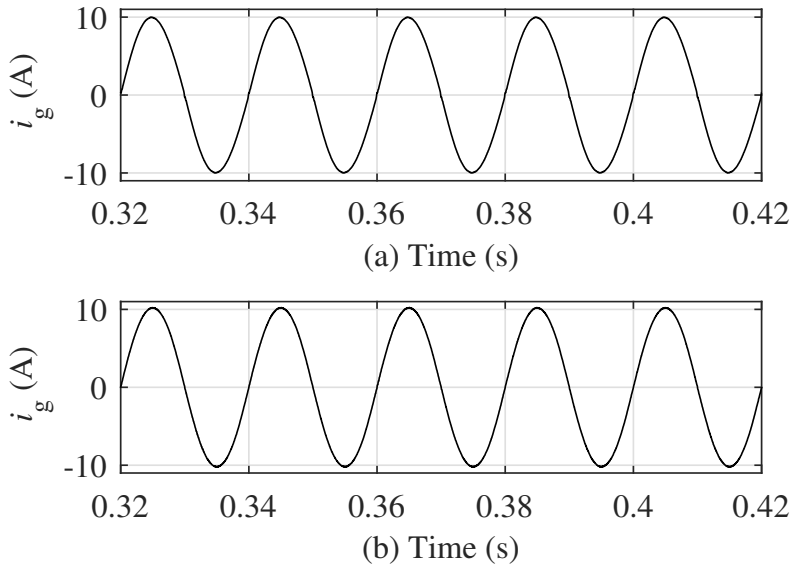

Figure 18. The 17-level simulation results under DC link, including second-harmonic ripple. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM.

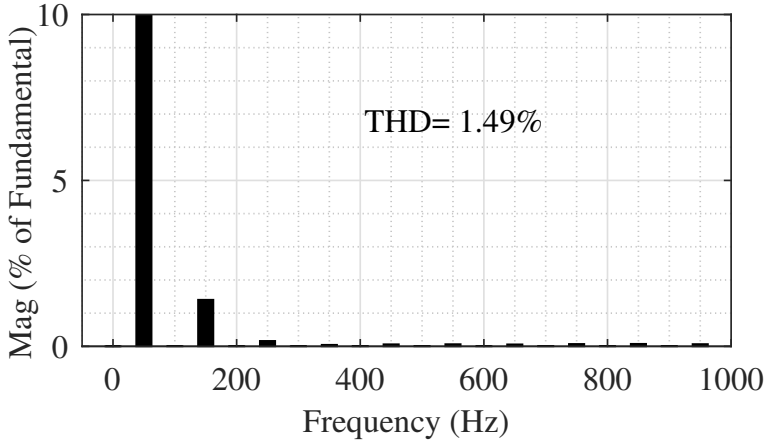

Figure 19. The 17-level FFT analysis result with the proposed controller under DC link, including second-harmonic ripple.

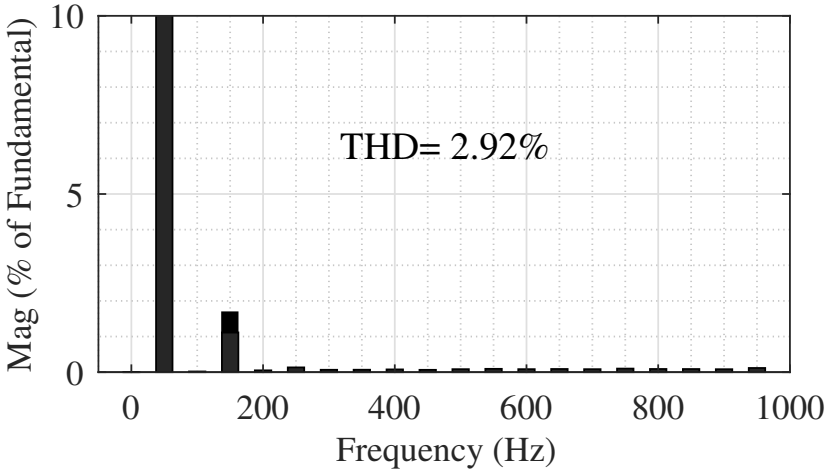

Figure 20. The 17-level FFT analysis result with the PS-PWM under DC link, including second-harmonic ripple.

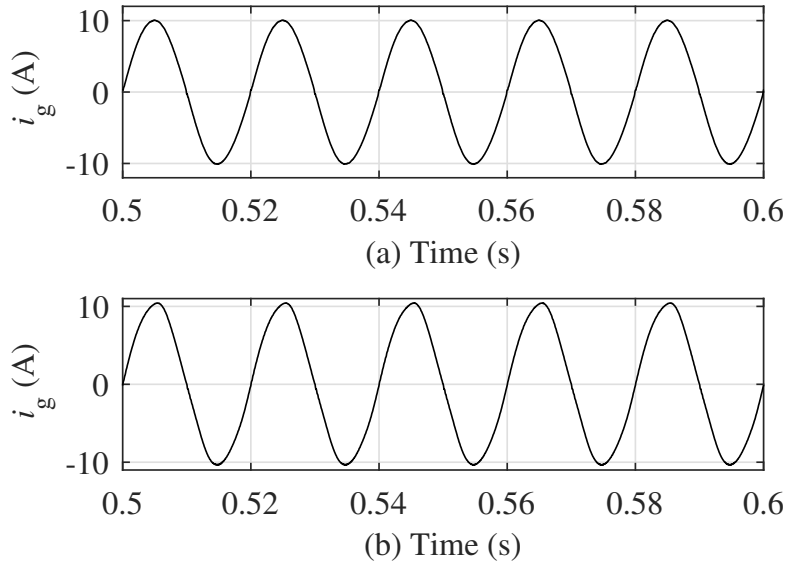

Figure 21. The 17-level simulation results under DC link, including third-harmonic ripple. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM.

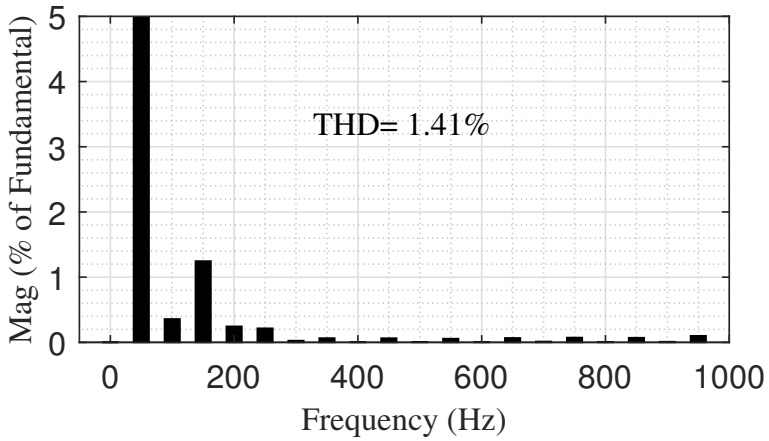

Figure 22. The 17-level FFT analysis result with the proposed controller under dDC link, including three-harmonic ripple.

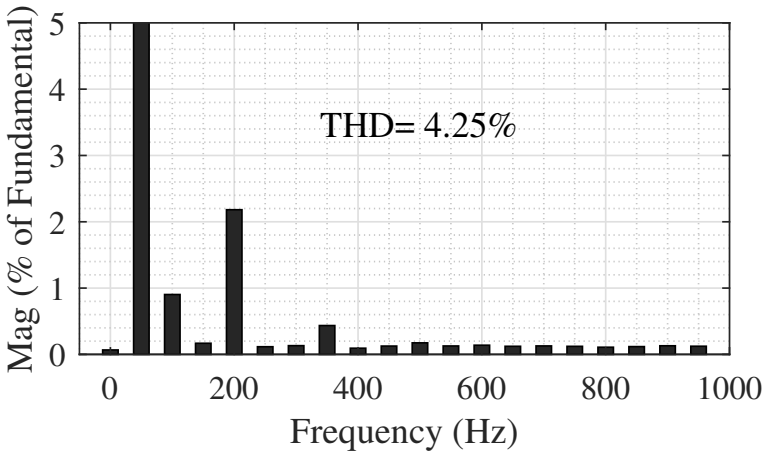

Figure 23. The 17-level FFT analysis result with the PS-PWM under DC link, including second-harmonic ripple.

5. Experimental Verification

According to the parameters listed in Table 2, a 5-level experimental prototype was built, as shown in Figure 24. In the experiment, a real-time implementation of the hardware-in-the-loop (HIL) system was used to verify the proposed CPS energy balance control method. The model of a 5-level CSD topology was developed in the electromagnetic transient simulation software StarSim, and ran on a PXI-FPGA-based real time HIL system with a time step of 1×10^{-3}. The HIL testing system parameters were the same as the ones in the simulation tests. The control methods were implemented using the RTlab 5600 platform. The sampling period of the controller and the switching frequency were selected as 20 μs and 2.5 kHz, respectively. The connection of the HIL simulation system and RTlab 5600 was implemented by using many IO channels. The oscilloscope measured the output voltage and grid current of the 5-level CSD topology.

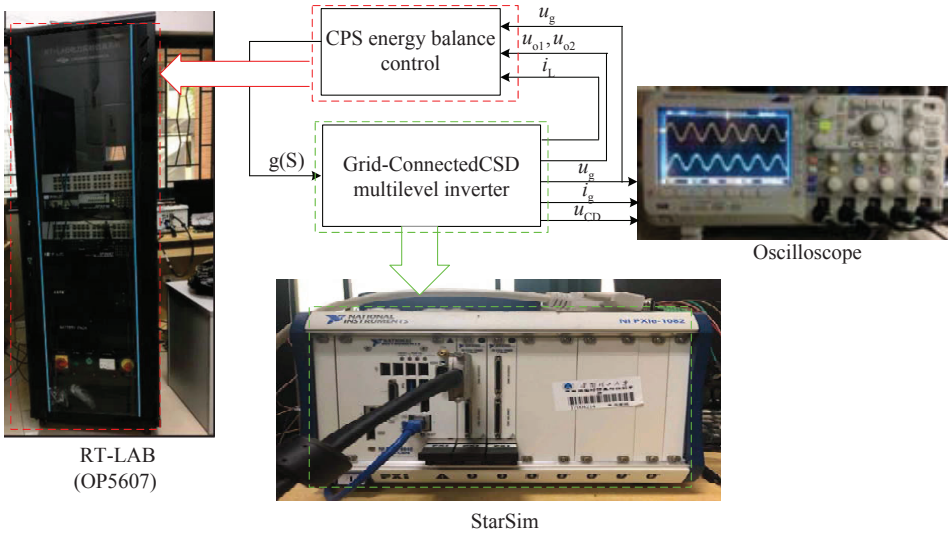

Figure 24. The 5-level experimental topology.

Figure 25 shows the experimental results of the 5-level topology using the proposed control method. The stepped voltage, grid voltage and current are depicted. It can be observed that the experimental results are consistent with the simulation results in Figure 5. A 5-level staircase waveform was implemented, the grid current was sinusoidal and synchronization took place with the grid voltage. The results of the FFT analysis illustrate that the THD is 40.47% of u_{CD} and 4.09% of i_g. The power factor is calculated as 98.28%.

Figures 26 and 27 show the comparison results of the prevention of low-frequency ripples of the DC link propagating to the power grid. From the results, it can be demonstrated that the experimental results are consistent with the simulation results shown in Figures 26 and 27, meaning that i_g using PS-PWM contains corresponding harmonics from the fluctuations in the DC link. In contrast, when using the proposed control method, there are almost no new harmonics propagated to i_g. These results illustrate that the proposed control method has a superior ability and can prevent the low-frequency ripple of the DC link propagating to the power grid.

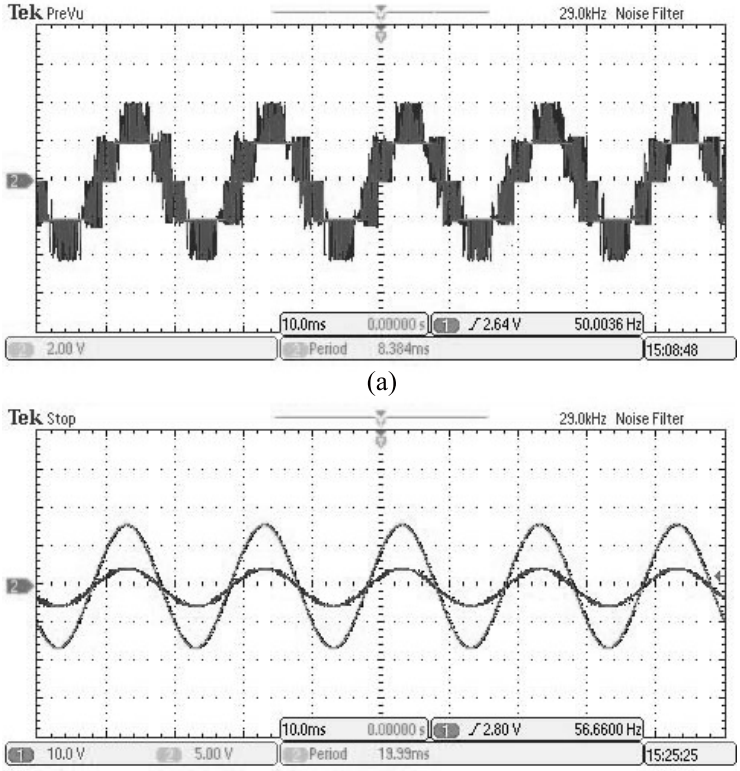

Figure 25. The experimental results of the 5-level prototype using the proposed control method. (**a**) The stepped voltage u_{CD}; (**b**) the grid voltage u_g and current i_g after filtering.

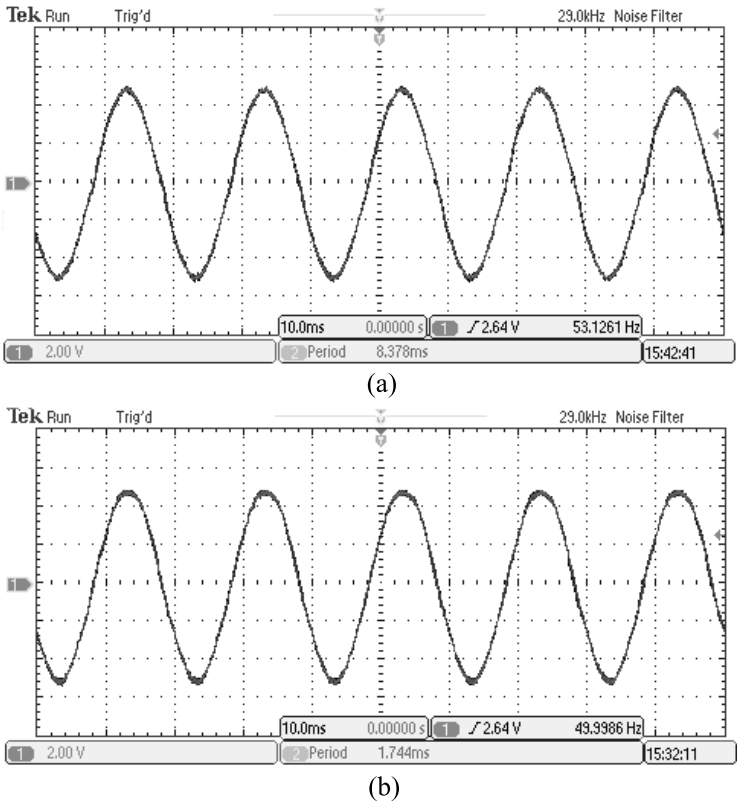

Figure 26. The experimental results under DC link, including three harmonic ripples. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM

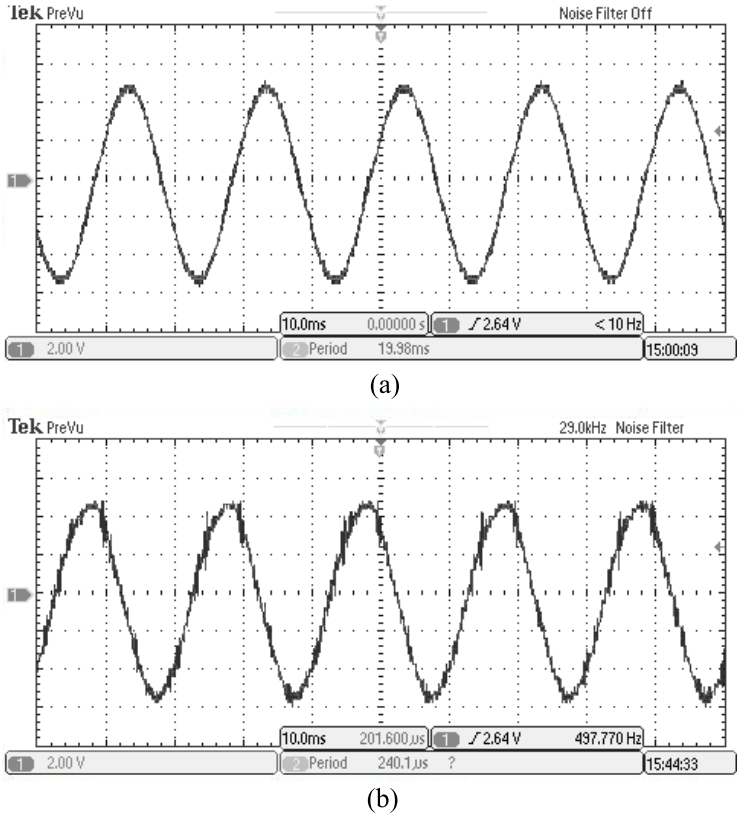

Figure 27. The experimental results under DC link, including third-harmonic ripple. (**a**) i_g using the proposed control method; (**b**) i_g using PS-PWM

6. Conclusions

Based on the energy balance principle in the circuit, a CPS energy balance control method was proposed for PV-cascaded multilevel grid-connected inverters in this paper. At first, the control principle is introduced and the control equation was analyzed and derived. By shifting the phase of the clock pulse of each cascaded unit, the control method was implemented using a comparator and integrator. The analysis and results illustrate that it has a simple structure and is simple to implement. Taking the 5-level and 17-level prototypes as examples, the feasibility and performance of the method were tested and verified by performing simulations and experiments. The results reveal that the proposed CPS energy balance control method can obtain staircase-like voltage waveforms and a grid sinusoidal input current with a low harmonic distortion. Moreover, compared to the PS-PWM method, the proposed CPS energy balance control method has a superior ability in the prevention of low-frequency ripples of the DC link propagating to the power grid. These results provide new insights for the control of multilevel inverters of grid-connected PV applications. In this study, we assessed the proposed CPS energy balance control method's ability to prevent low-frequency ripples in the DC link; in the future, its ability to alleviate the inter-bridge power imbalance and tracking ability of the reference current will be studied.

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Abbreviations

The following abbreviations are used in this manuscript:

CPS	clock phase-shifted
PV	photovoltaic
DG	distributed generation
CSD	cascaded switched-diode
THD	total harmonic distortion
PS-PWM	phase-shifted pulse width modulation
MPPT	maximum power point tracking

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