Photonic A/D Conversion Using Low-Temperature-Grown GaAs MSM Switches Integrated With Si-CMOS

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***Abstract*—By linking the unique capabilities of photonic devices with the signal processing power of electronics, photonically sampled analog-to-digital (A/D) conversion systems have demonstrated the potential for superior performance over all-electrical A/D conversion systems. We adopt a photonic A/D conversion scheme using low-temperature (LT)-grown GaAs metal–semiconductor–metal (MSM) photoconductive switches integrated with Si-CMOS A/D converters. The large bandwidth of the LT GaAs switches and the low timing jitter and short width of mode-locked laser pulses are combined to accurately sample input frequencies up to several tens of gigahertz. CMOS A/D converters perform back-end digitization, and time-interleaving is used to increase the total sampling rate of the system. In this paper, we outline the development of this system, from optimization of the LT GaAs material, speed and responsivity measurements of the switches, bandwidth and linearity characterization of the first-stage optoelectronic sample-and-hold, to integration of the switches with CMOS chips. As a final proof-of-principle demonstration, a two-channel system was fabricated with LT GaAs MSM switches flip-chip bonded to CMOS A/D converters. When operated at an aggregate sampling rate of 160 megasamples/s, the prototype system exhibits ∼3.5 effective number of bits (ENOB) of resolution for input signals up to 40 GHz.**

***Index Terms*—Photonic analog-to-digital (A/D) conversion, low-temperature (LT)-grown GaAs, metal–semiconductor–metal (MSM) devices, optical data processing, sample-and-hold circuits.**

I. Introduction

With rapidly increasing signal bandwidths along with the predominance of digital technologies and techniques, the need for higher speed analog-to-digital (A/D) conversion arises in order to interface between the analog and digital domains. Applications for A/D conversion at tens of gigasamples/s (GSa/s) exist in the areas of high-speed test and measurement [1], optical communications, and wireless communications and radar. For the last area, a high-speed A/D converter would allow direct digitization of the input signal at the front-end of the receiver, eliminating many performance limiting components used in a traditional receiver by digitally processing the input.

Despite the demand for higher speed A/D conversion systems, progress has been incremental in electrical mixed-signal technologies [2]. With CMOS-based high-speed A/D converters, multiple channels are time-interleaved to increase the total sampling rate of the system [1], [3]. With a large number of channels, however, performance is often limited by phase error in the clock (timing jitter and skew), due to difficulty in distributing a precise, high-speed clock over a large area. As an example, the state of the art in CMOS/SiGe A/D conversion technology utilizes a time-interleaved architecture with 80 channels, but is limited by a root-mean-square (rms) clock phase error of 700 fs, achieved after extensive calibration of skew [1]. A survey of A/D conversion systems conducted by Walden highlights this problem, indicating that most high-speed systems' performance corresponds to a phase error value $>\sim$500 fs [2]. As an alternative, research on GaAs- and InP-based circuits for mixed-signal systems has occurred in order to take advantage of the higher speed of III–V technologies, but advances have been slow, with the additional drawback of high power consumption for these systems [4]–[6].

II. Photonic A/D Conversion

The notion of using photonics to obtain superior sampling capability of electrical signals has been considered for several decades [7]. In particular, the mode-locked laser provides an ideal clock source for sampling applications as a result of its low-timing-jitter and short-width output pulses. Equally significant is the relative ease of clock distribution to multiple nodes without a consequential increase in amplitude and phase noise, due to the robust nature of photons for transmitting information. Extensive research on mode-locked lasers over the years has led to shorter pulses, higher efficiencies, and better noise performance [8].

To leverage these exceptional characteristics of mode-locked lasers and photonic technology for sampling, Taylor initially proposed a photonically sampled A/D conversion scheme using an array of electrooptic (EO) waveguide modulators [9], [10]. Recent research efforts have built upon this early work, with

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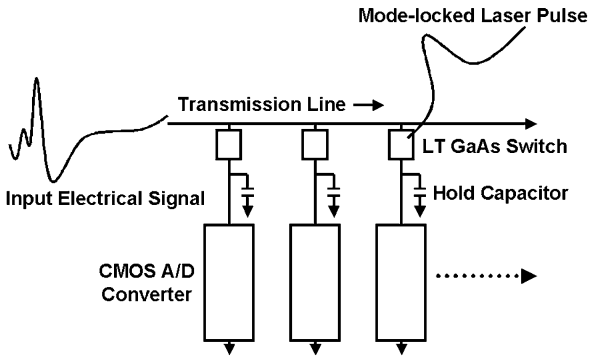

Fig. 1. Diagram of proprosed photonic A/D conversion system. A high-speed optoelectronic sample-and-hold is followed by digitization with a CMOS A/D converter. Multiple channels are time-interleaved to increase the aggregate sampling rate of the system.

various approaches demonstrating the potential for performance surpassing that of all-electrical systems. Many of these photonic A/D conversion systems encode the input electrical signal onto an optical pulse train using a lithium niobate Mach–Zehnder modulator. A time-interleaving architecture is implemented by demultiplexing these pulses to multiple quantization channels, each running at a fraction of the total sampling rate [11]–[14]. Time-stretching techniques in which the encoded optical signal is linearly scaled in time using dispersion have been successful in obtaining high effective sampling rates, at the expense of potential information loss [15]. A number of other schemes have also been investigated [16]–[19].

Our proposed photonic A/D conversion system utilizes a sample-and-hold scheme with low-temperature (LT)-grown GaAs metal–semiconductor–metal (MSM) switches. A diagram of the system is shown in Fig. 1. The switch is attached to a high-speed electrical transmission line, with the other end attached to a hold capacitor. As the input electrical signal propagates down the line, a mode-locked laser pulse optically triggers the switch, sampling the signal onto the hold capacitor. An electrical A/D converter running at the laser repetition rate then digitizes this held signal. By time-interleaving a number of these channels, with an appropriately phase aligned optical clock for each channel, the aggregate sampling rate of the system is increased. In this architecture, the bandwidth and timing requirements for high-speed sampling are placed on the input sample-and-hold, allowing use of slower electrical A/D converters to perform digitization at the back-end of the system. The mode-locked laser allows distribution of a low-timing-jitter, short-aperture-time gating function over a large area, enabling accurate sampling of high frequency inputs in a time-interleaved architecture with a large number of channels. The short carrier lifetime of LT-grown GaAs leads to picosecond-order switch turn-off times. Thus, the large bandwidth of the optically triggered electrical switches allows direct utilization of the low-timing-jitter, high-bandwidth nature of the optical pulses to provide the desired broadband sample-and-hold.

Our system offers advantages over other photonic A/D conversion systems due to its simplicity. An optical clock can be generated for each channel by splitting the master clock into multiple beams and subsequently aligning their phases with low skew, both of which are fairly common optical functions. Presumably, no tuning of the optical fabric occurs after initial calibration. More significantly, no switching functionality is required of the fabric, obviating the difficulties associated with optically demultiplexing to many channels [20]. Using a sample-and-hold scheme relaxes the need for switch linearity, provided the held signal saturates to the input voltage value during sampling. In addition, the sample-and-hold is relatively immune to amplitude fluctuations and spatial misalignment of the optical pulses. Finally, the system could be made compact with low power dissipation, by integrating the MSM switches and CMOS A/D converters onto a single chip.

In this paper, we describe the development of our A/D conversion system, from optimization of the LT GaAs material, speed and responsivity measurements of the switches, bandwidth and linearity characterization of the sample-and-hold, to integration of the switches with CMOS chips. The final system is a two-channel test chip, with CMOS A/D converters fabricated in a 0.24-μm CMOS technology for 1 GSa/s, 4-bit operation per channel. LT GaAs MSM switches were integrated with the CMOS circuits using a flip-chip bonding technique. This prototype system demonstrates a peak signal-to-noise-plus-distortion ratio (SNDR) of $\sim$23 dB [3.5 effective number of bits (ENOB)] and a spurious-free dynamic range (SFDR) of $\sim$ 29 dB over a 40-GHz input bandwidth. For a 25-μs measurement period, an rms timing jitter of $<$80 fs is obtained. To our knowledge, our system is the first hybrid photonic/CMOS A/D conversion system. Portions of this work have been briefly described elsewhere [21]–[24].

III. LT GaAs

The semiconductor material used for the MSM switch is LT GaAs, which is GaAs grown at a lower substrate temperature (200–400 °C) than the normal growth temperature of $\sim$600 °C. Growth at these temperatures incorporates excess arsenic into the crystal lattice, creating various arsenic related point defects in the form of gallium voids $(\mathrm{V_{Ga}})$, arsenic interstitials $(\mathrm{As_i})$, and arsenic substitutionals $(\mathrm{As_{Ga}})$ that can act as carrier trapping sites. As the growth temperature is decreased, defect densities increase dramatically, leading to subpicosecond carrier lifetimes. $\mathrm{As_{Ga}}$ is the most numerous defect, with concentrations of 10^{20} cm^{-3} reported for lower growth temperatures [25]. These large concentrations lead to hopping conduction within the deep defect band of $\mathrm{As_{Ga}}$ and low material resistivity [26]. In addition, thicker growths can result in poor crystal quality due to built-in strain in the LT-grown material caused by the substitutionals [27].

Postgrowth annealing of LT GaAs causes formation of arsenic precipitates within the material, reducing the $\mathrm{As_{Ga}}$ and $\mathrm{V_{Ga}}$ populations in the process [28]. In general, higher temperature and longer duration anneals lead to larger average precipitate size, lower precipitate concentration, and further reduction in $\mathrm{As_{Ga}}$ and $\mathrm{V_{Ga}}$ concentrations [29]. The precipitates behave as effective trapping sites for both electrons and holes.

Annealing has several important consequences. Despite a reduction in the $\mathrm{As_{Ga}}$ and $\mathrm{V_{Ga}}$ populations, precipitate formation

maintains a short overall carrier trapping time. The material becomes semi-insulating as a result of reduced hopping conduction and the remaining substitutionals pinning the Fermi-level near midgap [25]. In addition, the mobility of the material may improve due to the reduced number of substitutionals and repair of any large-scale defects. Overall, different combinations of growth temperature, anneal temperature/length, and growth thickness can cover a large range of material properties, including various mobilities and carrier trapping times.

LT GaAs compares favorably to other "fast" materials for use in photoconductive switches [30]. Picosecond-order carrier trapping times lead to fast switch turn-off and large bandwidth. LT GaAs switches have a relatively good responsivity (defined here as output charge per input photons) due to good mobility and the short optical absorption length of GaAs. In addition, the semi-insulating nature of annealed LT GaAs results in low dark currents. The last two characteristics lead to good switch turn-on and turn-off, which are critical for a well-behaved sample-and-hold, giving LT GaAs switches a distinct advantage for use in sampling applications.

All LT GaAs samples were grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE). Growth was initiated with a 0.3-μm thick undoped buffer layer at 600 °C substrate temperature, followed by decrease in substrate temperature and LT GaAs epitaxy at $\sim$1 μm/h. Postgrowth annealing was performed using a rapid thermal annealer, with a dummy GaAs wafer placed on top of the sample to prevent outgassing of arsenic [31].

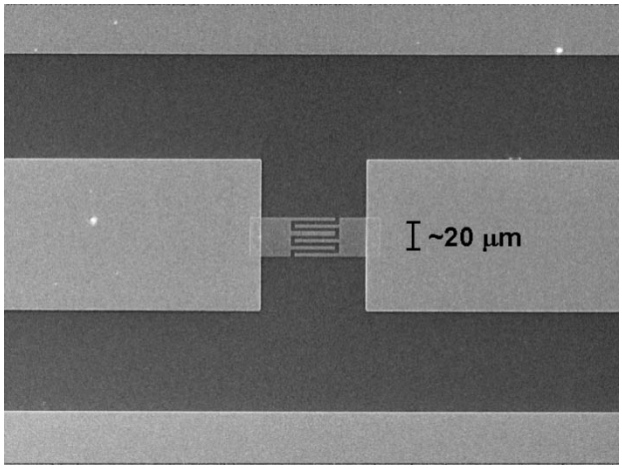

Fig. 2. SEM image of switch response test structure. The MSM switch was placed in the middle of a CPW transmission line to minimize loading effects.

TABLE I
GROWTH AND ANNEAL CONDITIONS OF SAMPLES

Wafer Number	Growth Temperature (°C)	Annealing Conditions (°C, min)	Growth Thickness (μm)	Etch Stop (y/n)
1	250	700, 1	1.8	y
2	250	700, 10	~2	n
3	250	700, 1	0.6	y
4	280	700, 1	~2	n
5	320	700, 1	~2	n
6	Semi-insulating	N/A	N/A	N/A

IV. SWITCH CHARACTERIZATION

The MSM device structure was chosen due to its positive/negative symmetry with respect to bias voltage, low device capacitance, ease of device fabrication and device variation, and simple growth structure. MSM interdigitated patterns were defined on top of the LT GaAs epitaxial layer by depositing titanium/gold contact metal through a standard liftoff process. Three different MSM patterns were made by varying the finger spacing (1, 2, or 5 μm) with a constant finger width (1 μm), covering a $\sim 20 \times 20$ μm^2 area. The range of finger spacings was chosen based on a tradeoff between device responsivity and capacitance, which will become more evident later in the section.

For high-speed characterization, MSMs were placed in the middle of a coplanar waveguide (CPW) transmission line structure, in order to minimize loading effects [32]. A scanning electron micrograph (SEM) image of the configuration is shown in Fig. 2. The transmission-line pattern was defined using the same titanium/gold metal deposition process. To obtain the switch impulse response, the MSM was dc-biased and optically triggered with a titanium/sapphire mode-locked laser ($\sim$80 MHz repetition rate, $\sim$150 fs full-width at half-maximum (FWHM) pulse width, $\sim$850 nm center wavelength). Photogenerated carriers conduct current, launching a voltage transient down the transmission line that characterizes the responsivity and speed of the switch. Transients were measured using a time-resolved EO sampling technique, with a lithium tantalate EO crystal placed on top of the transmission line [33]. The top and bottom surfaces of the crystal were antireflection (AR) and high-reflection (HR) coated, respectively, to maximize EO signal strength. Signal readout was done close to the MSM ($\sim$50 μm away) in order to minimize attenuation and distortion of the transient caused by the transmission line.

Six different samples were prepared with various growth and anneal conditions (Table I). For two of the samples, the LT GaAs epitaxial layer was grown on top of a 0.3-μm-thick $Al_{0.6}Ga_{0.4}As$ layer (wafers 1 and 3). This etch-stop layer was not expected to affect LT GaAs growth [34]. The last wafer is a bare semi-insulating GaAs sample with no epitaxial growth. Each sample contains the three different MSM patterns described above.

EO sampling measurements were taken for all devices while varying the voltage bias (0.5–10 V) and optical pulse energy (12–250 pJ). Fig. 3 shows normalized results for the 1-μm finger spacing MSM of the six different wafers. Bias voltage was 1 V, with a 62-pJ pulse energy for all measurements. For all materials, a sharp initial peak ($\sim$2.5 ps FWHM) is seen, followed by a dip we believe is likely caused by a parasitic inductance. A second peak, whose magnitude and decay vary greatly as a function of material, characterizes subsequent current flow.

The shape of the first peak is fairly constant across all parameters, including bias, optical energy, MSM pattern, and different materials. Due to the large optical pulse energies used, initial photogenerated carrier movement is thought to quickly cause significant field-screening within the center region between the anode and cathode. The large change in the internal field induces a sharp current spike. This phenomenon likely occurs on a subpicosecond time scale. Thus, parasitic loading of the

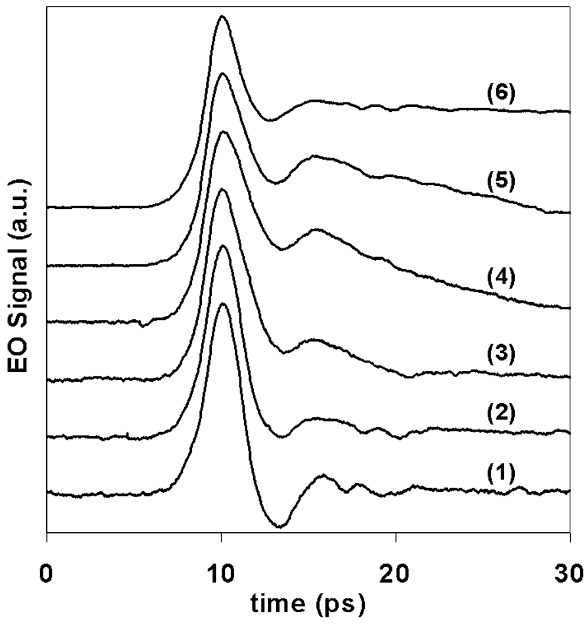

Fig. 3. Normalized switch response for 1-μm finger spacing MSM of various samples. Plots are labeled by corresponding wafer number and vertically offset for clarity. A 1-V bias and a 62-pJ pulse energy were used for all measurements.

device and/or the limited resolution capability of the EO sampling setup largely determine the apparent switch time response, leading to a relatively constant shape for the first peak [32], [33].

Additional contributions to the signal come from subsequent carrier movement at the edges of the field-screened region, with larger mobilities leading to larger photocurrent. Trapping of photogenerated carriers likely causes the decay of the second peak, with faster extinction for larger trap densities and capture cross sections. The relative decay times agree with anticipated changes in defect and precipitate concentrations as a result of variations in growth temperature, anneal temperature/length, and growth thickness. Due to the dynamics of the LT GaAs material, there is an inherent tradeoff between responsivity (mobility) and speed (carrier lifetime) of the switches. A 250 °C growth temperature was chosen for subsequent devices in order to maximize bandwidth.

Fig. 4 shows the normalized response of the 1-μm finger spacing switch (wafer 2) for bias voltages of 0.5 V (bottom trace) and 10 V (top trace). A 62-pJ pulse energy was used for both measurements. The shape of the response is nearly identical for the two widely spaced voltages and all voltages in between, indicating the weak dependence of the switch response to bias. This observation was consistent within the entire range of optical energies tested. For a sample-and-hold, variations in switch response as a function of the input voltage can lead to sampling inaccuracies, making insensitivity to bias particularly important for the targeted applications.

The dependence of the normalized response on pulse energy is shown in Fig. 5. The same device was used as in Fig. 4, with optical energy varied from 12 to 250 pJ and a constant 1-V bias. The inset shows the 12- and 250-pJ plots superposed. Increase in optical energy slightly increases the height of the second peak relative to the first peak. In addition, the overall decay of the

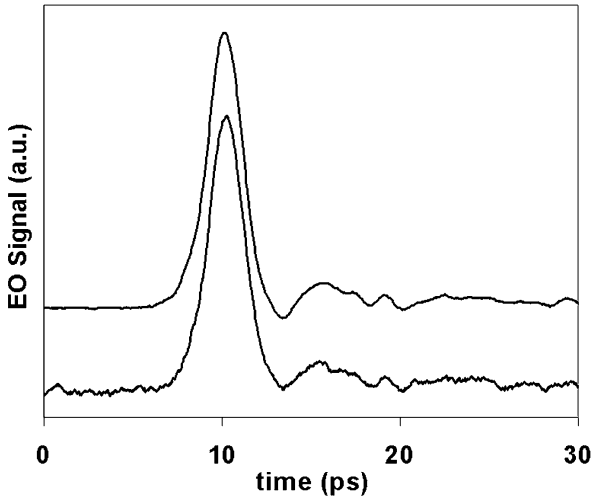

Fig. 4. Normalized switch response of 1-μm finger spacing MSM (wafer 2) for 0.5-V (bottom trace) and 10-V (top trace) biases. Plots are vertically offset for clarity. The response is nearly identical for the two voltages and all voltages in between. A 62-pJ pulse energy was used for both measurements.

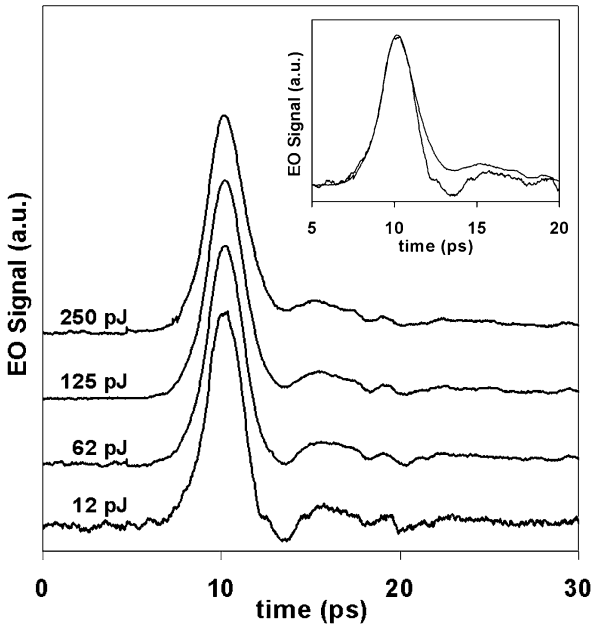

Fig. 5. Normalized switch response of 1-μm finger spacing MSM (wafer 2) for 12-, 62-, 125-, and 250-pJ pulse energies, vertically offset for clarity. The inset shows the 12- and 250-pJ plots superposed. Switch turn-off time becomes longer for larger optical energies. A 1-V bias was used for all measurements.

response may become slower due to trap saturation and carrier pileup, exacerbated at high pulse energies [35]. These effects combined will lead to a degradation of sample-and-hold bandwidth, shown in Section V. This trend of longer switch turn-off for larger optical energies was seen for the entire range of voltage biases tested.

Although reduction of MSM finger spacing did not appreciably change the normalized switch response, an increase in responsivity was observed. Fig. 6 shows the responsivity (determined from the average photocurrent out of the MSM) versus bias voltage for various finger spacing MSMs (wafer 2) with a 62-pJ pulse energy. We also see that responsivity increases

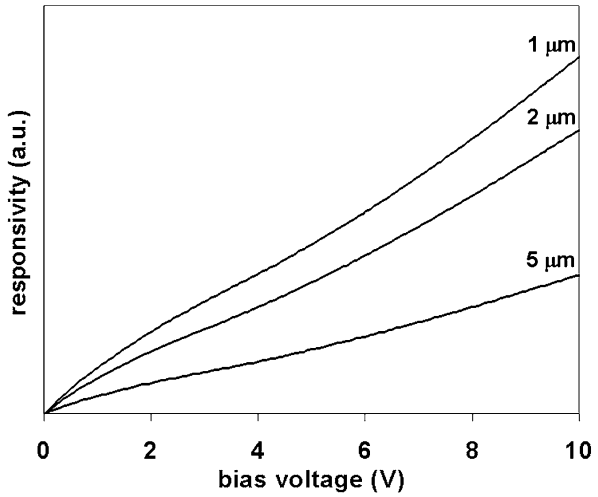

Fig. 6. Switch responsivity as a function of bias voltage for different finger spacing MSMs (wafer 2). A 62-pJ pulse energy was used on all three devices.

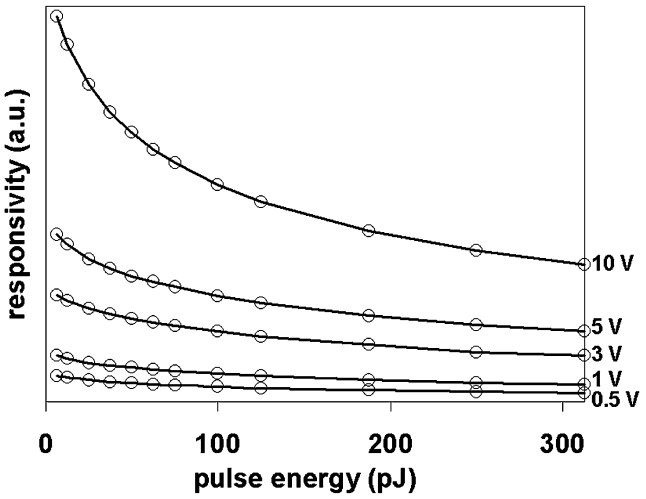

Fig. 7. Switch responsivity as a function of pulse energy for various bias voltages. The 1-μm finger spacing MSM (wafer 2) was used.

somewhat linearly with bias. There are several processes that are linear with bias that may be causing this linearity. First, the polarization induced by the initial carrier movement (described above) is proportional to voltage bias [36]. In addition, the velocity of the photogenerated carriers is likely linear with bias, even for the large biases used here, because of the lower mobility of the LT GaAs material and low internal fields caused by field-screening. Thus, larger biases lead to approximately linearly increasing output current. This trend was consistent for the entire range of pulse energies tested (6–312 pJ).

Fig. 7 shows that the responsivity of the switch decreases with increasing pulse energy. Due to the short carrier lifetime of LT GaAs, the field-screening effect mentioned above, and a weak internal field at deeper points in the epitaxial layer, only photogenerated carriers close to the electrodes of the MSM experience movement and contribute to the output current. The rest of the carriers are lost to traps and recombination. With the near band-edge wavelength of $\sim$850 nm, as the optical energy increases, the number of photogenerated carriers near the surface of the device saturates due to the finite density of states (absorption saturation), consistent with the behavior seen in Fig. 7.

Although the measurements and trends noted are from wafer 2, all samples grown at 250 °C and subsequently annealed show closely similar switch response and responsivity dependencies on bias, optical energy, and finger spacing.

V. Sample-and-Hold Testing

To characterize the switch in a sample-and-hold configuration, a test circuit was made by attaching two MSM devices in series across the signal and ground lines of a transmission line. The first device serves as the switch, while the second serves as the hold capacitor (C_H). Fig. 8 shows a layout of the circuit. Both MSMs are 1-μm finger spacing, 1-μm finger width patterns covering a $\sim 20 \times 20$ μm^2 area. The device/hold capacitance is $\sim$20 fF. Material from wafer 2 was used to make the test circuit.

Measurements were performed using the same titanium/sapphire mode-locked laser previously mentioned. When the pump

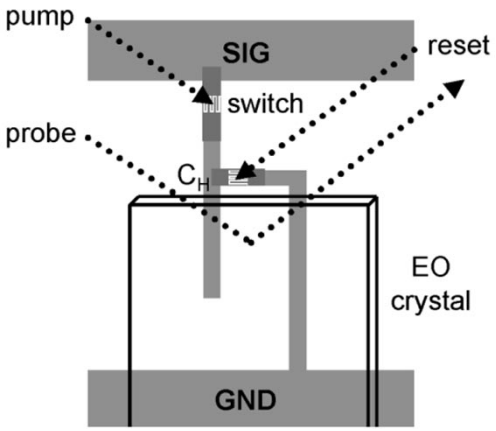

Fig. 8. Layout of sample-and-hold test circuit and EO sampling measurement setup. The lithium tantalate EO crystal allows probe readout of the held signal.

pulse triggers the switch, photogenerated carriers conduct current and sample the input signal onto the hold capacitor. Time-resolved EO sampling was used to measure the voltage across the hold capacitor. The lithium tantalate EO crystal was placed on top of the metal lines probing the ends of the hold capacitor, as seen in Fig. 8. The held voltage biases the crystal, enabling probe readout. A subsequent reset pulse ($\sim$5 ns wide, 190 pJ/pulse) hits the hold capacitor MSM, discharging the held signal to ground and restoring the circuit to initial conditions. An electrical pulse train phase-locked to the pump and probe pulses was used to directly modulate a Fabry–Pérot semiconductor laser and create the reset optical beam.

Due to the low responsivity of the switch, the use of EO sampling for this measurement is critical, because of its minimally invasive nature [33]. Other probing techniques would severely load the circuit, attenuating and potentially distorting the output signal. Loading by the EO crystal is minimal, with a slight increase in the hold capacitance as a result of the increased dielectric constant in the space above the pattern.

Initial measurements were done with a dc electrical input, with results shown in Fig. 9. A step-like signal is observed, corresponding to fast charge-up of the hold capacitor initiated by switch turn-on. The oscillations are caused by parasitic

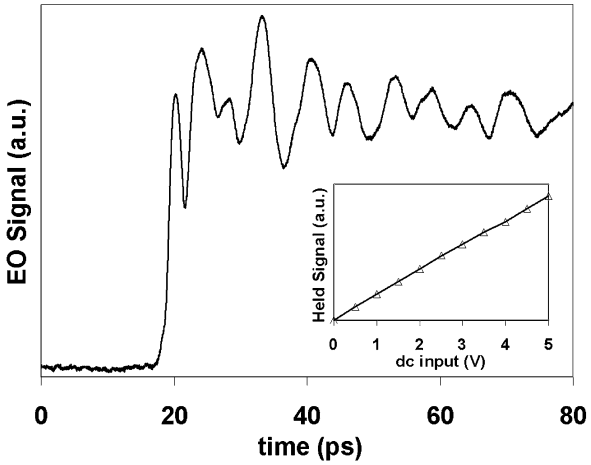

Fig. 9. Sample-and-hold of a dc input. The voltage across the hold capacitor was measured using EO sampling (Fig. 8). The inset shows step height as a function of input voltage. The data exhibits 6.2 bits of linearity for the sample-and-hold process.

inductance ($\sim$200 pH) in the test circuit. The oscillations eventually die out, leaving a constant held signal. The inset of Fig. 9 shows the step height plotted as a function of the input voltage for a 250-pJ pump pulse energy. The held signal was taken 100 ps after the leading edge to avoid ringing effects. The sample-and-hold exhibits 6.2 bits of linearity for the input voltage range used.

An inherent problem with the sample-and-hold originates from the switch having a parasitic device capacitance, causing the circuit to form a capacitive voltage divider. Thus, after the switch has turned off, fluctuations in the input signal on the transmission line will feed through, corrupting the held signal during digitization by the CMOS A/D converter, according to

$$\Delta V_{\text{held}} = \left(\frac{C_{\text{switch}}}{C_{\text{switch}} + C_H} \right) \times \Delta V_{\text{input}}.$$

In order to eliminate this feedthrough error, we adopt a differential configuration sample-and-hold. Fig. 10 shows a layout of the test pattern used to demonstrate the concept. Each side of the pattern consists of a sample-and-hold test circuit. Both sides are made identical within fabrication tolerances. The sample-and-hold is performed on one side while the other side serves as a dummy, with its hold capacitor tracking only the feedthrough voltage. Due to symmetry, the fluctuation on both hold capacitors is equal. By taking the differential signal between the hold capacitor voltages, feedthrough is eliminated. Using this test circuit, we previously demonstrated this differential scheme by measuring the voltage across each hold capacitor and the differential signal between them using time-resolved EO sampling [24].

To characterize the LT GaAs sample-and-hold for dynamic inputs, a sample-and-hold was performed with microwave input frequencies using the same test circuit and EO crystal configuration as the dc input measurement (Fig. 8). The measurement setup is nearly identical, with pump, probe, and reset pulses generated in the same fashion. A photodetector monitoring the mode-locked laser output generated a phase-locked 80-MHz electrical signal. This fundamental frequency was then fed into

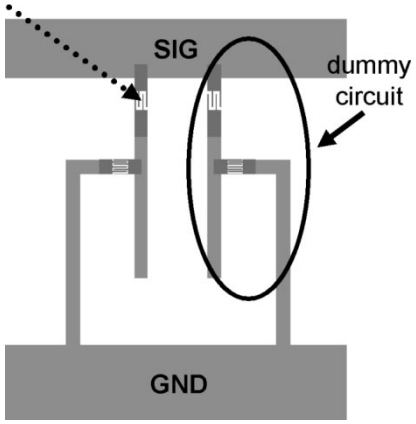

Fig. 10. Differential sample-and-hold test pattern. The sample-and-hold is performed on the left side, while the right side tracks the feedthrough voltage. Differential detection eliminates feedthrough.

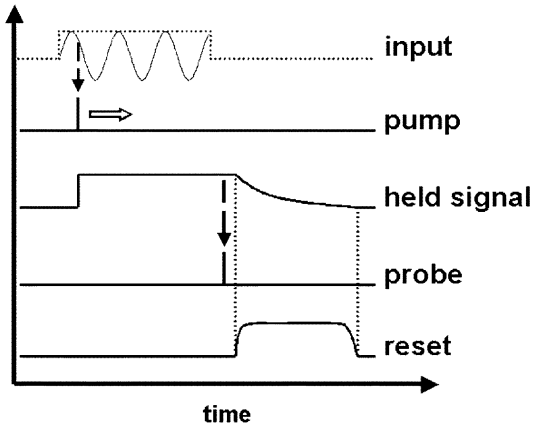

Fig. 11. Timing diagram for the dynamic input sample-and-hold measurement. All signals are phase-locked, with relative phase of the pump pulse varied to sample different points of the input signal. For simplicity, the held signal does not indicate feedthrough effects.

various frequency multipliers to generate a 2-, 10-, or 20-GHz sinusoid (25th, 125th, and 250th harmonic) to use as the input for the sample-and-hold. Electrical mixers (Marki Microwave M1-0420, hp 11665B) allowed windowing of the input signal and lock-in detection for EO sampling. Fig. 11 shows a timing diagram for the measurement. The pump pulse hits the switch MSM, sampling the input signal onto the hold capacitor. The probe pulse then detects the held voltage through the EO crystal. The reset pulse is positioned during the off period of the input signal to discharge the hold capacitor and return the circuit to initial conditions. By varying the phase of the pump pulse, different points of the input signal are sampled, enabling a dynamic input sample-and-hold measurement. Feedthrough effects are not shown in the timing diagram, for simplicity.

Results of the EO sampling measurement are shown in Fig. 12 for a pump energy of 250 pJ. The top trace is 2 GHz, the middle trace is 10 GHz, and the bottom trace is 20 GHz. All traces are normalized. Dots indicate sampled points with solid lines showing pure sinusoids fit to data using a minimum mean squared error fit. The data exhibit 4.8, 5.5, and 4.0 bits of linearity, respectively, with the two lower values (4.8 and 4.0) attributed to distortion of the original input signals. Good linearity of the sample-and-hold was also observed for

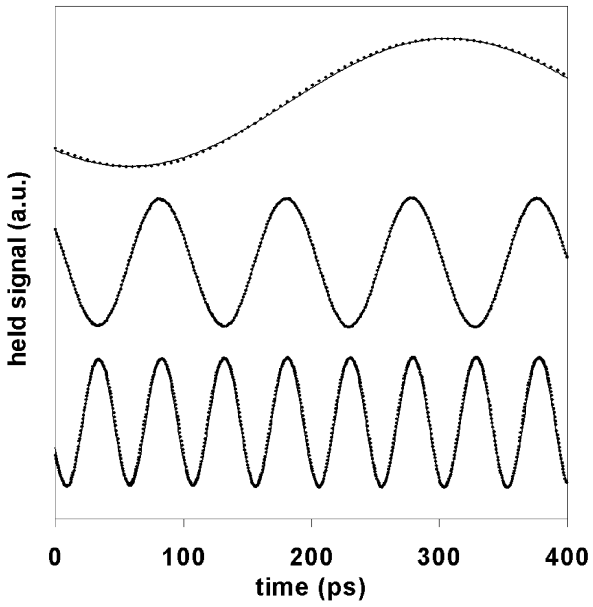

Fig. 12. Results of dynamic input sample-and-hold measurement for a 250-pJ pump energy. The top trace is 2 GHz, middle trace 10 GHz, and bottom trace 20 GHz. All traces are normalized. Dots indicate sampled points with solid lines showing pure sinusoids fit to data using a minimum mean squared error fit.

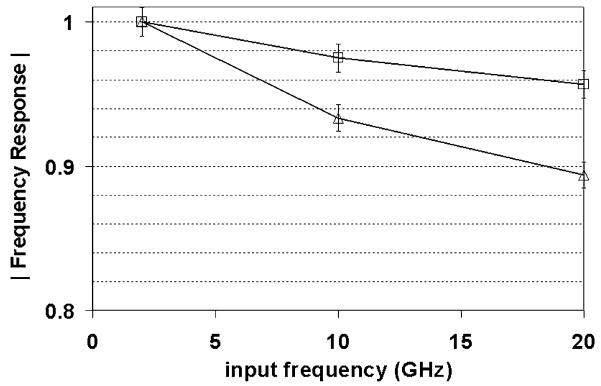

Fig. 13. Magnitude of sample-and-hold frequency response. The response is shown for 62- (squares) and 250-pJ (triangles) pump energies. The 2-GHz points are scaled to unity for both plots.

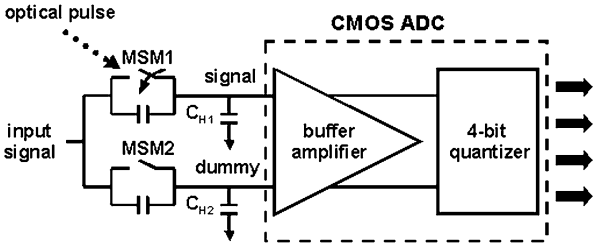

Fig. 14. Diagram of a single channel. Differential configuration MSMs allow feedthrough cancellation. Input/hold capacitance (C_{H1}, C_{H2}) is ~30 fF. The buffer amplifier drives a 4-bit flash converter.

lower pump energies, with slight degradation as optical energy decreased [21].

With increasing pump energy, the amplitude of the held signal gradually increases and eventually saturates to ~70% of the signal amplitude measured without resetting. This indicates that the hold capacitor is not charging up to the full input voltage during sampling. Due to the switch being in series with the transmission line impedance (Z_o), the time constant for charge up is given by $\tau = (R_{\text{switch}} + Z_o/2) \times C_H$, assuming a constant switch turn-on resistance and ignoring the switch capacitance, for simplicity. This first-order expression highlights the fact that a sufficiently low switch turn-on resistance (sufficient carrier movement) must be accompanied by a long enough turn-on time for the hold capacitor to charge up to the input voltage. Thus, incomplete charge-up is likely due to inadequate switch turn-on, coupled with too short of a gating function. Despite this problem, the sample-and-hold exhibits good linearity. Although explanation of this phenomenon requires further investigation, it can most likely be traced back to the switch responsivity being proportional to bias voltage, as seen in Section IV.

The frequency response of the sample-and-hold process was characterized by taking the held signal amplitude at each input frequency and dividing it with the corresponding input signal amplitude. EO measurement of the input signal was done on the transmission line, next to the sample-and-hold circuit, to account for frequency dependent loss from the transmission line and test setup. Fig. 13 shows results for two pump energies, with rolloff to 95.7% and 89.4% at 20 GHz for 62- and 250-pJ pump energies, respectively. Due to the large expected bandwidth of the response, the 2-GHz points are scaled to unity for both plots. Degradation in sample-and-hold bandwidth as pump energy increases can be attributed to a corresponding increase in switch turn-off time, as seen in Fig. 5. The small rolloff indicates a large bandwidth for the sample-and-hold process [21].

VI. CMOS Integration

The CMOS A/D converter was designed and fabricated in a National Semiconductor 0.24-μm CMOS process. Critical design constraints were the need for a low input capacitance due to the limited responsivity of the MSM switches, a differential input with high common-mode rejection to match the differential configuration sample-and-hold, low area in order to fit as many channels as possible in a given area, and low power consumption.

Fig. 14 shows a diagram of a single channel. A front-end differential buffer amplifier provides a low input capacitance and drives a 4-bit flash converter. The buffer consists of a PMOS source-follower for both signal and dummy inputs, followed by a linear transconductance amplifier having a differential gain of ~4 and rejecting the input common-mode variation due to feedthrough. The settling time of the buffer amplifier largely determines the speed of the converter.

Due to the extremely short aperture time of the sample-and-hold, a significant amount of the settling of internal nodes within the amplifier occurs after the MSM switch has turned off, while the inputs of the amplifier are floating. These voltage changes can kick back to the inputs through the gate capacitance of the input transistors. With the amount of kickback being dependent on previously sampled values, a memory effect is introduced. To alleviate this problem, the signal input

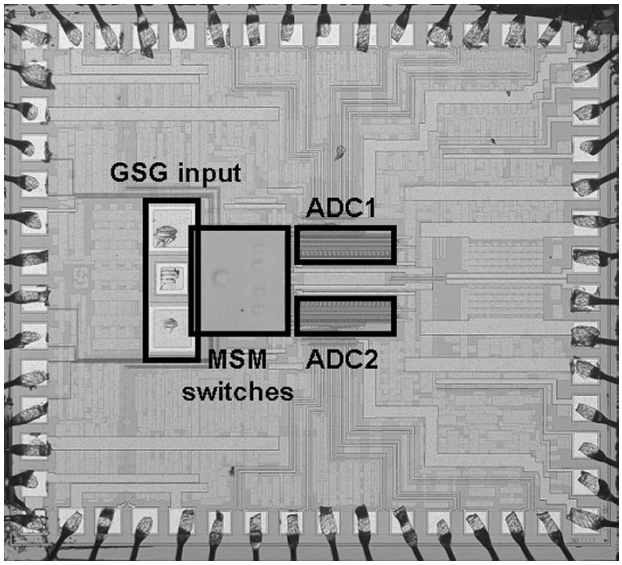

Fig. 15. Photograph of two-channel test chip. MSM switches were flip-chip bonded to a CMOS chip with two A/D converters (ADC1, ADC2). The rectangular LT GaAs mesa in the middle of the chip contains the MSM switches. GSG pads allow insertion of high-speed input signals.

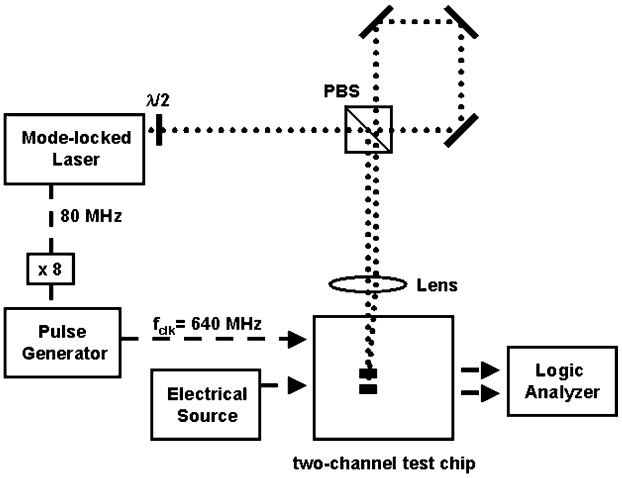

Fig. 16. Measurement setup for two-channel test chip. The initial mode-locked laser output is split in two to generate an optical clock for each channel. The CMOS A/D converters are run at the eighth harmonic of the 80-MHz laser repetition rate. A low jitter microwave source creates the input signal. The 4-bit binary code output of each channel is fed into a logic analyzer for data storage. $\lambda/2$: Half-waveplate. PBS: Polarizing beam splitter.

of the amplifier is reset with a CMOS switch. By resetting the input node to a reference voltage (common-mode) before every sample-and-hold event, the kickback signal is made proportional to only the present sampled signal and memory is eliminated.

The quantization circuitry consists of 15 main comparators, with six additional dummy comparators and an averaging resistor network to improve linearity [37]. The final thermometer code output is decoded to the corresponding 4-bit binary code using digital circuitry. Additional details of the circuit design can be found elsewhere [22].

The fabricated prototype chip consists of two A/D converter channels. The die area for each channel is 150×450 μm^2. Power consumption is $\sim$70 mW per channel at a 640-MHz clock rate.

As seen in Section V, reduction of the input/hold capacitance is critical in obtaining a large held signal, due to the limited responsivity of the LT GaAs switch. In order to reduce parasitics at the buffer input nodes, a flip-chip bonding process was used to integrate the differential configuration MSM switches with the CMOS A/D converters [38]. The input capacitance (C_{H1}, C_{H2}) is the sum of the bond pad capacitance ($\sim$15 fF) and input gate capacitance ($\sim$15 fF). Indium solder was used as a conducting adhesive between the desired points of contact on the switches and the CMOS chip. Substrate removal leaves a LT GaAs mesa with an $Al_{0.6}Ga_{0.4}As$ etch-stop layer on top, allowing backside illumination of the switch.

MSMs with a 2-μm finger spacing from wafer 3 (Table I) were bonded to the CMOS chip. Although the bandwidth of the devices from this wafer is slightly lower than those from wafers 1 and 2 (Fig. 3), the thinner epitaxial growth leads to larger mobility and higher photogenerated carrier concentration near the electrodes. This results in better responsivity and full charge-up of the hold capacitor to the input voltage value during sampling. Larger feedthrough can lead to larger common-mode variation, causing more distortion in the amplifier circuit. Thus, the 2-μm finger spacing MSM with its lower capacitance ($C_{\text{switch}} \sim 10$ fF), and consequently lower feedthrough, was chosen to balance the device responsivity and channel linearity tradeoff.

Fig. 15 shows a photograph of the prototype chip with flip-chip bonded MSMs. Because the MSM pattern is on the "down" side of the bonded LT GaAs structure, it is not visible here. Input ground-signal-ground (GSG) pads allow insertion of high-speed input signals into a CPW transmission line that connects to the MSM switches. The transmission line is defined by the top metal layer of the CMOS chip. A 50-Ω termination is implemented in polysilicon at the end of the line.

The chip was tested using the available 80-MHz titanium/sapphire mode-locked laser to trigger the MSMs, and a low-timing-jitter electrical source (Agilent E8244A) for the input signal. Fig. 16 illustrates the test setup. The laser beam is split in two to generate an optical clock for each channel, with a translation stage used for proper phase alignment. Although the sampling rate per channel is limited to the repetition rate of the laser, the 80-MHz fundamental is multiplied up to 640 MHz with a frequency multiplier and used to clock the A/D converters to confirm CMOS circuit functionality at this higher repetition rate. The 4-bit output of each channel is fed into a logic analyzer (hp 16 702A), with every eighth point taken to give the final output. Input sinusoids from 3 MHz up to 40 GHz were sampled using $\sim$50-pJ optical pulses for a measurement time window of 25 μs (limited by logic analyzer memory). In this setup, the mode-locked laser pulses and input signal are not phase-locked, indicating a real time sampling measurement. Full charge-up of the hold capacitor to the input voltage was achieved with lower optical energy than used in Section V, due to the benefits of backside illumination of the MSM and improved mobility of the LT GaAs. Although aliasing occurs for input frequencies beyond the Nyquist limit, linearity of the system can be characterized by looking at the output signal spectrum within the Nyquist band. Frequency-dependent loss of the test setup and

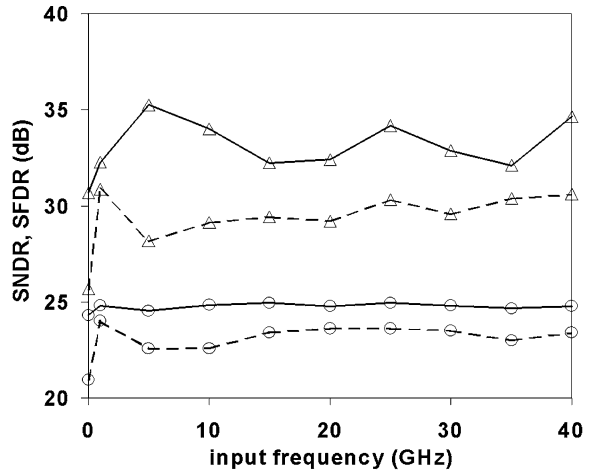

Fig. 17. Results of single-channel (solid line) and two-channel (dashed line) testing. Peak SNDR (circles) and SFDR (triangles) are plotted for various input frequencies.

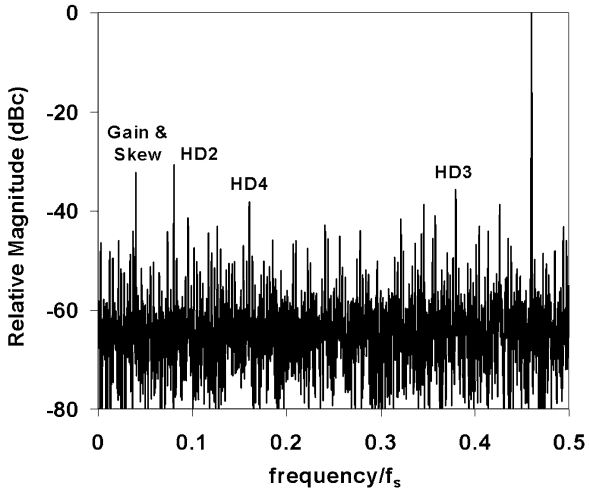

Fig. 18. Nyquist band spectrum of two-channel testing output for a 40-GHz input signal. Harmonic distortion tones are labeled along with the distortion tone due to gain and phase mismatch. HD2: Second harmonic distortion. HD3: Third harmonic distortion. HD4: Fourth harmonic distortion.

test chip was compensated for by increasing the amplitude of the input signal.

Results for testing of a single channel are shown in Fig. 17, with peak SNDR and SFDR plotted as a function of input frequency. For the entire 40-GHz input band, SNDR is $\sim$25 dB, corresponding to 3.8 ENOB, and SFDR is $>$30 dB. The SNDR is fairly constant as input frequency increases, indicating that jitter from the input source and the laser is not limiting the performance of the system. By taking the output signal, subtracting quantization noise and the largest harmonic distortion contribution, and attributing all other noise to timing jitter, an rms value of $\sigma_{\text{jitter}} \sim 80$ fs is obtained for the system. Most of the distortion in the system can be attributed to buffer amplifier nonlinearity. For higher A/D converter clock speeds, the performance worsened due to inadequate settling time for the buffer amplifier.

Results for two-channel testing are also shown in Fig. 17. With the exception of the low frequency data point (3 MHz), the peak SNDR is $\sim$23 dB, corresponding to 3.5 ENOB, and SFDR is $\sim$29 dB. In comparison to single-channel results, degradation in performance is caused in part by channel mismatch errors, present in all time-interleaved systems [39]. Channel-to-channel variations in gain and offset of the conversion transfer function, along with phase error due to skew between channels, can increase distortion. In addition, interaction of scattered light with the CMOS circuitry is believed to cause stray currents most likely within the input amplifier stage, resulting in more distortion. The presence of two optical beams seemed to significantly increase this effect. The problem could be eliminated with proper optical shielding of the circuitry. Fig. 18 shows the spectrum of the output signal for a 40-GHz input sampled at 160 megasamples/s. The main distortion tones are labeled, with second harmonic distortion (HD2) giving the largest contribution. The second largest distortion tone is due to gain mismatch and skew between the two channels. Overall, performance is not limited by timing jitter, demonstrating the advantage of utilizing the mode-locked laser optical clock.

VII. Conclusion

We have introduced and developed a photonic A/D conversion system using LT GaAs MSM switches integrated with CMOS A/D converters. Initial characterization of the switch led to optimization of switch speed and efficiency through material and interdigitated pattern variation. Good linearity and large bandwidths were measured for sample-and-hold test circuits employing these optoelectronic switches. In addition, a differential device configuration was adopted to eliminate feedthrough in the circuit. For the final demonstration, a prototype two-channel system was fabricated by flip-chip bonding MSM devices to CMOS A/D converters. The system achieves $\sim$3.5 ENOB of resolution over a 40-GHz input signal band. The 40-GHz maximum frequency was set by source availability, and the fundamental limit of system performance is expected to extend well beyond this frequency. Using a nonoptimized mode-locked laser setup, a timing jitter value of $<$80 fs is obtained. In addition, phase error beyond the clock source timing jitter can be easily minimized as a result of the optical nature of clock distribution. By using the advantages of photonic technology, our system readily achieves several tens of gigahertz of input bandwidth and extremely low clock phase error.

The extension of this two-channel prototype to a system with a large number of channels faces several obstacles. The limited bandwidth and attenuation from the transmission-line network will lead to input signal distortion. In addition, every optical sampling event will create transients along the line, potentially introducing interchannel coupling effects. Reducing the size of the transmission line and components directly interconnected to it would alleviate these problems. A more compact scheme could be realized by utilizing self-electrooptic effect devices (SEEDs) to optically transmit the held signal away from the input sample-and-hold, with subsequent digitization done remotely [40]. Another possibility is to implement the buffer am-

plifier stage in GaAs. The ability to drive larger interconnect loads would increase routing possibilities, allowing circuit layouts that keep the transmission line short.

Improvements in system performance could be obtained with further optimization of switch responsivity and bandwidth through continued investigation of LT GaAs. Improvements in LT GaAs mobility while maintaining fast carrier trapping times may be possible by growing at higher temperatures and beryllium doping [41]. Ultimate limits of the LT GaAs switch sample-and-hold could be explored by integrating the switches with a higher resolution CMOS A/D converter.

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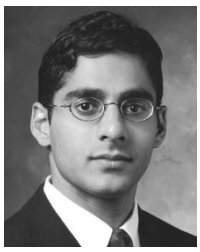

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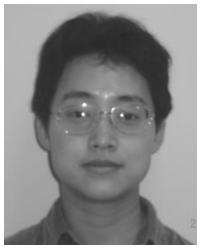

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Dr. Harris is a Fellow of the American Physical Society. He received the 2000 IEEE Morris N. Liebmann Memorial Award, the 2000 International Compound Semiconductor Conference Walker Medal, an IEEE Third Millennium Medal, and an Alexander von Humboldt Senior Research Prize in 1998 for his contributions to GaAs devices and technology.