Photonic Damascene Process for Low-Loss, High-Confinement Silicon Nitride Waveguides

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(Invited Paper)

***Abstract*—We report on fabrication of high-confinement and low loss silicon nitride (Si_3N_4) waveguides using the photonic Damascene process. This process scheme represents a novel fabrication approach enabling reliable, wafer-scale fabrication of high-confinement optical waveguides. A reflow step of the silica preform reduces sidewall scattering to values not attainable with conventional etching, and reduces losses and backscattering significantly, resulting in a waveguide attenuation of 5.5 dB/m. We discuss the critical aspects of the process in detail and demonstrate the fabrication of high stress Si_3N_4 waveguides with unprecedentedly large dimensions (1.75 μm $\times$ 1.425 μm) providing high-confinement at midinfrared wavelengths. A device characterization strategy allowing for systematic extraction of statistically relevant loss values is discussed and reveals the effects of the sidewall smoothing.**

***Index Terms*—Optical waveguides, optical losses, optical resonators.**

I. Introduction

LOW loss, planar optical waveguides have the potential to be a key enabling technology for a wide range of applications, such as delay lines [1], optical gyroscopes [2], [3], ultra narrow linewidth lasers [4], compact chipscale reference cavities [5], nonlinear photonic devices [6] such as soliton Kerr frequency combs [7] or quantum photonic circuits [8], [9]. While optical fibers have attained linear losses as low as 0.2 dB/km [10] more than 40 years ago, today most chip-based planar optical waveguides suffer from losses $\approx$1000 times larger, on the order of 0.1 dB/m. Closing this technological gap would enable miniaturization of devices currently implemented using optical fibers and reduce the power requirements of active devices such as lasers or soliton Kerr frequency combs, in addition to lowering their cost through component integration and use of CMOS fabrication technology.

Among the diverse low loss, planar waveguide platforms silicon nitride (Si_3N_4) based waveguides, first reported in 1987 [11], have recently attracted increasing interest [12]. Compared to other platforms, such as silicon-on-insulator (SOI), Silica-on-Silicon or indium phosphide (InP), Si_3N_4 waveguides embedded in a SiO_2 cladding offer an attractive compromise between index contrast, low propagation losses and fabrication using standard CMOS technology [13]. Moreoover, the material's low optical phonon frequencies and large optical bandgap of ca. 5 eV enables its application in a broad wavelength range from the mid-infrared down to visible wavelengths, and leads to negligible two-photon absorption in the telecommunication band. Si_3N_4 waveguides exibit a high effective nonlinearity, ca. 50 larger than optical fiber in the telecommunication band, making the platform a promising candidate for nonlinear optical applications, as well as quantum optical and bio-medical applications operating at wavelengths shorter than 1 μm [14], [15], as well as mid-infrared photonics [16]. A review of recent research efforts and commercially available Si_3N_4 platforms can be found in [17].

The early works employing Si_3N_4 as waveguide material were limited by the high tensile stress of stoichiometric Si_3N_4 thin films [18], [19]. Such waveguides were initially investigated for application in the visible spectral range [20], and later as ultra-low loss, though low confinement waveguides for telecom C-band wavelengths [21]. A high tensile film stress exceeding 1 GPa is intrinsic to stoichiometric Si_3N_4 deposited at temperatures around 800 °C using low pressure chemical vapour deposition (LPCVD). It makes Si_3N_4 a prominent material for elastic strain engineering e.g. for high performance silicon transistors [22], but provides severe challenges to the fabrication of optical waveguides. Therefore, plasma enhanced chemical vapor deposition (PECVD) methods and non-stoichiometric Si-rich materials [23], [24] are actively investigated as they allow a significant reduction of the thin film stress and a higher optical nonlinearity. However, despite intensive research efforts

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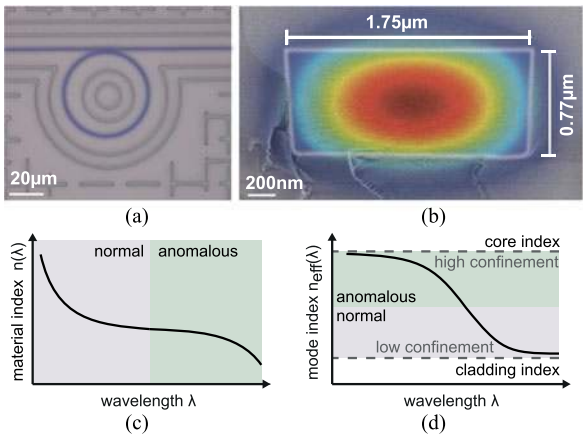

Fig. 1. (a) Optical ring resonator formed by low loss, high confinement Si_3N_4 waveguide (blue). (b) Cross sectional view of a highly confined mode in a Si_3N_4 waveguide. (c), (d) Schematic showing the general behaviour of material and geometric dispersion over wavelength. The anomalous geometric dispersion of high confinement waveguides can compensate the normal material dispersion, resulting in anomalous GVD.

high stress LPCVD Si_3N_4 remains the material of choice for low loss optical waveguides due to its low content of residual hydrogen.

The nonlinear refractive index of Si_3N_4 ($n_2 = 2.5 \times 10^{-15}$ cm^2W^{-1}) is about an order of magnitude larger than for SiO_2. Moreover, the high band gap renders two photon absorption inside Si_3N_4 waveguides negligible at telecom C-band wavelengths [6]. This enables applications requiring high intensities inside the waveguide core and is the foundation of the increasing success of the Si_3N_4 platform for chip-based nonlinear photonics. Examples are nonlinear wavelength conversion, Kerr soliton optical frequency comb and coherent supercontinuum generation [25] additionally profit from the possibilities of waveguide dispersion engineering. In this context, especially microresonators based on Si_3N_4 waveguides with mode areas larger than 1 μm^2 are of interest. As shown in Fig. 1(b) the waveguides typically have lateral dimensions exceeding 1 μm and a height around 800 μm, providing highly confined optical modes in the telecom C-band. The high confinement of the optical mode inside the waveguide core allows for tight bending radii with low propagation losses and results in a higher effective nonlinearity. More importantly it enables broadband engineering of the group velocity dispersion (GVD) into the anomalous regime, a key requirement for parametric frequency conversion as well as pulse compression and dissipative Kerr soliton formation in microresonators. Fig. 1(c) and (d) illustrate the principle of GVD engineering for Si_3N_4 waveguides. The material dispersion of Si_3N_4 is normal in the telecom C-band, due to the electronic material resonances in the UV which dominate the anomalous dispersion of the phonon resonances the mid-infrared. The geometric dispersion provided by the waveguide confinement is anomalous for highly confining geometries and can compensate the material dispersion, rendering the total GVD anomalous. In practice, the accurate tailoring of GVD requires control of the waveguide dimensions on the order of 10 nm [26]. While this is a significant challenge for CMOS technology based fabrication processes, additionally the reliable deposition of low loss Si_3N_4 thin films to the required thickness is a key obstacle for the realization of Si_3N_4 for nonlinear applications. Only recently the introduction of a thermal cycling process enabled for the first time the deposition of high quality Si_3N_4 with the required thickness [27].

The conventional processing scheme for Si_3N_4 waveguides, here called *subtractive processing scheme*, is schematically illustrated in Fig. 2(a) [28]. The waveguides are etched into the deposited Si_3N_4 thin film using a patterned mask layer. Then a cladding material is deposited and annealing drives residual hydrogen out of the film, reducing the absorption losses. Such a subtractive processing scheme provides sufficient dimensional accuracy and is at the basis of most published works to date. However, record low propagation losses on the order of 0.1 dB/m [21], [29], [30] were so far only obtained for waveguide cross sections with widths exceeding 3 μm. Despite their low losses such waveguides suffer from a high number of supported mode families and can not readily be applied for nonlinear optics as the dispersion of the low loss modes is normal. Moreover, the subtractive process scheme itself entails several fabrication challenges which have mostly remained unsolved to date: crack formation, wafer bow and film de-lamination due to the high tensile stress in the deposited Si_3N_4 thin films and critical dimensions dictated by the limitations on aspect ratios imposed by the etch and the cladding deposition processes. Finally, with respect to their loss performance, waveguide sidewall roughness remains critical despite the development of sophisticated lithography and etching techniques.

Fig. 2(b) and (c) show examples of crack formation in Si_3N_4 thin films. As seen in the scanning electron micrograph shown in Fig. 2(c) such cracks locally interrupt the waveguide, causing strong transmission losses and backreflection. The high tensile film stress limits the deposition thickness of LPCVD Si_3N_4 in many cases to maximal values between 250–400 nm [31], [32]. Additionally, stress induced wafer bow, typically visible after augmenting film stress during annealing, poses limitations to the fabrication process. The Si_3N_4 films moreover tend to peal of the wafer after several days, requiring immediate further processing after their deposition.

Many basic building blocks of photonic integrated circuits rely on closely spaced waveguides which can represent critical aspect ratios for subtractive processing. An example in the context of microresonator based nonlinear optics is the coupling gap between resonator and bus waveguide. Especially high confinement waveguides have a shorter evanescent field leaking out of the waveguide core. Thus narrow waveguide spacing on the order of 200 nm can be desirable in order to achieve significant coupling of the optical modes between them. For a typical waveguide height of 0.8 μm this results in an aspect ratio of about 4:1 which poses difficulties to processes for dry etching and oxide cladding deposition. Dry etching processes have a limited anisotropy of the etch rates. As a consequence the resulting waveguide spacing can deviate significantly from the designed value defined by the high resolution lithography process. Moreover, aspect ratio dependent etch (ARDE) rates can cause slower etching in the narrow gap between the waveguides,

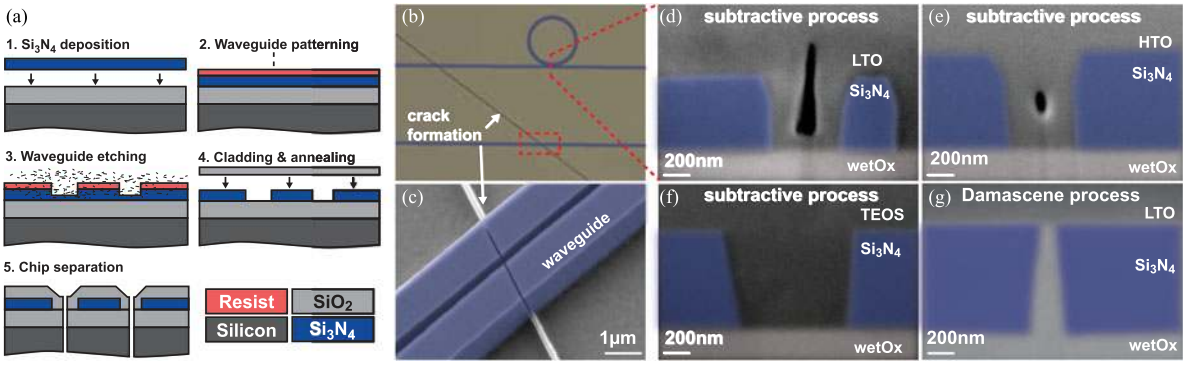

Fig. 2. (a) Schematic overview of the essential steps within a conventional subtractive process. (b) Microscope image of a crack propagating through subtractively fabricated Si_3N_4 waveguides (blue). (c) Scanning electron micrograph of a crack propagating through two adjacent Si_3N_4 waveguides (blue). (d)–(g) Comparison of void formation in between closely spaced Si_3N_4 waveguides (blue) for different cladding deposition processes. The wet thermal oxide forming the bottom cladding is highlighted in white. (d) Void formation observed for low temperature oxide (LTO) cladding deposition. (e) The high temperature oxide (HTO) deposition process offers better step coverage than LTO but shows void formation for gaps with aspect ratios less than 2:1. (f) The gap is well filled by the TEOS cladding oxide, but void formation is expected for smaller coupling gaps. (g) Closely spaced waveguides realized by the photonic Damascene process. The gap has an aspect ratio of almost 4:1.

requiring significant over-etching in order to remove the core material completely.

During cladding deposition the waveguide gap is expected to be uniformly filled with the cladding material. Fig. 2(d)–(f) compares three common LPCVD oxide cladding deposition processes regarding their ability to fill the gap between two adjacent Si_3N_4 waveguides. The different precursor gasses and process temperatures, $SiH_4 + O_2$ at 425 °C for LTO, $TEOS + O_2$ at 700 °C for TEOS oxide and $SiCl_2H_2 + N_2O$ at 920 °C for HTO, lead to different deposition characteristics [28]. As can be seen the limited step coverage of the low temperature oxide (LTO) process leads to the formation of a large void. The effect of such voids on the waveguide propagation loss is to date not studied, but excess losses are expected due to the rapid index change. Moreover, due to the unpredictable geometry of the void, the coupling rate between both waveguides can hardly be predicted a priori using simulations. The high temperature oxide (HTO) process offers better conformality as its deposition temperature is higher, but is still unable to fill an aspect ratio of less than 2:1. The TEOS process in Fig. 2(c) is known to offer excellent step coverage and fills the gap entirely. However, void formation is expected for narrower gaps and all three processes fall behind the aspect ratio of almost 4:1 realized using a photonic Damascene process, shown in Fig. 2(d).

II. The Photonic Damascene Process

The copper interconnects in today's microprocessors were enabled by the invention of an additive patterning process, which is commonly referred to as "Damascene process" or "dual-Damascene process" [33]. As the dry etching of copper is challenging the process scheme relies on electroplating it onto a structured substrate and subsequent planarization. Recently, it was shown that a photonic Damascene process meets the common challenges for high confinement waveguide fabrication described above and enables high yield, wafer-scale fabrication of high confinement Si_3N_4 waveguides [34]. Within the process, schematically shown in Fig. 3, the core material layer is deposited on a substrate that is pre-structured with the waveguide

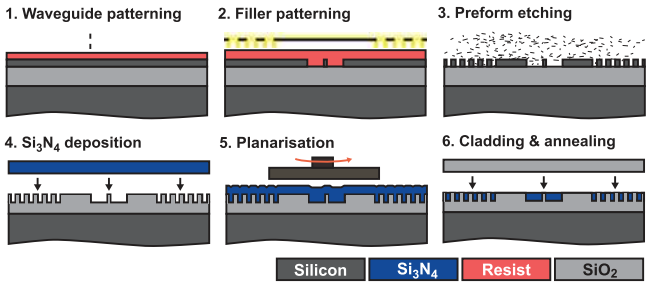

Fig. 3. Schematic process flow of the photonic Damascene process. 1. The waveguides are patterned using electron beam lithography. 2. The filler pattern is defined using photolithography. 3. The preform is etched using an amorphous silicon hardmask. 4. The required thickness of high-stress, stoichiometric Si_3N_4 is deposited. 5. Excess material is removed using chemical mechanical planarization, resulting in a flat top surface. 6. The cladding oxide is deposited and annealing densifies the deposited thin films.

and an additional filler pattern. Subsequently chemical mechanical polishing (CMP) removes the excess Si_3N_4 material, providing a planar and smoothly polished top surface. This process scheme enables several advantages over conventional subtractive processing: A dense filler pattern surrounding the waveguides allows to locally relax the tensile film strain of LPCVD Si_3N_4 thin films, efficiently suppressing crack formation and wafer bow. The planarized top surface prevents void formation even for cladding deposition processes with low conformality. Moreover, a planar top surface is beneficial for heterogeneous integration of advanced optical materials and devices via bonding, as recently demonstrated for $LiNbO_3$ [35]. Finally, a reflow of the oxide preform at high temperatures prior to Si_3N_4 deposition reduces the waveguide sidewall roughness and enables low loss values of ~5 dB/m even for highly mode-confining waveguide geometries. In the following the most important aspects of the individual processing steps are discussed.

A. Filler Pattern Based Stress Management

The success of the photonic Damascene process is closely linked to the dense filler pattern surrounding the waveguides.

After defining the waveguide pattern by electron beam lithography, photolithography is used here to add the filler pattern around them. Such patterns cover the whole wafer and are commonly applied to homogenize structure density and limit microloading effects during reactive ion etching, thin film deposition and CMP [36]. In the context of high stress Si_3N_4 thin films we demonstrated that such filler pattern can additionally prevent crack formation after film deposition. The mechanical impact during CMP can cause extensive cracking and a well designed filler pattern is critical to the high yield fabrication of Si_3N_4 waveguides using the photonic Damascene process.

Crack formation occurs if the tensile stress in the thin film surpasses the breaking stress threshold and the available elastic energy distribution determines the crack propagation. Nam *et al.* demonstrated that surface structures can control the cracking in Si_3N_4 films and that a stair-case structure with critical dimensions of 5 μm can efficiently stop crack propagation in Si_3N_4 films by locally lowering the available elastic energy [37]. This technique was quickly adopted for Si_3N_4 waveguide fabrication [29], [38] providing crack-free regions on the wafer that improved the yield of subtractive process schemes. With such approaches cracking and peeling can still occur outside of the defined zones for waveguide fabrication. Preventing crack formation entirely is thus different as it entails stress management and a reduction of the elastic energy on the wafer-scale. The thick SiO_2 bottom cladding layer separates the Si_3N_4 from the Si substrate and its crystalline structure has thus little influence on the film's internal stress field. Hence, a dense substrate topography can dictate the local stress field inside the thin film and reduces the overall strain significantly. This enables the elegant use of the dense filler pattern used for process control also for stress management. Within the photonic Damascene process this approach efficiently releases the stress in thick LPCVD Si_3N_4 thin films and allows for crack free film deposition up to 1.52 μm thickness.

Fig. 4 gives an overview over different examples of filler patterns evaluated for stress management and crack prevention. All are defined using photolithography and composed of rectangles measuring 2 μm by 20 μm forming regularly tiled elements. These dimensions are chosen to reproduce typical waveguide pattern densities with typical waveguide widths between 1.5–2 μm and minimum distance of optically independent waveguides between 10–20 μm. Actual waveguide recess structures are not visible in Fig. 4, but their position is indicated as blue dashed line within the continuous protection structures surrounding them. The patterns were etched 1.4 μm deep into a 4 μm thick SiO_2 layer of a 700 μm thick Si substrate. Subsequently LPCVD Si_3N_4 was deposited up to a thickness of 1.52 μm within a single deposition step. For most patterns fine cracks in the Si_3N_4 film form after deposition and their density is evaluated based on optical microscope images. Only the pattern shown in 4(d) alleviates the stress sufficiently to yield crack free deposition. The influence of topography on the film stress distribution is illustrated in Fig. 4(a). As the chosen pattern provides mostly film stress modulation in the vertical direction, the stress can build up in the horizontal direction (indicated by red arrows) leading to crack formation. The direction of the cracks formed is

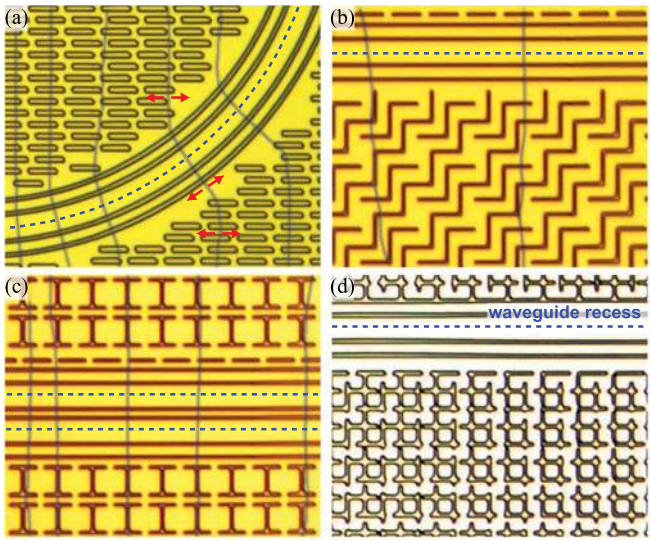

Fig. 4. Comparison of stress relaxation properties of different filler patterns. All rectangles forming the pattern have dimensions of 2 μm by 20 μm and are etched 1.4 μm deep in the SiO_2 preform. The continuous lines forming a protection around the waveguide (indicated as blue dashed lines) are also 2 μm in width. The optical micrographs compare the crack formation after deposition of a 1.52 μm thick Si_3N_4 film on the preform. a) Filler pattern with preferentially horizontal direction causes vertical cracks which are redirected by the continuous protection recess. The red arrows indicate the local direction of the tensile stress. b), c) Cracks run approximately vertical but less directed than in a). d) No crack formation is observed after deposition indicating that the denser topography allows for sufficient stress release.

additionally influenced by the continuous protection structures. Similar effects can be observed for the patterns shown in (b) and (c). Only the pattern in (d) has a higher density of recess lines provides sufficient stress modulation in all directions to completely inhibit crack formation. It is noted that for most cases a deposited Si_3N_4 thickness of less than the exemplified 1.52 μm is needed, relaxing the needs for stress dispersing performance of the filler pattern.

B. Preform Etching With An Aspect Ratio Dependent Etch Rate

The preform etch process transfers the waveguide and filler pattern to the 4 μm thick wet thermal SiO_2 forming the buried oxide layer. The processing problem and requirements are similar to the contact hole etch step in CMOS technology [39]: a highly selective etch process for definition of high aspect ratio holes in a SiO_2 layer. Amorphous silicon (a-Si) is an ideal hardmask for etching of SiO_2 as it is easy to structure and to strip and offers high selectivity for SiO_2 etching. Here, we use an a-Si hardmask layer of 0.4 μm thickness and an etch process based on He/C_4F_8. As shown in Fig. 5, the process yields recess structures with sidewall angles of 85°. The a-Si hardmask offers excellent selectivity greater than 8:1 but its erosion during the etch process can still lead to additional sidewall roughness. Thus a significantly thicker hardmask than needed for selectivity reasons is chosen to achieve low sidewall roughness.

A particular characteristic of the etch process is its significant aspect ratio dependent etch rate (ARDE). Also known as *RIE lag*, such pattern size dependent etch rates are a

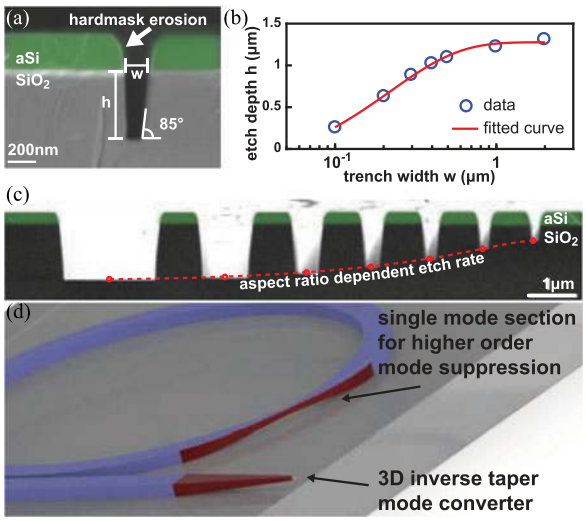

Fig. 5. Amorphous silicon (a-Si) hardmask based etching of SiO_2 preform. (a) SEM micrograph of a high aspect ratio trench etched into the SiO_2 preform layer with a sidewall angle of 85°. The a-Si hardmask (green) shows signs of erosion after the etch. (b), (c) Aspect ratio dependent etch rate (ARDE) of the process. The etched trench depth depending on the structured opening width of the a-Si hardmask is measured and shows that for trench widths below 0.5 μm their height is significantly smaller. The measured values are fitted with an exponential model shown in red. (c) Cross sectional view of a the ARDE effect. Parallel lines with varying width were defined in the hardmask and etched into the preform layer. (d) Illustration of the use cases for waveguides with reduced cross section in photonic integrated circuits.

common problem limiting the critical dimensions of a process [40]. We characterize the ARDE of our process by measuring the width and height of adjacent trenches forming an array as shown in Fig. 5(c). The ARDE effect can be seen as decreasing trench depth for smaller widths. Fig. 5(b) plots the values obtained for a targeted etch depth of 1.2 μm. The data is fitted to good agreement with an exponential model (height $h = a \times exp(-w/b) + c$ with $a = -1.61\ \mu$m, $b = 0.22\ \mu$m and $c = 1.28$).

As a result of the ARDE effect designing a trench width of only 200 nm results in a waveguide of only 300 nm height. The observed RIE lag does not depend on the local pattern density and is thus repeatable and controlled across the wafer, given that the etch reactor provides uniform etch rates. Thus the ARDE does not result in limitations for pattern designs but rather provides an additional degree of freedom. In the context of photonic integrated circuits, this can be a great advantage as it allows the fabrication of small more area waveguides without additional effort. Fig. 5(d) illustrates two examples where such such waveguides with reduced width and height are beneficial. First, the commonly used inverse taper mode converters for efficient input-/output-coupling of light at the chip facets [41] can be realized as *true 3D structure*. Such tapering in both dimensions not only enlarges the final mode diameter but also reduces the polarization dependency through an almost quadratic waveguide cross section. Using such 3D inverse taper mode converters, typical samples fabricated using the photonic Damascene process have a loss of 3 dB per facet [26], [42]. Second, the ARDE effect allows to fabricate true single mode waveguides next to the multimoded, high-confinement waveguides. Such single mode waveguides are important to enable high ideality coupling to resonators [26] as well as for suppression of unwanted higher-order mode families [43]. Moreover, it enables efficient coupling of the optical mode in a bonded film (such as $LiNbO_3$) ensuring sufficient mode overlap [35]. In the context of the photonic Damascene process the ARDE effect can thus be significant advantage.

C. Preform Reflow for Ultra-Smooth Waveguide Sidewalls

The roughness of waveguide sidewalls is a decisive factor that demetermines loss performance and backreflection. The random roughness created during the dry etch process defining the waveguide causes scattering losses. For tightly confined modes in a high index contrast waveguide platform such scattering can be the dominant loss mechanism [44], [45]. It is thus very important to limit the sidewall roughness through optimized lithography and etchings protocols. However, this has proven to be difficult for typical subtractive processing and diverse post-etching smoothing strategies have been developed, ranging from isotropic etching processes to oxidative processes [46], [47]. Here, we integrate for the first time a reflow step of the SiO_2 preform into a photonic Damascene process which allows to significantly reduce the sidewall roughness.

Similar oxide reflow techniques have been employed in the context of silica microtoroid resonators [48]. Heating the SiO_2 above its glass transititon temperature for sufficient time lowers the viscosity and enables for a surface tension driven reorganization. Here, we heat the substrates to 1250 °C which is slightly above its glass transition temperature of 1200 °C [49]. As shown schematically in Fig. 6(a) and by comparing Fig. 6(c) and (d) the sharp corners of non-reflown waveguides become rounded and the sidewall inclination raises from 85° to approximately 80°. The top view on two adjacent waveguides in Fig. 6(d) and (e) illustrates the effect of the reflow on sidewall roughness. While being well focused, roughness is not visible for the preform after reflow in Fig. 6(e). Atomic force microscopy provides a more accurate tool to quantify roughness and record low values of 1.2 nm rms deviation and a correlation length of 155 nm are reported in [50]. The photonic Damascene process provides thus an opportunity to fabricate waveguides with exceptionally low roughness sidewalls, unattainable with conventional substractive RIE etching techniques. The effects of preform reflow on the waveguide losses and backreflection are analyzed in detail in Section III. Further we note that the smoothingreflow process also enables the use of faster lithography techniques ofwith lower resolution compared to EBL, such as stepper lithography [50]. This is of advantage as the latter allows to combine the filler pattern with the waveguide lithography and reduces the lithography time per wafer from several hours to few minutes.

D. Large Mode Area Waveguides Through Conformal Deposition

The previously described filler pattern based stress management allows for crack free deposition and processing of Si_3N_4 thin films with up to 1.52 μm thickness. While different filler pattern can provide improved relaxation to the film

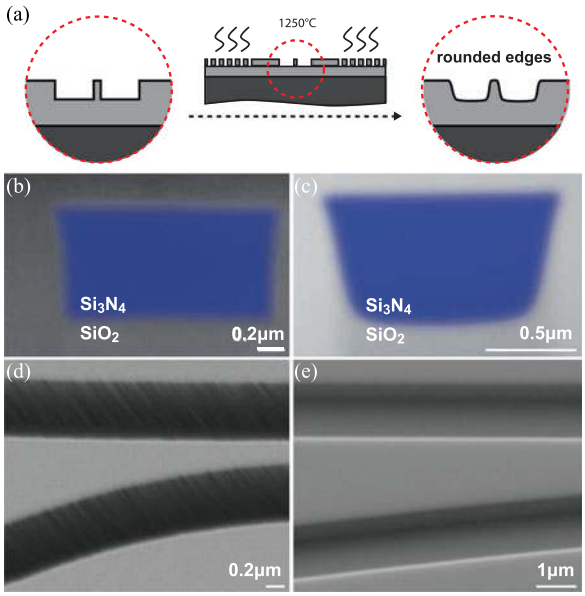

Fig. 6. Preform reflow process for waveguide sidewall smoothing. (a) Schematic representation of the process and its effects on the waveguide profile. (b), (c) Waveguide cross section resulting from a preform fabricated without (b) and with (c) reflow step. As can be seen the reflow step leads to rounded corners of the Si_3N_4 waveguide core (blue). (d), (e) Comparison of sidewall roughness for a preform without (d) and with (e) reflow step. While vertical striations due to the plasma etch process are clearly visible in (d), no roughness is perceived for the reflown preform in (e).

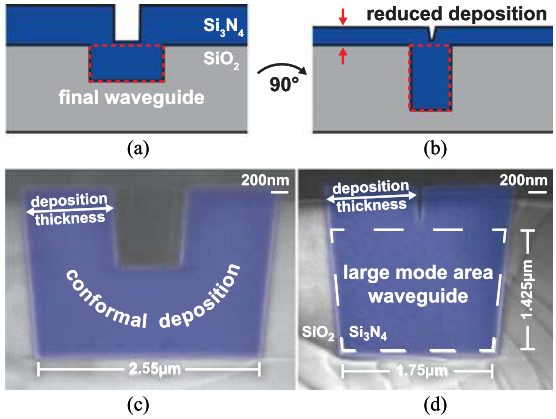

Fig. 7. Fabrication of large mode area waveguides through conformal deposition in inverted aspect-ratio recess. (a) Schematic indicating the final waveguide mode area in recess structures with the typical larger than high dimensions and for an inverted aspect ratio. The latter is filled entirely by a thin film with much reduced thickness compared to the standard approach requiring a deposition exceeding the final waveguide height. (b) Recess structure defined in the SiO_2 preform layer conformally filled by the LPCVD Si_3N_4 (blue). The film thickness on the sidewalls is nearly the same as on the bottom of the recess, indicated excellent step coverage. (c) Large mode area waveguide recess after partial planarization. The deposition thickness is significantly less than the final waveguide height of 1.425 μm.

compromises have to be accepted e.g. in the planarization process. For applications at wavelengths longer than 2.5 μm, in the mid-infrared wavelength region, such supercontinuum generation or frequency comb generation [51], [52] waveguides with larger dimensions can be desirable. As the silicon dioxide cladding is a major source for absorptive losses in this spectral region, engineering high confinement waveguides guiding a majority of light in the core area is paramount for low propagation losses [53]. However, in a subtractive processing scheme, even when employing stress management techniques such as thermal cycling or trench definition, deposition up to such film thicknesses is impossible without extensive film cracking.

As shown in early works [54] and schematically illustrated in Fig. 7(a) the photonic Damascene process provides a solution to the above problem through the fabrication of waveguides with larger depth than width. When defining the waveguide recess structure with a width larger than its height, the thin film deposition thickness needs to exceed the final waveguide height. For an inverted aspect ratio the recess structure can be filled by a thin film with reduced thickness. In case the etched waveguide recess is filled without formation of voids during deposition, this approach yields waveguides with width and height dimensions being exchanged and allows the reduction of film deposition thickness by about 50%. In fact, a high deposition conformality of the waveguide core material is of central importance for the success of the photonic Damascene process. Here, we use a standard dichlorosilane (DCS) and ammonia (NH_3) based high stress LPCVD Si_3N_4 deposition process. As can be seen in Fig. 7(b) the step coverage of the LPCVD Si_3N_4 process is excellent. Little difference between the deposited film thickness on the side and on the top of the substrate is observed. This allows filling of trenches with aspect ratios larger than 1:1 without formation of voids. In Fig. 7(c) the final large mode area of the waveguide is indicated in the void-free filled recess structure. In this way very large mode area waveguides providing high confinement also at mid infrared wavelengths can be realized.

E. Chemical Mechanical Planarization With High Precision

Even though chemical mechanical planarization (CMP) is heavily used in today's CMOS technology yielding extraordinarily smooth surfaces, its process control and understanding is still limited. Within the photonic Damascene process the planarization step is critical in defining the height of the final waveguides. Ensuring uniform material removal rates and consequently minimal waveguide height variation across the wafer is a major challenge, driving the choice of process parameters. The resulting waveguide top surface' roughness (RMS approx. 0.3 nm) is negligible compared to its sidewalls and thus of secondary importance, as well as the overall planarity of the wafer after CMP.

During CMP the wafer is pressed against a rotating polishing pad, constantly wetted by an abrasive slurry. In order to remove the excess Si_3N_4 a slurry based on fumed silica particles of 30 nm diameter in an acidic environment is used. Optical interferometry allows to precisely track locally the film thickness and removal rates across the wafer. The parameters for pad and wafer rotation speed, as well as the pressure between wafer and polishing pad are chosen depending on the intial wafer bow.

With respect to the planarization uniformity two effects were found to be dominant in the photonic Damascene process: the overall wafer bow induced by the highly stressed, asymmetric coating before polishing and a local loading induced non-uniformity. The backside Si_3N_4 thin film needs to be

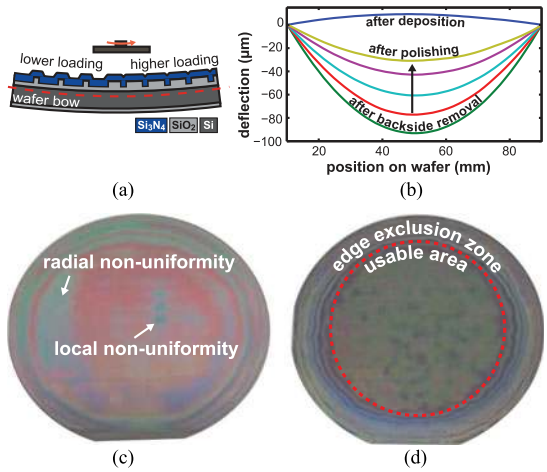

Fig. 8. Chemical mechanical planarization in the photonic Damascene process. a) Schematic representation of the origin of non-uniform planarization. Local structure density variations provide different loading and result in locally varying removal rates during CMP. Asymmetric thin film coating causes wafer bow and radial non-uniformity. b) Measurement of the wafer bow evolution during planarization for a 525 μm thick Si substrate. c) Example of non-optimized planarization showing radial and local non-uniformity through differently colored thin film interference. d) Wafer planarized using an optimized CMP process. The central area uniformily planarized region is about 60 mm in diameter.

removed before planarization as it was found to cause extensive cracking during CMP. This causes an extensive wafer bow prior to planarization due to the assymetric coating of the wafer. In Fig. 8(b) such bending is measured via optical reflectometry and amounts to approx. 90 μm for the 525 μm thick Si substrate coated with 4 μm SiO_2 and 1.04 μm Si_3N_4. During planarization the wafer bow gradually reduces the more Si_3N_4 is polished away. In order to achieve good global uniformity and circumvent the typical radial non-uniformity caused by changing wafer bow, an optimized polishing process using a high down force pressure is used. Additionally an increased substrate thickness of 700 μm provides a more rigid substrate, limiting the initial wafer bow.

Non-uniformity caused by local loading differences originates from different amounts of Si_3N_4 surface being in contact with the polishing pad. If areas with largely different loading are in the vicinity of a waveguide, the removal rates vary slightly over distances of 10–50 μm, resulting ultimately in local variations of the waveguide height [26]. In order to reduce such microloading related effects an optimized filler pattern providing a uniform loading as well as continuous guard structures around the waveguide (parallel lines following the waveguide) were introduced. The waveguide is thus better isolated from surrounding variations in loading ensuring a controlled and repeatable planarization process with a precision sufficient for octave spanning dispersion engineering [26].

III. Loss Analysis

The analysis of waveguide propagation losses is important to improve their fabrication and benchmark different processes. In general, the process related propagation losses are either absorptive (e.g. due to overtones of the O-H, Si-H or Si-N bonds) or due to scattering at the waveguide's sidewall or inhomogeneities inside its core. The attenuation coefficient α for a straight waveguide or the resonator's Q factor at a given wavelength serve as figure of merit and allow the comparison of loss performance. However, in practice the precise measurement of α is not trivial, especially in the case of low loss, on-chip waveguides. Unless the waveguides are sufficiently long the excess losses due to light coupling easily dominate the overall losses. Thus advanced techniques like optical frequency domain reflectometry (OFDR) techniques relying on backscattering inside the waveguides are required [55].

Resonators allow to measure propagation losses independently of coupling losses or reflections at the waveguide facets. The resonance Q factor can be expressed through an extrinsic (output coupling related) and intrinsic loss rate κ_{ex} and κ_0 as $Q = \omega/\kappa = \omega/(\kappa_0 + \kappa_{\mathrm{ex}})$. The intrinsic loss rate κ_0 originates from propagation losses and the extrinsic loss rate relates to the power loss from the resonator to the bus waveguide. The intrinsic loss rate is related to the attenuation coefficient α as: $\alpha = (n_{\mathrm{eff}}\,\kappa_0)/(\nu\lambda) = (2\pi n_{\mathrm{eff}})/(c\nu)Q_0^{-1}$, with n_{eff} being the effective refractive index and ν and λ denoting frequency and wavelength. Varying the distance between the bus and the resonator waveguide allows to change κ_{ex} and the resonator's operation regime can be tuned from under-coupled ($\kappa_{\mathrm{ex}} < \kappa_0$) to over-coupled ($\kappa_{\mathrm{ex}} > \kappa_0$). In order to infer waveguide propagation losses it is best to measure in the under-coupled regime with κ_0 dominating the total resonator losses.

The random sidewall roughness of the resonator waveguide causes backscattering of light into the counter-propagating mode. Such coupling of the counterpropagating resonant modes can lift their degeneracy, cause splitting of the Lorentzian line shape and make the resonator an efficient backreflector [56], [57]. The coupling rate is here denoted as κ_{c} and causes perceivable resonance splitting if it is of the same order as κ_{ex} and κ_0, as shown in Fig. 9(d). Such splitting varies randomly across the resonances of the same resonator as the random distribution of backreflectors does not always lead to coherent build-up of a counter-propagating mode. This makes the direct calculation of the associated scattering losses non-trivial. Nevertheless, the measurement of resonance splitting allows to qualitatively infer the amount of scattering present in the waveguides.

In frequency domain the full width at half maximum (FWHM) linewidth of the resonance's Lorentzian line shape corresponds to the total loss rate $\kappa/2\pi$. Here, we scan a widely tunable diode laser across many resonances of a microresonator in order to systematically characterize losses in our waveguides. The setup used for this purpose is shown schematically in Fig. 9(a). The resonance's line shapes are recorded as dips in the transmission amplitude, as shown in Fig. 9(b). In the case of low losses and correspondingly narrow resonance linewidths, tight calibration of the laser scan is required to accurately determine the resonance linewidths. We use a combination of the continuous sinusoidal signal of an imbalanced Mach-Zehnder interferometer and the regular marker grid provided by a frequency comb to accurately calibrate the laser scan. Alternative techniques like single sideband modulation [58] or cavity ring down measurements [29] offer higher precision for very low loss,

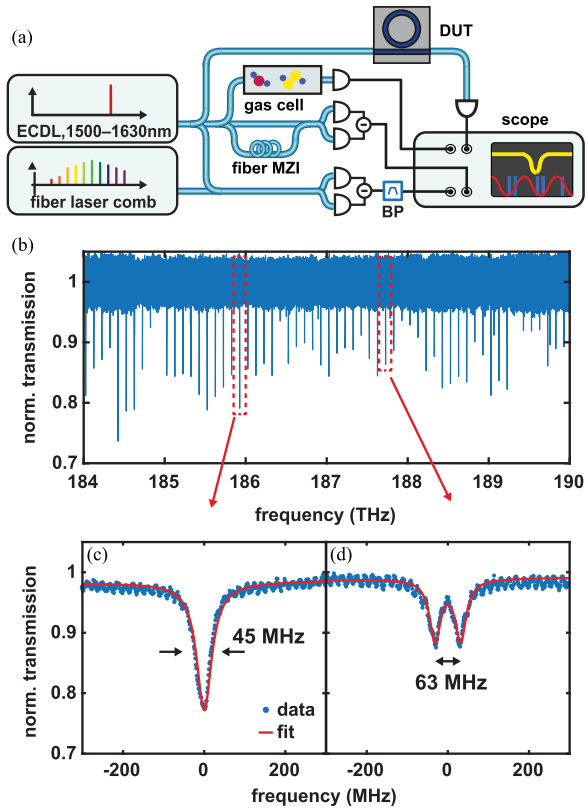

Fig. 9. (a) Setup used for acquisition of calibrated transmission traces of microresonator devices. Frequency calibration of the scan is achieved through reference markers provided by a fiber frequency comb, a gas cell and the sinusoidal signal of an imbalanced MZI. (b) Transmission trace acquired for loss analysis of a microresonator with 230 μm radius corresponding to 100-GHz FSR. The resonances belong to the quasi-TE mode family and are under-coupled. (c) Fit of single resonance using a the model for a Lorentzian line shape. The extinction on resonance is low due to the under-coupled operation regime. Based on the fit the total linewidth is estimated to be 45 MHz corresponding to a Q of 4.1×10^6. (d) Fitted resonance doublet splitted due to coherent backscattering. The fitted splitting rate is 63 MHz and the internal loss rate is found to be $\kappa_0/2\pi = 31.3$ MHz, corresponding to an intrinsic $Q_0 \approx 6 \times 10^6$.

narrow resonances. However, they allow to infer only individual resonances, rendering systematic spectroscopy tedious. The absolute wavelength is calibrated using the absorption peaks of a fiber-coupled gas cell. Our automated data analysis finds and fits resonances within the acquired transmission traces and sorts them into different mode families. As polarization maintaining fibers are used to couple light on the chip only mode families of a single polarization are excited. The individual mode families are differentiated by their different free spectral ranges and dispersion properties. Resonances featuring simple Lorentzian line shapes are fitted using a Lorentzian model and splitted resonances are fitted using a corresponding model [57]. In this way, depending on the resonator's FSR, from 10 to 100 measurement points are recorded between 1500 nm and 1630 nm. All resonators investigated have a constant waveguide cross section along the ring's circumference and its dimensions are specified for the individual measurements.

Fig. 9 shows data acquired for a microresonators fabricated using the photonic Damascene process with reflow step. The resonator and bus waveguides are 0.87 μm high and 2 μm wide. With a radius of 230 μm the resonator features under-coupled resonances for a gap distance of 950 nm. While most resonances belong to the quasi-TE mode family, few other resonances are visible as well. In Fig. 9(c) and d) two examples of fitted resonances are shown. While a perfect Lorentzian with $\kappa/2\pi = 45$ MHz is observed in (c) the resonance in (d) of the same mode family shows strong splitting with $\kappa_c/2\pi = 63$ MHz. However, the fitted intrinsic loss rate $\kappa_0/2\pi = 31.3$ MHz is lower than for (c) and corresponds to an intrinsic Q_0 of 6×10^6 and an attenuation coefficient of 5.5 dB/m. It is noted that the low number of points acquired for such narrow linewidth resonances reduces the precision of the method.

Two parameters corresponding to κ_{ex} and κ_0 are extracted from fitting of the Lorentzian line shape. Unless prior knowledge on the microresonator coupling regime exists or a phase resolved measurement is performed, it remains ambiguous which parameter corresponds to the internal loss rate κ_0. Therefore, we measure several microresonators of the same waveguide cross section with varying distance between bus waveguide and resonator waveguide. Plotting the transmitted power on resonance against the linewidth allows to compare with the ideal model of a coupled resonator. Moreover, the coupling ideality can be evaluated which is the agreement with the ideal model of two coupled modes in bus and resonator waveguide [42]. In the ideal case the power transmitted past the resonator solely depends on κ_0 and κ_{ex} and the laser detuning Δ as $T = [|\kappa_0 - \kappa_{\mathrm{ex}} + 2i\Delta)/(\kappa_0 + \kappa_{\mathrm{ex}} + 2i\Delta)|^2$. In the case of the high confinement, multimoded waveguides described in this paper, systematic excess losses due to the intermode interactions at the resonator coupling section can occur. This phenomenon, called *coupling ideality*, causes severe deviations between the model and the measured resonance behaviour, especially in the overcoupled regime. Additionally, it renders the estimation of loss rates erroneous as the excess losses due to coupling into higher order modes of the bus waveguide are not considered. Fig. 10 shows data acquired for microresonators made from waveguides with 0.87 μm height and 2 μm width and a radius of 230 μm, corresponding to a free spectral range of 100-GHz. The comparison between the ideal model with an intrinsic linewidth of $\kappa_0/2\pi = 60$ MHz shown as red dashed line and the acquired data shows good agreement. All resonators operate in the under-coupled or critically coupled regime. The fitting value related to the internal loss rate can thus unambiguously identify for those resonators. In Fig. 10(b) the mean value as well as the standard deviation of the extracted internal loss rates $\kappa_0/2\pi$ is plotted for the same devices. While individual resonances might feature lower losses we conclude that in average an intrinsic linewidth of $\kappa_0/2\pi = 40$ MHz can be achieved, corresponding to a propagation loss of 6.7 dB/m. As can be seen the statistical mean value of the internal linewidth decreases with increasing gap and correspondingly decreasing external coupling rate. This is partially due to the reduced contribution of coupling ideality related excess losses. However, also the fitting related imprecision of our method is decreasing with reduced linewidth. In general it is thus most interesting to base an estimation of the internal loss rate on the measurement of well undercoupled resonances as the internal loss rate dominates coupling and excess losses.

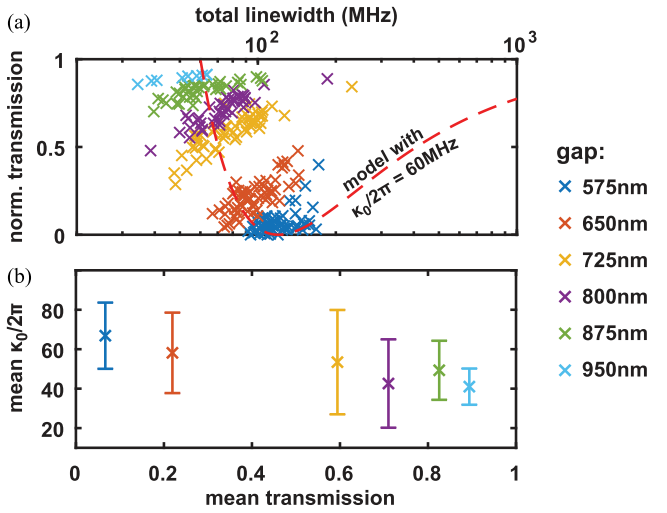

Fig. 10. Systematic analysis of resonance data for 100-GHz FSR resonators with varying coupling gap fabricated using the photonic Damascene process with reflow step. (a) Evaluation of the coupling ideality by plotting the transmission of the fitted resonances against their total linewidth. With increasing coupling gap distance the linewidth reduces and the transmission increases, indicating an undercoupled operation regime in good agreement with the ideal model (red dashed line). (b) Mean of the internal loss rate extracted through systematic fitting of the resonances of the devices shown in a). The error bars indicate the standard deviation associated to the mean value. As can be seen the lowest mean intrinsic loss rate is ∼40 MHz, corresponding 6.7 dB/m propagation loss.

Next, we investigate the effect of sidewall smoothening via preform reflow on the propagation losses and backscattering. We measure the resonances of the lowest order quasi-TE and -TM mode families for resonators with 1-THz free spectral range fabricated with and without sidewall smoothing. For the 1-THz FSR microresonators the quasi-TM mode's FSR is approximately 10-GHz lower than the quasi-TE mode's FSR. The measurement setup's polarization maintaining fibers ensure excitation of only one of the two throughout the measurement range and the comparison of FSR between both polarizations allows to unambiguously identify the mode family. The small mode volume of the resonators renders the splitting more visible [56] and thus allows for precise fitting. We note that the observed splitting can vary largely for the modes of different azimuthal order of the same resonator. This is in agreement with theory which predicts such variation in the case of statistically distributed scattering along the sidewall [59]. We thus rely here on mean values calculated based on at least 3 fitted resonances per resonator.

Fig. 11 shows a comparison between values obtained based on different 1-THz FSR microresonators with varying coupling gap distance and constant radius of 23 μm, height of 0.85 μm and width of 1.5 μm. As can be seen the reflow process improves the losses for both TE and TM mode families, reaching around 100 MHz intrinsic linewidth. We note that the intrinsic losses are higher than for the 100-GHz FSR resonators shown in Fig. 10. This is in agreement with the common dependence of microresonator Q factor on radius [60]. Interestingly TE polarized modes exhibit in both cases lower intrinsic losses than TM polarized modes, which is contrary to findings made for straight SOI waveguides [61]. Besides the differences in field strength

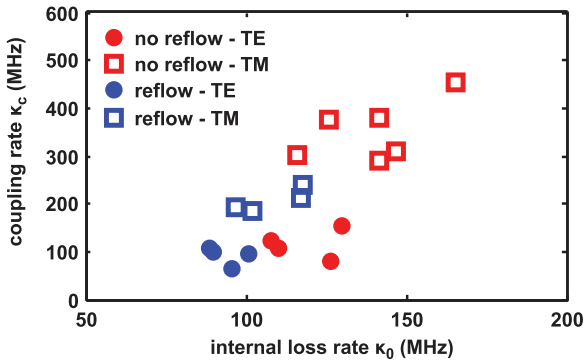

Fig. 11. Comparison of mean internal loss rate and coupling rate for the lowest order quasi-TE and -TM mode families of 1-THz FSR samples with and without reflow. Each data point represents the mean value for a resonator and is calculated based on at least 3 measured resonances. Reflown samples (blue data points) show reduced internal loss and coupling rates compared to non-reflown samples (red data points). Fundamental TM mode resonances (squares) have high losses and stronger resonance splitting compared to TE mode resonances (solid circles).

at the sidewalls, also their confinement in the Si_3N_4 waveguide core is different. The TE polarized modes are better confined and the correlation with lower loss values, while being in agreement with results obtained for large mode area waveguides, indicates a loss origin at the waveguide boundary or in the cladding oxide. Nevertheless, for both polarizations the internal loss rate $\kappa_0/2\pi$ and the mean resonance splitting are reduced for samples fabricated with the reflow step. As the reduced sidewall roughness represents the most significant difference between both sample types, we attribute the reduced losses and the reduction of scattering to the reflow induced reduction in sidewall roughness.

IV. Conclusion

In conclusion we have presented a novel photonic Damascene process extended by a preform reflow step enabling the fabrication of ultra-smooth sidewall Si_3N_4 waveguides that exhibit low loss and simultaneously high confinement. The challenges and beneficial aspects associated to the process approach were discussed, demonstrating record large mode areas as well as exceptionally low sidewall roughness. The elegant use of aspect ratio dependent etch rate allow to realize 3D tapered sections that allow to realize mode filters and efficient on-chip coupling. A methodology for systematic loss analysis based the linewidth analysis of microresonators was presented. The comparison of values acquired for waveguides fabricated with and without reflow step clearly reveals the improvements achieved through the additional sidewall smoothening. The loss performance achieved approaches the best values reported for high confinement Si_3N_4 waveguides fabricated by subtractive processing. Most importantly the reported values are the highest Q values reported for waveguides with dimensions allowing for anomalous GVD. The photonic Damascene process with reflow step is thus especially interesting for nonlinear photonic applications, and can prove the basis for further loss improvement towards record ultra low loss waveguides for integrated photonics, as it provides unparalleled roughness advantages compared to substrative processing.

REFERENCES

[1] H. Lee, T. Chen, J. Li, O. Painter, and K. J. Vahala, "Ultra-low-loss optical delay line on a silicon chip," *Nature Commun.*, vol. 3, 2012, Art. no. 867.

[2] F. Dell'Olio, T. Tatoli, C. Ciminelli, and M. N. Armenise, "Recent advances in miniaturized optical gyroscopes," *J. Eur. Opt. Soc.*, vol. 9, 2014, Art. no. 14013.

[3] S. Gundavarapu *et al.*, "Integrated ultra-low-loss silicon nitride waveguide coil for optical gyroscopes," *Opt. Fiber Commun. Conf.*, 2016, Paper W4E.5.

[4] T. Komljenovic *et al.*, "Widely tunable narrow-linewidth monolithically integrated external-cavity semiconductor lasers," *IEEE J. Sel. Topics Quantum Electron.*, vol. 21, no. 6, Nov./Dec. 2015, Art. no. 1501909.

[5] H. Lee *et al.*, "Spiral resonators for on-chip laser frequency stabilization," *Nature Commun.*, vol. 4, 2013, Art. no. 2468. [Online]. Available: http://www.nature.com/doifinder/10.1038/ncomms3468

[6] D. J. Moss, R. Morandotti, A. L. Gaeta, and M. Lipson, "New CMOS-compatible platforms based on silicon nitride and Hydex for nonlinear optics," *Nature Photon.*, vol. 7, no. 8, pp. 597–607, 2013.

[7] T. J. Kippenberg, R. Holzwarth, and S. A. Diddams, "Microresonator-based optical frequency combs," *Science*, vol. 332, no. 6029, pp. 555–559, Apr. 2011. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/21527707

[8] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O'Brien, "Silica-on-silicon waveguide quantum circuits," *Science*, vol. 320, no. 5876, pp. 646–649, 2008.

[9] N. C. Harris *et al.*, "Large-scale quantum photonic circuits in silicon," *Nanophotonics*, vol. 5, no. 3, pp. 456–468, 2016.

[10] M. E. Lines, "Ultralow-loss glasses," *Annu. Rev. Mater. Res.*, vol. 16, pp. 113–35, 1986.

[11] C. H. Henry, R. F. Kazarinov, H. J. Lee, K. J. Orlowsky, and L. E. Katz, "Low loss Si3N4-SiO2 optical waveguides on Si," *Appl. Opt.*, vol. 26, no. 13, pp. 2621–2624, 1987.

[12] M. J. R. Heck, J. F. Bauters, M. L. Davenport, D. T. Spencer, and J. E. Bowers, "Ultra-low loss waveguide platform and its integration with silicon photonics," *Laser Photon. Rev.*, vol. 8, no. 5, pp. 667–686, 2014.

[13] A. Rahim *et al.*, "Expanding the silicon photonics portfolio with silicon nitride photonic integrated circuits," *J. Lightw. Technol.*, vol. 35, no. 4, pp. 639–649, Feb. 2017.

[14] R. Hainberger *et al.*, "Silicon nitride waveguide integration platform for medical diagnostic applications," in *Proc. Prog. Electromagn. Res. Symp.*, 2016, Paper 781.

[15] Q. Li, M. Davanço, and K. Srinivasan, "Efficient and low-noise single-photon-level frequency conversion interfaces using silicon nanophotonics," *Nature Photon.*, vol. 10, no. 6, pp. 406–414, 2016.

[16] P. Tai Lin, V. Singh, L. Kimerling, and A. Murthy Agarwal, "Planar silicon nitride mid-infrared devices," *Appl. Phys. Lett.*, vol. 102, 2013, Art. no. 251121.

[17] P. Muñoz *et al.*, "Silicon nitride photonic integration platforms for visible, near-infrared and mid-infrared applications," *Sensors*, vol. 17, no. 9, pp. 1–25, 2017.

[18] M. J. Shaw, J. Guo, G. A. Vawter, S. Habermehl, and C. T. Sullivan, "Fabrication techniques for low-loss silicon nitride waveguides," *Proc. SPIE*, vol. 5720, pp. 109–118, 2005.

[19] M. Melchiorri *et al.*, "Propagation losses of silicon nitride waveguides in the near-infrared range," *Appl. Phys. Lett.*, vol. 86, 2005, Art. no. 121111.

[20] E. S. Hosseini, S. Yegnanarayanan, A. H. Atabaki, M. Soltani, and A. Adibi, "High quality planar silicon nitride microdisk resonators for integrated photonics in the visible wavelength range," *Opt. Express*, vol. 17, no. 17, pp. 14543–14551, 2009.

[21] J. F. Bauters *et al.*, "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding," *Opt. Express*, vol. 19, no. 24, pp. 24090–24101, 2011.

[22] J. Li, Z. Shan, and E. Ma, "Elastic strain engineering for unprecedented materials properties," *MRS Bull.*, vol. 39, no. 2, pp. 108–114, 2014.

[23] C. J. Krückel *et al.*, "Linear and nonlinear characterization of low-stress high-confinement silicon-rich nitride waveguides," *Opt. Express*, vol. 23, no. 20, pp. 25827–25837, 2015.

[24] K. J. A. Ooi *et al.*, "Pushing the limits of CMOS optical parametric amplifiers with USRN:Si7N3 above the two-photon absorption edge," *Nature Commun.*, vol. 8, 2017, Art. no. 13878.

[25] R. Halir *et al.*, "Ultrabroadband supercontinuum generation in a CMOS-compatible platform," *Opt. Lett.*, vol. 37, no. 10, pp. 1685–1687, 2012.

[26] M. H. P. Pfeiffer *et al.*, "Octave-spanning dissipative Kerr soliton frequency combs in Si3N4 microresonators," *Optica*, vol. 4, no. 7, pp. 684–691, 2017.

[27] A. Gondarenko, J. S. Levy, and M. Lipson, "High confinement micron-scale silicon nitride high Q ring resonator," *Opt. Express*, vol. 17, no. 14, pp. 11366–11370, 2009.

[28] M. J. Madou, *Fundamentals of Microfabrication and Nanotechnology, vol. II*. Boca Raton, FL, USA: CRC Press, 2011.

[29] Y. Xuan *et al.*, "High-Q silicon nitride microresonators exhibiting low-power frequency comb initiation," *Optica*, vol. 3, no. 11, pp. 1171–1180, 2016.

[30] X. Ji *et al.*, "Ultra-low-loss on-chip resonators with sub-milliwatt parametric oscillation threshold," *Optica*, vol. 4, no. 6, pp. 619–623, 2017.

[31] N. Daldosso *et al.*, "Comparison among various Si3N4 waveguide geometries grown within a CMOS fabrication pilot line," *J. Lightw. Technol.*, vol. 22, no. 7, pp. 1734–1740, Jul. 2004.

[32] Y. Huang, J. Song, X. Luo, T.-Y. Liow, and G.-Q. Lo, "CMOS compatible monolithic multi-layer Si_3N_4-on-SOI platform for low-loss high performance silicon photonics dense integration," *Opt. Express*, vol. 22, no. 18, pp. 21859–21865, 2014. [Online]. Available: https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-18-21859

[33] C. W. Kaanta *et al.*, "Dual Damascene: A ULSI wiring technology," in *Proc. 18th Int. IEEE VLSI Multilevel Interconnection Conf.*, 1991, pp. 144–152.

[34] M. H. P. Pfeiffer *et al.*, "Photonic Damascene process for integrated high-Q microresonator based nonlinear photonics," *Optica*, vol. 3, no. 1, pp. 20–25, 2016.

[35] L. Chang *et al.*, "Heterogeneous integration of lithium niobate and silicon nitride waveguides for wafer-scale photonic integrated circuits on silicon," *Opt. Lett.*, vol. 42, no. 4, pp. 803–806, 2017.

[36] A. B. Kahng, S. Member, K. Samadi, and S. Member, "CMP fill synthesis: A survey of recent studies," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 1, pp. 3–19, Jan. 2008.

[37] K. H. Nam, I. H. Park, and S. H. Ko, "Patterning by controlled cracking," *Nature*, vol. 485, no. 7397, pp. 221–224, 2012.

[38] K. Luke, A. Dutt, C. B. Poitras, and M. Lipson, "Overcoming SiN film stress limitations for high quality factor ring resonators," *Opt. Express*, vol. 21, no. 19, pp. 22 829–22 833, 2013.

[39] N. Ikegami, A. Yabata, T. Matsui, J. Kanamori, and Y. Horiike, "Characteristics of very high-aspect-ratio contact hole etching," *Jpn. J. Appl. Phys., Part 1, Reg. Papers Short Notes Rev. Papers*, vol. 36, no. 4, pp. 2470–2476, 1997.

[40] R. A. Gottscho, C. Jurgensen, and D. J. Vitkavage, "Microscopic uniformity in plasma etching," *J. Vacuum Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 10, no. 5, pp. 2133–2147, 1992.

[41] V. R. Almeida, R. R. Panepucci, and M. Lipson, "Nanotaper for compact mode conversion," *Opt. Lett.*, vol. 28, no. 15, pp. 1302–1304, 2003.

[42] M. H. Pfeiffer, J. Liu, M. Geiselmann, and T. J. Kippenberg, "Coupling ideality of integrated planar high- Q microresonators," *Phys. Rev. Appl.*, vol. 7, no. 2, 2017, Art. no. 024026.

[43] A. Kordts, M. H. P. Pfeiffer, H. Guo, V. Brasch, and T. J. Kippenberg, "Higher order mode suppression in high-Q anomalous dispersion SiN microresonators for temporal dissipative Kerr soliton formation," *Opt. Lett.*, vol. 41, no. 3, pp. 452–455, 2015.

[44] A. Snyder, "Excitation and scattering of modes on a dielectric or optical fiber," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-17, no. 12, pp. 1138–1144, Dec. 1969.

[45] D. Melati, A. Melloni, and F. Morichetti, "Real photonic waveguides: guiding light through imperfections," *Adv. Opt. Photon.*, vol. 6, no. 2, pp. 156–224, 2014.

[46] S. J. Spector, D. K. Sparacin, S. J. Spector, and L. C. Kimerling, "Silicon waveguide sidewall smoothing by wet silicon waveguide sidewall smoothing by wet chemical oxidation," *J. Lightw. Technol.*, vol. 23, no. 8, pp. 2455–2461, Aug. 2005.

[47] C. Bellegarde *et al.*, "Improvement of sidewall roughness of sub-micron silicon-on-insulator waveguides for low-loss on-chip links," *Proc. SPIE*, vol. 10108, 2017, Art. no. 1010816.

[48] D. K. Armani, T. J. Kippenberg, S. M. Spillane, and K. J. Vahala, "Ultra-high-Q toroid microcavity on a chip," *Nature*, vol. 421, no. 6926, pp. 925–928, 2003.

[49] M. I. Ojovan, "Configurons: Thermodynamic parameters and symmetry changes at glass transition," *Entropy*, vol. 10, no. 3, pp. 334–364, 2008.

[50] M. H. P. Pfeiffer *et al.*, "Probing the loss origins of ultra-smooth Si3N4 integrated photonic waveguides," 2018, arXiv: 1802.08315.
[51] K. Luke, Y. Okawachi, M. R. E. Lamont, A. L. Gaeta, and M. Lipson, "Broadband mid-infrared frequency comb generation in a Si3N4 microresonator," *Opt. Lett.*, vol. 40, no. 21, pp. 4823–4826, 2015.
[52] H. Guo *et al.*, "Mid-infrared frequency comb via coherent dispersive wave generation in silicon nitride nanophotonic waveguides," *Nat. Photon.*, 2018.
[53] S. A. Miller *et al.*, "Low-loss silicon platform for broadband mid-infrared photonics," *Optica*, vol. 4, no. 7, pp. 5–10, 2017.
[54] J. Epping *et al.*, "High confinement, high yield Si3N4 waveguides for nonlinear optical applications," *Opt. Express*, vol. 23, no. 2, pp. 642–648, 2015.
[55] U. Glombitza and E. Brinkmeyer, "Coherent frequency-domain reflectometry for characterization of single-mode integrated-optical waveguides," *J. Lightw. Technol.*, vol. 11, no. 8, pp. 1377–1384, Aug. 1993.
[56] T. J. Kippenberg, S. M. Spillane, and K. J. Vahala, "Modal coupling in traveling-wave resonators," *Opt. Lett.*, vol. 27, no. 19, pp. 1669–1671, 2002.
[57] M. L. Gorodetsky, A. D. Pryamikov, and V. S. Ilchenko, "Rayleigh scattering in high- Q microspheres," *J. Opt. Soc. Amer. B*, vol. 17, no. 6, pp. 1051–1057, 2000.
[58] X. Xue *et al.*, "Mode-locked dark pulse Kerr combs in normal-dispersion microresonators," *Nature Photon.*, vol. 9, no. 9, pp. 594–600, 2015.
[59] Q. Li, A. A. Eftekhar, Z. Xia, and A. Adibi, "Unified approach to mode splitting and scattering loss in high-Q whispering-gallery-mode microresonators," *Phys. Rev. A, Atomic, Mol., Opt. Phys.*, vol. 88, no. 3, pp. 1–11, 2013.
[60] M. Borselli, T. Johnson, and O. Painter, "Beyond the Rayleigh scattering limit in high-Q silicon microdisks: Theory and experiment." *Opt. Express*, vol. 13, no. 5, pp. 1515–1530, 2005.
[61] F. Morichetti *et al.*, "Roughness induced backscattering in optical silicon waveguides," *Phys. Rev. Lett.*, vol. 104, no. 3, pp. 1–4, 2010.

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