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PHOTOVOLTAIC POWER CONDITIONING SUBSYSTEM: STATE OF THE ART AND DEVELOPMENT OPPORTUNITIES

By
S. Krauthamer
K. Bahrami
R. Das
T. Macie
W. Rippel

January 15, 1984

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Jet Propulsion Laboratory
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ABSTRACT

Photovoltaic systems, the state of the art of power conditioning subsystem components, and the design and operational interaction between photovoltaic systems and host utilities are detailed in this document. Major technical issues relating to the design and development of power conditioning systems for photovoltaic application are also considered, including: (1) standards, guidelines, and specifications; (2) cost-effective hardware design; (3) impact of advanced components on power conditioning development; (4) protection and safety; (5) quality of power; (6) system efficiency; and (7) system integration with the host utility. In addition, theories of harmonic distortion and reactive power flow are discussed, and information about power conditioner hardware and manufacturers is provided.

FOREWORD

Power conditioning development has been a significant component of the Photovoltaics (PV) Program of the U.S. Department of Energy (DOE). This document establishes a perspective for that effort. Because alternative renewable energy sources are expected to become competitive with more conventional utility energy generation sources, realization of the full potential of the alternative energy will ultimately require interconnections with the utility grid. Power conditioners must therefore be grid compatible. The DOE has long recognized the need to resolve interconnection issues to ensure a smooth integration of Dispersed Storage and Generations (DSG) systems into the utility grid. The Electric Energy Systems Division (DOE/EES) has been given the generic responsibility for ensuring the integration of DSG systems with the utility grids without undue difficulties. The Photovoltaics Energy Technology Division has the responsibility for developing photovoltaics as a renewable alternative energy source.

In concert with the generic EES programs and in the context of making photovoltaics viable as an alternative energy source, the DOE/PV program has a continuing interest in facilitating the integration of photovoltaics with the utility grid. More specifically, the DOE/PV program complements the DOE/EES program by addressing the interconnection issues from a point of view unique to the PV program. To that end, the JPL Photovoltaics Technology Development and Applications Lead Center published "Distributed Photovoltaic Systems: Utility Interface Issues and Their Present Status" (JPL Publication 81-89) in September 1981. The study addressed the outstanding utility interconnection issues from a photovoltaics point of view and identified relevant unresolved technical issues. This led in turn to the preparation in November 1981 by the JPL Lead Center, in conjunction with the Electric Power Research Institute, of a draft entitled "Interim Working Guidelines and Discussion Concerning the Interface of Small Dispersed Photovoltaic (PV) Power Producers with Electric Utility Systems." These guidelines were ultimately published by EPRI as "Interconnecting D.C. Energy Systems: Responses to Technical Issues" (EPRI Publication AP/EM-3124) in June 1983. These documents provide a source of technical input in support of the national consensus standards process sponsored by the IEEE and others.

The aforementioned activities in the Photovoltaics Program to resolve utility interface issues have made the critical role of PV power conditioning systems increasingly evident. The objective of this current publication is to complement those earlier efforts by bringing together in one report the essentials of the photovoltaics power conditioning discipline needed for a complete understanding of photovoltaics interconnection issues.

Robert V. Powell
Manager
Systems Research and Technology
Photovoltaics Program
TD&A Lead Center
Jet Propulsion Laboratory

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PART ONE

EXECUTIVE SUMMARY

EXECUTIVE SUMMARY

1.0 BACKGROUND

As the cost of conventional fuels has increased and their availability has decreased, other methods of generating electricity have attracted a great deal of attention, particularly those methods that do not use scarce resources. Solar- and wind-based generations are examples. One of the solar-based generation technologies is photovoltaics (PV), a process that uses solid-state devices to generate electricity from sunlight. Direct current is produced and is subsequently converted to ac power. The power output range of these systems could be from a few kilowatts to greater than 10 megawatts. Photovoltaic power generation has various applications. It may be used in residential, intermediate, and central station systems and has the potential of economically displacing significant amounts of centrally generated electricity.

There are several factors that affect the design and development of a PV system. The major factors include safety and economics. The objective would be to design and build the system to maximize the return or the invested capital within the safety and operational requirements. In this process of optimization, the selection, design, and development of various parts of the PV system play important roles. The power conditioning subsystem (PCS) is one such element whose selection, design, and development affect the economic and technical viability of the PV system.

2.0 PURPOSE, APPROACH, AND SELECTION

The purpose of this document is to provide an overview of power conditioning design elements, concerns, and issues for large, intermediate, and small (residential) photovoltaic systems. Specific objectives include:

(1) Defining important issues and tradeoffs relating to the design and development of power conditioning subsystems for photovoltaic application.

(2) Providing an integrated and generic discussion of photovoltaic systems, state of the art of power conditioning components and design, and the operational interaction between the photovoltaic (PV) systems and the host utilities.

The approach to this document is based on the philosophy that the power conditioning subsystem cannot be considered by itself but must be considered as one element of an integrated photovoltaic system. The consideration must include the challenging problems of working with a highly variable dc source (variable insolation and variable characteristics of PV cells due to ambient temperature and cell-age dependence), having to meet demanding requirements from the host utility (relating to operational safety, quality of power, and reliability), and providing acceptable performance at reasonable costs.

There are many external requirements being placed on the power conditioning subsystem (such as harmonics and power factor) that may preclude the use of a less complex power conversion method. The electrical characteristics

of the array and its output need to be studied to provide insight into optimal energy extraction methods and its impact on PCS sizing, cost, and rating. The PV array interface is unique in its demand on PCS design and must be clearly understood to design power conditioning equipment and to apply power conditioning technology intelligently. The utility interface impacts the PCS design cost and performance. The implication of these impacts must be understood. As the penetration of PV systems into the utility increases and more stringent utility requirements relating to power quality (harmonics), reactive power, etc., are imposed, the need for understanding the issues involved in power conditioner design and development assume an even greater importance. The current industrial power conditioning experience may not be sufficient to provide power conditioning subsystems that meet stringent cost and projected performance requirements for PV systems but will have to be augmented by the pursuit of new development opportunities.

This document begins with a historical perspective of power conversion technology in an attempt to lay the foundation for subsequent discussions. Advantages and disadvantages of rotary and solid-state power conversion technologies are provided. Generic discussions of large, intermediate, and small PV systems follow. The configuration of the PV systems, the characteristics of their elements, as well as their interactions with each other and with the host utility, are discussed. The complex nature of power conditioning designs is demonstrated and assessed by reviewing the requirements of complete PV systems in various operating modes. Fundamentals of inverters are discussed in some detail. Then specific design approaches to power conditioning for both current and advanced topologies are explored.

The aforementioned criteria establish the groundwork for defining the important issues and tradeoffs that are brought about in the development of power conditioning technologies and their applications suitable for PV application. These issues and tradeoffs are explored in depth in this document.

3.0 PHOTOVOLTAIC SYSTEM CONFIGURATON, REQUIREMENTS, AND OPERATION

3.1 SYSTEM CONFIGURATION

A block schematic diagram of a utility-interactive photovoltaic system is shown in Figure 1. The system consists of a PV array subsystem, power conditioning subsystem, utility interconnection subsystem, and control subsystem.

The PV array subsystem converts solar energy into electrical power. It collects dc power and provides protection for PV arrays. The subsystem consists of PV cells assembled into modules, dc cabling and certain protection equipment. The cells and modules are electrically connected in series and in parallel to obtain the desired operating voltage and current levels. Means of protection for the array and means of isolating the array from the PCS are provided to facilitate the maintenance of the array. The array subsystem includes any field fuses, switches, and disconnects that may be necessary. It may include a distribution panel for array wiring and may also include experimental instrumentation.

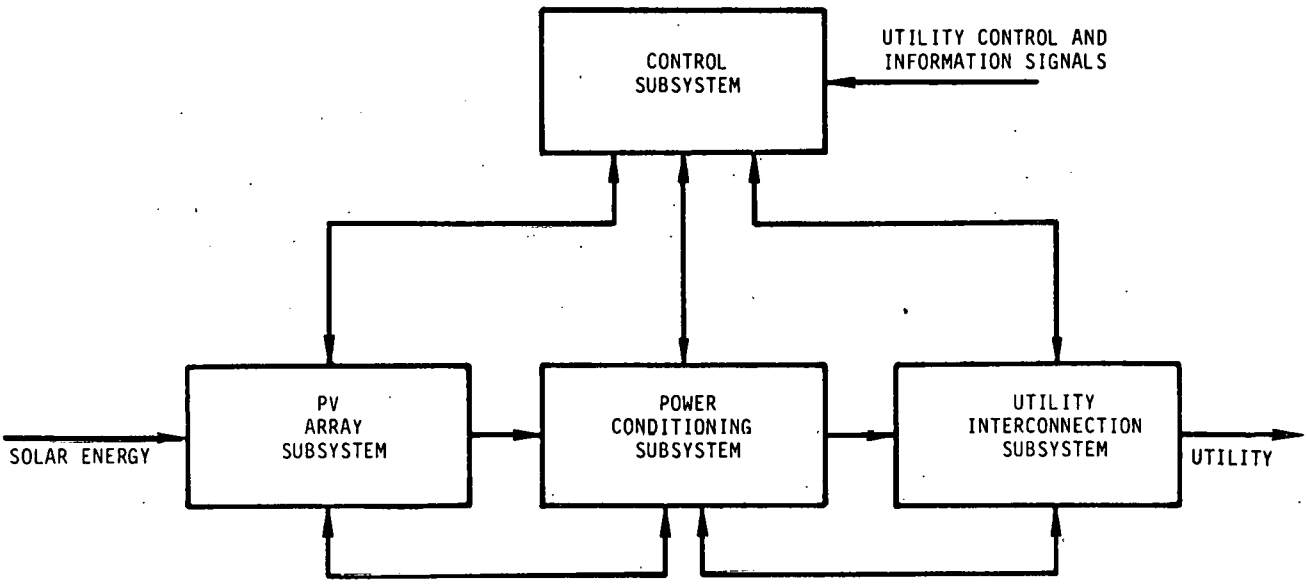

Figure 1. Block Diagram of a Utility Interactive Photovoltaic System

PCS converts dc-power to ac-power and also does the following: regulates the amount of power extracted from the PV array at any given insolation and environmental condition, causes the desired voltage and frequency levels to be achieved at the output (ac side) of the PV system, and provides the necessary protection for the components within the PCS as well as a certain amount of protection for equipment outside the PCS. It also provides the necessary control action within the PCS.

The utility interconnection subsystem provides means for synchronization with the connection to the utility. Also, it provides the means for the isolation of the PV system from the utility when necessary. It protects the utility system from malfunctions within the PV system. Similarly, it protects the PV system from utility abnormal conditions. The subsystem may include appropriate meters and instrumentation equipment as specified within the utility interface requirements.

The control subsystem oversees the operation of the PV system and performs the following functions: provides overall coordination of system protection, communicates status information to the utility dispatch center, and if so desired, provides signals for tracking the PV array. In the case of larger PV systems it can also receive operational commands from the utility dispatch center.

3.2 SYSTEM PERFORMANCE REQUIREMENTS

The system performance requirements may include requirements on efficiency, voltage regulation, voltage flicker, dc injection into the utility system, output reactive power, harmonics, and voltage unbalance.

3.3 SYSTEM PROTECTION REQUIREMENTS

The PV system and the utility systems should be protected against abnormal operating conditions such as under/overvoltage, overcurrent, over or under frequency. Some of these abnormal conditions may originate either in the PV system or the utility system. If the utility bus is de-energized, the PV system should be isolated and should remain isolated until conditions permit resynchronization. Protection systems should be mutually time-coordinated to disconnect the PV system from the utility under these abnormal conditions.

3.4 SYSTEM OPERATION

There are three possible conditions of PV system operation: constant current operation, constant voltage operation, and maximum power operation. Independent of the operational mode, the primary objective is to be able to extract maximum energy from the array. Therefore, an understanding of the array characteristics for a specific site is essential in designing an efficient PV system. In this section, PV system operation will be examined. Although these discussions will refer to flat-plate arrays, tracking arrays exhibit similar electrical behavior in a particular mode of operation.

Constant Current Operation. Because the PCS consists of solid-state components that are limited by current ratings, the PV array may be operated in a constant current mode. As a result, a fluctuation in array output power will cause PCS input voltage to change. If the dc voltage is within specified limits, constant current operation will continue; otherwise, the PCS will be shut off.

Constant Voltage Operation. Here the dc array voltage is compared with a reference value and the difference is kept to a minimum. In general, however, fixed-voltage operation does not guarantee maximum power output. Adjusting reference voltage may improve efficiency, but it requires adjustment seasonally.

Maximum Power Operation. In this mode of operation a closed-loop feedback control system is used, PCS output power is sensed, and operation at maximum power is achieved by continuously shifting the operating point on the array characteristics. There are many schemes of maximum power tracking.

One scheme of maximum power tracking is the perturb-and-observe scheme. In this scheme, the operating point of the array/inverter combination is shifted slightly by a change in the inverter controls. The power before and after the change is compared. If the power is found to have increased, then the previous operating point was not the point of maximum power. A further change in the same direction is made. If the power is found to have decreased, the direction of the perturbation is changed, and the process repeated. When the temperature and insolation are constant, this maximum power tracker will operate in a limit cycle around the point of maximum power.

There is another interesting peak power tracking approach. In this approach, ripple power is sensed and, when ripple power is equal to zero, the maximum power point is reached.

3.5 SELECTION AND SIZING OF PCS

In the selection and sizing of a PCS for a given PV array, the primary objective is to be able to capture maximum solar energy at the least possible cost. That is, the levelized energy cost or the bus bar energy cost associated with the selected PCS and the given array must be minimum. The selection of a PCS in terms of voltage, current, and power ratings must be based on the cost per unit of energy output. Therefore, the sensitivity of these ratings to the energy cost must be examined.

Voltage Rating. Selection of voltage rating of a PCS may be dictated by the application. However, presently available power conditioners have only discrete voltage ratings. As a result, there may be two ways to match the load voltage to the PCS output (ac) voltage: (1) Select a PCS with output voltage rating equal to the load voltage; and (2) Select a PCS with output voltage rating not equal to the required load voltage and use a transformer to match the load voltage. For small and intermediate size systems, power conditioning subsystems presently available have discrete dc/ac voltage ratings. For large PV systems, they are not available and have to be designed specially. Input (dc) voltage rating is provided by the manufacturer of the selected PCS or will depend on the inverter topology for a PCS if it is to be designed for special applications.

Current Rating. Once power and voltage ratings are determined, current ratings for ac and dc sides can be specified.

Energy Conversion Performance Factor. The energy conversion performance factor (ECPF) is a measure of the ability of the PCS to convert available array energy into usable ac output. If is defined in terms of array energy utilization capability, weighted average conversion efficiency, and miscellaneous loooco.

PCS Voltage Limits. Any time the PCS is not loaded, the array open-circuit voltage will rise. Therefore, allowable dc input voltage limits for the PCS must be examined in selecting a PCS.

PCS Sizing and Selection. Given an array, the selection of a PCS for a small and intermediate-size, utility-interactive PV system involves the following steps:

Step 1: Develop a data base consisting of:

(a) Weather data for the site.

(b) Available PCS cost and performance data.

(c) Utility operational requirements, if any.

(d) Utility interface requirements.

Step 2: Select shutdown, partial, or total rejection strategies for overlimit conditions.

Step 3: Select constant voltage or maximum power operation strategy.

Step 4: Determine power, voltage, and current ratings for the PCS.

Step 5: Determine power, voltage, and current limits for overlimit PCS conditions.

Step 6: Performance life-cycle cost (LCC) analysis subject to one set of variables in Steps 1 through 5.

Step 7: Repeat Steps 1 through 6 with other sets of variables until LCC is minimum.

Step 8: Select PCS corresponding to minimum LCC. PCS parameters and operating strategies in Steps 1 through 5 will correspond to minimum LCC.

For large PV systems, PCS cost and performance data is limited. LCC analysis in this case may be performed with respect to various PCS topologies and other variables of Steps 1 through 5. The PCS selected will ensure minimum LCC. Figure 2 is a flow chart illustrating the above procedure for selecting a PCS.

4.0 INVERTER TECHNOLOGY

4.1 HISTORY

In the early 1900s, the conversion of electrical energy from dc to ac was accomplished by dc motor motor/alternator rotating machines. In the late 1920s, static power converters were developed using thyratron-type (mercury arc) valves.

In the 1950s, with the development of the power transistor and the silicon controlled rectifier (SCR) and the discovery of a means of feeding reactive loads without power factor correction, a significant change occurred in the dc-to-ac inversion methodology. The need for high-efficiency and high-reliability inverters for both military and space needs sparked a resurgence in the development of static inversion technology. The technologies used during the 1950s were also used for synthetic textile fiber manufacturing applications.

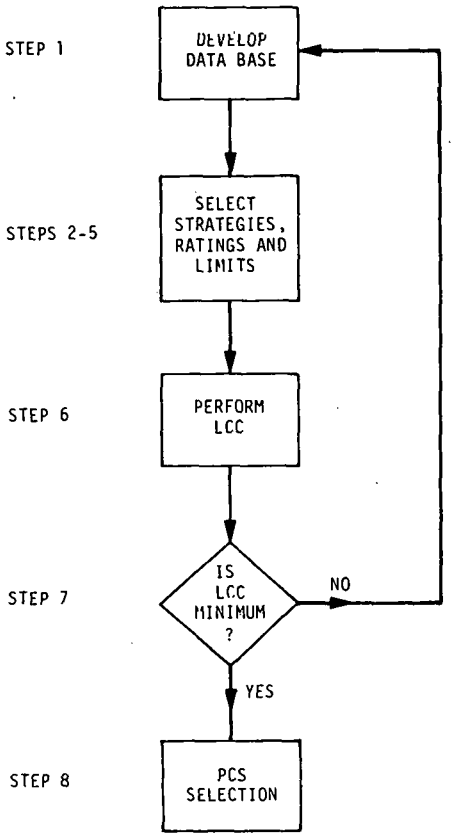

Figure 2. Procedure for Selecting a Power Conditioning Subsystem

In the late 1950s, two developments were commercialized that resulted in the first solid-state, dc-to-ac inverter. These developments were the power transistor and the thyristor. With the early power transistors, collector voltages were typically limited to less than about 60 V. Thus, these devices were limited to low-power linear applications such as audio amplifiers. Because of their low-switching speeds, inverter applications were limited to 400 Hz and less. In contrast to power transistors, thyristors quickly developed into high-power devices capable of switching hundreds of amps at over 1000 V. By the end of the 1960s, devices rated at over 1000 A and 1500 V were in production.

During the past 20 years, semiconductor switching speeds have been improved and their costs have reduced. Self turn-off devices have been introduced. Two major thrusts have occurred:

(1) Transistor systems are continuing to displace thyristor systems to increasingly higher power levels.

(2) Totally new inverter and converter applications and techniques are being developed.

Bipolar transistors and thyristors have been widely used in inverter design. Gate turn-off thyristors (GTOs) are currently available for use in advanced inverter design.

Many new high-power semiconductor devices are in development. When these devices become available, new opportunities will be presented for new inverter topology development, affording potentially low-cost and high-performance power conditioner subsystems. Some devices are available in prototype or initial production phase quantities and others are in the research phase. Several of these devices are:

(1) Gallium Arsenide Field-Effect Transistor (GaAsFET).

(2) Insulated Gate Transistor (IGR).

(3) Static Induction Transistor (SIT).

(4) Field-Controlled Thyristor (FCT).

(5) Reverse-Conduction Thyristor (RCT).

(6) Asymmetrical Thyristor (ASCR).

Table 1 is a comparison of operating characteristics for gate turn-off devices. These include bipolar, GTO, MOSFET, SIT, FCT, GaAsFET devices. These devices have applications in both low-, medium-, and high-power applications. It should be noted that the technology distribution is toward high-frequency operation (2 MHz) and high junction temperature (200°C).

4.2 FUNDAMENTALS OF INVERTERS

Various topologies of inverters are available for application in PV systems. The topologies reviewed in this report were selected out of a pool of the commercially available, breadboard-proven or only conceptually conceived inverter circuits.

Two fundamental types of inverters are being used in utility interactive photovoltaic power conditioners: line-commutated and self-commutated. Line-commutated systems without output filters inject high levels of harmonic currents into a utility system. Line-commutated inverters with comparable performance to self-commutated inverters require output filters that approximate a large percentage of the kVA rating of the power conditioner. The effect of these large filter elements and harmonics on a utility system under large PV penetration is presently unknown.

Utility interactive inverters are divided into three categories: small, intermediate, and large inverters. These inverters are discussed as follows.

Table 1. Comparison of Operating Characteristics for Gate Turn-off Devices

Device Characteristic	Bipolar Transistor	Gate Turn-Off Thyristor	MOSFET	JFET and Static Induction Transistor	Field-Controlled Thyristor (FCT)	GaAs FET
Normally On/Off	Off	Off	Off	On	On	On/Off
Reverse Blocking Capability, V	≈50	500 to 2500	0	0	500 to 2500	0
Breakdown Voltage Range	50 to 500	500 to 2500	50 to 500	50 to 500	500 to 2500	50 to 500
Forward Conduction Current Density,* A/cm^2	40	100	10	10	100	100
Surge-Current-Handling Capability	Poor	Good	Poor	Poor	Good	Poor
Maximum Switching Speed (approximate)	200 kHz	20 kHz	2 MHz	2 MHz	20 kHz	2 MHz
Gate-Drive Power	High (large base-drive current required during on-state and for turn-off)	Medium (large turn-off gate currents required)	Low (only small capacitive charging currents required)	Low	Medium	Low
Operating Temperature, ^oC	150	≈125	200	200	200	200

*The forward current densities are compared here for 500-V devices operating at a forward voltage drop of 1.5 V.

Small Inverters (1 to 15 kW). Small inverters are residential-size units intended to link the photovoltaic source with the utility for the parallel system operation. Rating of the units does not exceed 15 kW. Inversion is single-phase, with ac output of 240 V.

There is a strong trend toward the use of transistors instead of thyristors for power switching; however, some thyristor inverters are still being produced and installed. In addition, the emergence of the GTO thyristor has created new opportunities that are beginning to be exploited. Selected configurations that are reviewed are as follows:

Single-Phase Small Inverters

Inverter Type	Power Semiconductor Usage
Transistor, single-bridge	Transistor
Transistor, dual-bridge	Transistor
Gate turn-off, half-bridge	Gate turn-off thyristor
High-frequency link	Transistor
Line-commutated	Thyristor
dc/dc converter controlled bridge	Transistor

Intermediate Inverters (15 to 1000 kW). Inverters in the intermediate-size range are intended to provide power conversion for photovoltaic systems for various industrial, commercial, and agricultural customers. They will be operating in parallel with the utility. The inverter output power will be delivered at 208 V or 480 V, 3-phase, 60 Hz. Certain applications require a utility interface at 3 kV or above.

The majority of the commercially available inverters use thyristors for power switching. Some advanced configurations, which include GTOs and power transistors, are presently being evaluated for efficiency, reliability, and cost. Selected configurations that are reviewed are as follows:

Three-Phase Intermediate Inverters

Inverter Type	Power Semiconductor Usage
Six-pulse, line-commutated	Thyristor
Twelve-pulse, line-commutated	Thyristor
Transistorized bridge	Transistor
Pulse-width modulated six-pulse	Transistor
Twelve-pulse inverter	Transistor
Gate turn-off, six-pulse	Gate turn-off thyristor
Hybrid	GTOs and thyristor

Large Inverters (Above 1 MW). Large inverters are used to provide the power conversion for photovoltaic systems for small generating stations that will partially supply power to small communities or become part of the dispersed power generation system of the future.

The power inverter consists of one or more high-power bridges of a three-phase variety. Thyristors for high-power applications are paralleled to increase the inverter power handling capability. Paralleling of the individual power conditioner units is used if increased power is required. Selected configurations that are reviewed are as follows:

Three-Phase Large Inverters

Inverter Type	Power Semiconductor Usage
Six-pulse, line-commutated, 1-MW	Thyristors
Twelve-pulse, line-commutated	Thyristors
Twelve-pulse, self-commutated, 500-kW, 750-kW	Thyristors
Eighteen-pulse, self-commutated, 4.8 MW	Thyristors
Chopper-controller, line-commutated, twelve-pulse, 5-MW	GTOs and thyristors

5.0 NEEDED RESEARCH AND OPPORTUNITIES FOR DEVELOPING IMPROVED POWER CONDITIONING SUBSYSTEMS

Power conditioning subsystem technology has advanced rapidly in recent years. As experience has been acquired, various requirements for PCS cost, performance, safety, and utility integration have surfaced. The current understanding of these requirements and their implications for PCS design are detailed in the document. Many of these power conditioner subsystems use microprocessor control and have what may be constituted a "brain." They do not require the usual synchronizing and protective relaying that are essential for conventional cogeneration and dispersed energy systems connected to the utility line. These units were developed to provide this intelligence by internal electronic means to reduce PCS costs because conventional synchronizing and protective relaying would have increased PV system costs excessively. Experience has shown that acceptable integrated operation can be expected with proper PCS design; however, there are still unknowns in the design of a utility interactive power conditioner subsystem.

With the development of advanced circuit topologies, losses and costs associated with filters in line- and self-commutated inverters can be materially reduced. In addition, costs and power losses associated with commutation circuitry in self-commutated systems can be substantially reduced. These cost- and power-loss reductions can provide for power conditioner subsystems of substantially improved cost, efficiency, and performance.

It is apparent that static and dynamic voltage and frequency changes on the utility system can seriously affect PCS design. Audible noise is also a concern because most small photovoltaic power conditioners may be installed inside a residence or in a critical work area. To meet adequate cost and electrical performance requirements, there are serious concerns in meeting various safety codes to guarantee the safety of users as well as PCS maintenance and utility personnel. A detailed description is provided of the current open issues and concerns that remain for the power conditioner subsystem designer to consider.

5.1 STANDARDS, GUIDELINES, AND SPECIFICATIONS

Standards, guidelines, and specifications are needed to inform manufacturers, utilities, and consumers about the specifics of adequate performance, characteristics, and safety concerns related to the design, manufacture, and installation of power conditioning subsystems.

Insolation characteristics over an operational day will vary in different parts of the United States. Power conditioning efficiencies at full or part loads do not necessarily reflect energy efficiency of the power conditioner with specified insolation profile. Thus, the energy efficiency for power conditioners will vary in different parts of the United States.

Different types of arrays such as flat plates, concentrator arrays, and tracking flat-plate arrays will have power output characteristics that will differ from each other even though operating in the same environment. Power conditioning efficiencies, either at full load or part loads, are predicted upon power conditioning design. Thus, one power conditioner may have a high efficiency at full load and only a modest efficiency at one-quarter load. Another power conditioner may be designed for high efficiency at a three-quarter load and a somewhat lower efficiency at full load. The net effect is that power efficiency may in fact not reflect the important significant function of a power conditioner, which is to process the maximum amount of energy available. It is suggested that a figure of merit be determined for each power conditioner that will relate the available insolation characteristics (in a particular region where the PCS will be used) to the PCS energy efficiency. This will allow the system designer and/or the consumer to choose a power conditioner for a specific PV system by proper tradeoff of power conditioning cost and energy efficiency of the power conditioner.

Because of discrepancies in available documents, there is substantial confusion in determining design practice by system designers and power conditioning manufacturers in determining acceptable functional and safety requirements and performance parameters. Acceptable terms of design and integration for one region of the country may be unacceptable in another region. Currently, there are various national and international groups whose objectives include the development of standards, guidelines, and specifications. There are proposed modifications for the 1984 National Electrical Code (NEC) relating to photovoltaic integration that, if approved, will be in Section 690 of the Code. There are also various activities in the Institute of Electrical and Electronic Engineers (IEEE) Photovoltaics Power Conditioning Subcommittee, both in the area of power conditioning recommended practice and power conditioning testing recommended practice. The IEEE Photovoltaic System Subcommittee has promulgated a trial standard for integration of small and intermediate photovoltaic systems into a utility.

There are currently no acceptable standards or requirements for electromagnetic interference (EMI) and radio frequency interference (RFI) for power conditioning subsystems. Current field testing by the National Bureau of Standards reflects that most of the units tested interfered with AM-band radio operation, indicating the need for EMI filters for the PCS. Development of EMI and RFI standards and guidelines would assist power conditioning manufacturers to determine requirements for acceptable operation of power conditioning subsystems.

Currently, there are no definitive design guidelines for power conditioning subsystems. However, some of these activities have had substantial efforts to date.

5.2 OPPORTUNITIES TO REDUCE COST AND INCREASE EFFICIENCY OF POWER CONDITIONERS

Acceptable photovoltaic power conditioning subsystem hardware can be defined as hardware that satisfies the performance and safety needs of a photovoltaic utility interactive installation. There are various concerns relating to the design and development of such power conditioning subsystem hardware that affect safety, performance, and cost. The optimum design configuration of a power conditioning subsystem would reflect low-cost and acceptable performance. Such factors as the dc array voltage, harmonics, power factor, and safety also affect cost and performance; therefore, they also have a direct impact on power conditioning design.

Power Conditioning Subsystems. Transformerless power conditioning subsystems have potential advantages over systems that contain isolation transformers. Transformers add substantially to the cost and size of the power conditioner as well as to a reduction of power conditioning subsystem efficiency. Transformerless systems can also reduce audible noise. The various concerns that must be answered for satisfactory transformerless systems relate to National Electric Codes, effects on distribution component ratings, ground-fault detector operation, dc-current injection, and effects on utility operation.

Development of Cost- and Performance-Effective, Intermediate Power Conditioning Systems. With advanced semiconductor components there is an opportunity to develop new circuit configurations that reduce PCS cost and improve performance. The new circuit configurations will allow for process-intensive designs instead of material-intensive designs (large magnetic and capacitor structures) for medium-size power conditioners.

Development of Cost- and Performance-Effective, Large Power Conditioning Systems. The cost and performance of large power conditioners is limited by the availability of new, advanced semiconductors with improved switching speeds. Thus, with newly developed semiconductors, large power conditioning subsystems that reflect process-intensive designs with low cost and high performance should be possible. Can commutation components be eliminated for self-commutated designs? What is an acceptable array dc voltage for minimum levelized energy cost? What new design opportunities exist for very large PV systems (above 50 MW)?

Impacts of Advanced Semiconductor Devices on Power Conditioner Design. The new, advanced, high-power semiconductor devices that are becoming available are high-voltage, high-current transistors; high-speed, high-voltage, gate turn-off control rectifiers; and induction-type thyristors (high-speed,

high-voltage, high-current devices) will impact PCS design. Several of the major power conditioning research organizations under contract to the Department of Energy have indicated that advanced, megawatt-size power conditioner implementation PCS should be oriented toward the use of gate turn-off devices for next-generation PCS hardware. At present, there are no medium or high-powered inverters using GTOs available in this country in either the UPS, photovoltaics, or other dispersed-storage and generation markets.

Impacts of Advanced Magnetic Materials on Power Conditioner Design. New magnetic materials (amorphous steels, etc.) can be integrated in designs so that they can be manufactured in an economical and practical method to satisfy the needs of photovoltaic power conditioners.

Harmonic Current Effects on PV Filter Components. Research to determine the power spectrum and magnitude of harmonics on existing utility lines would be of significant value to designers of power conditioner filters. This would assist PCS designers to consider the effect of utility-line harmonics on filter component selection and sizing.

Power Conditioner Self-Excitation. If a power conditioner self excites and reapplication of utility voltage occurs out of phase of the self-excited generator voltage, large surges of current will flow. This large, out-of-phase current may damage components of the power conditioner. When there is a utility disconnect, the power conditioner must turn off immediately under all conditions of load and in the presence of other connected generators. In addition, self-excitation may provide unsafe conditions for maintenance personnel. Although this design requirement is understood, the best approach to meeting it has not been determined. Several manufacturers are doing development and testing of residential PCSs to meet this need. Sandia National Laboratories and various utilities are also conducting intensive testing with positive results reported.

5.3 SAFETY ISSUES

It is important that PV systems connected to a utility system should not cause any safety hazard to either the PV source owners or to utility personnel. The safe installation of residential, commercial, and industrial electrical systems is guided by the National Electrical Code (NEC), which is published by the National Fire Protection Association (NFPA) every 3 years. The current code does not address photovoltaics. It is anticipated that revisions to the NEC (1984) will emphasize the unique aspects of photovoltaics and address those concerns that could result in an unsafe installation. Some issues of concern are grounding of PV arrays and the PCS, electrical isolation (through a transformer) of the PV system from the utility system, and disconnection of the PV array from the PCS and the PCS from the utility during times of maintenance. These and other issues directly related to safety must be thoroughly analyzed and included in any revision of the code.

Effect of Array Grounding on Ground Fault Indicators and PCS Logic Circuits and Protective Circuit Operation. Array grounding or equivalent is required by code. Code requirements relate to small and intermediate systems. Large utility systems do not necessarily follow national electrical code with regard to grounding. In large systems, major design concerns are protection of personnel, protection of equipment, and safety of maintenance personnel.

Arrays may be positive or negative-ground or center-tap ground. There is reason to believe that the National Electrical Code, when approved, will allow for equivalency of grounding with approved photovoltaics power conditioners. Currently, large systems use either center-tapped ground or high-resistance, center-tapped ground. Due to the various grounding methods, it is unknown whether available ground-fault detectors, protective circuits, interrupters, and conventionally designed power conditioning logic circuits will operate reliably.

5.4 PCS ARRAY/INTERCONNECTION DESIGN FACTORS

Various factors affect the efficient extraction of energy from the array. Factors other than those that affect energy production (insolation levels, wind, temperature, and array degradation) are:

(1) Inverter ripple.

(2) Power extraction control methods.

(3) The ratio of power conditioner rating to array rating.

Effects of Inverter Ripple on Array Energy Delivery. Excessive array ac ripple due to the inverter can affect array energy extraction by reducing effective array energy output. There have been several curves published that quantify the loss in energy production to ripple level. The validity of these curves should be verified by testing.

Power Extraction Control Methods. Two methods of power extraction have been basically detailed for photovoltaic systems. One method tracks the maximum power point of the array I-V curve. The other method operates the array at fixed voltage.

Whether maximum power tracking is in fact an improvement over fixed-voltage operation will ultimately require empirical data on both cost, PCS sizing, efficiency, and reliability. Additional field engineering evaluation is required to determine the effectivity of the different maximum-power trackers and evaluating the differences of maximum-power tracker operation and fixed-voltage operation.

Power Conditioner to Array Size Ratio. Inverter design and requirements will be affected if it is required to process less than 100% of the energy developed by the array at nominal operating voltage. The ability

to process less than 100% of the array can be economically desirable. Design procedures are needed that will allow power conditioner size to be selected in a manner that minimizes the cost of power production.

5.5 FACTORS RELATING TO UTILITY INTEGRATION

Utility System Voltage Range and Voltage Unbalance Effect on PV Power Conditioner Design and Cost. Excessive voltage unbalance can cause problems with power conditioning operation, component overheating, and nuisance tripping of power conditioning protective devices. Utility system voltage range will affect the power conditioning cost according to the range required by specification.

Better information on actual voltage ranges and the degree of voltage unbalance experienced could be of help in minimizing power losses and the cost of PCS components. Ultimately the cost to the utility for improving its voltage regulation needs to be traded off against the cost of PV system accommodating voltage deviation and unbalance. While ultimately important, this type of research is site specific.

Voltage Regulation and Reactive Compensation. Utilities must maintain the voltage at the customer's terminals with limits specific in tariff schedule offered to the customer.

When PV systems are connected to the utility distribution system, voltage regulation is affected and must be considered:

(1) Improved models will need to be developed for the PV systems, voltage regulators, and the loads.

(2) Line-commutated converters operate at lagging power factors. In other words, they draw reactive volt amperes (VARs) from the system. The utility system must be in a position to supply the additional VARs in addition to the VARs needed to satisfy the load requirements. A self-commutated inverter can be operated at a unity power-factor or possibly even a leading power factor. At this stage, however, it is not clear that a unity power factor converter is the answer because the ratio of volt amperes to watts at the substation would still be rather high.

Further research is required, particularly to determine the effects on voltage at the point of interconnection of the system to the utility.

Stability. Source or system stability is defined as the ability of an individual or multiple PV systems connected to the utility system to maintain operation without large fluctuations in voltage, power, etc.

Any such fluctuations in output parameters could cause nuisance tripping of the PV source following a disturbance. In some cases, it could also cause damage to the PV system. Any undesirable interaction between various PV

systems connected to the same distribution system could cause nuisance tripping at the lateral feeder or substation level, causing unnecessary outages to customers. It could also result in damage to customer equipment connected to the system.

Harmonics. The term "harmonics," as used in this document, is the maximum amount of voltage and/or current harmonics produced by a PV system (at its terminals) when connected to a utility power system. Harmonics (both current and voltage) have many undesirable effects associated with them. Excessive harmonics can cause problems with the utility power system with connected loads and with communication equipment.

The risk that any of the undesirable effects of harmonics will manifest themselves depends largely on the characteristic of the utility and its connected load. Power conditioner designers currently face a great deal of uncertainty concerning the level of harmonics that are tolerable in a given application.

Research is needed to finally establish standards that balance the risk of problems with the cost of limiting harmonics. The research would involve determining the maximum allowable harmonic limits at any point on the system and translation of this number into an allowable harmonic injection (voltage or current) at the terminals of the converter. This limit would depend on the characteristics of the distribution system, background harmonic level from other sources on the system and, most importantly, to the penetration level (both local and system-wide) of PV sources. System simulation and field measurements are a necessary part of this research.

PART TWO

PHOTOVOLTAIC POWER CONDITIONING SUBSYSTEM:

STATE OF THE ART AND DEVELOPMENT OPPORTUNITIES

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SECTION 1

PURPOSE AND APPROACH

1.1 PURPOSE

The purpose of this document is to provide an overview of power conditioning design elements, concerns, and issues for large, intermediate, and small (residential) photovoltaic (PV) systems. Specific objectives include:

(1) Defining important issues and tradeoffs relating to the design and development of power conditioning subsystems for photovoltaic application.

(2) Providing an integrated and generic discussion of photovoltaic systems, state of the art of power conditioning components and design, and the operational interaction between the PV systems and the host utilities.

1.2 APPROACH

The approach to this document is based on the philosophy that the power conditioning subsystem (PCS) cannot be considered by itself but must be considered as one element of an integrated photovoltaic system. The consideration must include the challenging problems of working with a highly variable dc source (variable insolation and variable characteristics of PV cells due to ambient temperature and cell-age dependence), having to meet demanding requirements from the host utility (relating to operational safety, quality of power, and reliability), and providing acceptable performance at reasonable costs.

There are many external requirements being placed on the power conditioning subsystem (such as harmonics and power factor) that may preclude the use of a less complex power conversion method. The electrical characteristics of the array and its output need to be studied to provide insight into optimal energy extraction methods and its impact on PCS sizing, cost, and rating. The PV array interface is unique in its demand on PCS design and must be clearly understood to design power conditioning equipment and to apply power conditioning technology intelligently. The utility interface impacts the PCS design cost and performance. The implication of these impacts must be understood. As the penetration of PV systems into the utility increases and more stringent utility requirements relating to power quality (harmonics), reactive power, etc., may be imposed, the need for understanding the issues involved in power conditioner design and development assume an even greater importance. The current industrial power conditioning experience may not be sufficient to provide power conditioning subsystems that meet stringent cost and projected performance requirements for PV systems but will have to be augmented by the pursuit of new development opportunities.

This document begins with a historical perspective of power conversion technology in an attempt to lay the foundation for subsequent discussions. Advantages and disadvantages of rotary and solid-state power conversion technologies are provided. Generic discussions of large, intermediate, and small PV systems follow. The configuration of the PV system, the characteristics of their elements, as well as their interactions with each other and with the host utility, are discussed. The complex nature of power conditioning designs is demonstrated and assessed by reviewing the requirements of complete PV systems in various operating modes. Fundamentals of inverters are discussed in some detail. Then specific design approaches to power conditioning for both current and advanced topologies are explored.

The aforementioned criteria establish the groundwork for defining the important issues and tradeoffs that are brought about in the development of power conditioning technologies and their applications suitable for PV application. These issues and tradeoffs are explored in depth in this document.

SECTION 2

INTRODUCTION

As the cost of conventional fuels has increased and their availability has decreased, other methods of generating electricity have attracted a great deal of attention, particularly those methods that do not use scarce resources. Solar- and wind-based generations are examples. One of the solar-based generation technologies is photovoltaics, a process that uses solid-state devices to generate electricity from sunlight. Direct current is produced and is subsequently converted to ac power. The power output range of these systems could be from a few kilowatts to greater than 10 megawatts. Photovoltaic power generation has various applications. It may be used in residential, intermediate, and central-station systems and has the potential of economically displacing significant amounts of centrally generated electricity. Because many PV systems will be connected to utility systems, they must be designed so they have the capability of operating safely and economically within the utility system. This requires an understanding of the requirements that the utility will impose on the PV system to design a system to satisfy these requirements. On the other hand, the PV system itself will have characteristics that will affect the utility operation. Thus, the utilities must understand the characteristics of the PV systems so that they can successfully incorporate them into their operation.

As the block diagram of the utility-interconnected PV system indicates (Figure 2-1), there are external requirements that are imposed on the PV system. These may include utility system power management requirements, utility system operation requirements, or requirements from the customer. There are also internal requirements in the PV plant that must be satisfied. The arrays themselves have certain characteristics that must be considered in designing the PV system. If there is any storage in the PV system, the characteristics of the storage method must also be considered. Any loads must be considered that are directly or indirectly fed by the PV system. And, finally, the power conditioning subsystem is an important block which, with appropriate controls, provides dc to ac conversion and system integration.

In smaller PV systems (for example, in residential applications), functions relating to operation and control of the PV system are incorporated within the power conditioning subsystem. However, in larger PV systems (1 megawatt or higher), functions relating to the control and operation of the PV system are usually assigned to the control subsystem. Therefore, in the design and development of a PV system there are many tradeoffs that must be made and many issues to be resolved.

Figure 2-2 is a block diagram of a PV system. The dc output of the PV array is converted into ac power by the power conditioning subsystem and then is fed into the utility system.

There are several factors that affect the design and development of a PV system. Safety is a very important factor. However, the overall governing factor is one of economics. The objective would be to design and build the system to maximize the return on the invested capital within the safety and operational requirements. In this process of optimization, and depending

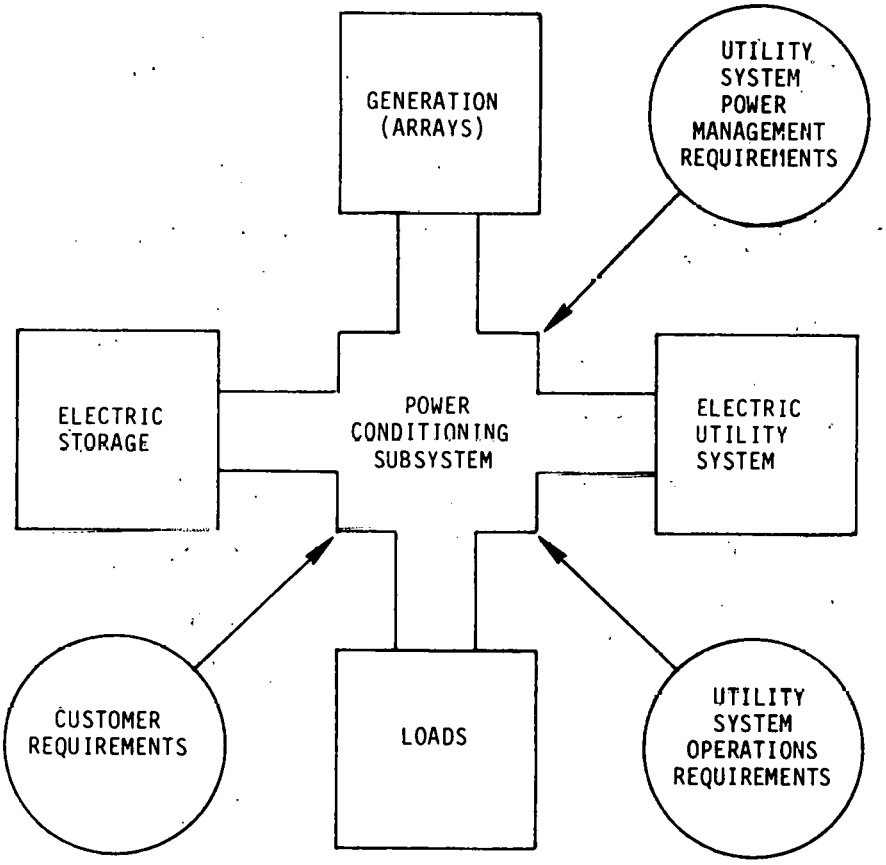

Figure 2-1. Block Diagram of a Utility Interactive Photovoltaic System

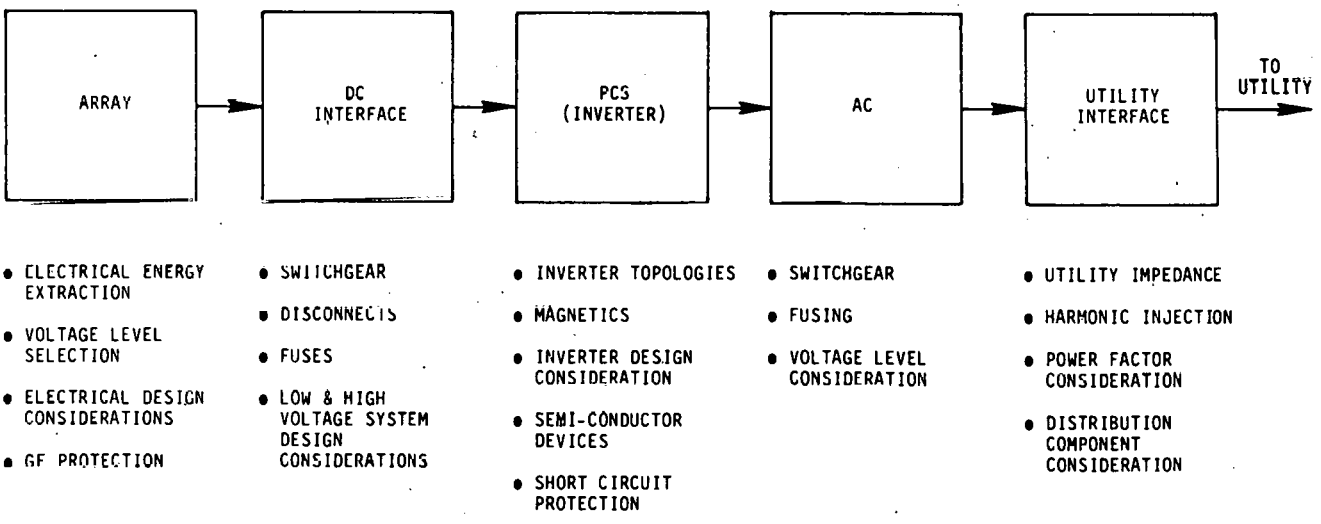

Figure 2-2. Power Conditioning Subsystem Functions and Interface Functions

on the application, one may want to optimize the annual amount of energy produced by the plant, and/or optimize the daily profile of power generated by the plant, which is coincident with the user's load profile (peaking application).

In this process of optimization the power conditioning subsystem is a significant element whose selection, design, and development impacts the economic and technical viability of the PV system. The factors involved in this process of PCS selection, design, and development include the following:

(1) The most efficient method of extracting electrical energy from the array.

(2) The selection of voltage level of the array.

(3) The electrical design of the array.

(4) The protection of the array from damage due to ground faults.

(5) Selection and rating of the switchgear.

(6) Inclusion and type of disconnects.

(7) Inclusion, type, and rating of dc fuses.

(8) The type of inverter.

(9) Selection of magnetics for the inverter.

(10) Inverter circuit (topology) selection.

(11) Selection of the power semiconductor devices.

(12) The protection of the inverter in the event of short circuits.

(13) Selection and rating of ac fusing.

(14) Selection of the voltage level at the ac side of the inverter.

(15) The impedance of the utility at the interconnection.

(16) The harmonic injection and harmonic output requirements.

(17) Power factor and reactive power consumption.

(18) The utility-required distribution components.

(19) PCS electrical performance requirements.

This document concentrates primarily on the solid-state means of conversion of solar energy into alternating current. Additionally, it focuses on utility interconnected PV systems in which energy is fed into the utility

system. Single-phase systems under 15 kW and three-phase intermediate and central station power systems from 15 kW to above 10 MW are addressed, and various power conditioning subsystem circuit topologies are discussed. It is expected that utility-interconnected PV systems will be most widely used in the mature utilization of PV technologies and will probably present the most difficult implementation problems. Other types of PV systems that feed dedicated loads rather than those which are utility-interconnected are not considered in this document. Furthermore, because dc-to-ac conversion is the main thrust of this report, dc-output PV systems are not considered.

This document also outlines research needed to advance the PV power conditioning and control technologies and suggests opportunities for developing higher-efficiency, lower-cost units. Areas covered include those relating to the design of the power conditioner, to the interconnection of the power conditioner to the PV array, and to the electric utility system. Theory of harmonic distortion, reactive power flow, and certain information regarding power conditioning characteristics and manufacturers are provided in the appendices.

SECTION 3

HISTORICAL PERSPECTIVE

3.1 INTRODUCTION

The need to convert electrical power from one form to another dates from the inception of electrical technology. The first electrical generating and distribution systems developed by Thomas Edison were dc. To facilitate transmission over moderate distances, dc motor generator sets were used both to raise and lower voltage levels. These systems, based on the then-current technology of the dc machines, were history's first power conversion systems.

With the turn of the century, a new electrical technology was born: ac power. With this new technology, the process of raising and lowering voltage levels was greatly simplified and improved. Static transformers replaced their rotating machine counterparts with the result of drastically improved economics and efficiency. It might seem that the days of the machine type converter had come to an end, but the opposite was true. Until World War II, dc technology continued to be used by certain utilities, especially in regions of older eastern U.S. cities such as the industrial areas of New York City. Even in the more western cities, dc power remained attractive for electric rail and certain industrial processes. Accordingly, the need to convert dc energy has grown over the years and, until the 1960s, rotating machines were the best option for generated power.

3.2 ROTARY CONVERTERS

Although ac and dc can be bidirectionally converted via a motor-generator set consisting of coupled ac and dc machines, it is possible to integrate the two machines into one, thereby improving cost, size, and efficiency. Specifically, by adding slip rings to a dc machine that connect to appropriate portions of the armature winding, a dc-to-ac converter is effected. Single-phase and polyphase dc-to-ac converters are achieved by selecting the appropriate number of symmetrically spaced slip ring connections. Limited control of voltage, power, and frequency parameters may be achieved by field-current control.

In addition to the dc-to-ac rotating converter, various other converter systems have been developed over the years. Most of this development had been accomplished prior to World War II. For example, two synchronous machines, having different numbers of poles, are integrated into one machine, thus effecting a frequency converter. With such d- ces, bidirectional conversions between frequencies such as 25, 50, 60 and 400 Hz may be achieved.

Semiconductor type static converters have supplemented rotary systems in most, but not all applications. Despite the dramatic achievements over the past two decades in the technology of solid-static conversion, rotary converters are still used in certain new equipment designs. It is expected, however, that by the end of the 1980s, rotary systems will have become extinct in terms of new equipment applications. The reasons for continued use of

rotary systems and for their expected demise is discussed in Section 3.4 where rotary and solid-state systems are compared for various applications.

3.3 SOLID-STATE (STATIC) CONVERTERS

In a broad sense, static power conversion was initiated with the introduction of ac power and the use of step-up and step-down transformers. During the early 1900s saturating reactor magnetic amplifiers were used to control ac power. Thus, without the help of switching elements, inversion and rectification could not be achieved.

During the 1930s and 1940s, vacuum-tube technology expanded into the power field. During this time, multi-kilowatt mercury arc vapor tubes were developed that enabled rectification, inversion, and even switch-mode regulation processes. Thus, some three decades before the birth of solid-state, switch-mode technology, a static-type technology emerged based on vacuum-type devices. This technology was seldom used at the sub-kilowatt level because rotary systems were generally superior both in cost and performance.

In the 1950s, with the development of the power transistor and the silicon controlled rectifier (thyristor) and the discovery of a means of feeding reactive loads without power factor correction, a significant change occurred in the dc-to-ac inversion methodology. The need for high-efficiency and high-reliability inverters for both military and space needs sparked a resurgence in the development of static inversion technology. The technologies used during the 1950s were also used for synthetic textile fiber manufacturing applications. These applications required precise motor speed control (ac synchronous motors) and levels of reliability and accuracy unobtainable with dc motors. The requirements were satisfied by the transistor and SCR developing technologies. This area of effort resulted in the production of thousands of low-and high-power static inverters for motor-drive applications.

In the late 1950s, two developments were commercialized that resulted in the first solid-state, dc-ac inverter. These developments were the power transistor and the thyristor. With the early power transistors, collector voltages were typically limited to less than 60 V. These devices were limited to low-power linear applications such as audio amplifiers. Because of their low switching speeds, inverter applications were limited to 400 Hz and less; 12-V battery to 60-Hz power (usually less than 200 W) was the predominant application.

In contrast to power transistors, the thyristor quickly developed into high-power devices capable of switching hundreds of amperes at over 1000 V; by the end of the 1960s, devices rated at over 1000 A and 1500 V were in production.

Throughout its entire history, the primary application for thyristors has been in phase-controlled systems wherein single-phase and polyphase ac power is "control rectified" to pulsating dc. Although this process has disadvantages because of poor power factor and high levels of current harmonics combined with slow transient response times, the technology has proven both cost-effective and rugged.

The thyristor is an almost exact analogue of the thyratron tube. As such, the circuit techniques developed during the 1940s and 1950s were available for thyristor applications. In particular, polyphase thyristor techniques such as delta-star rectification and various inverter and regulator techniques were borrowed from these previous decades. Unlike the gas tubes of the 1940s, thyristor systems proved cost- and performance-competative with rotary systems for small, sub-kilowatt, as well as for multi-kilowatt applications.

In terms of device economics, ease of drive and ruggedness, the thyristor remains to this day unchallenged. Unfortunately, it has one major drawback: Device turn-off is accomplished only by external interruption of anode current. Accordingly, with virtually all inverter and regulator applications, external commutation circuitry is required. The cost and power loss associated with this external circuitry represents a considerable penalty. As a result, self turn-off devices such as transistors and gate turn-off thyristors are now used in inverter applications.

Following the 1960s and the advent of large-scale computer systems, reliability of 60-Hz power became an industry-wide requirement, particularly for on-line computer systems. Similar static inverter technologies were developed for the uninterruptable power supplies (UPS) applications for backup of critical loads such as computers.

Currently, many of the technologies used in the UPS market are also being used for the purpose of dispersed generation connected to the utility-grid system. The dispersed generation systems include wind, photovoltaics, magneto hydrodynamics, and fuel cells. Table 3-1 provides an historical perspective of PCS technologies with reference to conversion from dc to ac. This historical view shows the time sequence of transition from rotary-type converters to static converters.

Table 3-1. Historical View of Power Conditioning Subsystem Technology

Approximate Range	Technology Developed
1900 - 1920	dc motor/alternator
1920 - 1930	Static converters with thyratron-type valves
1940 - 1950	Military use of dc motor alternator and thyratron valve type power conditioner
1950 - 1960	Transistor and thyristor static inverters for military and space applications in addition to transmission of high-voltage dc
1960 - 1970	Thyristor static inverters for ac motor adjustable speed control
1970 - 1980	Thyristor and transistor static inverters for uninterruptable power supplies
1980 - present	Thyristor and transistor inverters for dispersed generation systems

3.4 ROTARY versus SOLID-STATE CONVERSION

In view of the revolutionary improvements achieved with solid-state switches and circuit topologies, these questions arise: Why are rotary converters still in use? Will rotary technology eventually be forced into obscurity? If so, when?

The answers to these questions are that, in certain applications having particular requirements, rotary converters may be more cost effective. An example of this would be in ac inversion with short-term storage (flywheel). As cost and performance of solid-state systems are reduced, applications of rotary converters will be sharply limited due to cost, maintenance, and performance differences. To gain some perspective on this issue and to help answer the second question, a listing of relative advantages and disadvantages of both rotary and solid-state technologies is provided for the current levels of the two technologies (Table 3-2).

Table 3-2. Comparisons Between Solid-State and Rotary Technologies

Rotary	Solid State
Advantages of Each Technology	
Inherent bidirectional power conversion	Superior to rotary converters in cost, weight, and efficiency for dc-to-ac and 60-Hz ac-to-dc applications
Inherent ruggedness with respect to overloads and transient	Precision voltage and frequency regulation possible at low cost
Inherent sinewave output for dc-to-ac inverters	Flexible control easily achieved (e.g., soft start, disable, synchronization, etc.)
Cost effective for certain applications such as ac-to-ac frequency changers with minimum flywheel storage	Operate in vacuum or harsh atmospheres
	Free of acoustic noise if switching is above 20 kHz
	Maintenance free
Disadvantages of Each Technology	
Not cost effective for ac-to-dc conversion	Transient sensitive unless design precautions taken
Limited control of voltage, current, and frequency	Sinewave outputs require added complexity
Acoustic noise	Bidirectional power flow not inherent
Maintenance required due to brushes, commutators, slip rings, and bearings	
Unity power factor operation requires use of synchronous machines	
Mechanical balancing required	
Low efficiency compared to static conversion	

3.5 THE FUTURE

At the present time, typical PCS costs are in the $500 to $1500/kW range for both residential and intermediate systems. Because these cost levels have a significant impact on the overall economy of PV energy, the question arises as to whether new technologies are on the horizon that can significantly reduce costs.

Within the last two years, ion implantation and hybrid techniques have opened up the realm of power-integrated circuits in which switching devices and control circuitry are integrated into one low-cost, mass produced, integrated package. This technology is only now coming into use for off-line, switcher-type supplies, rated up to 1 kW. Cost projections for a PV PCS with these new devices are in the $200 to $400/kW range.

As applied to the larger intermediate and central-station systems, corresponding new technologies are also on the horizon. Because technologies are now under development, the question is not whether or not significant advances will occur, but rather which technologies will rise above the others. The current production 50-kVA Darlington transistor will likely grow in size while improving in cost and performance. One or more radically new devices such as the Gallium-Arsenide or the Field-Controlled Thyristor may enter the marketplace during the next decade.

The future of residential systems, therefore, seems to lie in the area of integration, while the future of larger systems will be impacted more by new devices. One thing appears certain: rotary systems will probably become extinct during this decade; and conventional, force-commutated thyristor systems will continue to be displaced by systems based on transistors and other self-commutated switching devices.

SECTION 4

SYSTEM CONFIGURATION, REQUIREMENTS, AND OPERATION

The objective of this section is to provide a general introduction to a utility-interactive PV system and its subsystems: what an interconnection problem is; how a PV system differs from other dispersed storage and generation (DSG) systems; what technical requirements may be imposed both by and on the PV system and its subsystems; how the PV system may be required to operate; and what factors must be considered in selecting a suitable power conditioning subsystem. In meeting this objective, subsystems have been considered exclusive of their interaction within the system.

4.1 SYSTEM DESCRIPTION

A block schematic diagram of a utility-interactive photovoltaic system without storage is shown in Figure 4-1. The system consists of a PV array subsystem, power conditioning subsystem (PCS), utility interconnection subsystem, and control subsystem.

These subsystems must function in such a manner that they meet all external and internal requirements imposed on the system, individually or collectively. External requirements include utility system power management, operation, safety, and protection. Internal requirements may be imposed due to the characteristics of the array, PCS, and the storage (if used). In addition, there also is the dynamic interplay between the PV system and the utility system. As a result, PV system characteristics may affect utility operation. Therefore, utilities should be familiar with the PV system

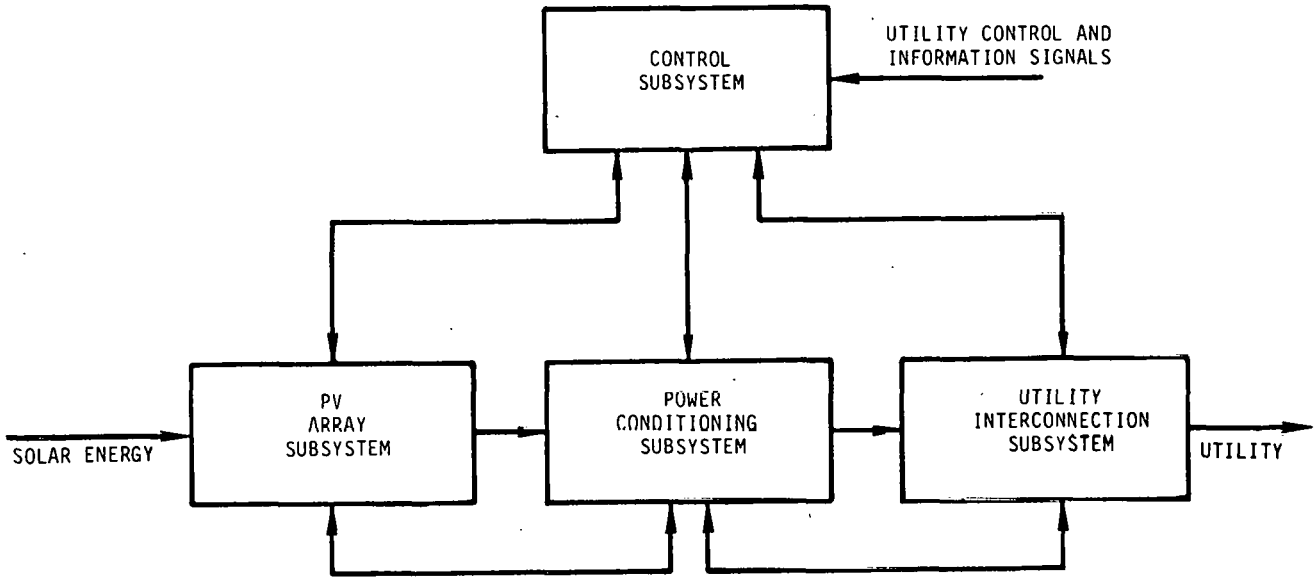

Figure 4-1. Block Diagram of a Utility Interactive Photovoltaic System

characteristics and include such characteristics in their operational procedures. Proper interconnection requires identification of functional constraints imposed by both the utility and the PV system on each other and to meet these constraints in the design of PV subsystems.

It should be added that a utility-interactive PV system may be different from many other dispersed storage and generation (DSG) systems because it must function within input and output conditions that may not be in common with other DSGs. For example, PV systems must respond to highly variable energy input due to variable insolation, temperature, and cell degradation. They must also meet the host utility requirements of safe and reliable operation and produce utility-grade output power economically.

4.2 SUBSYSTEM DESCRIPTION

Figure 2-2 includes some design functions associated with each subsystem. Some of the tradeoffs essential in the PV system design were also listed in Section 2. Any approach to design a PV system will involve tradeoff analysis with respect to each of these design functions. In addition, hardware options and associated limitations and their cost and performance parameters must be considered. With an understanding of PV system design, subsystems are then selected on the basis of minimum cost of unit energy produced. The resultant system should be low-cost, safe, reliable, and provide utility-grade output power. Clearly, in finalizing the system design, some compromise between cost and performance may be desired. Factors such as safety requirements and operational and protective requirements must also be considered in the selection of subsystems so that compatibility exists between subsystems and their interfaces.

4.2.1 Array Subsystem

The PV array subsystem consists of the photovoltaic modules, panels, interconnect cables between modules and between panels, cables between the array and the PCS, any blocking and/or bypass diodes, any field fuses, disconnects, switches, and any equipment used for array ground fault protection. The following functions are performed by the PV array electrical subsystem:

(1) Conversion of sunlight to dc electrical energy at the desired dc operating voltage.

(2) Collection and delivery of dc power to the PCS.

(3) Subsystem protection against damage by lightning strikes, shorts to ground, and over-current and over and under voltage conditions.

To understand relationships that exist between array voltage, current and power, voltage-current characteristics of an array should be considered. Figure 4-2 shows I-V characteristics of an array at a particular set of environmental conditions. The array behaves more or less as a constant current source for low-impedance load and as a constant voltage source for high-impedance load. If the array is to be operated at constant power output, the intersection of hyperbola, VI = constant, and the array I-V characteristics determine the operating point. Point P, where slopes of both characteristic curves are equal, represents the maximum power point. V_{Pmax} and I_{Pmax} are corresponding array voltage and current. V_{OC} and I_{SC} are array open-circuit voltage and short-circuit current, respectively. The short-circuit current is more sensitive to insolation and increases with increasing insolation. Open-circuit voltage, on the other hand, is more sensitive to temperature and decreases with increasing temperature.

As the current drawn from the array is increased from 0 to I_{Pmax}, the array output power also increases until the maximum power point P is reached. Any further attempt to draw current higher than I_{Pmax} will result in a decrease of output power. A typical array P-I curve is shown in Figure 4-3.

Three parameters that help define array performance are: fill factor (FF), normal operating cell temperature (NOCT), and standard operating conditions (SOC). Fill factor is defined as the ratio of maximum power to the product of open-circuit voltage and short-circuit current. The shape or

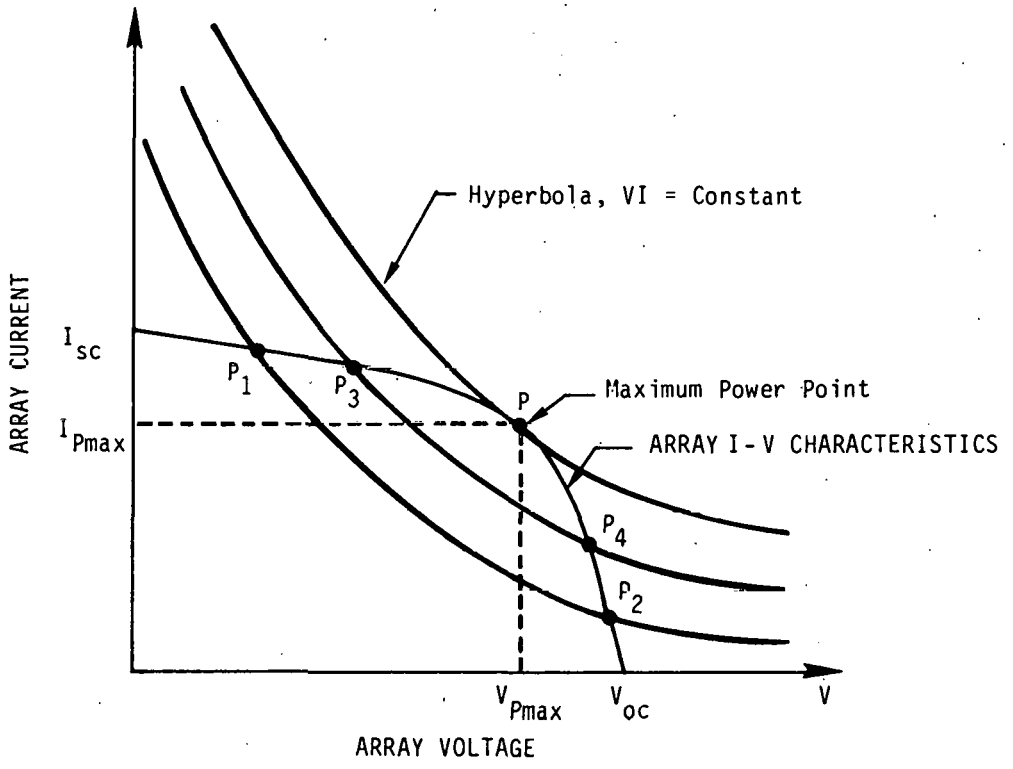

Figure 4-2. Array I-V Characteristics and Constant Power Operation

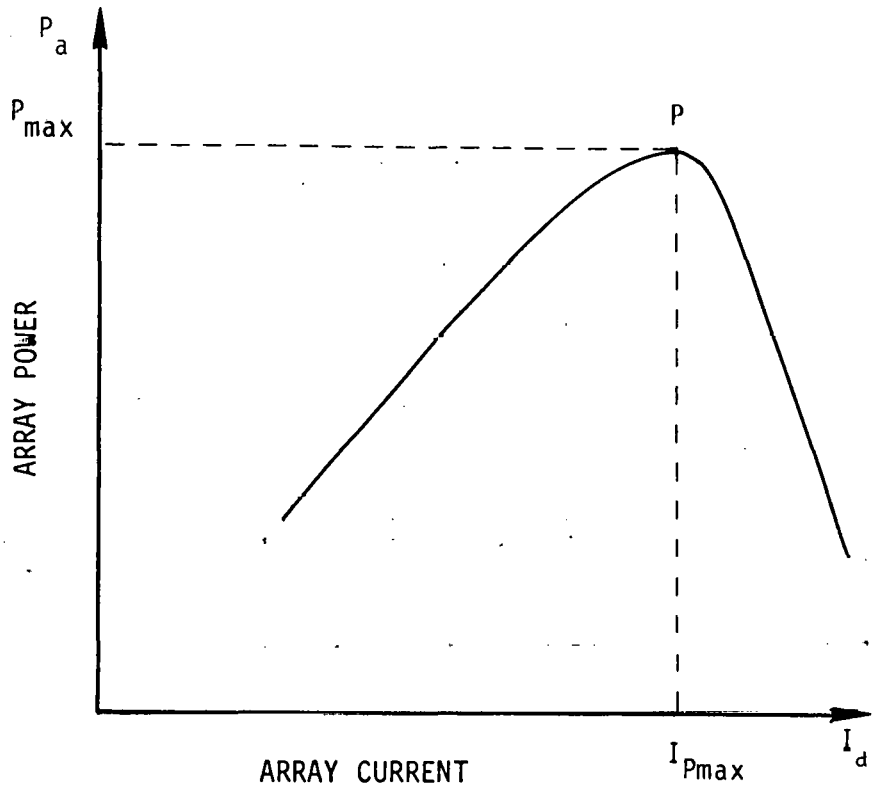

Figure 4-3. Typical Power versus Current Characteristics of a Solar Array

squareness of the I-V curves, which may vary for different manufacturers and for different degrees of degradation with age, is expressed in terms of fill factor. Fill factors have values ranging from 0.60 to 0.76 for new arrays, with an average value of approximately 0.68 to 0.70. The fill factor of an array decreases with age. A lower fill factor signifies reduced output power. The NOCT for an array is defined as the operating temperature of the cells in the intended mounting configuration with incident insolation of 80 mW/cm^2, air temperature of 20°C, wind velocity of 1 m/s, and the array open circuited. The SOC refers to an insolation of 100 mW/cm^2 with array operating at NOCT (Reference 4-1).

The use of these parameters in the analysis of array performance is discussed when different modes of operation of PV systems are considered in in this report. These parameters have significant impact on the system performance and on sizing of an inverter for a given array, sizing of an array for a given inverter, and on operational strategies when both inverter and array sizes are given.

4.2.2 Power Conditioning Subsystem

The term power conditioning subsystem (PCS) is applied to a power inverter that includes the dc-side and ac-side controls and protection. The PCS converts dc-power to ac-power and also does the following: regulates the

amount of power extracted from the PV array at any given insolation and environmental condition, causes the desired voltage and frequency levels to be achieved at the output (ac side) of the PV system, and provides the necessary protection for the components within the PCS as well as protection for certain equipment outside the PCS. It also provides the necessary control action within the PCS. Input and output filters are considered part of the PCS package.

A detailed description of the theory of inverter operation and various inverter circuit topologies is provided in Sections 6 and 7.

Inverters can be line- or self-commutated. Two major types of inverters exist: voltage-fed and current-fed. The voltage-fed inverter is a dual of a current-fed inverter.

In a voltage-fed inverter, the input dc voltage is directly transferred through the inverter in such a way that it appears at the output terminals with alternations of polarity dependent on inverter switching pattern; the output amplitude is equal to the dc input voltage, while its frequency will be determined by the utility 60-Hz, synchronizing signal. The current waveform at the output terminal depends on the inverter switching methodology and the impedance to which the inverter is connected.

Current-fed inverters may be line- or self-commutated. Line-commutated, conventional current-fed inverters draw lagging quadrature current from their ac source. Current-fed inverters operate at a low-lagging power factor, and they are susceptible to commutation faults initiated by utility line faults.

Voltage-fed, self-commutated inverters are capable of delivering both real and reactive power (leading and lagging VARs). Commutation is achieved by components internal to the PCS.

There are no real difficulties in meeting performance requirements for either type of inverter, if properly designed. However, inherent inverter characteristics may impact cost, efficiency, dc and ac voltage range, output harmonic content, and power factor. Array dc voltage levels impact PCS cost and may increase or lower cost, depending on voltage level and PCS rating. The cost impact for harmonic content and power factor improvement is substantial for line-commutated inverters (see Section 6.2.4) due to filtering hardware requirements. Voltage-fed self-commutated inverters can provide low harmonic content and high power factor without major cost impacts (see Sections 6 and 7).

4.2.3 Control Subsystem

The control subsystem oversees the operation of the PV system and performs the following functions: sets PCS operational and protective parameters; provides overall coordination of system protection, if required; may communicate status information to the utility dispatch center; and, if so

desired, provides signals for tracking the PV array. In small PV systems the control subsystem is normally part of the PCS, whereas in large central station systems, the control subsystem may be a separate unit. In the case of larger PV systems it can also receive operational commands from the utility dispatch center. Control of power and power factor is provided generally by the PCS.

4.2.4 Utility Interconnection Subsystem

For small PV systems, utility interconnection subsystem is usually part of the PCS whereas in large PV systems, it is a separate entity. The utility interconnection subsystem may provide the means for the isolation of the PV system from the utility when necessary. It protects the utility system from malfunctions within the PV system. Similarly, it may protect the PV system from abnormal utility conditions. The subsystem may include appropriate meters and instrumentation equipment as specified within the utility interface requirements.

4.3 SUBSYSTEM REQUIREMENTS

Performance of a PV system will depend on individual characteristics of its subsystems. Therefore, in the design or performance evaluation of the system, it is always essential to have complete knowledge of its subsystems. One subsystem may also impose certain constraints on the selection of another subsystem, thereby affecting the cost and performance of the overall system. This subsection examines individual requirements imposed by these subsystems. Knowledge of these requirements will not only assist in the selection of these subsystems but in the design and performance evaluation of the PV systems as well.

4.3.1 Array Subsystem Requirements

Array subsystem requirements will depend on the size of the system and may differ somewhat from system to system. Some of array subsystem requirements are listed below:

(1) Subsystem parasitic ac power and I^2R losses should be small losses due to fans, cable, etc.

(2) The PV array field should be designed for unattended operation.

(3) The ripple current injection of ac signals on the array should be limited due to reduced array energy efficiency.

(4) Grounding for equipment, structure, and frames should be provided.

(5) Surge arrestors between ground mat (if used) and both the hot legs of each polarity of all circuits should be provided.

(6) Ground-fault equipment protection should be provided, if required.

(7) Overcurrent equipment protection should be provided.

(8) Safety disconnect should be provided to allow isolation of source circuit from the ac bus and to interrupt current in the source circuit during maintenance.

(9) Voltage limits for components should be specified and not exceeded.

4.3.2 PCS Requirements

A power conditioning subsystem of a PV system should meet all operational and protective requirements specified by the PV system owner. While these requirements may vary from one system to the other, there is a minimum set of requirements that most power conditioning subsystems should meet. A PV PCS is not a simple power conversion device. It is subjected to many external requirements. As discussed in Subsection 4.8, the design or selection of a PV PCS is possible only when array and utility interface requirements are provided. System cost and performance analysis should be performed for the whole system. Some typical PCS requirements are as follows:

4.3.2.1 Performance Requirements. A PCS should meet all items of its specification, including ac power rating, dc voltage range, ac voltage range, percentage of dc ripple current, power factor, harmonics, frequency, voltage unbalance (if three-phase), and electromagnetic interference.

4.3.2.2 Operational Requirements. Some operational requirements may vary from one PCS to another. However, a minimum set of operational requirements may consist of the following:

(1) Manual Control. Manual control capability should be provided for an intermediate or large PCS as determined by customer requirements. This will include control for startup, shutdown, and power flow through the inverter. Manual controls should be capable of overriding the automatic controls.

(2) Peak Power Tracking. The inverter should have suitable circuitry and logic to sense and determine the array power to ensure that the maximum available solar power is delivered at the PCS output. Such a scheme might be accomplished by maintaining the dc input voltage constant, at the level of the optimum PV array center voltage.

(3) Automatic Startup. Startup should be automatic and possible when a predetermined minimum amount of solar power is available at a prescribed minimum dc voltage, and when the

inverter output voltage matches the utility voltage in amplitude, frequency, and phase. During startup, loading of the array should be increased gradually, until the load requirements are satisfied or the array's maximum power point is reached.

(4) Automatic Shutdown. Shutdown should be automatic and operate under the following conditions: (1) when the array power is low during a cloud cover or at the end of the day, (2) if there is a fault in the PV array subsystem or power conditioning subsystem, (3) when the utility power is lost, and (4) if operation is out of limits. However, PCS shutdown due to low array power should be delayed. In this way, unnecessary shutdown due to rapidly changing cloud cover will be avoided. Automatic shutdown due to a fault in the PV array or PCS should not be delayed and should occur immediately. Also, following the opening of the distribution feeder reclosure, the PCS should automatically disconnect from the line and should not fail if utility voltage reappears.

(5) Restart. An automatic restart should be initiated when the utility recovers within a short interval of time or when cloud cover causes shut down. After long duration outages the PV should be restarted manually.

(6) Reliability. The reliability of a PCS should be as high as possible. Nuisance outages should be prevented. The PCS should be able to withstand or survive transients, originating within the utility or PCS, without failure. Provisions for fail-safe shutdown should be incorporated.

Operational characteristics of the power conditioning subsystem can significantly influence the suitability of a PV system for parallel operation with an electric utility system. For example, on the unit level, the start-up and shut-down procedures, as well as the ability to operate within the limits of the frequency bandwidth and voltage range must be considered. On the system level, where a PV system is one of many dispersed storage generating units (DSGs), the consequences of higher penetration have to be assessed and means found to assure that during utility-line disturbances (reclosure operation) PV systems do not self-excite and cause unsafe conditions.

Initiation of the starting procedure must be contingent upon the availability of the solar and utility power. Connection of a de-energized PCS or a PCS out of phase with the utility line could cause a reverse power flow and lead to possible component damage. Similarly, interconnecting a PV system to the utility line should not be attempted if the utility line is de-energized. An attempt to feed a de-energized line from the PV system could lead to PCS damage as well as create a possible safety hazard. If both the solar power and utility power are available, paralleling may be initiated by automatic means when synchronous operating conditions are met.

4.3.2.3 Protective Requirements. Some of the protective requirements for a PV PCS are:

(1) A dc circuit interrupter or fused disconnect at input terminals to provide overcurrent protection, system separation, and secondary ground-fault protection (as required).

(2) Protective relays, limit switches, temperature switches, and auxiliary interlocks that may be necessary for a particular PCS design.

(3) An ac circuit-interrupter at output terminals to provide overcurrent protection, safety disconnect for the PCS, and system separation.

4.3.3 Control Subsystem Requirements

The control subsystem of a PV system oversees the operation of the PV system and performs functions such as overall coordination of protective devices, communication with the utility dispatch center, and determination of safe operating region. It may provide signals for array tracking, may receive and respond to operational commands from the utility. The control system must be stable and steer the PV system subjected to abnormal or normal disturbance conditions to safe operating conditions. It must protect both PV system and the utility system under all conditions or isolate them safely. Whereas these requirements may also vary from system to system, some of them consist of (1) a digital computer, sensors, a display board, and a data logger; and (2) a plant or system controller implemented within the computer to determine the mode of operation of the system at any instant of time. It may accept analog and digital signals.

Whereas the equipment mentioned above will probably be required for large PV systems, for small PV systems much of the equipment mentioned is not needed. Indeed, the necessary control functions may be carried out within the PCS, and thus one can eliminate the need for a separate control subsystem.

4.3.4 Utility Interconnection Subsystem Requirements

As stated earlier, this subsystem may provide means for PV system isolation from the utility. It also protects the utility system from malfunctions within the PV system and the PV system from malfunctions due to abnormal utility conditions.

Because PCS interfacing with the utility is electronic in nature, usual synchronization means required by conventional generators paralleling with the utility line are not required by PV systems and are accomplished internal to the PCS. In other words, measurements or determination of phase, phase sequence, frequency, and voltage will be accomplished by PCS logic design and no external hardware is required for this purpose.

Utility interconnection subsystem requirements typically may include the following:

(1) An electromagnetic interference (EMI) filter.

(2) ac switchgear.

(3) Protection equipment for separating utility and the PCS in the event of overcurrent/overvoltage, overfrequency and such abnormal conditions.

(4) Metering equipment.

(5) Isolation transformer to prevent dc injection into utility.

(6) Safety disconnect on utility HV side.

Not all equipment mentioned above may be required for all applications. In small PV systems, some of this equipment may be part of the PCS.

4.4 SYSTEM REQUIREMENTS

These requirements refer to overall system performance requirements during normal or steady-state conditions and protective requirements during normal and abnormal conditions. Some of these requirements may vary depending upon the size of the system, requirements imposed by the utility, and preference of the plant owner. However, most systems will be designed to meet some common performance and protective requirements.

4.4.1 System Performance Requirements

4.4.1.1 Voltage Flicker. Voltage flicker conditions from slow change in insolation as a result of haze or clouds may not impair customer service. Of particular concern is voltage flicker due to rapid rate of change in power output during turn-on or turn-off at mid-day, when the insolation is greatest. PV system design should ensure that voltage flicker conditions, due to sudden utility turn-off, an out-of-range situation, or cloud cover changes do not affect other utility users adversely.

4.4.1.2 Voltage Regulation. The term "voltage regulation" refers to proper maintenance of the voltage at the customer's terminals, within an acceptable range with PV generators connected, while also maintaining the flow of reactive power within limits.

In present-day radial distribution systems, the flow of power is in one direction only (from the central power station to the customer). It is relatively simple to control the one-way power flow on a radial distribution system and determine the voltage levels, compensating I^2R losses within the

system. With distributed PV sources on the system, such a task can become complicated because of bidirectional power flow and, in the case of deployment of line-commutated inverters, the possible need for supplementary compensation of the reactive voltage drop.

Voltage regulation should be within the limits specified by ANSI C84.1-1980 (American National Standard Voltage Ratings For Electrical Power Systems and Equipment).

4.4.1.3 dc Injection into the Utility. The PV system should not inject dc into the utility line. High levels of dc injection into the distribution transformer may saturate it, culminating in power outage for all customers served by the transformer. Therefore, electrical isolation or equivalency should be provided between the PV system and the utility system point to prevent dc current from entering the distribution transformer or other user loads (Reference 4-2).

4.4.1.4 Power Factor. The power factor is defined as the ratio of real power to volt-amperes. It is also defined as the cosine of the angle between the terminal voltage and the terminal current. Inductive devices absorb VARs while capacitive devices produce VARs. In other words, power factor is lagging for inductive devices while it is leading for capacitive devices.

The major disadvantages of operating photovoltaic systems at a low power factor are that cost of distribution equipment is more, voltage regulation is worse at the point of interconnection, and for the same power requirement, the conductor size is greater for the same energy loss. PCS costs are increased due to the greater current flow in switchgear and output transformer.

Because PV systems with line-commutated inverters will consume significant amounts of reactive power, the host utility may be required to install power factor correction equipment and charge for low power factor, or have the photovoltaic system add power factor correction capacitors at its output. For a mathematical analysis of reactive power flow see Appendix A. Power factor levels are detailed in various documents (see References 4.3 and 4.4).

4.4.1.5 Harmonics. Utility systems operate at a fundamental frequency of 60 Hz. Harmonics present in the system may adversely affect the system operation and its load as well as contribute to electro-magnetic interference. Some of the undesirable effects of excessive harmonics are summarized below:

(a) Interference with utility ripple and carrier current systems.

(b) Malfunctioning of protective relays.

(c) Overheating in rotating machines and transformers. Harmonics influence motor torque for synchronous and induction motors.

(d) Interference with voice communication (telephone interference).

(e) Overvoltages due to resonance.

(f) Overheating of capacitor banks due to lower impedance to higher order harmonics.

Line-commutated inverters inject current harmonics into the utility. Voltage-fed, self-commutated inverters, on the other hand, would normally inject voltage harmonics into the utility. However, because a tie inductance is used to tie the inverter to the utility and because the utility impedance is very low, the harmonics injected into the utility by the PCS are current harmonics. In both cases, the level of harmonics imposed on the system is a function of system impedance at the point of interconnection as well as the characteristics of the inverter itself.

Specified limits of total harmonic distortion (THD) for power conditioning equipment should safeguard a trouble-free operation of PV systems. Should the newly connected PV generator, however, interfere with other utility customers, the utility may request the generating customer to install additional filtering to bring the harmonic output of the PV generator to an acceptable level or to disconnect.

The Photovoltaics System Subcommittee of the Institute of Electrical and Electronics Engineers (IEEE) has prepared a trial standard for photovoltaic systems (Reference 4-2). Permissible level of harmonic current is recommended at 5% for current THD and 2% for voltage THD. For the theory of harmonic distortion see Appendix B. Percentage is calculated with respect to fundamental frequency components.

4.4.1.6 Voltage Unbalance. System voltage unbalance is defined as the unbalance generated in utility system voltages and currents due to unequal loading of system phases. Excessive unbalance can cause problems with utility system operation, component overheating, nuisance tripping of protective devices, propagation of multiples of third harmonics and excessive negative sequence voltage, which could cause motor overheating. The main concern in this study is to address the impact on power conditioner subsystem design. Voltage unbalance will require the reduction of PV-PCS nameplate rating. The degree of derating is a function of the magnitude of the unbalance and the value of the PCS-utility line tie reactance.

A simple method of expressing the phase voltage unbalance is to measure the voltage in each of the three phases (Reference 4-5) and express

$$\text{Phase voltage unbalance} = \frac{\text{Maximum deviation from average phase voltage}}{\text{Average phase voltage}}$$

Another method of expressing voltage unbalance is in terms of voltage unbalance factor, which is equal to the negative sequence voltage divided by the positive sequence voltage.

A PCS operating under unbalanced voltage conditions on the utility has both the positive sequence currents and negative sequence currents. It can be shown from symmetrical components analysis that if the utility voltages are unbalanced and the inverter is required to operate in a balanced condition, then the inverter kW rating should be higher than in the case when there is no utility voltage unbalance. Therefore, due consideration should be given to the effects of voltage unbalance in terms of cost and performance before a PV system design is finalized. A summary of the impact of voltage unbalance on the PCS size is shown in Table 4-1, where x represents reactance between the converter and the utility system, in per-unit on the converter's kW base (Reference 4-6). It is apparent from the Table 4-1 that for the same value of x, the inverter required rating is higher for greater voltage unbalance. For example, for 100 kW output power and tie-line reactance of 0.5 per unit, the kVA rating of the PCS required will be 111.8 kVA without any voltage unbalance whereas it will be 145 kVA for 10% voltage unbalance.

4.4.2 System Protection Requirements

The protective devices are installed to perform numerous functions such as isolating permanent faults, minimizing fault location and clearing times, preventing equipment damage and minimizing the probability of disruptive failure and safety hazards to public and operating personnel.

There is a substantial amount of knowledge available on electronic protection of power conditioning subsystems. Protection against the utility-generated transients need additional attention. Some guidelines on protection requirements for dispersed generators have been already formulated by various utilities (Reference 4-7). These guidelines are in many cases governed by the geographical considerations and are not necessarily applicable elsewhere. Selection of the protective elements should be based on thorough overall system analysis of the operating environment in the actual utility-interactive mode.

The PV system and the utility systems should be protected against abnormal operating conditions such as under/overvoltage, overcurrent, over or under frequency. Some of these abnormal conditions may originate either in the PV system or the utility system. If the utility bus is de-energized, the PV system should be isolated and should remain isolated until conditions permit resynchronization. Protection systems should be mutually time-coordinated to disconnect the PV system from the utility under these abnormal conditions. Protection requirements may be as follows:

(1) Overvoltage Protection. Overvoltage conditions may be created by various mechanisms such as repetitive, intermittent, short circuits, switching surges, resonance effects in series, inductive/capacitance circuits as well as lightning. In addition, malfunction of the PCS may cause

Table 4-1. Voltage Unbalance Effect on Inverter Rating (Reference 4-6)

Per Unit Reactance, x	Balanced System Inverter Rating, kVA per unit	Increased Inverter Rating, kVA per unit (needed for) 3%	5%	7%	10%	Unbalance
0.05	1.001	1.698	2.165	2.633	3.338	
0.1	1.005	1.358	1.596	1.835	2.196	
0.15	1.011	1.252	1.414	1.578	1.826	
0.2	1.020	1.205	1.330	1.458	1.651	
0.25	1.031	1.184	1.288	1.394	1.555	
0.3	1.044	1.176	1.267	1.359	1.500	
0.35	1.059	1.178	1.258	1.341	1.468	
0.4	1.077	1.185	1.259	1.335	1.452	
0.45	1.097	1.197	1.266	1.337	1.447	
0.5	1.118	1.213	1.278	1.346	1.450	
0.55	1.141	1.232	1.294	1.359	1.459	
0.6	1.166	1.253	1.314	1.376	1.473	
0.65	1.193	1.277	1.336	1.396	1.491	
0.7	1.221	1.303	1.360	1.420	1.513	
0.75	1.250	1.331	1.387	1.445	1.537	
0.8	1.281	1.360	1.415	1.473	1.563	
0.85	1.312	1.391	1.445	1.502	1.592	
0.9	1.345	1.423	1.477	1.533	1.622	
0.95	1.379	1.456	1.509	1.565	1.654	
1.00	1.414	1.490	1.543	1.599	1.687	

overvoltages. Overvoltage protection within the power conditioning subsystem will include protection against transient overvoltages originating in the utility system or the PV system itself. If these voltage surges are allowed to pass through directly without suppression, they could damage the components of the power conditioning subsystems. The PV system should be isolated during sustained overvoltage conditions.

(2) Overcurrent Protection. PCS overcurrent sensing will detect and eliminate overcurrent conditions caused by faults on the system. The PV system protection devices should be properly coordinated with the utility protective devices. Inadequate overcurrent protection could result in damage to the power conditioning subsystem and distribution transformer. In addition, inadequate overcurrent protection may also cause temporary utility faults to become permanent, resulting in prolonged interruption of normal utility operation. System should be isolated on overcurrent conditions.

(3) Over/Under Frequency Protection. During conditions of mismatch between utility generation and load, the system frequency will fluctuate. If the load exceeds generation, frequency will drop. On the other hand, if the generation exceeds the load, the frequency will exceed its nominal value of 60 Hz. If this mismatch is severe, the frequency fluctuation may exceed a preset range.

Over/under frequency protection should isolate the PV system from the utility if the utility frequency falls outside the range preset by the interacting utility. A typical range of frequency is specified in Reference 4-3.

(4) Undervoltage Protection. Utility undervoltages may be caused by excessive loading, reclosure opening, large inrush loads or high resistance faults. Under these sustained conditions, the PCS undervoltage protective circuitry should disconnect the photovoltaic system. Utility voltage limits are prescribed by ANSI Standard C81.1-1980.

(5) Protection against Current/Voltage Unbalance. Voltage unbalance occurs due to unequal voltages of utility phases. An excessive unbalance may result in overheating of PV and utility system components and in nuisance tripping of protective devices. Protection against excessive current/voltage unbalance should be provided.

(6) Ground Fault. For PV systems, separate ground-fault protection may or may not be necessary depending upon its size and the interacting utility. While the NEC does not require ground-fault detectors, many intermediate and most large PV systems use them primarily to protect maintenance personnel and equipment.

(7) Grounding. Photovoltaic system grounding is required by the NEC. As part of this protection, it is customary to connect one side of the array bus to electrical ground in a two-wire system or the neutral in a three-wire system, and to utilize surge protectors from both dc leads to an outside earth ground.

Grounding of large systems varies according to the system designers. An ARCO Solar 1-MW installation at Hesperia, California, uses a solid array center-tapped ground. Sacramento Municipal Utility District (SMUD) intends to use a high-impedance center-tapped ground for their projected 1-MW installation. This will provide for equipment protection that has the capability of switching in a higher impedance to protect personnel entering the array field.

(8) Surge Protection. The PCS must be protected at its dc and ac interfaces against over-voltages caused by induced lightning (except direct strikes) or switching transients. The PCS should be capable of withstanding a transient voltage pulse of 6 kV crest value across its ac terminal required by IEEE Standard 587-1980. Protection at the dc interface will be provided in the PV array subsystem. The PCS manufacturer should provide secondary protection for the PCS as required by inverter design, dc interface elements, and requirements imposed by applicable codes, standards, and guidelines.

In summary, it is important that the PV systems connected to a utility should operate reliably and not cause any safety hazards to either the PV source owners, other customers, or to utility personnel. Each PV system must satisfy the existing national, regional, and local codes and utility requirements before it can be integrated into any utility system. Layout, wiring, and grounding of the system facility should conform to the existing guidelines, and, in 1984, the National Fire Protection Association (NFPA)-sponsored, revised National Electric Code. Protection of the PV system must be ensured to minimize damage and risk of injury and to assure the highest possible reliability of service.

4.4.3 System Stability

Stability of a PV system connected to a utility refers to its ability to maintain operation without excessive fluctuations in voltage, power, etc., as a result of disturbances, within or outside the PV system. Nuisance tripping of the PV source should be avoided.

It is highly important that all control loops operate in a stable mode under the wide fluctuations in operating conditions that can be expected in a utility-interactive operation. These fluctuations could either be array specific, such as changes in available insolation and array temperature, or utility specific, such as resonances caused by changes in the VAR compensation capacitance.

The transfer functions of elements of the control loops will affect the stability of the PV system. If a PV system is found to be unstable or marginally stable under certain operating conditions, it may be necessary to modify the control system to achieve a stable operation. It is advisable to evaluate the stability margins during acceptance testing of each PV system.

Initial studies based on modeling of many utility-interactive systems indicate that stable operation can be expected at modest levels of penetration (Reference 4-8).

Stability analysis of a PV system depends on the PCS design parameters. The general problem of dynamic simulation of dispersed grid-connected PV power systems has been studied (Reference 4-8). Single-phase and three-phase, line-commutated, and self-commutated inverters have been examined. These inverters were simulated and steady-state and transient behaviors of the PCS and the whole PV system were studied under various disturbance conditions. Primary control systems internal to inverter circuits, secondary control systems external to primary controls, and maximum power tracking control systems have been studied. Given an inverter, the study shows how to select proposed control system parameters. There is no shortcut method to predict local or global stability of a given PV system. A general approach to examine stability is to analyze transfer functions or state equations for the whole system.

A study was performed for the purpose of verifying small perturbation characteristics of the PV system and to investigate the PV system response following large changes in system variables (Reference 4-8). A static converter representation was used in conjunction with established dynamic representations of other PV system components. Figure 4-4 shows a simplified PV system block diagram. A phase locked loop was used that maintains the phase difference, ϕ, between the ac bus voltage and the synthesized inverter voltage, at a specified reference, ϕ_{ref}. The phase reference, ϕ_{ref}, is determined by a voltage regulator which adjusts the phase setting so as to maintain the array voltage at a specified set point value, V_{ref}. The converter dc current, I_{dc}, is established in terms of dc power, P_{dc}, and array voltage, V_{PVA}. The array voltage is related to the converter dc current and the PV array current, I_{PVA}, by the equation

$$V_{PVA}(s) = \frac{1}{sC} (I_{PVA} - I_{dc})$$

where

s = Laplace operator

C = capacitance connected in parallel with the array

The stability was studied with the help of transfer functions of various blocks and plots of responses due to several disturbances. Similar studies for a given PV system with known subsystem control characteristics will help to determine the stability of that system.

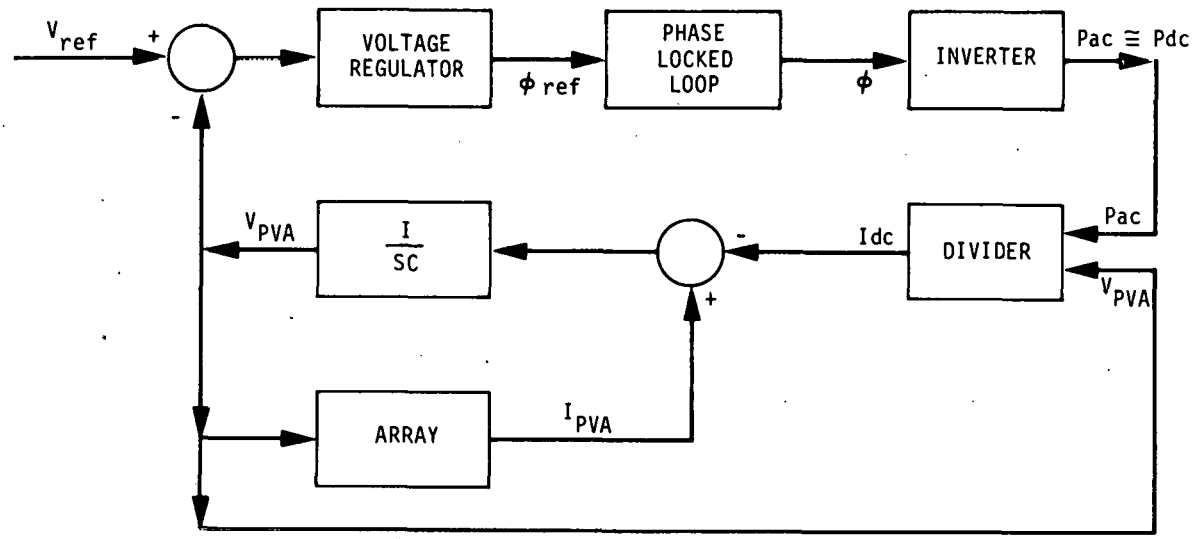

Figure 4-4. A Simplified PV System Block Diagram (Reference 4-8)

4.5 SYSTEM OPERATION

There are three possible conditions of PV system operation: current limited operation, constant voltage operation, and maximum power operating. Independent of the operational mode, the primary objective always is to be able to extract maximum energy from the array. Therefore, an understanding of the array characteristics for a specific site are essential in designing an efficient PV system. In this section, PV system operation will be examined. Although these discussions will refer to flat-plate arrays only, tracking arrays exhibit similar electrical behavior in a particular mode of operation.

Because the PCS consists of solid-state components that are limited by current ratings, the PV array may be operated in a current limited mode. As a result, a fluctuation in array output power will cause PCS input voltage to fluctuate. If the dc voltage is within specified limits, current limited operation will continue; otherwise, the PCS will be shut off. If the array output voltage exceeds the limit due to excessive generated power, current limited operation can be maintained by dissipating the extra power. While this approach does compromise system efficiency, it keeps the size of PCS small.

Most systems use maximum power method for optimal energy extraction. Some systems use constant voltage method for energy extraction. Current limited operation may be used in conjunction with either mode of operation to protect PCS components.

4.5.1 Constant Voltage Operation

In any scheme ensuring constant voltage operation, the dc array voltage is compared with a reference value and the difference is kept to a minimum. When array voltage rises, the PCS output is phase shifted with respect to the utility voltage. As a result, array dc current is increased, and array voltage is decreased. In general, however, fixed-voltage operation does not guarantee maximum power output, particularly under severe conditions of array degradation. Adjusting reference voltage may improve efficiency, but it requires adjustment seasonally (Reference 4-1).

Consider, as an example, a plot of normalized energy output versus normalized power conditioner voltage for Albuquerque, New Mexico (Figure 4-5). The ordinate represents the fraction of available energy drawn from the array during the indicated periods of the year (spring, fall, summer, winter and full year) by a constant voltage system. The ratio of the PCS operating voltage to the array maximum-power voltage (V_{mp}) at SOC is represented along the abscissa. It is evident that the optimum voltage without seasonal adjustment is approximately 96% of the array V_{mp} at SOC, and that this fixed-voltage system will lose about 2% of the available energy. If, however, seasonal adjustment is used, the voltage would vary from about 92% of V_{mp} in the summer to 103% of V_{mp} in the winter and the energy loss will be reduced to about 1%. Table 4-2 summarizes similar numbers for 26 sites (Reference 4-1).

4.5.2 Maximum Power Operation

In this mode of operation a closed-loop feedback control system is used, array output power or PCS output power is sensed, and operation at maximum power is achieved by continuously shifting the operating point on the array characteristics. There are many schemes of maximum power tracking. A peak or maximum power tracker allows a PV array to be loaded over the full range of operating conditions so that the maximum electrical output power is extracted from the array.

One such scheme of maximum power tracking is the perturb-and-observe scheme (Reference 4-9). In this scheme, the operating point of the array/inverter combination is shifted slightly by a change in the inverter controls. The power before and after the change is compared. If the power is found to have increased, then the previous operating point was not the point of maximum power. A further change in the same direction is made. If the power is found to have decreased, the direction of the perturbation is changed, and the process repeated. When the temperature and insolation are constant, this maximum power tracker will operate in a limit cycle around the point of maximum power. Figure 4-6 shows a flow diagram of a perturb-and-observe method. Both analog and digital versions operating on this principle have been built.

If it is assumed that the insolation does not change as a function of time and that, if at a given instant the reference voltage is V_A (Figure 4-7) corresponding to the peak power point, then an increment in voltage at a given

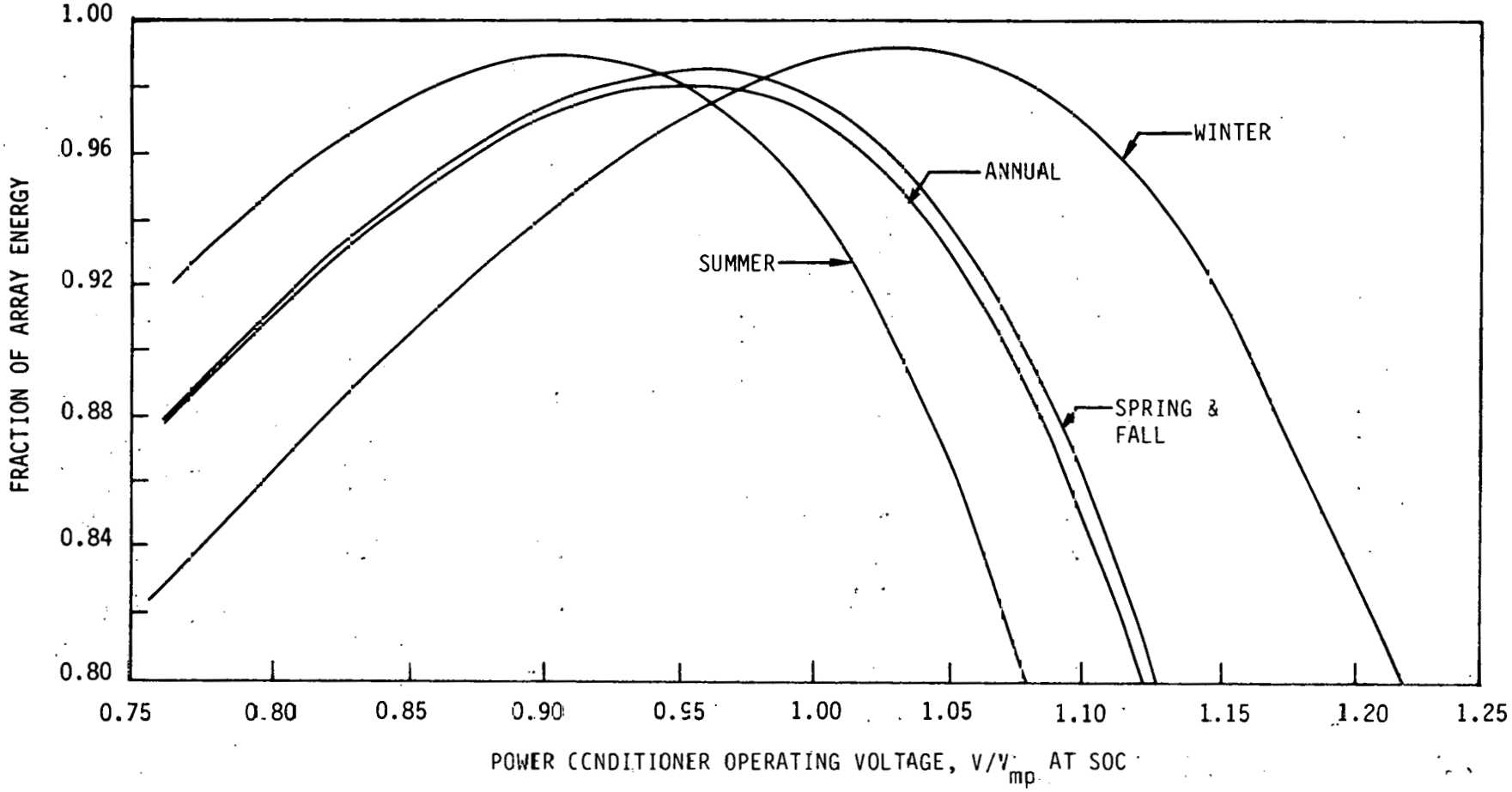

Figure 4-5. Variation of Array Energy Output versus Power Conditioner Operating Voltage at Standard Operating Conditions for Albuquerque, New Mexico (Reference 4-1)

Table 4-2. Simulation Results for Fixed-Voltage Power Conditioner (Reference 4-1)

Site	Fixed-Voltage Power Conditioner Optimum Operating Voltage (V_{op}/V_{mp} at SOC)				% Loss in Energy with Fixed Voltage Power Conditioner no seasonal adjustment	% Loss in Energy with Fixed Voltage Power Conditioner with seasonal adjustment
	Annual	Spring/Fall	Summer	Winter		
Albuquerque NM	0.96	0.96	0.92	1.03	1.7	1.0
Apalachicola FL	0.94	0.94	0.91	0.97	1.1	0.9
Bismarck ND	0.97	0.98	0.94	1.07	2.5	1.9
Boston MA	0.97	0.98	0.94	1.03	2.0	1.7
Brownsville TX	0.92	0.92	0.91	0.95	0.8	0.7
Cape Hatteras NC	0.95	0.96	0.93	0.99	1.3	1.1
Caribou ME	1.00	1.01	0.96	1.06	2.2	1.8
Charleston SC	0.95	0.95	0.93	0.98	1.1	0.9
Columbia MO	0.96	0.96	0.92	1.02	2.0	1.5
Dodge City KS	0.95	0.96	0.92	1.03	1.9	1.4
El Paso TX	0.94	0.94	0.91	1.00	1.3	0.9
Ely NV	0.98	0.98	0.95	1.05	1.7	1.2
Fort Worth TX	0.93	0.94	0.91	0.98	1.5	1.2
Fresno CA	0.94	0.94	0.91	1.00	1.3	1.0
Great Falls MT	0.97	0.98	0.94	1.04	2.0	1.6
Lake Charles LA	0.93	0.93	0.92	0.97	1.1	1.0
Madison WI	0.97	0.98	0.94	1.05	2.3	1.8
Medford OR	0.96	0.96	0.94	1.00	1.4	1.3
Miami FL	0.93	0.93	0.92	0.94	0.7	0.6
Nashville TN	0.95	0.95	0.93	1.00	1.6	1.4
New York NY	0.97	0.98	0.95	1.02	1.7	1.5
Omaha NB	0.96	0.97	0.93	1.04	2.1	1.6
Phoenix AZ	0.92	0.92	0.89	0.97	1.4	1.0
Santa Maria CA	0.97	0.97	0.96	0.98	0.7	0.7
Seattle WA	0.97	0.97	0.96	0.97	1.4	1.3
Sterling VA (Washington D.C.)	0.96	0.96	0.94	1.02	1.7	1.3

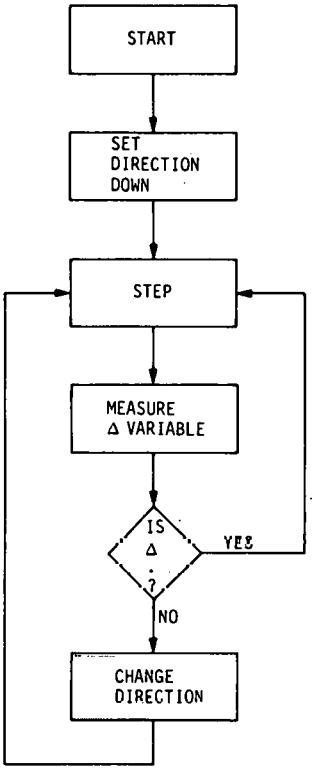

Figure 4-6. Flow Diagram of a Perturb-and-Observe Method (Reference 4-9)

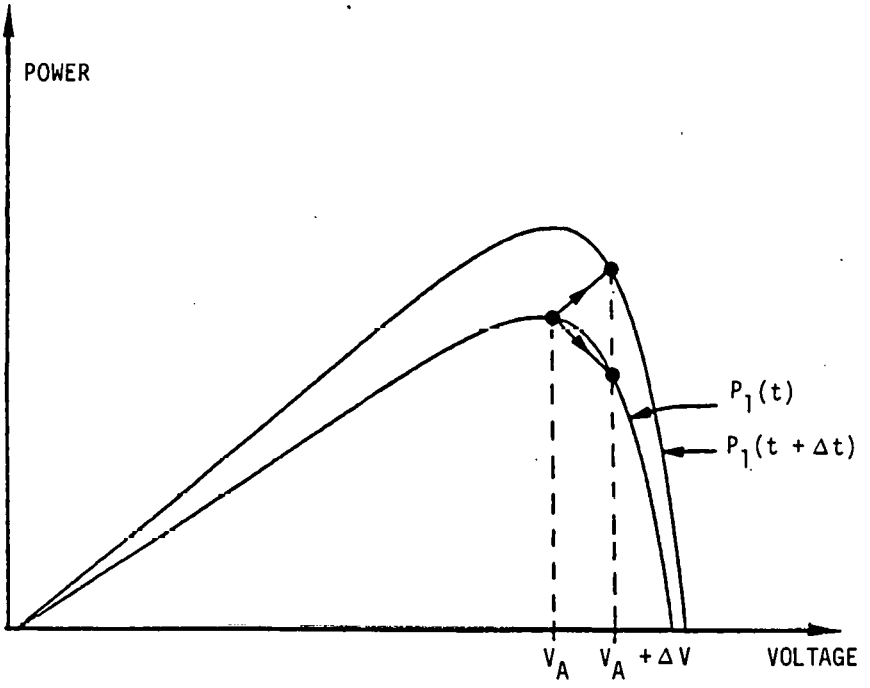

Figure 4-7. Array Power versus Voltage Characteristics at Two Insolation Levels in a Perturb-and-Observe Peak Power Tracker (PPT) (Reference 4-8)

timing cycle will give rise to a decrease in array power. As a consequence, the power tracker will make the subsequent perturbation in the opposite direction or toward the peak power point. However, if the insolation increases by a substantial amount during the given timing cycle, then the array power will increase. By sensing an increase in array power, the power tracker will make the subsequent perturbation in the same direction or away from the peak power point. As long as the insolation continues to increase at a substantial rate, the power tracker will continue to move from maximum power until one of the following conditions occur: (1) the array voltage becomes substantially larger or smaller than the value at peak power wherein the array power becomes less sensitive to insolation variations and more sensitive to array voltage or (2) the inverter upper or lower voltage limits are exceeded wherein the normal peak power tracking algorithm is overridden. When either of these conditions occur, the direction of movement changes. In view of these operational aspects, an apparent approach toward the reduction of these large variations in V_{ref}, is to increase the sampling frequency associated with the power tracker. The change in array power during a given timing cycle, therefore, becomes less sensitive to insolation variations and more sensitive to V_{ref} (see Reference 4-8).

A second type of maximum power tracker is discussed next (Reference 4-10). Figure 4-8 shows its circuit. The inverter is operated at unity power factor. As a result, it appears as a resistor to the array. The maximum power tracker makes small changes in its equivalent resistance and observes the effect on power. Because the ac line current is in phase with the utility voltage, the maximum current delivered by the inverter corresponds to the maximum output power. The tracker is in constant search of this condition.

The command current, I_L^*, is used as a signal proportional to power. When insolation increases, both array current, I_A, and I_L^* increase and the change in I_L^* is sensed by the sgn (d/dt) switch block. The array power is recomputed. I_A is increased further if the power is still increasing. This process continues until power begins to decrease. The search for maximum power point continues as long as the array voltage, V_A, is within limits. If the voltage V_A cannot be limited, the inverter is shut down. When insolation decreases, a new (lower) maximum power point is reached by similar process. When I_L^* increases corresponding to an increase in output power, the signal output to the integrator will have the same polarity, which will cause the integrator to slew in the same direction. As a result, I_A^* changes and a different value of equivalent resistance is commanded. When I_L^* decreases corresponding to a decrease in output power, the integrator slews in the other direction. Under certain fault conditions the system is shut down and disconnected.

A third version of a peak power tracker is shown in Figure 4-9 (Reference 4-11). This scheme measures array power ripple. When the array power ripple is zero, the maximum power point is reached. The voltage at which the peak power point lies is determined by using a small amount of 120 Hz ripple present on the array to trace out a small portion of its I-V characteristic. Because the I-V curve is being measured at a relatively high rate (120 Hz), conditions of rapidly changing insolation will not be misleading to the tracker. At the 120-Hz frequency of the ripple voltage, the

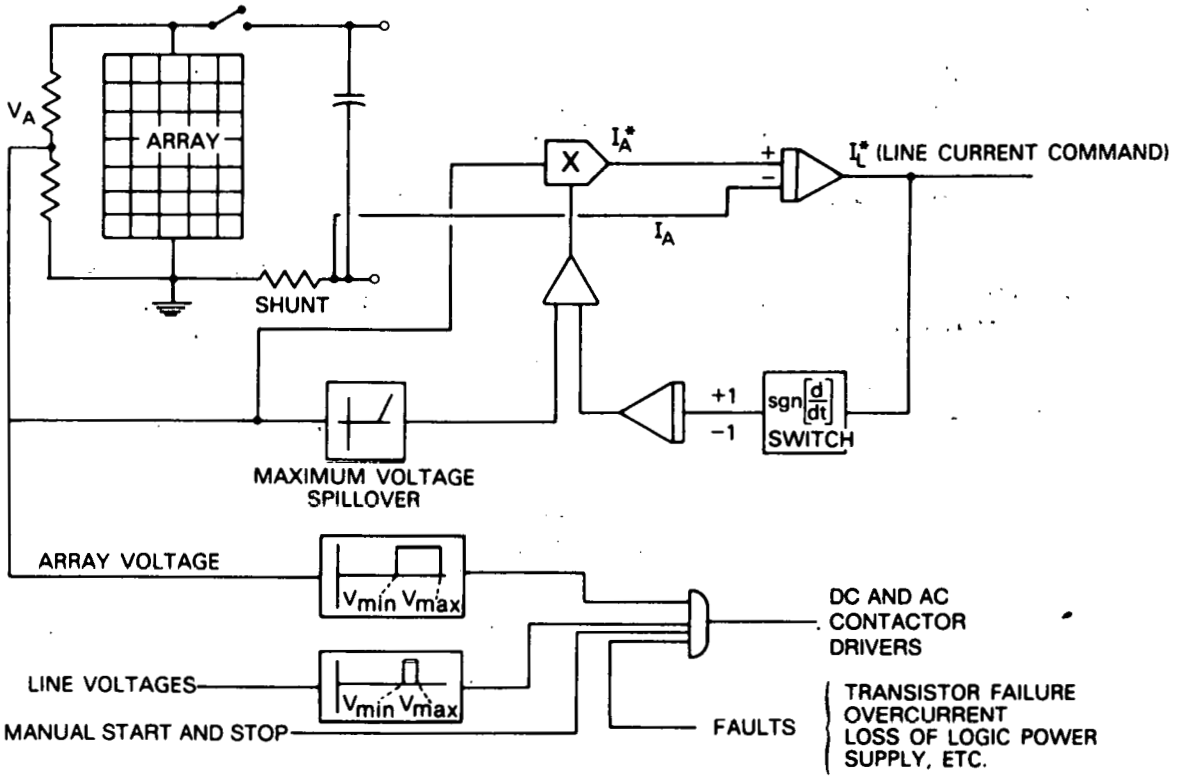

Figure 4-8. Maximum Power Tracker and Contactor Control

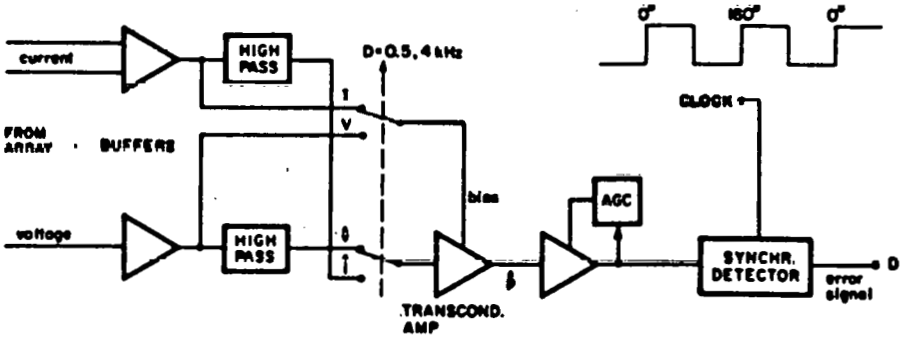

Figure 4-9. Block Diagram of the Peak Power Tracker (Reference 4-11)

array impedance is large relative to the large capacitor across the dc input of the inverter. Therefore, ac component $\hat{v}$ of the array voltage can be expressed as

$$\hat{v} = \frac{I}{2\omega C} \sin 2\omega t$$

where

I = constant array current

C = input filter capacitance

ω = radian frequency

If V, I and P are array voltage, current and power, respectively, then $P = VI$. Also, if $\hat{v}$, $\hat{i}$ and $\hat{p}$ are small perturbations around V, I and P, then $\hat{p} = (P + \hat{p}) - P = (V + \hat{v})(I + \hat{i}) - VI \cong I\hat{v} + V\hat{i}$. If peak power point is reached, then $\hat{p} = 0$, which implies $I\hat{v} + V\hat{i} = 0$.

Near the peak power point, the small-signal array resistance is

$$r = \frac{V^2}{P} = -\frac{\hat{v}}{\hat{i}}$$

Therefore,

$$\hat{i} = -\frac{\hat{v}}{r} = \frac{-IP \sin 2\omega t}{2\omega CV^2}$$

or

$$\hat{i} = \frac{-P^2}{2\omega CV^3} \sin 2\omega t$$

which can be rewritten as

$$V\hat{i} = \frac{-P^2}{2\omega CV^2} \sin 2\omega t = \frac{-I^2}{2\omega C} \sin 2\omega t$$

$$= -I \cdot \frac{I}{2\omega C} \sin 2\omega t = -I\hat{v}$$

That is,

$$V\hat{i} + I\hat{v} = \hat{p} = 0$$

$\hat{v}$ is positive in intervals (0° - 90°) and (180° - 270°) and negative in intervals (90° - 180°) and (270° - 360°). The peak power tracker loop uses $[P(\hat{v}+) - P(\hat{v}-)]$ signal as an error signal to control the loaded array voltage. This signal is integrated and sent to the input voltage control circuit. The tracker is in constant search of achieving the condition of $\hat{p} = 0$, which takes place when power is maximum. If power ripple is in phase with $\hat{v}$, power is less than the maximum power. If power ripple is 180° out of phase, the power is above the peak power point. When there is no 120-Hz power ripple, the maximum power point is reached. The process to reach the maximum point power is achieved by changing input voltage to the inverter.

4.6 GENERAL DESIGN PRACTICES

Before designing a PV system or selecting its subsystems, it is helpful to keep the following facts in mind.

(1) High overall efficiency and low energy production cost. In designing a PV subsystem, the circuit designer should attempt to use components that will result in low busbar energy cost. Reliable, well-proven and commercially available components should be used.

(2) High reliability and availability. The system should be designed for reliable and unattended operation. Factors such as redundancy to increase reliability and derating of components should be carefully examined in finalizing a design.

(3) Good accessibility. The system should be designed for easy access to all components for testing and servicing.

(4) Proper cooling. Provisions for adequate cooling including convection or forced air should be made for all components, especially solid-state devices.

(5) Good performance evaluation means. Instrumentation to evaluate system performance should be incorporated in the system design, if required.

(6) Long system life. The system design should be such that it assures a given productive life of the system. It may be 10 to 15 years for residential applications, 20 to 30 years for intermediate and commercial applications, and 30 years for central station plants.

(7) Low degradation effects. Degrading optical surface resulting in array degradation to collect all the solar energy will deteriorate system performance. Similarly, component malfunction or failure will degrade PCS performance and, accordingly, the PV system performance. Maintenance and operating procedures should be included in designing a system.

(8) Safety and protection means. Sufficient protection ensuring equipment and personnel safety should be built into the design. All requirements of National Electric Code should be identified and complied with. Electrical equipment should be "approved for the intended use" by a nationally-recognized testing laboratory, such as Underwriters Laboratories, Inc.

4.7 SYSTEM CONFIGURATIONS

There are two cases in which a PV system may have to be configured: (1) to design or select a PCS and other subsystems for a given array

and (2) to select an array and other subsystems for a given PCS. Selection and sizing of subsystems in both situations will be based on minimum cost of unit energy. That is, an optimal design in each case will ensure minimum cost of unit energy produced and will meet all applicable operational, performance, protective, and interface requirements.

Whereas steps involved in the selection and sizing of subsystems for the two situations will differ because of differences due to knowns and unknowns, both configurations will have to conform to some common set of requirements, such as utility interface requirements. As an example, the next section discusses design steps for the first case in which an array is given and a PCS is to be selected and sized.

4.8 SELECTION AND SIZING OF PCS

In the selection and sizing of a PCS for a given PV array, the primary objective is to be able to capture maximum solar energy at the least possible cost. That is, the levelized energy cost or the bus bar energy cost associated with the selected PCS and the given array must be minimum. If the PCS is oversized, the energy output of the array may increase, but the PCS may cost more; as a result, the cost of unit energy may increase. Conversely, if the PCS is undersized, it will cost less but the energy output may also be less. Therefore, selection of a PCS in terms of voltage, current, and power ratings must be based on the cost per unit of energy output. Clearly, the sensitivity of these ratings to the energy cost must be examined. If the incremental cost of output energy increases as a result of increasing PCS size to capture a small percentage of additional energy, increased PCS size is not recommended.

Given an array, there are some operational issues involved in the selection or design of a PCS. These are:

(1) If the array output power is greater than the PCS rated power and if the excess energy is to be rejected, how much energy will be lost?

(2) How can the maximum limits on array voltage, current, and power be prescribed?

(3) What protective means must be built into the unit so that PCS maximum limits are not exceeded?

Apparently, all these considerations are interrelated and center around the cost of operation beyond limits versus energy lost or down-time. Whether the PCS should be operated at constant voltage or at maximum power is also a significant consideration in the selection or design of a PCS.

4.8.1 PCS Circuit Design Issues

This section addresses factors such as power, voltage, and current ratings; energy conversion performance factor; voltage, current, and power limits; operation at constant voltage or at maximum power; and a general approach in the selection of a PCS for a given array and other set of constraints.

4.8.1.1 PCS Power Rating. Presently, power conditioner subsystems can be selected only in discrete sizes. Tables C-1 and C-2 of Appendix C list power sizes for inverters presently available for small and intermediate size PV systems. They come in discrete sizes and have different full-load and part-load efficiencies. As a result of this limited availability of inverters in discrete sizes, the procedure to determine power rating of a suitable PCS will be to consider an inverter of one size and determine corresponding cost of unit energy output. Similarly, consider various other sizes available and determine cost of unit energy output for each size. The power rating of the selected PCS will correspond to the minimum cost of unit energy output.

Another factor to keep in mind while sizing a PCS is the variable nature of solar insolation. Figure 4-10 shows a typical variation of array power versus operating time, for Albuquerque, New Mexico (Reference 4-1). It is clear from the figure that higher output power is available for smaller number of hours. The area under the curve during a given operating time represents available energy during that time. As a result, if the PCS is sized corresponding to P = 1 instead of P = 1.2, energy output given by area above the line P = 1 is lost. But this energy is only a small percentage of total available energy whereas cost saving due to nearly 20% reduction in PCS power power size may be significant. As shown in Figure 4-11, some energy is lost due to PCS inefficiencies. Similar curves for a given location may be used in determining the size of a PCS that will operate at that location.

4.8.1.2 Output Voltage Rating. Selection of output voltage rating of a PCS will be dictated by the application. However, presently available power conditioners have only specified voltage ratings. As a result, there may be two ways to match the utility voltage with the PCS output (ac) voltage: (1) Select a PCS with output voltage rating equal to the utility voltage; and (2) Select a PCS with output voltage rating not equal to the required load voltage and use a transformer to match the load voltage. For small and intermediate size PV systems, power conditioning subsystems presently available have discrete power and dc and ac voltage ratings. For large PV systems, 750 kW is the maximum single unit commercially available. Units requiring larger PCS will either use paralleled units or a PCS designed for the application. In any case, the energy cost associated with the selection will be a dominant factor. Tables C-1 and C-2 in the Appendix C show dc and ac voltage ratings of available power conditioning subsystems. If an output transformer is used, its efficiency and cost must be included in the cost analysis. For small PV systems, the output voltage is normally 240 VAC single-phase; and for intermediate size PV systems the output voltage is usually 208 V, three-phase, with 480 V for larger intermediate systems. Large central station system output voltage will generally be dependent on the supplying utility.

4.8.1.3 Current Rating. Once power and voltage ratings are determined, current ratings can be specified for the PCS selected.

4.8.1.4 Energy Conversion Performance Factor. The energy conversion performance factor (ECPF) is a measure of the ability of the PCS to convert available array energy into usable ac output (PCS efficiency changes with the level of power processed). If is defined in terms of array

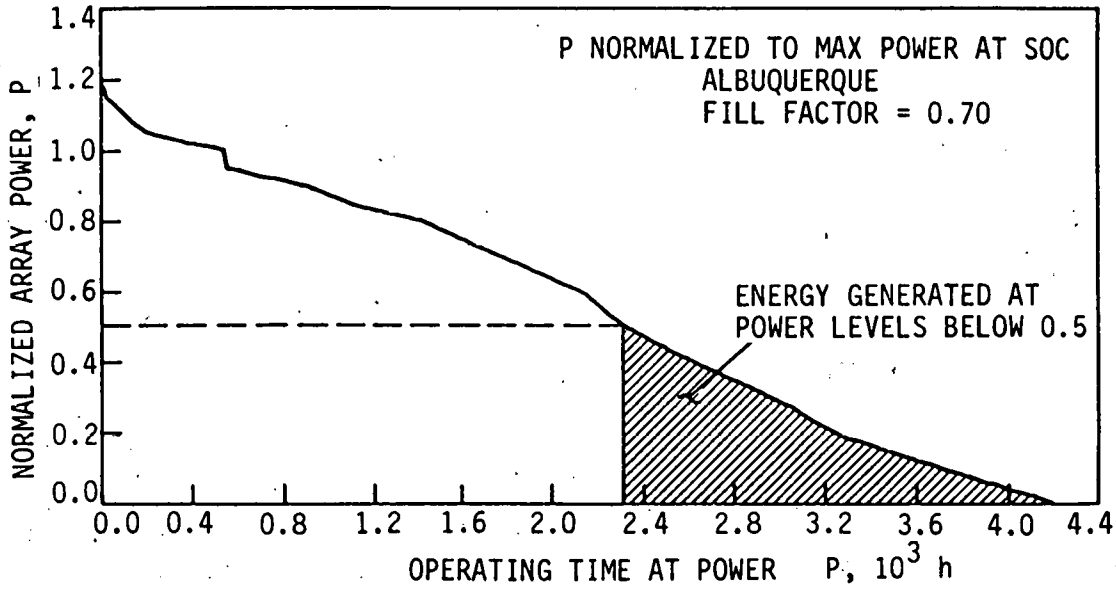

Figure 4-10. Normalized Array Power versus Operating Time (see Reference 4-1)

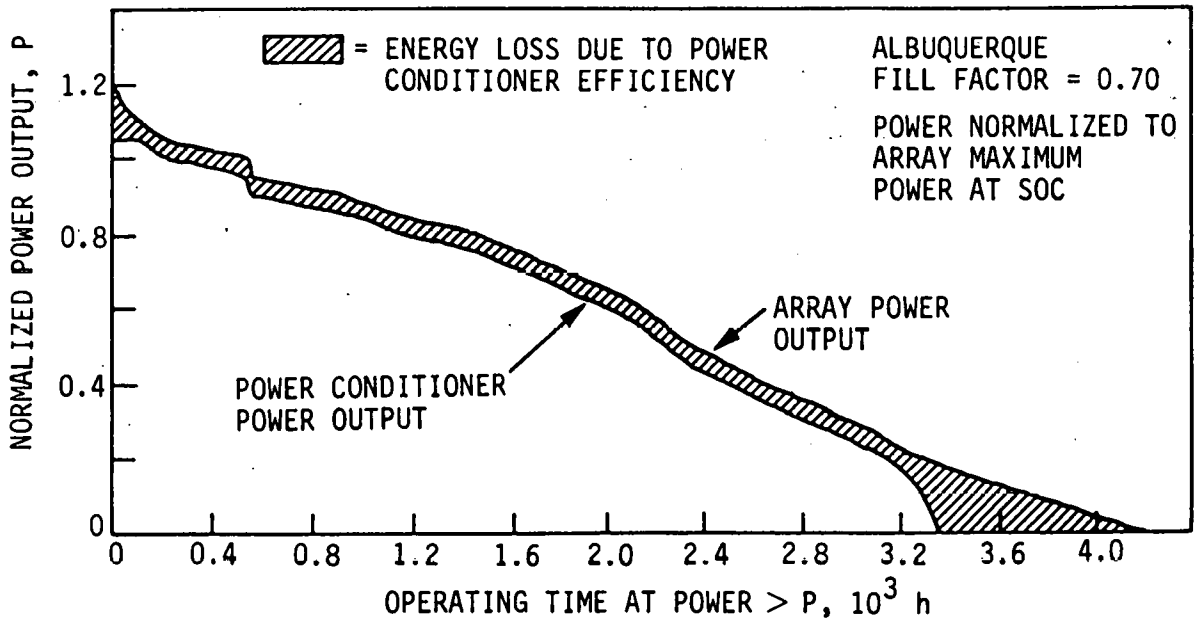

Figure 4-11. A Typical Variation of Array Power Over Operating Time (Reference 4-1)

energy utilization capability, weighted average conversion efficiency, and miscellaneous losses. When a maximum power tracker is used, ECPF for a PCS is given by the equation (Reference 4-12):

$$ECPF = K_1 \sum Ki.Ci.\eta i - K_2 R_{SB} - 0.5\ K_3\ R_{TL}$$

where

i = partitioning of input energy into power ranges from 0 to 100 percent (for example, 0 to 25, 25 to 50, 50 to 75, 75 to 100).

ηi = PCS conversion efficiency for input power range i.

Ki = measured max-power tracking accuracy (if max-power track provided) and dc ripple effect at average power level in range i.

Ci = fraction of array energy delivered within range 1.

K_1 = PCS array energy utilization capability, based on max-power tracking window (K_1 = 1 for a PCS with full-range max-power tracking capability).

$$K_2 = \frac{\text{standby hours}}{\text{operating hours x average array output/rated array output}}$$

R_{SB} = Standby losses/PCS rating

$$K_3 = \frac{\text{insolation hours - operation hours}}{\text{operating hours x average array output/rated array output}}$$

R_{TL} = No-load losses/PCS rating

The terms Ki, ηi, R_{SB} and R_{TL} are functions of the PCS performance. Whereas factors i, Ci, ηi, R_{SB}, R_{TL} and Ki are measured in a test laboratory, factors K_1, K_2, and K_3 are provided based on manufacturer array characteristics, installation, and location.

A simplified formula for ECPF that is suitable for practical applications is given by the equation:

$$ECPF = K_1(0.05\ \eta_{1/8} + 0.15\ \eta_{3/8} + 0.25\ \eta_{5/8} + 0.55\ \eta_{7/8}) - K_2\ R_{SB} - 0.5\ K_3\ R_{TL}$$

where $\eta_{1/8}$, $\eta_{3/8}$, $\eta_{5/8}$ and $\eta_{7/8}$ are measured PCS efficiency at 1/8, 3/8, 5/8 and 7/8 rated loads. This formula does not include the effects of geographical location and resulting variation in the distribution of the yearly array output. A location correction factor can be added for a specific application (Reference 4-12). This formula is applicable for fixed flat plate array operation.

4.8.2 PCS Operational Design Issues

This subsection discusses issues and procedures involved in operating a PCS at constant voltage or maximum power.

4.8.2.1 PCS Operation at Constant Voltage. Like any other device, a PCS would operate smoothly if its input voltage (dc) is reasonably constant during PV system operation. However, due to array temperature fluctuations during the day or a season and due to array degradation, PCS input voltage will not always be constant. Therefore, for constant voltage operation, seasonal or infrequent adjustments must be made on dc input voltages of the PCS. Because there is always a limit on current, the voltage may be allowed to rise slightly. However, during periods of high insolation, the current may tend to exceed its limiting value, at which time the PCS will be disconnected, and the system may be turned off. If array voltage is allowed to rise to higher values, operation may continue.

The amount of allowed voltage excursion or the decision to disconnect the PCS at certain voltage or current limits will affect energy cost. Therefore, in selecting a PCS, dc array operational voltage range should be examined.

4.8.2.2 PCS Operation at Maximum Power. As discussed earlier, to operate a PCS at constant input voltage, reference voltage is adjusted periodically. To achieve maximum energy output from the PV system, the PCS should operate at maximum power point. To do that, a peak power tracker is used. The tracker allows the array to be loaded over the full range of operating conditions so that the maximum electrical output power is extracted from the array. The key consideration in the tradeoff between the constant voltage operation and the maximum power operation is the difference in output energy cost. Therefore, factors affecting the energy conversion performance factor should be considered and the cost of unit output energy be evaluated for each option to reach a decision of whether the PCS should operate at maximum power or constant voltage. A PCS oversized to handle large array power levels occurring for only a few hours in a year is not desirable. This is because the cost for such a PCS is higher and efficiency is generally lower. Therefore, the cost of unit-energy associated with the oversized PCS may be higher even if the PCS operated at maximum power point.

4.8.2.3 PCS Voltage Limits. Any time the PCS is not loaded, the array open-circuit voltage will rise. Therefore, allowable dc input voltage limits for the PCS must be examined in selecting a PCS. If the array open-circuit voltage is high and the PCS is left connected to the array, it will have to withstand this high voltage. Similarly, if the PCS is loaded and the insolation increased substantially, PCS input voltage may also substantially increase. In either case, voltage limits must be prescribed beyond which the PCS will be disconnected. Needless to say, if the loaded PCS has to be disconnected due to high voltage, it may affect the energy cost. The following empirical equation gives a relationship between the maximum open circuit voltage and the voltage at maximum power at SOC (Reference 4-1).

$$\frac{\text{Maximum Voc}}{\text{V maxm. power at SOC}} = 0.475\ (2 - FF)(1 - \alpha T_L)(2 + \frac{NOCT}{100})$$

where

FF = fill factor

TL = coldest ambient temperature, °C

NOCT = nominal operating cell temperature, °C

α = fractional change in the open-circuit voltage at 25°C for degree of change in temperature, $0.003 < \alpha < 0.004$

Table 4.3 shows estimated maximum open-circuit voltages at NOCT for various sites in the United States (Reference 4-1).

4.8.2.4 PCS Power and Current Limits. Power and current that a PCS may be subjected to in abnormal conditions may be substantially higher than the corresponding PCS ratings. To address the question of prescribing limits on power and current while selecting a PCS, there are three strategies that can be pursued:

(1) PCS is shut down and reset manually. Operating limits under this strategy can be set near the maximum values that are foreseeable.

(2) Entire power is rejected, and the PCS input power is zero. When the operation returns to acceptable levels, automatic recovery takes place.

(3) Only enough power is rejected to bring the operation within limits.

Table 4-3. Estimated Maximum Open-Circuit Voltage for 26 Sites (NOCT = 50°C)

Site	Maximum Open-Circuit Voltage V_{maxp} at SOC	
	Lower Bound	Upper Bound
Albuquerque	1.49	1.69
Apalachicola	1.43	1.62
Bismarck	1.57	1.79
Boston	1.52	1.69
Brownville	1.43	1.57
Cape Hatteras	1.46	1.63
Caribou	1.57	1.79
Charleston	1.46	1.64
Columbia	1.55	1.74
Dodge City	1.52	1.71
El Paso	1.46	1.65
Ely	1.55	1.76
Fort Worth	1.46	1.66
Fresno	1.44	1.61
Great Falls	1.57	1.77
Lake Charles	1.46	1.64
Madison	1.57	1.79
Medford	1.49	1.66
Miami	1.40	1.56
Nashville	1.53	1.67
New York	1.50	1.69
Omaha	1.58	1.75
Phoenix	1.43	1.61
Santa Maria	1.40	1.61
Seattle	1.49	1.64
Sterling	1.52	1.71

Depending upon the decision to reject energy totally or partially when limits are exceeded, power and current limits can be calculated for a given percentage of available annual energy at a given site. Table 4-4 shows power and current limits for 99% and 99.9% of the available annual energy for various sites in the United States (Reference 4-1).

Table 4-4. Effect of Partial and Total Rejection Strategies on Power and Current Limits versus Fraction of Available Energy Obtained (Reference 4-1)

Site	PC Power Limit: Array Power at SOC to Gain 99% of Energy Obtained With No Limit		PC Power Limit: Array Power at SOC to Gain 99.9% of Energy Obtained With No Limit		PC Current Limit: Array I_{maxp} at SOC to Gain 99% of Energy Obtained With No Limit		PC Current Limit: Array I_{maxp} at SOC to Gain 99.9% of Energy Obtained With No Limit		Voltage Excursion from Center for 99.9% Limit, %
	Partial	Total	Partial	Total	Partial	Total	Partial	Total	
Albuquerque	1.04	1.15	1.13	1.19	1.06	1.19	1.17	1.20	11.5
Apalachicola	0.86	1.02	0.99	1.06	0.91	1.03	1.01	1.06	5.3
Bismarck	0.96	1.11	1.08	1.15	0.95	1.07	1.05	1.10	15.5
Boston	0.89	1.06	1.02	1.11	0.89	1.04	1.01	1.09	13.4
Brownsville	0.85	1.02	0.97	1.05	0.92	1.04	1.03	1.05	6.5
Cape Hatteras	0.89	1.06	1.03	1.10	0.92	1.06	1.03	1.09	14.7
Caribou	0.98	1.15	1.14	1.24	0.94	1.09	1.08	1.10	15.0
Charleston	0.87	1.03	1.00	1.09	0.90	1.04	1.01	1.08	9.5
Columbia	0.95	1.12	1.09	1.15	0.95	1.08	1.06	1.10	15.6
Dodge City	1.00	1.14	1.12	1.20	1.01	1.17	1.12	1.20	10.5
El Paso	1.01	1.12	1.10	1.15	1.03	1.17	1.15	1.20	9.6
Ely	1.05	1.17	1.15	1.23	1.05	1.19	1.16	1.20	9.2
Fort Worth	0.91	1.06	1.04	1.10	0.94	1.05	1.04	1.10	15.1
Fresno	0.92	1.04	1.03	1.07	0.98	1.05	1.04	1.05	10.6
Great Falls	0.94	1.09	1.07	1.16	0.96	1.06	1.05	1.10	15.5
Lake Charles	0.84	0.93	0.92	1.06	0.86	0.95	0.94	0.96	17.2
Madison	0.98	1.18	1.15	1.32	0.95	1.10	1.09	1.19	15.5
Medford	0.90	1.07	1.05	1.10	0.94	1.07	1.05	1.10	8.3
Miami	0.82	0.92	0.91	1.03	0.86	1.02	0.97	1.05	9.7
Nashville	0.89	1.06	1.03	1.11	0.91	1.06	1.03	1.09	14.7
New York	0.88	1.07	1.03	1.13	0.88	1.00	0.99	1.09	15.5
Omaha	0.97	1.12	1.10	1.21	0.95	1.09	1.08	1.26	12.5
Phoenix	0.93	1.06	1.05	1.10	1.00	1.06	1.05	1.16	9.8
Santa Maria	0.91	1.04	1.03	1.06	0.93	1.04	1.03	1.06	6.2
Seattle	0.86	0.94	0.93	1.05	0.88	0.95	0.95	0.96	12.4
Sterling	0.89	1.07	1.03	1.10	0.90	1.05	1.01	1.09	14.6

4.8.3 General Procedure for Selection of a PCS

Given an array, the selection of a PCS for a small and intermediate size utility-interactive PV system involves the following steps:

Step 1: Develop a data base consisting of:

(a) Weather data for the site.

(b) Available PCS cost and performance data.

(c) Utility operational requirements, if any.

(d) Utility interface requirements. (Use Subsection 4-4 and Appendix C.)

Step 2: Select shutdown, partial or total rejection strategies for overlimit conditions (use Subsection 4.8.2).

Step 3: Select constant voltage or maximum power operation strategy (use Subsections 4.5 and 4.8.2).

Step 4: Determine power, voltage, and current ratings for the PCS (use Subsection 4.8.1).

Step 5: Determine power, voltage, and current limits for PCS operating conditions (use Subsection 4.8.2).

Step 6: Perform life-cycle cost (LCC) analysis subject to one set of variables in Steps 1 through 5.

Step 7: Repeat Steps 1 through 6 with other sets of variables until LCC is minimum.

Step 8: Select PCS corresponding to minimum LCC. PCS parameters and operating strategies in Steps 1 through 5 will correspond to minimum LCC.

Figure 4-12 shows a flow chart illustrating the above procedure for selecting a PCS.

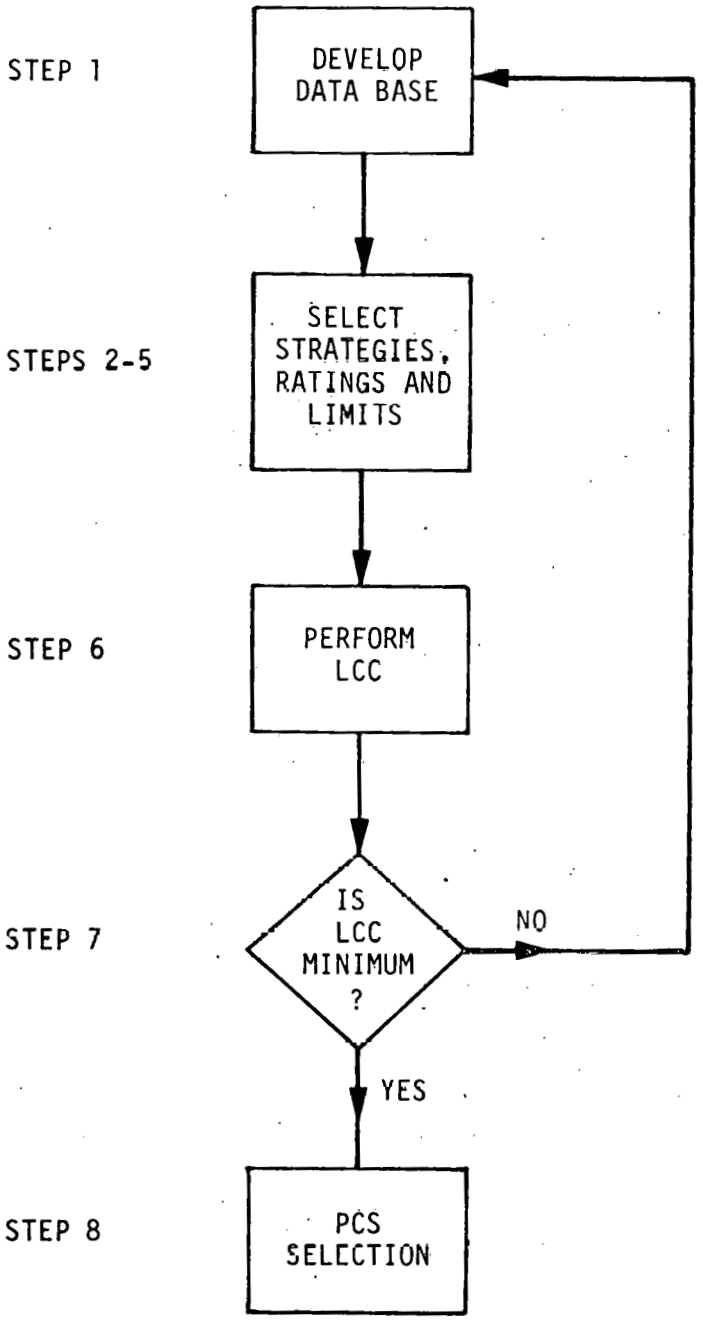

Figure 4-12. Procedure for Selecting a Power Conditioning Subsystem

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SECTION 5

POWER CONDITIONING COMPONENTS

5.1 INTRODUCTION

The goal of power conversion subsystems is to convert electrical energy from an available form (e.g., variable voltage dc) to a desired form (e.g., fixed-voltage, fixed-frequency ac) with power loss held to a minimum. Only three static power handling component types (discussed below) are used:

(1) Switches (e.g., electronic switches such as switching transistors and electromechanical switches such as circuit breakers).

(2) Magnetic components (e.g., transformers, linear and saturating reactors).

(3) Capacitive components (e.g., electrolyte and oil capacitors).

5.2 SWITCHES (ELECTROMECHANICAL)

Electromechanical switchgear, in the form of breakers, contactors, and switches, are typically used as interface isolating components placed at the inverter input and output. Power losses associated with these components are negligible (less than 0.1% of through power). Cost, size, and weight are, however, all sizable fractions of the system total. The technology is mature in the area of large ac electromechanical switchgear; it is therefore unlikely that costs and performance parameters will significantly improve. The availability of dc switchgear, however, is limited and it is likely that costs and performance will improve in the future. While semiconductor devices could ultimately replace electromechanical devices, there are impediments such as lack of transient ruggedness, power loss, off-state leakage currents, and lack of isolation based on NEC definition (positive disconnect). It is conceivable, however, that future semiconductor technology would be applicable in some cases and could replace electromechanical devices. There is limited availability of high voltage dc (above 600 V, less than 1000 A) switches, contactors, and circuit breakers.

High-voltage, low-current dc switches (for example, 1000 V_{dc}, 100 A) are not available commercially, whereas a 600-V device is available. The higher-voltage devices are presently unavailable primarily due to the lack of a commercial market.

5.3 MAGNETIC COMPONENTS

Magnetic components that include transformers and inductors require special design consideration especially where high-frequency techniques are used. With these applications, leakage inductance, parasitic

capacitance, and core loss become key design parameters. As new circuit topologies evolve, new magnetic structures are also born that accommodate newly developed magnetic materials. The trend is toward smaller, more integrated magnetic components that operate at higher frequencies and have more demanding specifications but which reduce cost and weight due to reduced conductor and core masses. Accordingly, as high-frequency switching mode semiconductor technology continues to evolve, new magnetic designs and optimization procedures will be required to enable optimal system designs. Magnetic components will continue to grow smaller, less expensive per kilowatt but more expensive per pound and more engineering intensive. Typical of the high-frequency materials available are amorphous steels and ferrites. Table 5-1 (Reference 5-1) shows the characteristics of these core materials compared to the conventional silicon steel.

5.4 CAPACITORS

The characteristic parameters for capacitors are capacitance, maximum voltage, equivalent series resistance (ESR), leakage inductance, maximum ripple current, and temperature. The focus of new technology has been

Table 5-1. Magnetic Material Comparison

Material	Mils	Characteristic	Frequency Range	Cost, $/lb	Conclusion
Si Steel (Baseline)	12	High B	60-1000 Hz	0.60	Power transformer standard at 60 Hz
	4	High B	400-6000 Hz	2.0	
Nickel Iron		Low loss		-	Too expensive
	4	Low loss	7000 Hz	23.00	
	2	Low loss	12000 Hz	32.00	
Supermendur	2	High B	60-1000 Hz	40-60	Expensive due to price of cobalt
Ferrite (Power)		High Freq. Pressed & Sintered	6 kHz-100 kHz	3.00	Considered above 6-10 kHz (Size limited)
Amorphous Metal	1.3	High B Low Loss- 1/10 that of Si Fe	60 Hz-30 kHz	0.60-0.80 (Est. 1986)	High potential due to low loss; should be available during 1980 decade

for small, low-ESR units that can handle high ripple currents at high frequencies. For high-power, high-voltage applications, research is ongoing for the development of high-performance, nontoxic organic dielectrics. Nonlinear and parametric capacitive elements have yet to be developed that have practical application to power processing.

Capacitor construction is one of the key elements for effective performance and reliability. For non-electrolytic types, extended foil construction, solid connection to braided connection leads are necessary. General-purpose, inserted tab capacitors are not used because of their inability to handle harmonic currents without overheating.

5.5 POWER COMPONENTS

Power dissipating components, such as resistors and linear mode transistors, are ruled out because of inherent dissipation requirements. Although switching type semiconductor components produce power loss, these losses may be minimized through proper design; given levels of power dissipation are not an inherent byproduct of their operation as it is with resistors and linear mode devices.

Of the three component types, switches (particularly semiconductor switches such as diodes, thyristors, and transistors) play the most critical role in power conditioner subsystem design. While the semiconductor switches themselves usually represent a significant fraction of the total system losses and costs, they also have strong indirect impacts on cost and efficiency. With thyristor self-commutated inverters, for example, the required commutation components frequently cost more and incur higher losses than the thyristors themselves. These indirect negative aspects are eliminated with transistor and GTO-based systems in which external commutation is not required. With transistor systems, however, drive circuits are typically more expensive than thyristor-firing circuits. Thus, there is at this time no ideal semiconductor switch.

5.5.1 Rectifier Diode

Although not usually classified as switches, diodes effectively perform as switches wherein a low impedance on-state is maintained for current flow in one direction (forward), and a high-impedance off-state is inherently provided for currents attempting to flow in the reverse direction (Figure 5-1, Reference 5-2).

Virtually all power handling diodes (often called rectifiers) are constructed of doped silicon as shown in Figure 5-2. The P-doped region containing excess holes is termed the anode; the adjoining N region containing excess electrons is called the cathode; the adjoining interface is called the junction. Ohmic solder-type electrical connections are made to the exterior anode and cathode faces as shown.

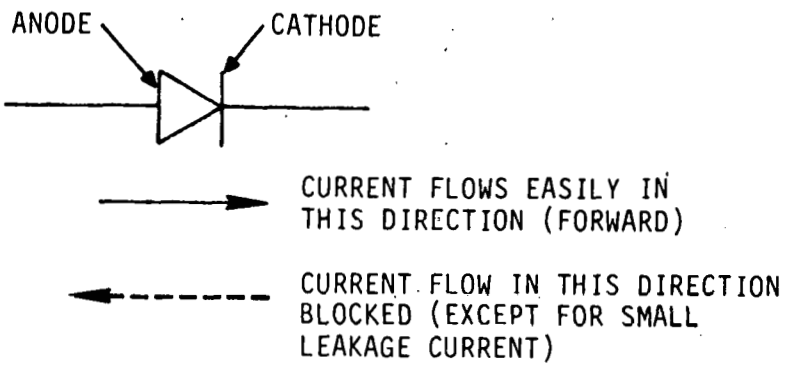

Figure 5-1. Diode Symbol

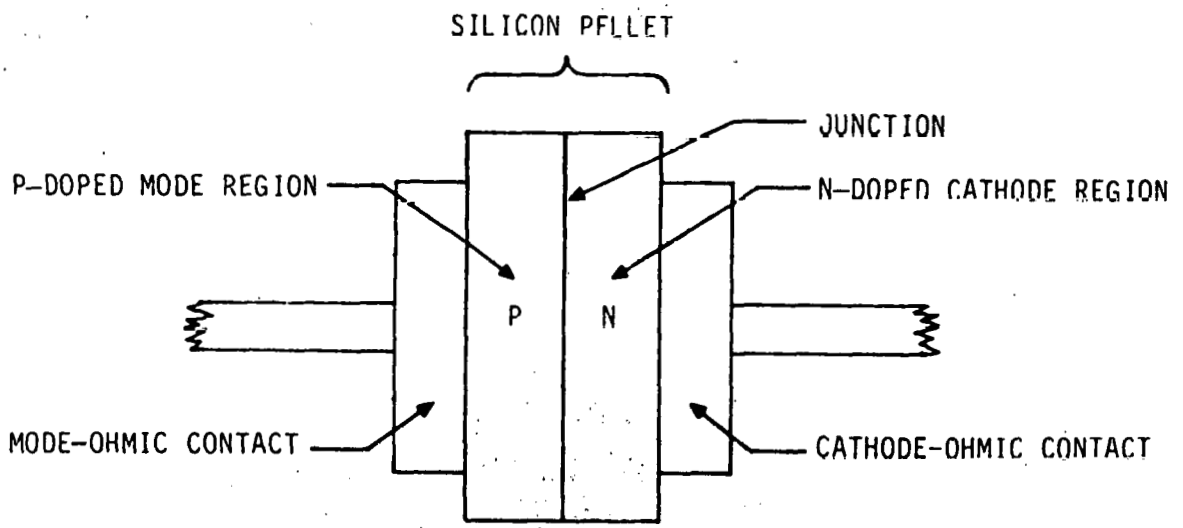

Figure 5-2. Rectifier Diode Construction

The doped silicon element is made by a diffusion process wherein "impurity" elements are diffused at high temperatures to form the N and P regions.

Diode pellets are usually hard-soldered to heat spreading metallic headers. Conventional stud-mount packages (Figure 5-3) are being replaced by modular packaging (Figure 5-4) in which two or more devices are integrated, and the base plate is electrically isolated from each of the devices. Advantages of the modular packaging include lower assembly costs, better heat transfer, and reduced volume of the completed system.

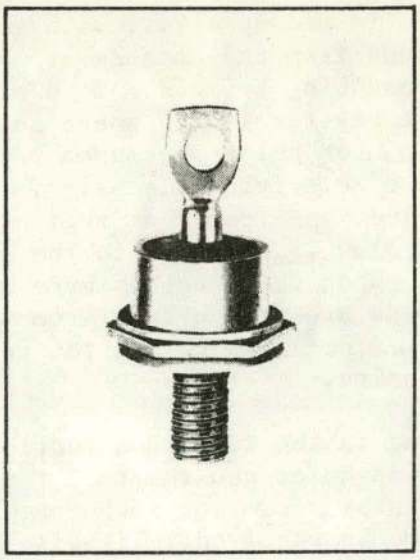

Figure 5-3. Rectifier Diode (Reprinted from Westinghouse Power Semiconductor Data Book, Westinghouse Electric Corporation, 1982)

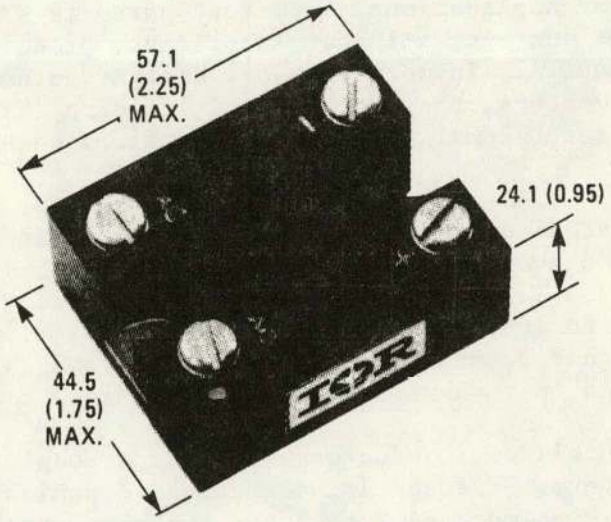

Figure 5-4. Rectifier Diodes (Modular Package). (Reprinted from Semiconductor Databook (1081/82), International Recifier)

When the anode is made positive with respect to the cathode, holes from the anode and electrons from the cathode are both driven toward the junction in response to the resulting E field. Both electrons and holes cross the junction and enter into "enemy territory" where annihilation occurs. Electrons entering the P region encounter holes whereupon recombination occurs, and neutral atoms appear in place of electron-hole pairs. Likewise, holes entering the N region recombine with electrons from that region. Thus, relatively large currents (~200 A/cm^2) can flow in response to the application of a small "forward voltage" (~1 V). When the anode is made negative with respect to the cathode, holes and electrons are driven away from the junction. Only small leakage currents flow (~1 $\mu A/cm^2$), which are the result of thermally generated, hole-electron pairs.

When conducting in the forward direction, N-side electrons cross into P territory (and P-side holes cross into N territory). Electrons injected in P material do not instantly recombine with P-region holes; on the average, a finite recombination time is required. Likewise, a finite time is required for "minority" holes to recombine with "majority" electrons. Because of these time constants, diodes are unable to switch instantaneously from forward conduction to reverse blocking. Specifically, if circuit polarities are stepwise reversed, large reverse currents will flow for a finite period until minority carriers (e.g., holes in N and electrons in P) either recombine or are swept out. This time interval, called the reverse recovery time (t_{rr}), is a strong function of the time required for recombination (minority carrier lifetime). In many power processing applications, especially those using high-frequency techniques, it is necessary to minimize t_{rr} (reverse recovery time) because switching losses are roughly proportionate to $(t_{rr})^2$.

For many applications, important parameters are the maximum voltage and maximum rms current ratings. At present, diode ratings extend up to about 3000 V and 2400 A. In more critical designs, other parameters, such as high-frequency converters, t_{rr}, forward-voltage drop (V_f), reverse-leakage current and transient thermal impedance, thermal impedance, and surge current may be important.

For most diodes, typical recovery times range between about 1 μs for 15-A devices and about 15 μs for 1000-A, 1000-V sizes with V_f ranging between about 0.9 and 1.2 V. With fast recovery diodes, t_{rr} values are reduced by about 5 to 10 times, but V_f is higher, usually around 1.4 V. (Because of the higher V_f and higher cost, it follows that fast recovery devices will be used only where specifically needed.)

As with all semiconductors, cost is strongly sensitive to volume and marketing strategy. Frequently, competing companies will offer price structures that vary as much as 2 to 1 for the same standard part. This difference in price might relate to inequitable pricing structures, manufacturing experience, or technology advances. Accordingly, price analyses are at best approximate.

Price lists supplied by major manufacturers such as General Electric Company, Motorola, International Rectifier, and Westinghouse revealed the following generalities:

(1) Small diodes in the 1 to 5 kVA range sell for between $0.40/kVA and $2.00/kVA in unit quantities and about half that at the thousand level.

(2) Large diodes in the 50 to 1000 kVA range sell for between $0.10/kVA and $0.25/kVA in unit quantities.

(3) Fast recovery diodes are typically twice the price of their standard diode counterparts.

(4) Diode bridge modules typically cost only half that of the sum of the four discrete diodes.

(5) Several new transistors and thyristors have diodes integrated into the package design, obviating the need for separate diodes.

5.5.2 Bipolar Transistors

A bipolar transistor is formed when two semiconductor junctions are formed in close proximity; two device types are possible, NPN and PNP, as shown in Figure 5-5. With this structure, a small current introduced into the center (base) region is capable of controlling a relatively large current between the two outer regions (collector and emitter). Under proper operating conditions, the transistor is able to function as "an electronic switch" that is turned on to a low-impedance conducting state by the application of base current and turned off by termination of the base current. As such, properly used or applied transistors may serve as the switching elements in switch-mode power processing systems (Reference 5-3).

For both linear and switch-mode operation, the collector base junction is back-biased. If the emitter current is zero, the collector current will be negligible, corresponding to the leakage current of the collector-base junction. When the base-emitter junction is forward-biased, current flows across this junction (as it does with a forward-biased diode). As a result, majority carriers from the emitter region are injected into the base region. Because the base region is thin, most of these carriers manage to reach the collector-base junction before recombining with base-majority carriers; crossing this junction, they constitute a collector current. As the base current is increased, the number of minority carriers within the base (and available at the collector-base junction) increases, thus increasing the conduction capability for current between the emitter and collector. A plot of collector current versus base current and collector-to-emitter voltage is shown in Figure 5-6 for a typical switching-type power transistor. Both NPN and PNP type power transistors are manufactured, and many topologies gainfully use NPN/PNP combinations. Because of differences in the physical constants that govern

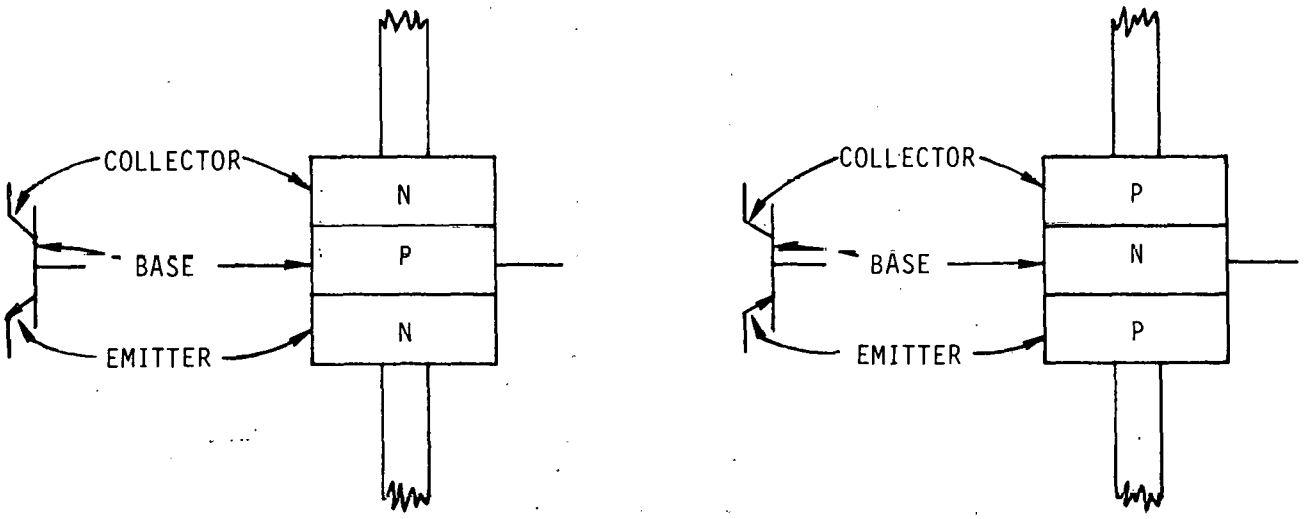

Figure 5-5. NPN and PNP Transistors

holes and electrons, it is easier to fabricate NPN devices of a given performance level. Accordingly, nearly all of the high-performance switching devices are of the NPN variety.

Maximum voltage and current ratings are the most important of the transistor parameters and are more complicated with transistors than with diodes. Furthermore, voltage and current ratings alone are seldom sufficient for acceptable designs.

The collector-to-emitter breakdown voltage is a function of the base termination. With the base open-circuited, breakdown occurs at a lower voltage than with the base voltage set at zero. Accordingly, the open base rating (V_{CEO}) is usually preferred. Unlike diode breakdown, collector breakdown has a foldback characteristic (Figure 5-7). Therefore, to add further conservatism, the sustaining voltage, $V_{CEO\ (SUS)}$, is often specified. Because of high doping concentrations in the emitter region, the base-emitter junction usually breaks down at a low value, typically about 6 to 10 V. Exceeding this rating can lead to thermal destruction of the transistor.

Unlike diodes, transistors do not have large surge current ratings. Exceeding a given threshold of collector current will cause a rapid rise in collector voltage and high junction dissipation. Accordingly, the maximum collector current rating (I_C) should be treated as meaning "peak instantaneous maximum." With some devices, peak single-event currents are also specified; they are usually about $2I_C$. Likewise, maximum allowable base currents are also specified.

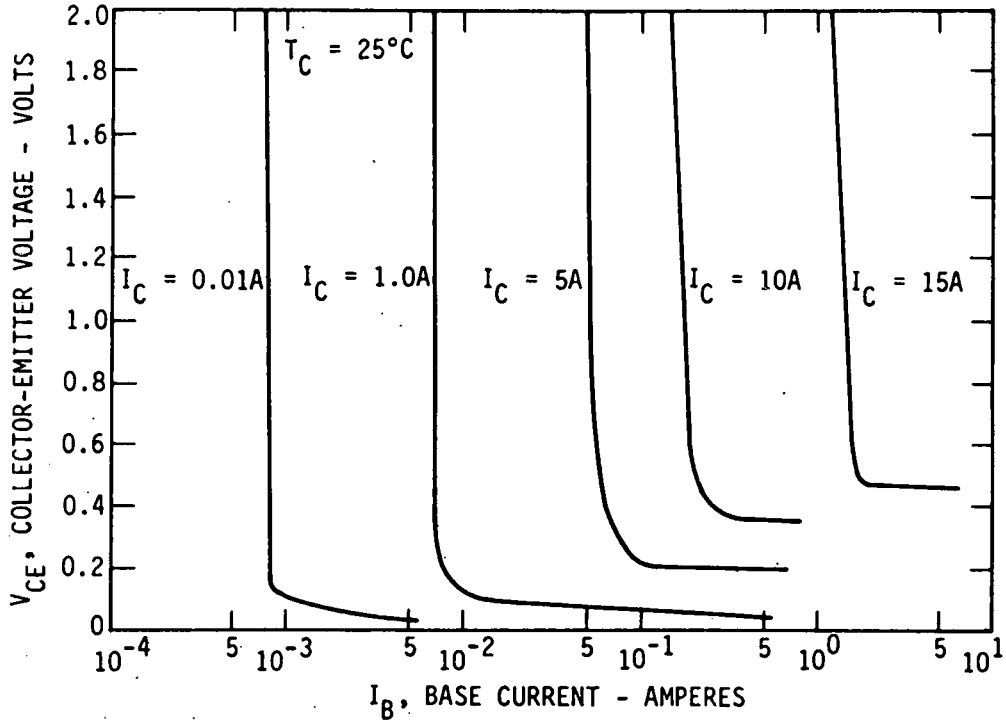

Figure 5-6. Typical Transistor Saturation Characteristic

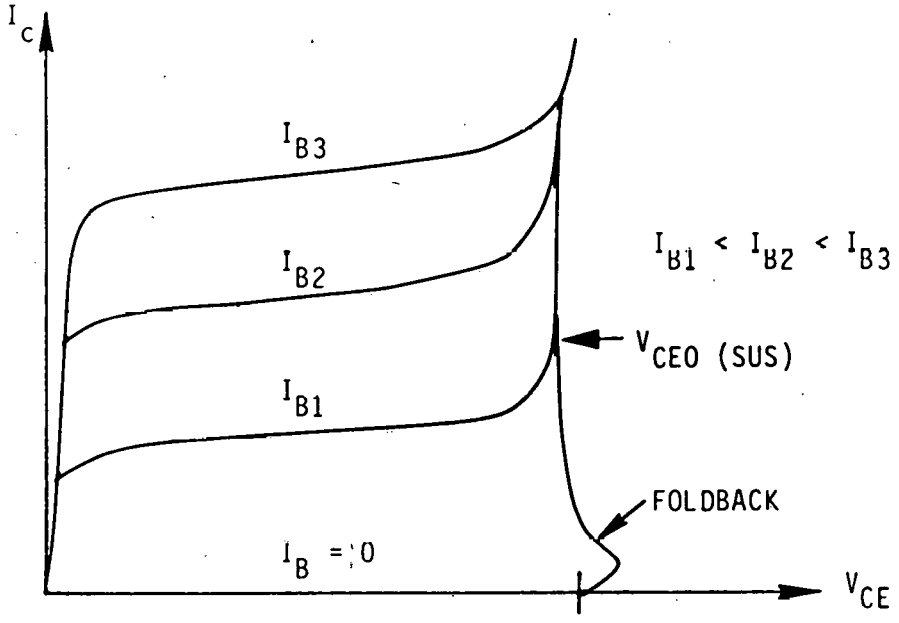

Figure 5-7. Typical Collector Breakdown Characteristic

Gain, which is the ratio between collector current (I_C) and base current (I_B), is also a crucial parameter. With inverter systems, sufficient base current must be provided to ensure saturation (low V_{CE} independent of I_B). Accordingly, both the gain under saturation conditions (forced gain - H_{fe}) and the collector-to-emitter saturation voltage ($V_{CE\ (sat)}$) are critical parameters; they determine the required base drive and the expected on-state losses. Forced gain is a complicated function of temperature and may or may not increase with increasing temperature (Figure 5-8).

At present, switching transistors with V_{CEO} ratings up to 1200 V and I_C ratings up to 1200 A are available as production items. The largest available VA ratings (V_{CEO} x I_C) are about 200,000 with 50,000 now commonplace.

Typical transistor saturation voltages are about 1 V. Darlington transistors (composed of a driver and main transistor) typically have higher $V_{CE\ (sat)}$) values (about 1.5 V). It is interesting to note that many of the new generation Darlington transistors have lower $V_{CE\ (sat)}$ values than their non-Darlington counterparts. Typical forced gain for non-Darlington devices is in the range of 5 to 10 with Darlingtons ranging between 25 and 100.

It should be noted that $V_{CE\ (sat)}$ is important in determining system efficiency because on-state losses are proportionate to $V_{CE\ (sat)}$. While $V_{CE\ (sat)}$ tends to be higher for higher voltage devices, it increases

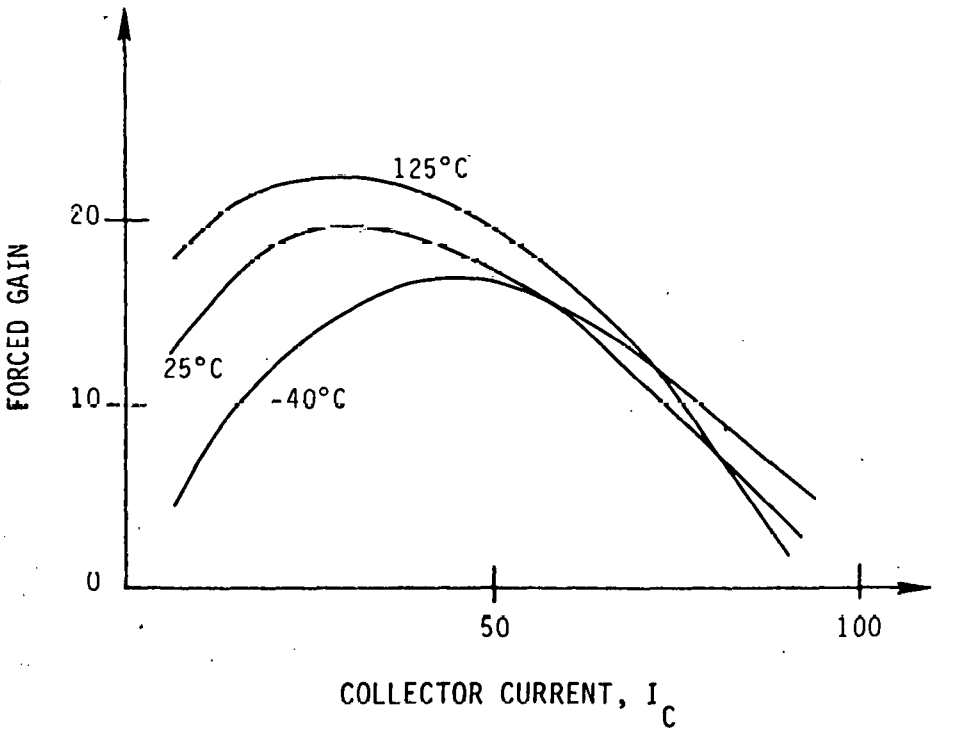

Figure 5-8. Example of Forced Gain versus Collector Current and Junction Temperature

less rapidly than V_{CEO}. Accordingly, percent on-state losses drop as system voltage is increased. Low-voltage inverters tend to have lower efficiency than high-voltage inverters, assuming the same type, but different voltage rated transistors. For low-frequency systems, in which on-state losses dominate over switching losses, both efficiency and heat dissipation improve with increased voltage.

While all power associated with base drive is waste power not transferred to the load, these power losses are small compared to the $V_{CE\ (sat)}$ losses. On the other hand, because base drive circuitry is sometimes more expensive than the transistors themselves, with the cost approximately proportionate to the required base current, it follows that forced gain is critical from an economic viewpoint. Noting that the forced gain drops off less rapidly than reciprocal V_{CEO}, it also follows that base-drive requirements and costs reduce as system voltage is increased.

The fact that transistors have finite turn-on and turn-off times leads to switching losses that are frequency proportionate. For non-Darlington devices (5 to 100 kW rating), turn-on times are typically in the range of 0.3 to 1.5 μs with turn-off times between 1 and 3 μs. Darlington devices are slower, especially regarding turnoff. For a given device technology, the higher voltage versions have slower switching characteristics (especially turn-off times). Thus, with respect to switching losses, efficiency drops with increasing voltage. For low-frequency operation (e.g., up to about 400 Hz), forward-drop loss remains dominant even for the highest voltage devices. However, for moderate and high frequencies (>5 kHz), switching losses impact most and system efficiency typically drops with increasing voltage. Advanced Darlington devices are available at 400-V, 300-A, and 1-μs collector current fall time.

Other time-related parameters are delay time (delay between application of base current and start of current rise) and storage time (delay between removal of base current and start of current fall). Although both of these parameters have impact on circuit design, neither contributes to added losses except where circuitry does not properly allow for these effects. Delay times are small, ranging from a few to several hundred nanoseconds. By contrast, storage times are long, ranging from a few microseconds to several hundred microseconds. Because storage time is the result of excess charge within the base, it increases with the amount of overdrive; conversely, the storage time becomes zero when the device desaturates.

As with all semiconductor devices, maximum power dissipation is determined by the maximum allowable junction hot-spot temperatures (125°C to 200°C, depending on design). For steady-state currents, the hot-spot temperature is determined by the junction-to-ambient thermal impedance and the power dissipation; accordingly, the thermal resistance between the junction and the device case is the only relevant parameter, providing current flows uniformly through the junction. With time-varying dissipations, the junction thermal capacity enters in, and information governing the transient thermal impedance is required.

Under transient conditions, (e.g., during switching), current flow is no longer uniform. Instead, current tends to funnel into a small portion of the junction, causing that portion to heat excessively. This action is regenerative in that the preferred current path is through the hotspot. This effect, termed "second breakdown," is destructive because portions of the junction reach excessive temperatures. In actual inverter use, it is "reverse-biased second breakdown" which is often the limiting factor. To prevent second breakdown and device destruction, power dissipation must be derated below that governed by the transient thermal impedance. Specifically, this derating is a voltage function and typically takes effect for V_{CE} values above one-fourth the breakdown voltage (Figure 5-9).

5.5.3 Transistor Fabrication and Packaging

As with diodes, the starting point for fabrication is the addition of impurities to an otherwise pure silicon chip. The transistor structure, unlike the one-dimensional diode structure, is three-dimensional. Steps in processing chips include masking, diffusion of impurities, addition of SiO_2

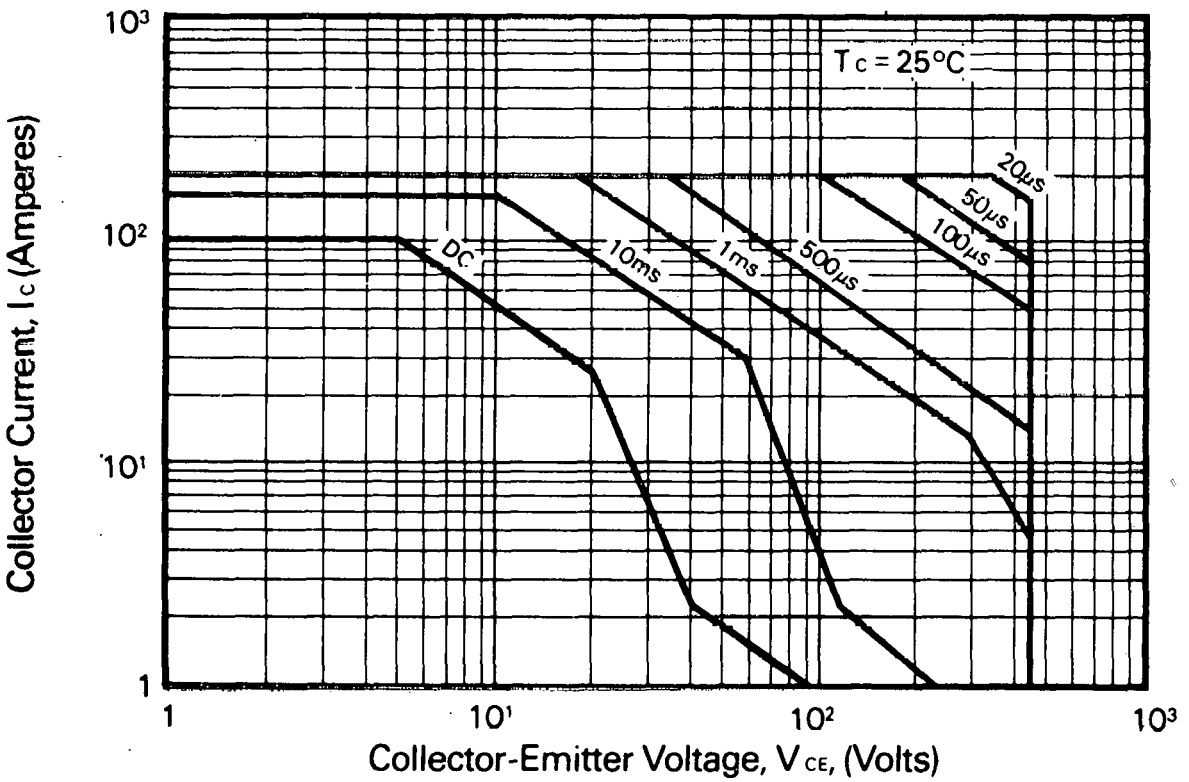

Figure 5-9. Safe Operating Area Characteristic (Reprinted from Westinghouse Electric Corporation Datasheet)

overcoats, etching, and metalizing. Numerous chips are processed simultaneously as part of a single silicon wafer. Upon process completion the silicon wafer is scribed, and the individual transistor chips are "broken out." Numerous structures and fabrication processes are now in use.

With modern high-performance transistors, highly interdigitated structures are used, and the fabrication thus resembles that of an integrated circuit. Unlike integrated circuit fabrication, however, higher purity silicon and more precise control of doping profiles are required. In a sense, therefore, high-power transistor chip fabrication represents the pinnacle of device technologies.

Completed chips are solder-bonded to the desired header, and emitter and base leads are ultrasonically bonded to the appropriate points of surface metalization.

The TO-204 package remains the dominant configuration for devices rated up to about 20 A (Figure 5-10). In the past, various packages were used for higher currents, ranging from stud type to hockey-puck packages. In the last few years a new trend, modular packaging, has been established. In this process, the base plate is usually isolated from the electrical elements, threaded inserts provide emitter and collector connections, and several transistors and diodes are integrated to perform a specific function (Figure 5-11). The module package is attractive to equipment designers because assembly cost, space, and weight are all reduced.

5.5.4 Field-Effect Transistor

The conductivity of doped silicon is altered when an electric field is established within the silicon. This principle is applied to achieve a voltage-controlled transistor wherein voltage applied to a gate element controls the conductivity between source and drain elements by action of an electric field. Unlike bipolar transistors, current does not flow across junctions, and minority carriers are not involved in the charge transport process. Several major advantages result from this alternative transistor operation:

(1) Because minority carriers are not involved, turn-on and turn-off time constants associated with minority carriers are eliminated. As a result, the field-effect transistor (FET) is capable of switching speeds that are 100 times better than their bipolar counterparts.

(2) Control currents are used only to charge and discharge gate-related capacitances. Although large currents are required to charge the gate capacitance and Miller-effect capacitance, the average drive power of an FET is nil compared with a bipolar device.

(3) Because only majority carriers are involved in the conduction process, second breakdown is virtually eliminated. For the same reason, FETs connected in parallel tend to load

Figure 5-10. TO-204 Package (Reprinted from General Semiconductor Industries, Inc., Catalog)

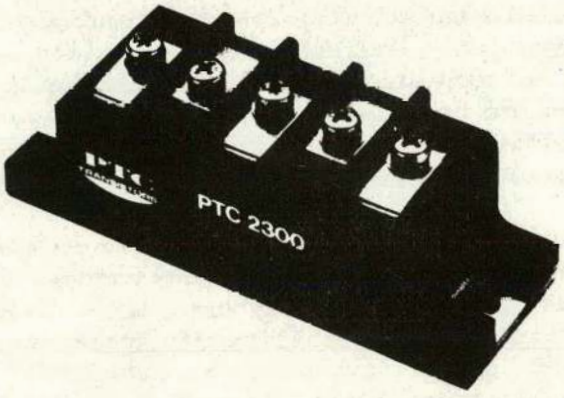

Figure 5-11. Example of a Modulator-Type Package (Reprinted from Data Sheet, Power Transistor Company, PTC 2300, 2301)

share, whereas bipolar transistors tend to be unstable (the hottest transistor carries the most current, thus it becomes even hotter).

Until recent years, power-rated FETs were not produced because the utilization of silicon (VA per cm^2) was poor compared with the bipolar transistor. Using new device geometrics and advanced processing techniques, silicon utilization is now within a factor of two of that of the bipolars. Compared to large-production Darlingtons, FETs are about ten times costlier. However, despite this significant price differential, FET designs often prove more economical because of lower drive circuit (and other ancillary circuit) costs. With growing sales volumes, FET prices should continue to fall and could eventually displace bipolars.

Whereas only two basic bipolar types exist (NPN and PNP), eight FET types are possible. First, the "channel," wherein conductivity is modulated, may be either N or P material (while N type dominates, P-channel complementary devices are available). For each of these categories, doping profiles may be such that the channel is either normally conductive under zero gate voltage or normally non-conductive. (The normally nonconductive type is nearly standard). Finally, for each of these four combinations, two gate structures are possible, junction gate and insulated gate. At present, the insulated gate (using SiO_2 as the insulating barrier) is the more frequently used.

The first-quadrant characteristics of a typical FET are shown in Figure 5-12. The maximum drain to source voltage, V_{DS} (gate voltage, $V_{GS} = 0$) is determined by avalanche breakdown within the channel. Presently available devices have V_{DS} ratings between 60 and 1000 V.

As noted in Figure 5-12, the on-state is characterized by a resistance; i.e., $V_{DS} = R_{DS\,(on)} \times I_D$. (In contrast, the collector-to-emitter saturation voltage of a bipolar transistor is a nonlinear function of the collector current.) The on-state resistance and the dissipation capability in turn determine the continuous current rating. The largest FETs have current ratings of about 50 A.

Because the on-resistance increases roughly as the square of the breakdown voltage (for fixed-chip size), high-voltage devices have reduced current ratings. The highest VA rating for a single chip device is currently about 4000, with a projected availability of 15,000 by mid 1984.

With bipolar transistors, current gain falls rapidly as the rated current is approached due to an effect called current crowding. Because of this problem, bipolar devices have virtually no overload capability, i.e., peak currents of even short duration must not exceed the continuous rating, or desaturation will result. In contrast, FETs, which are free from current crowding, have a relatively high overload capability; with maximum allowed V_{GS} applied, pulse-drain currents of up to about seven times the continuous rating may be handled without desaturation. This capability in turn translates into improved economics, assuring that the relatively high on-state V_{DS} can be tolerated. When operated in an overloaded pulse mode, the transient thermal

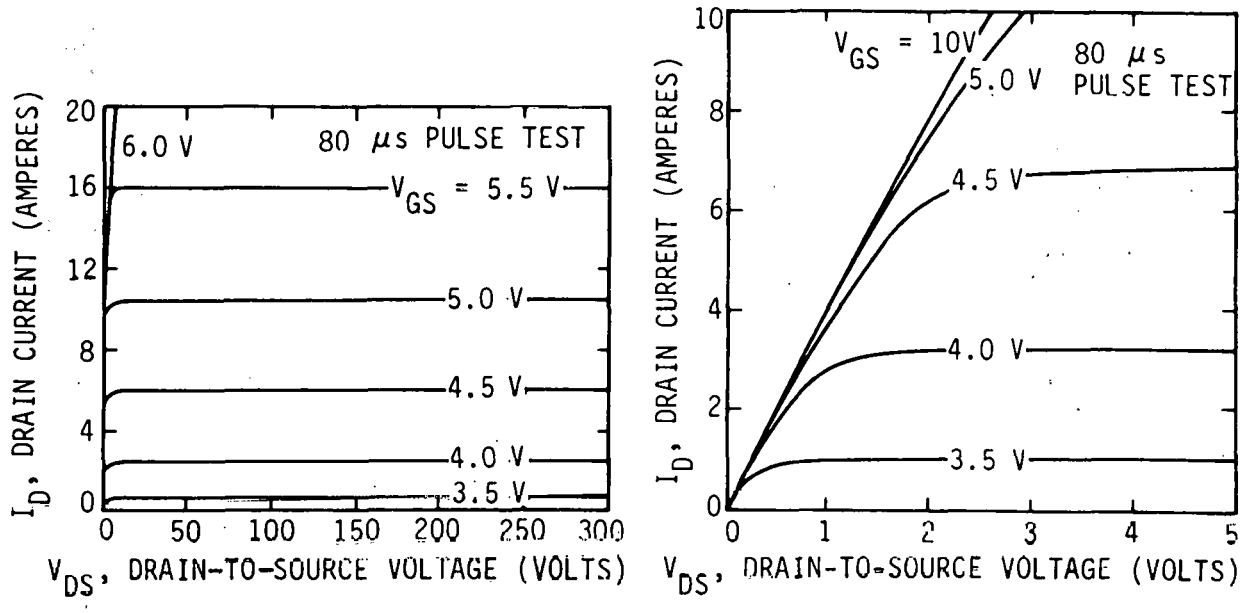

Figure 5-12. Field-Effect Transistor (FET) Characteristics (Reprinted from FET Data Sheet, International Rectifier)

impedance must be considered in addition to the average dissipation to ensure that peak junction temperatures are not exceeded. Because the FET is free from second breakdown, no related derating is required.

The gate element is usually sensitive to voltage-induced destruction. Exceeding the maximum gate voltage rating can easily destroy the SiO_2 gate underlay even where current capabilities are limited to microamperes. Accordingly, the maximum V_{GS} rating should be treated with respect, and zener or other protective means should be used to ensure that excessive gate voltages are never encountered. For moot power devices, the maximum allowed value is between $\pm$10 and $\pm$20 V.

Most commercial devices are of the N channel, enhancement, insulated gate variety. With these devices, drain current is limited to a leakage value ($\sim 10^{-5}$A of rated on-current) until V_{GS} is made sufficiently positive. The value of V_{GS}, where I_D starts to increase, is called the Gate Threshold Voltage, $V_{GS\,(th)}$; typical values are between 1 and 3 V.

Unlike bipolar devices, the switching speed of the FET is limited only by inter-element capacitance. Accordingly, the capacitance between source, gate and drain is frequently specified to enable in situ determination of switching speeds. Where the internal impedance of the gate-drive circuit is such that transient gate currents is 0.1 I_D, typical rise and fall times of 30 to 100 ns are achieved. Thus, efficient switch mode operation up to 100 kHz is possible, using present-generation FETs.

Figure 5-13 shows a typical FET structure. Power FET fabrication involves the marriage of two technologies: large-area, medium-scale integrated circuit technology and conventional power device technology. While the FET structure is less efficient than the bipolar in silicon utilization and requires more sophisticated processing, the possibility of large-volume production of a relatively few device types holds promise for low costs in the future. At present, FETs are between two and ten times the cost per VA of bipolar devices and are even more expensive when I_D is derated to produce comparable saturation voltages.

Currently, three package types are common. The high-power devices (4000 VA) are typically packaged in TO-3 cases. The more compact TD-220 plastic case is used for devices in the 100 to 2000 VA range and small (<100 VA) devices are frequently packaged as "multiples" in dual-in-line configurations.

5.5.5 Thyristor

A fundamentally different type of semiconductor, called a thyristor, results when a fourth layer is added to the transistor to form a PNPN structure as shown schematically in Figure 5-14. Unlike bipolar and FET structures, this new structure will not operate in a linear mode but only as a switching device. To understand this behavior, it is noted that the PNPN arrangement shown in Figure 5-14 resembles the bootstrap arrangement shown in Figure 5-15. With this arrangement, turn-on of either transistor results in a regenerative action that in turn causes both transistors to saturate and remain saturated even after removal of the initiating base drive. Turn-off of this latch is possible only by external interruption of the anode current.

It should also be noted that an actual four-layer device is not exactly equivalent to the two-transistor analog because current flow is almost entirely axial; current within layers two and three is composed of both holes and electrons, and doping concentrations are different. Because of these and other differences, the four-layer structure is able to operate at high, continuous-current densities (>100A/cm^2) and high peak-current densities (>1000A/cm^2) (References 5-4 and 5-5).

Transition from the off-state (forward blocking) to the on-state can be initiated by increasing the gain of either or both transistors to the point where $B_N B_P > B_N + B_P$, where B_N is the gain of the PNP section, and B_P is the gain of the NPN section. While this may be accomplished optically, thermally, or by transistor action, the latter method is the most common when a gate connection is provided to the third layer. The resulting structure is called a thyristor.

Numerous other four-layer thyristor structures are possible, including the "triac" (bidirectional SCR), the gate turn-off thyristor (GTO), and the "diac" (bidirectional diode thyristor).

With the thyristor, transition from the forward blocking to the on-state is triggered by application of a small positive gate current. Transition

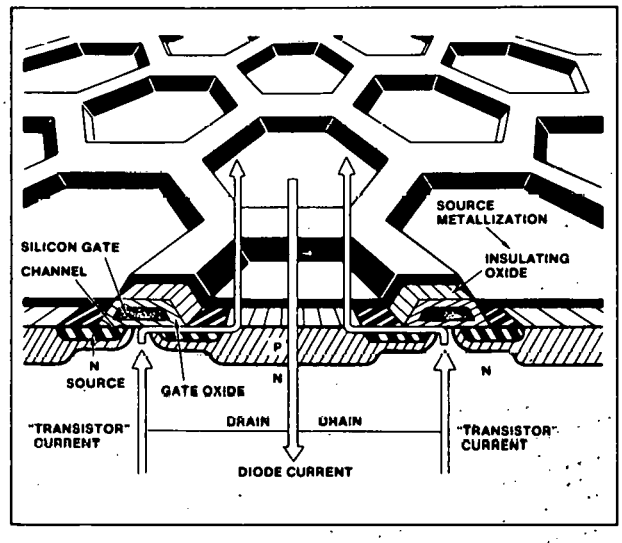

Figure 5-13. Example of Basic Field-Effect Transistor Structure (HEXFET) (Reprinted from Application Note 930, International Rectifier)

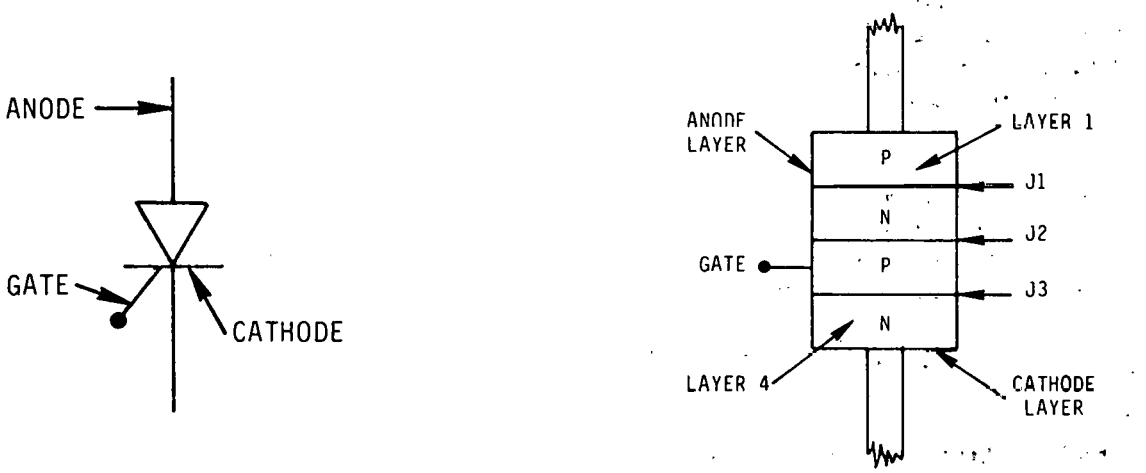

Figure 5-14. Symbol and Basic Thyristor Structure

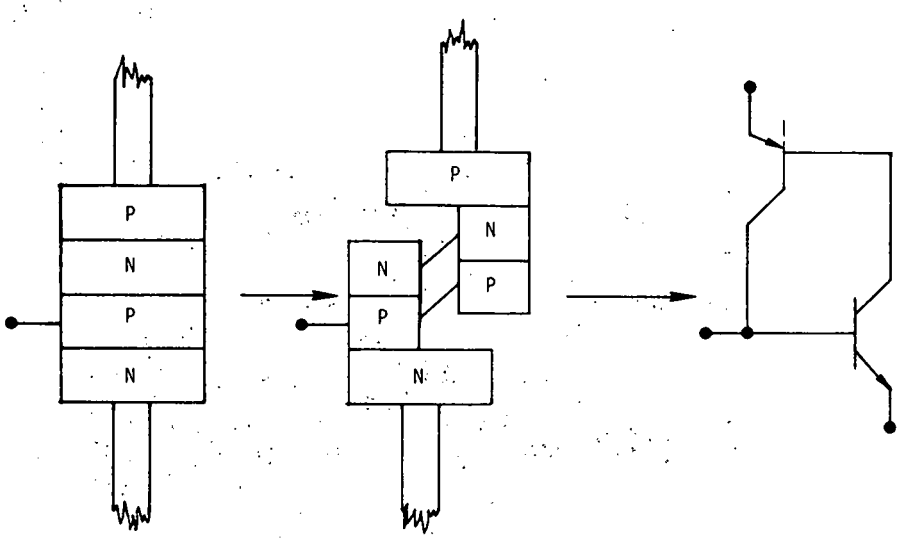

Figure 5-15. Two-Transistor Analog of PNPN Structure

from the on-state to the off-state requires external interruption of the anode current for time sufficient to allow recombination of excess minority carriers within layers two and three. This time factor, called the turn-off time (t_q) varies from less than 10 μs to more than 100 μs, depending on design details.

Unlike the transistor latch circuit, the thyristor is able to withstand high levels of reverse anode voltage. This is due to the lower doping concentrations in layer one and the greater width of layer two as compared with the base region of a transistor. In virtually all thyristor designs the reverse blocking voltage (anode negative with respect to cathode) is equal to the forward blocking capability. Asymmetric SCRs (ASCRs) have been built for special applications in which the reverse blocking voltage is compromised to provide improved turn-off times. Potentially, such ASCR devices could provide a considerable advantage for many inverter and chopper topologies in which high reverse blocking is not required.

Presently, thyristors with ratings in excess of 2000 V and 1500 A are available. With small devices (>10 kVA), the hundred price cost ranges between about \$0.15 and \$1.00/kVA, depending on parameters. Large high-voltage devices cost less than \$0.10/kVA with prices below \$0.05/kVA not uncommon. Thus, the thyristor is by far the least expensive switching device.

Typical forward voltage values range between about 1.0 and 1.4 V, with 1.4 V typical for fast recovery inverter types. As with diodes, V_f is more or less a log function of the forward current. Forward and reverse leakage currents are usually specified. Both are typically less than 10^{-4} of the rated current.

For a thyristor to remain in the on state directly after the gate signal is removed, a minimum value of anode current must be maintained. This minimum current is called the latching current. For most thyristors it is

about 10^{-3} to 10^{-2} of the rated current. Once regenerative action has been established, anode current must be reduced to a value specifically below the latching current before reversion to the off-state. This lower threshold is called the holding current.

Anode current must be interrupted for a minimum time (t_q) to ensure that a blocking state prevails when positive anode voltage is reapplied. Inverter-grade thyristors, like diodes, should be used only where the fast recovery is needed. For inverter-grade thyristors, t_q ranges between 7 and 50 μs. Non-inverter types typically are in excess of 100 μs. Because t_q increases with increasing junction temperature, t_q is usually specified at the maximum allowable junction temperature.

Turn-on time, while often not included in data sheets, may be important when considering high-frequency applications. Because the turn-on time is determined in part by the lateral spreading of the on-state plasma, thyristor turn-on is slow compared with the bipolar transistor in which the base element is highly interdigitated. Typical turn-on times range from 1 μs for small devices (~1 A in size) to more than 20 μs for large units (~1000 A in size).

Capacitance within the silicon between the anode and gate layers effectively limits the rate (dv/dt) at which anode voltage can be reapplied without spontaneous turn-on. Rated dv/dt values range between about 20 and 500 V/μs. If the gate is held negative during forward voltage application, higher than rated values may be withstood. Circuits have been operated with dv/dt values as high as 3000 V/μs.

Compared with the bipolar transistor, the thyristor is considerably more rugged. First, the thyristor is inherently a two-state device and will not operate in a sustained, high-dissipation mode. Second, it is free from second breakdown; current does not tend to funnel through a small junction hot spot as it does with the bipolar. These factors, coupled with the inherent mechanical superiority of the thyristor structure lead to excellent reliability when the "rules" are followed. The thyristor, however, does have one weakness of which the bipolar and FET are free: di/dt fatigue. For most designs, the gate signal is applied to the pellet periphery, and the turn-on action must spread radically inward. Accordingly, anode current does not flow uniformly during the transient, plasma-spreading interval (Reference 5-6).

If anode current is allowed to rise too rapidly, thermal stresses result that may cause immediate or delayed device failure. To prevent di/dt failure, two precautions must be followed: (1) the external circuit must limit di/dt to a value below the device rating and (2) the gate signal must be sufficiently hard, i.e., must rise sufficiently fast and reach a sufficient current magnitude. Typical di/dt ratings range from 20 to 800 A/μs. High di/dt capabilities are achieved by special design of the gate in which interdigitation is provided to reduce the plasma-spreading distance. As a result, high di/dt devices tend to have low turn-on times.

Figure 5-16 shows a typical thyristor structure, which is essentially one-dimensional, whereas transistors are three-dimensional. This

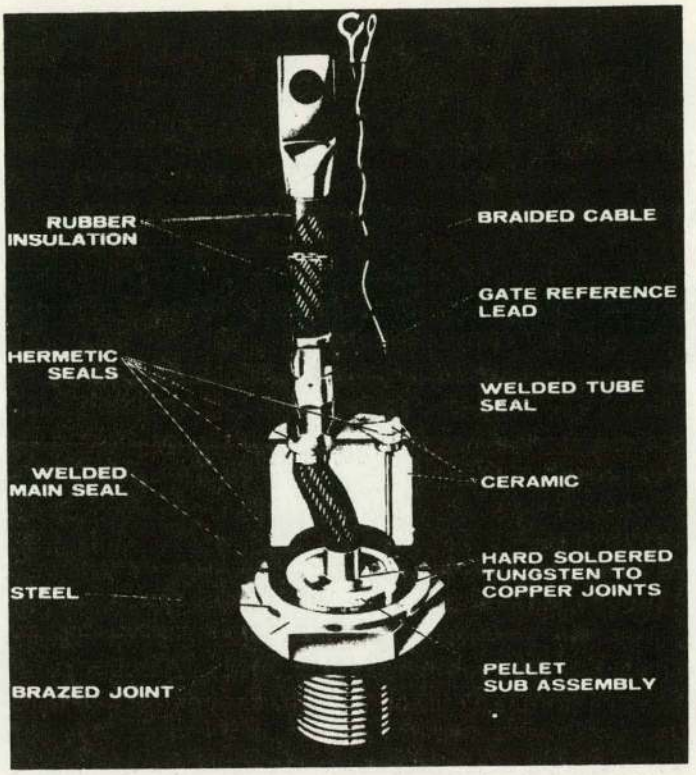

Figure 5-16. Typical Thyristor Construction (Reprinted from SCR Manual, Sixth Edition, General Electric Company, 1979)

simplification, in addition to the high silicon utilization, are the reasons for excellent economics. Fabrication steps, consisting of sequential diffusion, masking, passivating, etching, and metalizing, are similar to those of other semiconductors. With the simplest thyristor structure, fabrication is reduced to three diffusion steps and surface metalization. With more advanced structures that employ interdigitated gates, the fabrication steps and physical appearance resemble those of bipolar transistors.

Several packages are presently in use (Figure 5-17). Stud-mount packages of various types remain popular for currents between 15 and 500 A. With these large devices (270 to 1500 A), the hockey puck is generally used. With this package, compressive mounting is used that ensures a fatigue-free, low thermal impedance path from both faces of the pellet to ambient. The improved heat transfer allows increased current densities and improved economics. In recent years, modular packaging has been pioneered in which thyristors and diodes are interconnected within an isolated, base-plate, prismatic package. Because of compactness and ease of interconnection, these packages often save money at the system level and are therefore gaining widespread use.

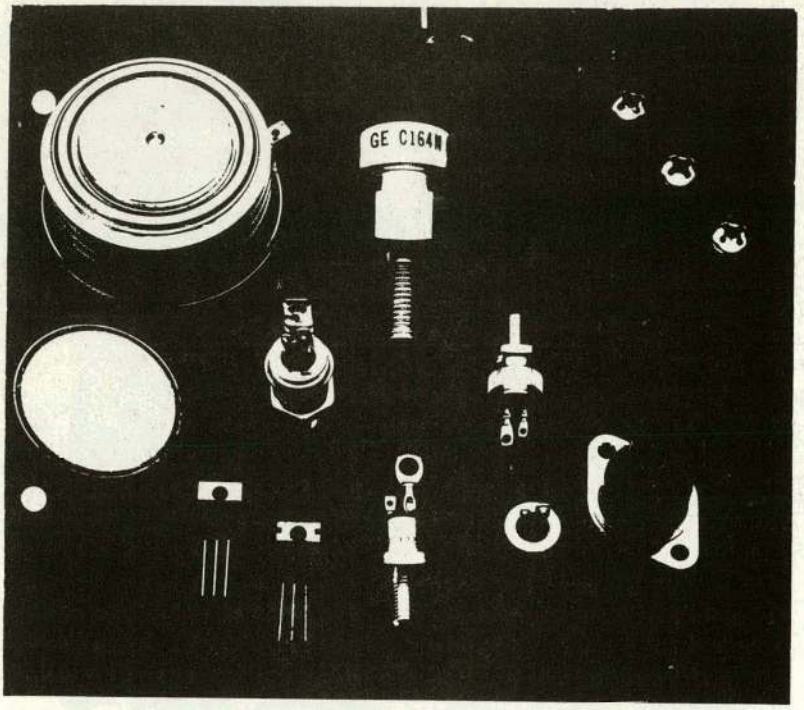

Figure 5-17. Various Thyristor Packages (Reprinted from Thyristor-Rectifiers, General Electric Company, 1982)

5.5.6 Gate Turn-off Thyristor (GTO)

As discussed in the theory section, the thyristor may be viewed as a bootstrap transistor combination. Accordingly, if the two transistors have equal gains, a large negative gate current approaching half the anode current would be required for a gate-induced turn-off. With conventional thyristors the corresponding internal resistance drops associated with the gate contact and with the third layer region are excessive, and gate turn-off is impossible except for very low anode currents.

With suitable modifications, it is possible to construct a thyristor that has gate turn-off capability for high anode currents (called gate turn-off thyristors), shown in Figure 5-18. The key element to this modification is the use of a highly interdigitated gate whereby the gate resistance problem is conquered. Another modification is that altered doping profiles are used so that third-layer hole currents are reduced, thereby reducing the required current and charge for gate turn-off, thus enabling increased turn-off gains.

Because of the interdigitated gate and other factors, GTO current densities are about half those of thyristors. The reduced silicon utilization and the complicated masking patterns lead to costs that range between three and eight times those of equally rated thyristors.

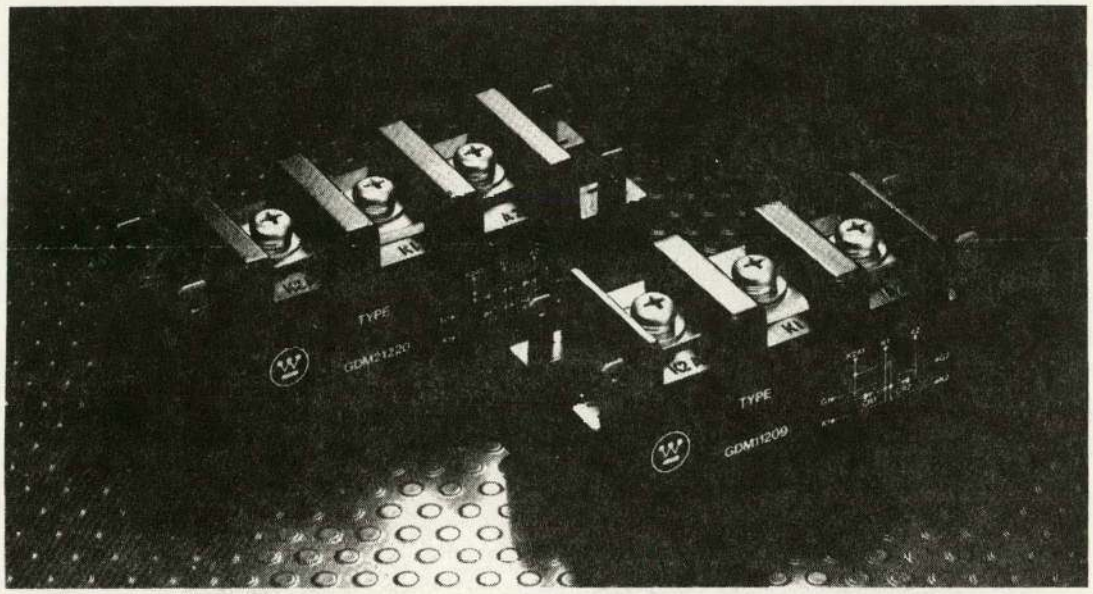

Figure 5-18. Gate Turn-off Thyristor (GTO) Modules (Reprinted from Westinghouse Electric Corporation Datasheet)

Benefits of the interdigited gate are improved turn-on time and high di/dt capability. Typical rise times are about 2 to 3 μs, and di/dt limits are usually higher than can be achieved by the turn rate of rise, i.e., external di/dt limiting is not required.

Because of the required doping profiles, present generation GTOs tend to have forward-blocking voltages ranging between about 600 and 1200 V with reverse-blocking of typically 200 V. Present continuous current ratings range between 10 and more than 1000 A. For most devices, the peak allowable current (under which reliable turn-off can be achieved) is between two and three times the continuous current.

5.5.7 Advanced Semiconductor Devices

Many new high-power semiconductor devices are in development (References 5-7 and 5-8). Some are available in prototype or initial production phase quantities and others are in research phases. Several of these devices are:

(1) Gallium arsenide field-effect transistor (GaAsFET).

(2) Insulated transistor (IGR).

(3) Static induction transistor (SIT).

(4) Field-controlled thyristor (FCT).

(5) Reverse-conduction thyristor (RCT).

(6) Asymmetrical thyristor (ASCR).

Table 5-2 shows a comparison of operating characteristics for self turn-off devices. These include bipolar, GTO, MOSFET, SIT, FCT, GaAsFET devices having applications in both low, medium, and high power.

Figure 5-19 is a comparison of breakdown voltage and on-resistance of various FET devices. The on-resistance of the gallium arsenide transistor at 500 V is two orders lower compared to the state-of-the-art MOSFET device. Thus, application of the gallium arsenide FET should result in very high-efficiency power conditioners. Gallium arsenide FET devices are not currently commercially available but are being developed.

Table 5-2. Comparison of Operating Characteristics for Self Turn-off Devices

Device Characteristic	Bipolar Transistor	Gate Turn-Off Thyristor	MOSFET	JFET and Static Induction Transistor	Field-Controlled Thyristor (FCT)	GaAs FET
Normally On/Off	Off	Off	Off	On	On	On/Off
Reverse Blocking Capability, V	≈50	500 to 2500	0	0	500 to 2500	0
Breakdown Voltage Range	50 to 500	500 to 2500	50 to 500	50 to 500	500 to 2500	50 to 500
Forward Conduction Current Density,* A/cm^2	40	100	10	10	100	100
Surge-Current Handling Capability	Poor	Good	Poor	Poor	Good	Poor
Maximum Switching Speed (approximate)	200 kHz	20 kHz	2 MHz	2 MHz	20 kHz	2 MHz
Gate-Drive Power	High (large base-drive current required during on-state and for turn-off)	Medium (large turn-off gate currents required)	Low (only small capacitive charging currents required)	Low	Medium	Low
Operating Temperature, °C	150	≈125	200	200	200	200

*The forward current densities are compared here for 500-V devices operating at a forward voltage drop of 1.5 V.

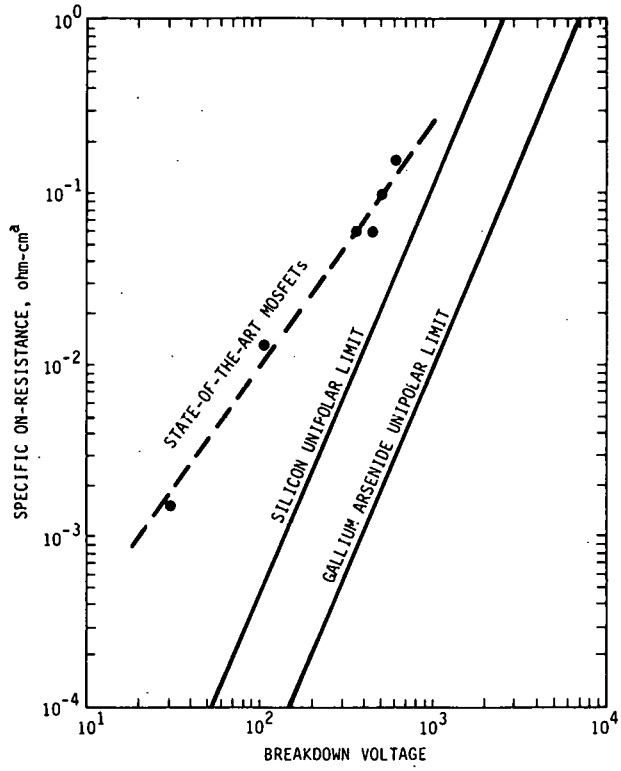

Figure 5-19. Comparison of Breakdown Voltage and On-Resistance of Various FET Devices. The Curves Show the Strong Dependence of Power-FET On-Resistance on Breakdown Voltage. The Decrease in On-Resistance With the Change From Siclicon to Gallium Arsenide is Also Apparent.

5.6 REFERENCES

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SECTION 6

FUNDAMENTALS OF INVERTERS

6.1 INTRODUCTION

One of the major components for the widespread use of photovoltaic systems is the availability of low-cost, highly efficient, and performance-effective power conditioning subsystems. The key element of the subsystem is the inverter, also called a power conditioner or converter, the basic purpose of which is to convert array dc power into usable ac current that is compatible with a utility system (Reference 6-1). Included in this subsystem are the required necessary controls and interfaces to the array, to the load, and to the utility. The primary purpose of this section of the document is to describe the process of dc-to-ac inversion and to present various concepts and topologies of inversion, such as self- and line-commutation (Reference 6-2).

Inverters have fundamentally three different modes of operation: stand-alone, utility interactive, and utility interactive with stand-alone capability. This report concerns itself with the utility interactive inverters whose performance is determined by array characteristics, inverter design, and utility characteristics.

6.2 INVERTER APPLICATIONS

6.2.1 Utility Interactive Inverters

A utility interactive inverter must be able to be connected to a utility line that has the capability of supplying or accepting essentially unlimited power (Reference 6-3). It is general practice in utility interactive inverter design to provide an impedance to decouple the inverter from the very low impedance of the utility. This simplifies the control system design for the inverter and in three-phase systems tends to reduce the negative effects on inverter rating of utility line voltage unbalance. Topologies that directly control the output current do not require a decoupling impedance per se. The utility line will determine the inverter operating voltage and frequency. Inverter synchronization to the utility line is accomplished by electronic means within the PCS. The utility interactive inverter must also be able to operate over voltage ranges that are specified by American National Standards Institute (ANSI) Standard C84.1a-1980 (Reference 6-4). It must be self protecting under overload and transient conditions on the utility line and must have the capability of being removed from service under conditions of utility out-of-tolerance voltage and frequency conditions. Electrical isolation and grounding are specified in the National Electrical Code (NEC) (Reference 6-5).

Utility interactive inverters have the following characteristics:

(1) The inverter power handling capability is predicated upon the desired power transfer from the array. The PV inverter has limited overload capability since designs are generally sized for rated or peak array power output. High overload capability in inverter and converter designs usually reflect decreased efficiency and increased inverter cost and provide only limited improved array energy transfer.

(2) Utility harmonic voltage and/or current injection is predicated on inverter design and utility network characteristics.

6.2.2 Stand-Alone Inverter

Stand-alone inverters are designed to service a specified set of loads, supplying a regulated voltage to these loads. Loads utilized in stand-alone operations are similar to loads connected to and operated by the utility. The inverter design for stand-alone operation is of a low-impedance type and provides a constant voltage. With a constant voltage the connected loads will determine the system power capability. Stand-alone inverters must be able not only to provide the steady-state power for a connected load, but also must be able to supply its surge requirements. Typical loads that have large surge requirements are compressor motors, air conditioners and lighting. Many motor-type loads have inrush currents that are many times the steady-state rating of the motor. Thus, a stand-alone inverter power capacity must satisfy steady-state and surge requirements of the load. To provide the stand-alone inverter with surge capability, the inverter surge power rating must be increased accordingly. If the overload requirement is for short periods, such as 5 or 10 seconds, the major impact on the inverter design may be only in an increase of semiconductor rating and circuit protective ratings. If surge requirements are sustained over a much longer interval, then ratings of other components, such as heatsinks, may have to be increased. The oversizing of the inverter to accommodate surge loads will increase inverter costs due to higher current requirements of the associated power semiconductors.

The harmonic voltages generated in stand-alone operation are predicated upon the specifics of the inverter design and the methodology for waveform generation. A typical harmonic level used in uninterruptible power supplies is a total of 5% harmonic distortion. The harmonic distortion level, which appears at the inverter output terminals, is the harmonic voltage that is applied to the connected loads. Thus, any harmonic currents that flow into the loads are determined by the load impedance and the harmonic voltage. In addition, stand-alone inverters of specified steady-state rating will usually be more expensive than a comparable utility interactive type.

A stand-alone inverter will tend to have a lower efficiency compared to the same power rating of a typical utility interactive inverter due to oversizing required by surge loads.

6.3 INVERSION METHODOLOGY

The ideal inverter takes power from a variable dc source (array) and converts it into single-frequency ac power of constant amplitude and low harmonic content. The degree in which inversion is accomplished that approaches the ideal situation depends upon the type of circuit design approach (topology) that is used. The types of circuit topologies that are used are varied, and some generalized approaches to inversion methods are discussed in this section of the report. Some of the simplest inverter technologies may reflect low-cost and high-efficiency approaches. Their resultant waveforms may be rich in harmonic content and, as a result, may not be acceptable for many types of loads or to the host utility. To reduce the harmonic content of simple inverters, filters are usually required, which adds substantially to inverter cost and lowers inverter efficiency. Section 7 details a varied choice of topologies that are based upon reliability, electrical performance, cost, volume, audible noise levels, weight, types of available cooling, and other diverse requirements. Several of these topologies are applicable to stand-alone operation. Many of these topologies also resemble the simple type of inverter but use switching methodology that greatly reduces filter requirements (References 6-6 through 6-8).

6.3.1 Basic Inverter

Because the input to an inverter is unidirectional (power from array) and its output produces an ac waveform, dc-to-ac interconnection must be performed. There are several elementary types of inverters: parallel, half-bridge, and full-bridge inverters (Figure 6-1). The switch elements S-1 through S-4 in these figures are solid-state switches. One leg of a bridge inverter is commonly called a power pole; the associated switches may be transistors, thyristors, GTOs, or other similar devices. The selection of inverter configuration depends upon availability of semiconductor devices; voltage rating and cost of the semiconductor devices; speed of operation; short circuit capacity; and application. For instance, the parallel inverter and the half-bridge inverter have application in small, single-phase power conditioners. This does not preclude the use of a full-bridge inverter, which is also popular in small-size inverters. The full-bridge inverter in the three-phase configuration is the most popular in the medium and large-size inverter systems (References 6-9 through 6-12). The voltage rating of the switches in the bridge-inverter configurations (see Figure 6-1) is minimally the source voltage (V_{DC}). The voltage rating of the switches in the parallel inverter is twice the source voltage (2 V_{DC}). The doubling of voltage is due to the transformer action of the transformer primary. Switching methodology is somewhat similar for the parallel inverter and the bridge-type inverters.

Figures 6-2b through 6-2d show the typical switching functions of a simplified full-bridge inverter of Figure 6-2a; 6-2b shows output waveform of a full-bridge inverter being operated so that switches 1 and 4 are on for half a cycle, or 180 deg. After switches 1 and 4 turn off, switches 2 and 3 are turned on for an additional 180 deg, thus constituting a full cycle of operation, or 360 deg. This waveform has no multiples of the second harmonic. Figure 6-2c is similar to Figure 6-2b with the exception that first

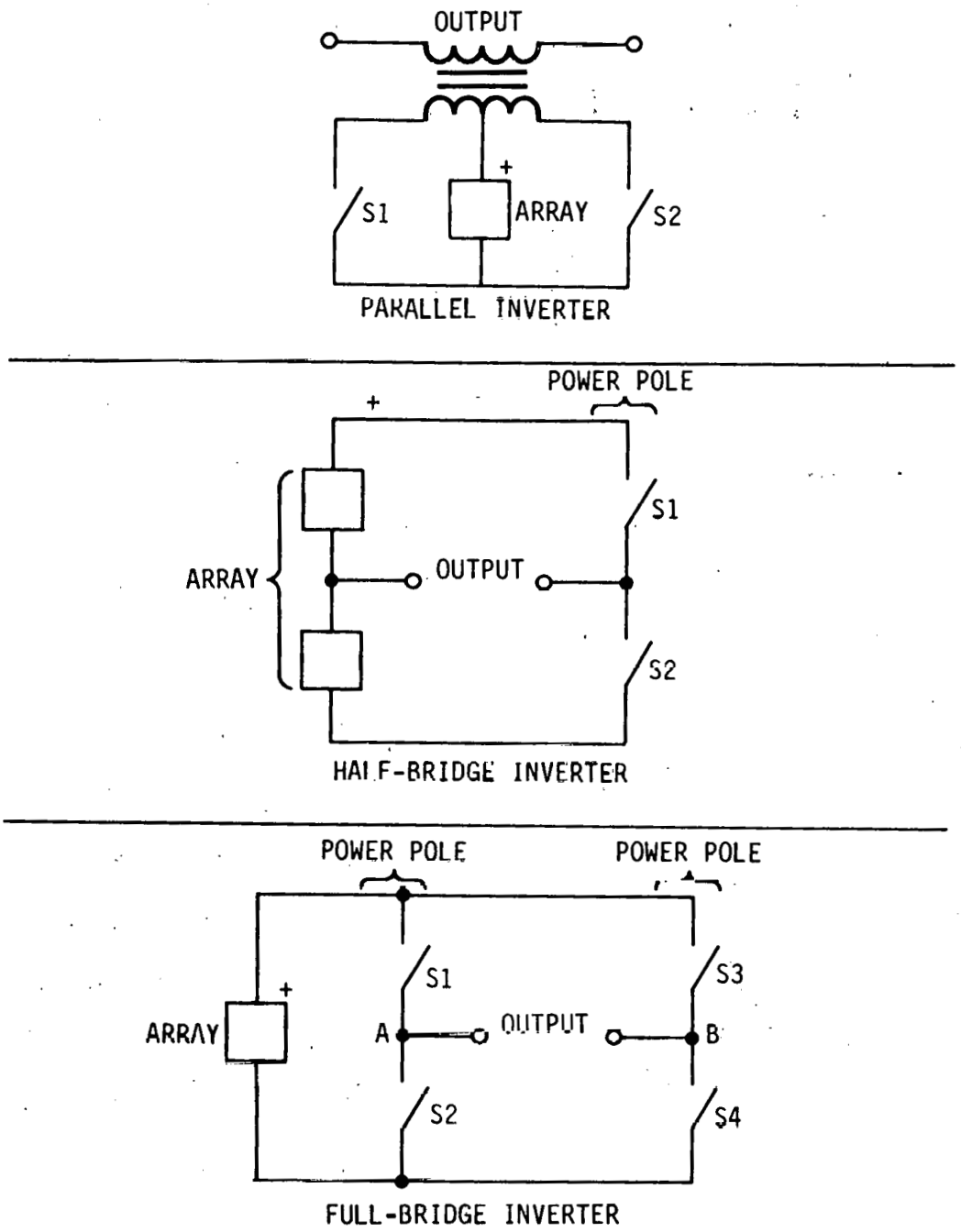
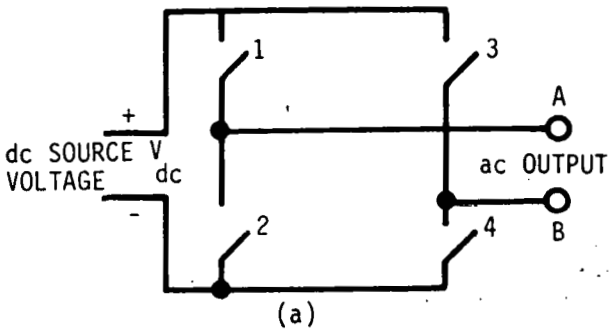


Figure 6-1. Types of Inverters (see Reference 6-9)

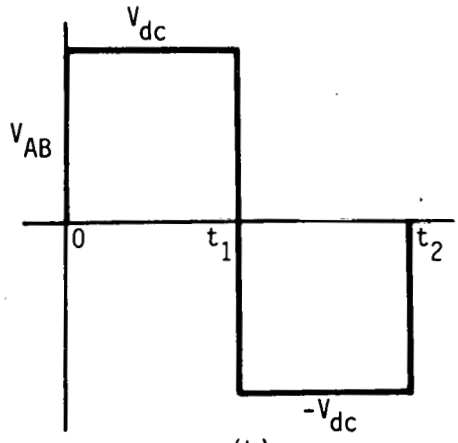


(a)

SWITCH OPERATION:

0 - t_1: 1, 4 CLOSED - 3, 2 OPEN

t_1 - t_2: 1, 4 OPEN - 3, 2 CLOSED

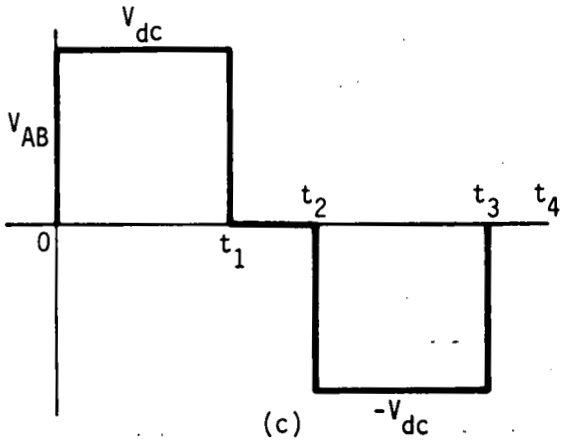


(b)

OUTPUT VOLTAGE V_{AB}

0 - t_1 = 180°

t_1 - t_2 = 180°



(c)

OUTPUT VOLTAGE V_{AB}

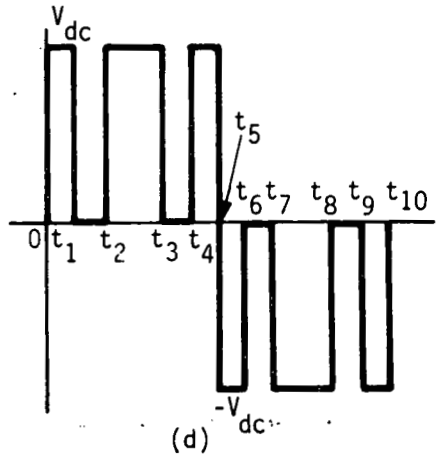
SWITCH OPERATION:

0 - t_1: 1, 4 CLOSED - 120°: 3, 2 OPEN

t_1 - t_2: ALL SWITCHES OPEN - 60°

t_2 - t_3: 3, 2 CLOSED - 120°: 1, 4 OPEN

t_3 - t_4: ALL SWITCHES OPEN - 60°



(d)

OUTPUT VOLTAGE V_{AB}

SWITCH OPERATION

FOR THE INTERVAL 0-180°
SWITCHES 1, 4 ARE CLOSED
SWITCHES 2,3 ARE OPEN
AT 0-t_1, t_2-t_3, t_4-t_5

AND OPEN AT t_1-t_2, t_3-t_4

ALSO SWITCHES 3,2 ARE
CLOSED IN A SIMILAR
FASHION FROM 180°-360°
AND SWITCHES 1,4 ARE OPEN

Figure 6-2. Bridge-Inverter Switching Methodology

switches 1 and 4 are closed for 120 deg; then all switches are open for 60 deg. Following this, switches 2 and 3 are closed for 120 deg, thereby completing one cycle of operation. This waveform is similar to the waveform in Figure 6-2b with the exception that all multiples of the third harmonic are absent. Figure 6-2d shows inverter operation similar to those in Figures 6-2b and 6-2c with the exception that, instead of a single switching taking place in a half-cycle of operation, multiple switchings occur in a half-cycle of operation. Configuration switches 1, 3 may perform the multiple on-off switching and switches 2, 4 may stay on for their respective half cycles. The objective of multiple switching in a half-cycle of operation is to allow the PCS designer by proper selection of the number of switchings per half cycle and the spacings T-1 to T-2, etc., to further reduce harmonic outputs at the terminals A, B. Voltage can be adjusted at terminals A, B by varying the time intervals o-t_1, t_1-t_2, etc. This process is called pulse-width modulation (PWM). The switching operation is discussed in detail in Section 6.4 (see Reference 6-7).

There are two classes of inverters: current-fed and voltage-fed inverters. Another class of dc/ac inverter (which may be a composite of a current- and voltage-fed inverter) is the high-frequency link inverter. These inverters can be line-commutated, self-commutated, and force-commutated. A detailed discussion of the various types of inverters follows.

6.3.2 Current-Fed Inverter

The current-fed inverter is characterized by a large source inductor to provide a constant-current source independent of load impedance (Figure 6-3). Current-fed inverters may be line-commutated or force-commutated and have the following characteristics (Reference 6-13) for photovoltaic applications:

(1) The dc source is constrained to be a constant current generator.

(2) Commutation is achieved by transferring the current flow from one output line to the other.

(3) The output of the system is capable of delivering real power only.

(4) The semiconductors are exposed to transients present at the inverter terminals.

(5) The system operates at a poor lagging displacement factor for current-fed, line-commutated inverters.

(6) The ac output current in a conventional, current-fed inverter is nonsinusoidal in nature and rich in harmonics. The current from the source will contain second harmonic in single-phase systems, sixth harmonic in three-phase, six-pulse systems and twelfth harmonic in three-phase, twelve-pulse systems.

(7) The utility voltage must be present to provide thyristor commutation. (Current-fed, line-commutated inverters)

(8) Reactive volt amperes are required from the utility when operating at all dc array voltage levels. (Current-fed, line-commutated inverters)

6.3.3 Voltage-Fed Inverter

A voltage-fed inverter is an inverter of the type described in Section 6.3.1 wherein the source has a low internal impedance compared to the load being fed. The voltage-fed inverter is characterized by a large capacitor across the source, thereby providing a low source impedance for the inverter. The output voltage waveform is determined by the method by which the inverter waveform is synthesized. The source and load current is in turn determined by the magnitude of the load impedance and the generated waveform (inversion methodology). Both voltage-fed and current-fed inverters have been successfully built for photovoltaic utility interactive operation (Reference 6-14).

6.3.4 Line-Commutated Inverter

Figure 6-3 shows the basic single-phase, current-fed, line-commutated inverter (Reference 6-15). The inverter configuration is the same for that of a rectifier except that the input is dc with ac output whereas a rectifier has an ac input with dc output. Standard rectifier analysis usually assumes that the inductor value is very large so that the dc current is constant. This leads to the continuous conduction mode wherein the inductor current never ceases during circuit operation, and the ac current waveform is a square wave with its well-known Fourier spectrum. Reduction of the inductor value can reduce the ac harmonics as well as the inductor size and cost. At low enough input dc average current, another mode of operation can appear.

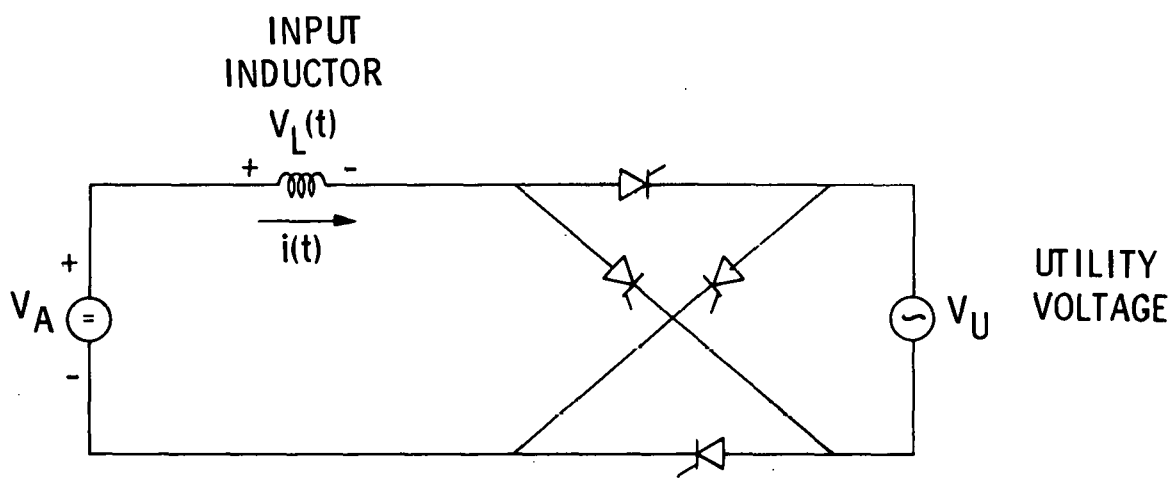


Figure 6-3. Basic Line-Commutated Inverter

This is called the discontinuous current mode, where the inductor current starts from zero and returns to zero during each half cycle of circuit operation. In discontinuous conduction the thyristors "naturally" communicate each half cycle as the inductor current goes to zero. In the continuous case this does not happen, and thyristor commutation must be forced by firing the other pair of SCRs.

Figure 6-3 defines the voltages on either side of the inductor and typical discontinuous and continuous mode currents are shown respectively in Figure 6-4a and 6-4b. Points of thyristor triggering are called firing angle. The amount of power transferred from the array to the utility system is controlled by these points of thyristor triggering. In this discussion, the thyristor trigger angle is measured positive from the positive slope voltage zero crossing for convenience. The traditional rectifier analysis choice is 180 deg sooner in time. At this point in time, the dc voltage on the left side of the inductor is greater than the ac voltage on the right side; the ac voltage may be negative if is negative. In the discontinuous mode can be either positive or negative and is shown positive in Figure 6-4a. In the continuous mode must be negative as shown in Figure 6-4b to have a line-forced commutation. Because inductor voltage is positive (left to right), the current increases as shown until the inductor voltage is zero, at which time the current is maximum. The current decreases thereafter while the inductor voltage is negative. If the inductor current reaches zero before the inductor voltage is again zero, the thyristors turn off naturally and discontinuous operation is assured. If not, the current again starts to rise and commutation must be forced before the next voltage zero crossing.

In the line-commutated inverter (see Figure 6-3), the fundamental component of ac current lags the utility voltage. As a result, the inverter appears as an inductive load to the utility system. The displacement factor (fundamental component power factor) would be determined by the relationship of the PV source voltage Vdc and the utility system voltage and will vary from 0.0 to 0.9. Improved harmonic injection and displacement factor is possible with an ac filter (Figure 6-5). The filter used for improved harmonics power factor improvement can be of a static type as shown or can be of a dynamic type similar to VAR generators used on high-voltage transmission lines. In the VAR generator, filter inductance or capacitance is switched into the circuit by thyristors as required, thereby continuously adjusting the effective power factor to its optimum value.

If the dc input inductor is an infinite inductance, the utility system's current would be a square wave. A smaller input inductor (see Figure 6-3) would provide a more sinusoidal current with less current harmonic injection into the utility system. The degree of harmonic injection is determined by the selection of the value of the input inductor.

A typical three-phase, line-commutated inverter is shown in Figure 6-5. This inverter is a three-phase, six-pulse type and operation is similar to that described above. A twelve-pulse, three-phase line-commutated

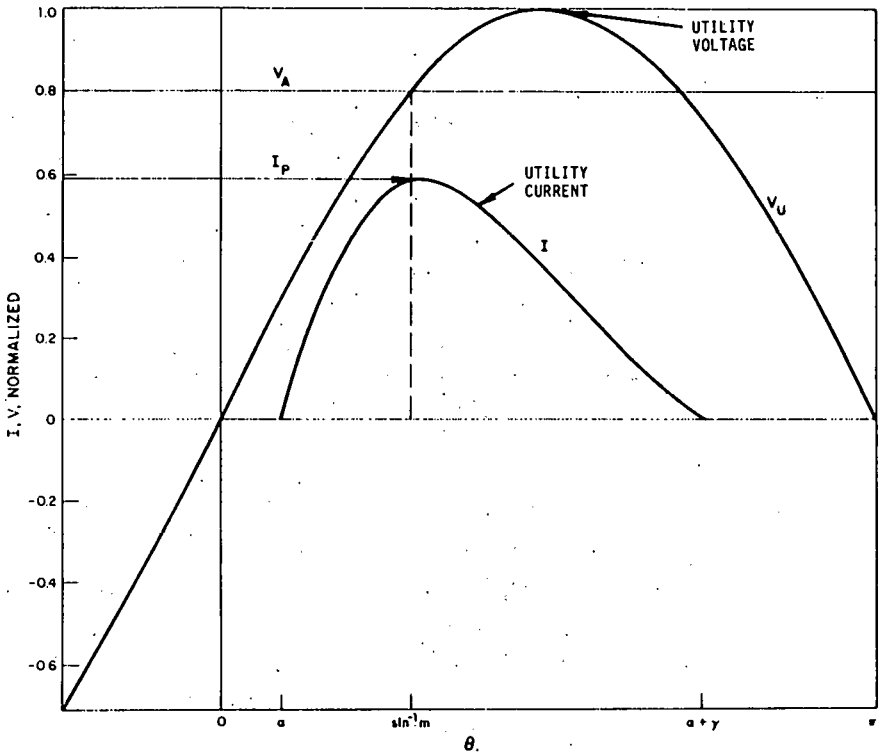


Figure 6-4a. Typical discontinuous Mode Waveforms

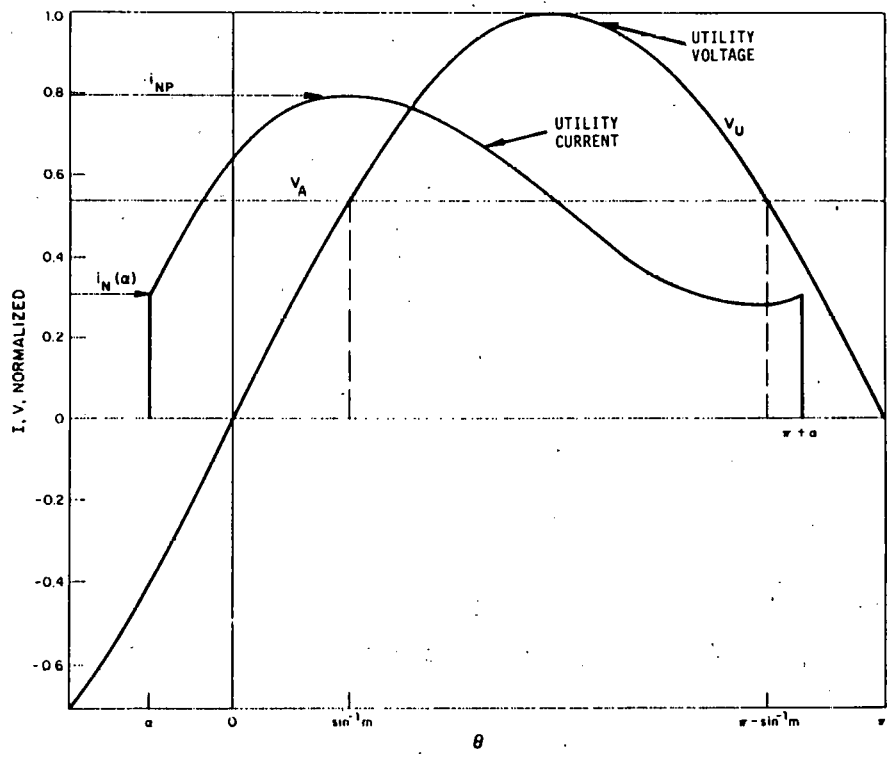


Figure 6-4b. Typical Continuous Mode Waveforms

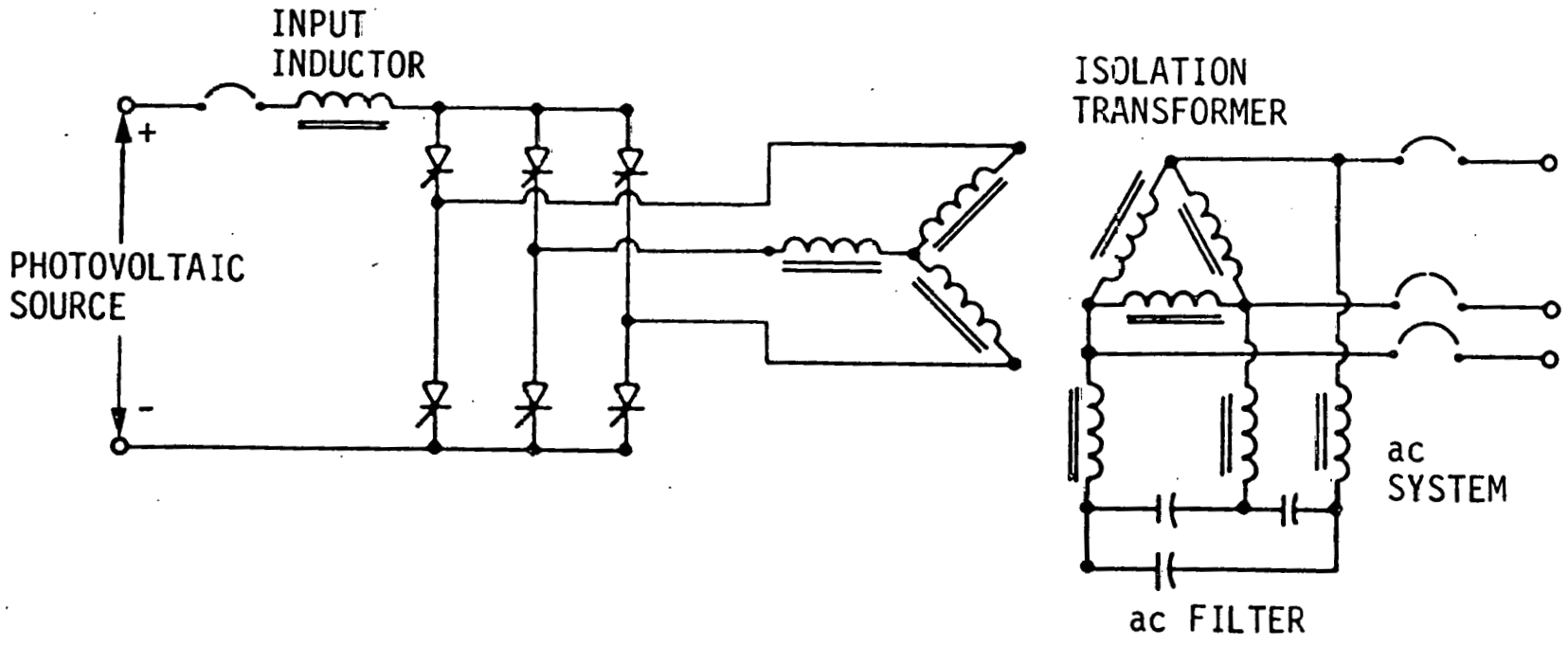


Figure 6-5. Line-Commutated Inverter with ac Filter

inverter is shown in Figure 6-6. Operation is similar to that of the basic line-commutated inverter shown in Figure 6-3. Twelve-pulse operation compared with six-pulse operation reduces harmonic current generation and improves the power factor. The phase shift between the two delta-wye output transformers is used to improve output waveform (References 6-16 and 6-17).

An innovative method to improve power factor and harmonics is to interject a dc/dc converter between the photovoltaics array and the inverter. This approach is currently in development for 3ϕ configurations. The objective is to have the dc/dc converter adjust the dc voltage to keep the ratio of ac utility voltage to dc voltage fixed and as close to a ratio that approximates rectifier operation.

6.3.5 Self-Commutated/Force-Commutated Inverters

Self-commutated and force-commutated inverters are inverters whose switching functions occur in the inverter itself and which are not dependent on the utility voltage for switch turn-off. Self-commutated inverters use semiconductors such as transistors and GTOs. These devices can be turned off by control signal action which, in turn, turns off the device. In force-commutated inverters, the inverter semiconductor switches are turned off by auxiliary commutation circuitry that is part of the inverter design. In transistorized, self-commutated inverters, transistor turnoff is accomplished by removal of the base signal. In thyristor, force-commutated circuits, thyristor current is reduced to zero prior to thyristor turnoff by imposition of current pulses that flow for a sufficient length of time to supply the load so that the thyristor gate can provide control. This process of thyristor turnoff is called commutation. One principle advantage for the self-, or force-commutated, inverter is the capability to operate in stand-alone mode. Force-commutated inverters, when using high-speed switching, can produce high levels of acoustic and electromagnetic interference (EMI), which must be suppressed in the basic system design. Using voltage-fed inverters to provide VAR (power factor) control requires the ability to adjust inverter output voltage amplitude relative to the utility voltage. Power transfer between the photovoltaic system and the utility line is controlled by adjusting the phase angle between the utility line and the inverter.

A simplified block diagram for voltage-source inverters is shown in Figure 6-7. Inverter operation is described above. The input filter reduces array ripple, and C_2 provides the necessary low source impedance to the inverter. The line-tie reactors provide the necessary decoupling to the utility to provide stable control and to limit harmonic current injection (Reference 6-18).

6.3.6 Forced Commutation

There are various methods for inverter forced commutation. Five voltage-fed, forced-commutation inverter methods are shown in Figure 6-8. Shown is one leg (power pole) of an inverter. There are various advantages and disadvantages of the different methods. The choice of commutation circuit is determined by cost and component parts count and stress. High parts count

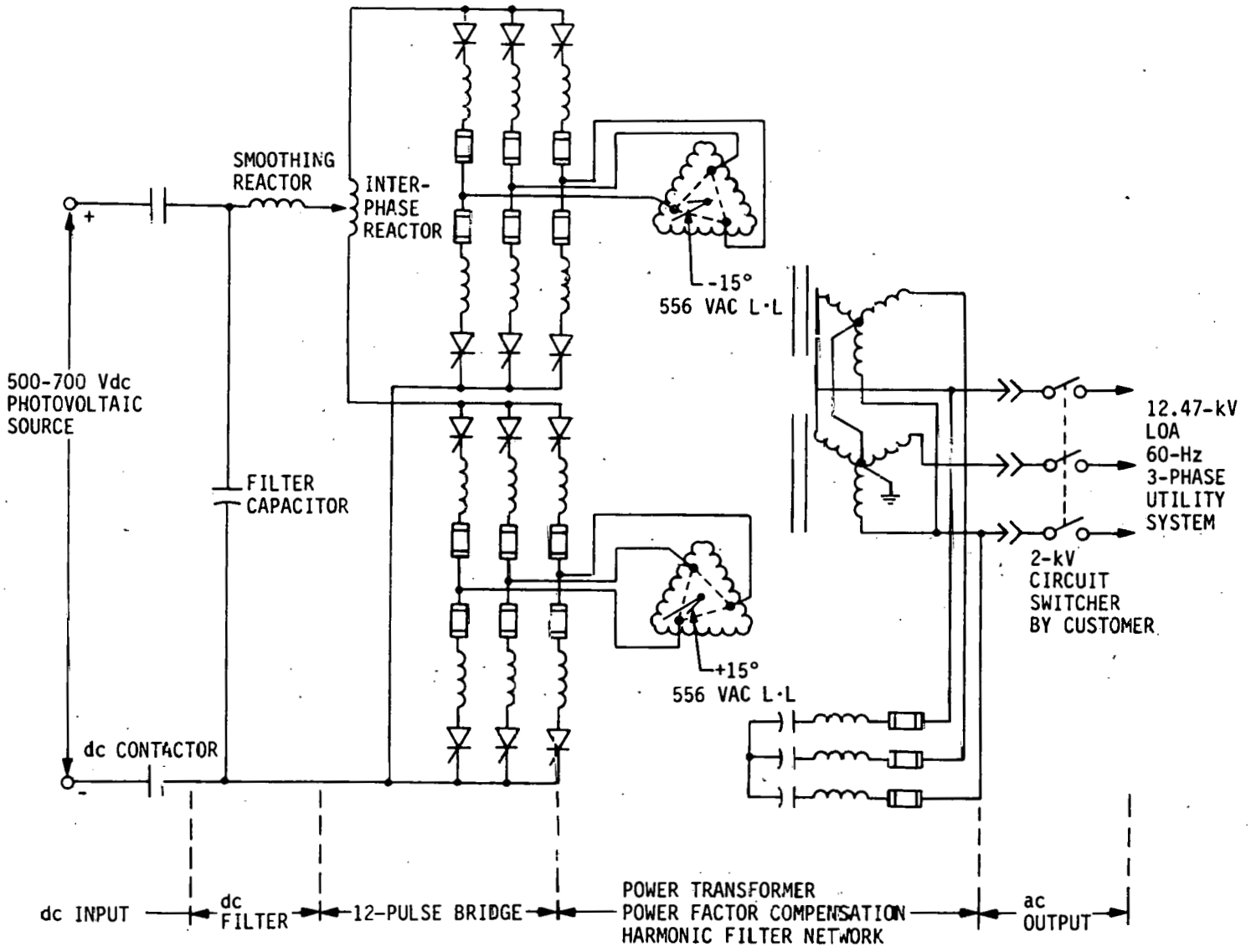


Figure 6-6. Twelve-Pulse, Line-Commutated Inverter (see References 6-16 and 6-17)

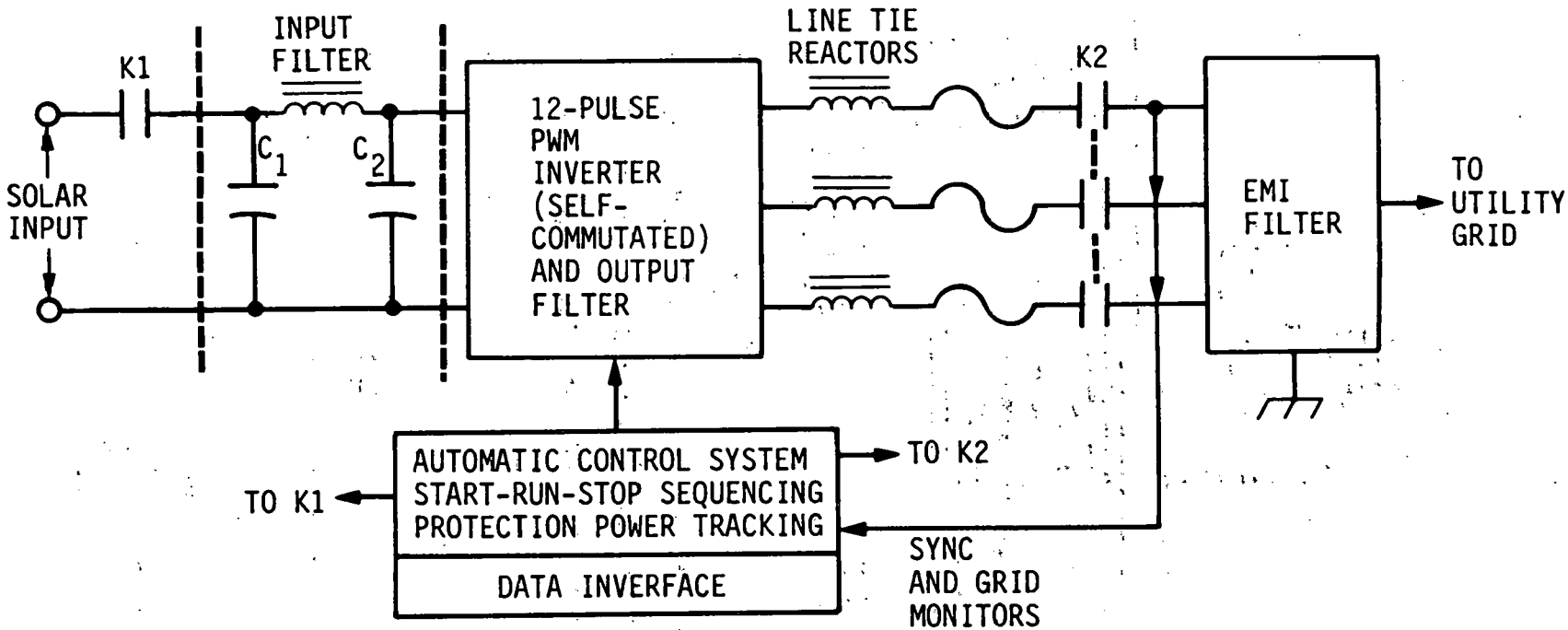


Figure 6-7. Voltage Source Inverter

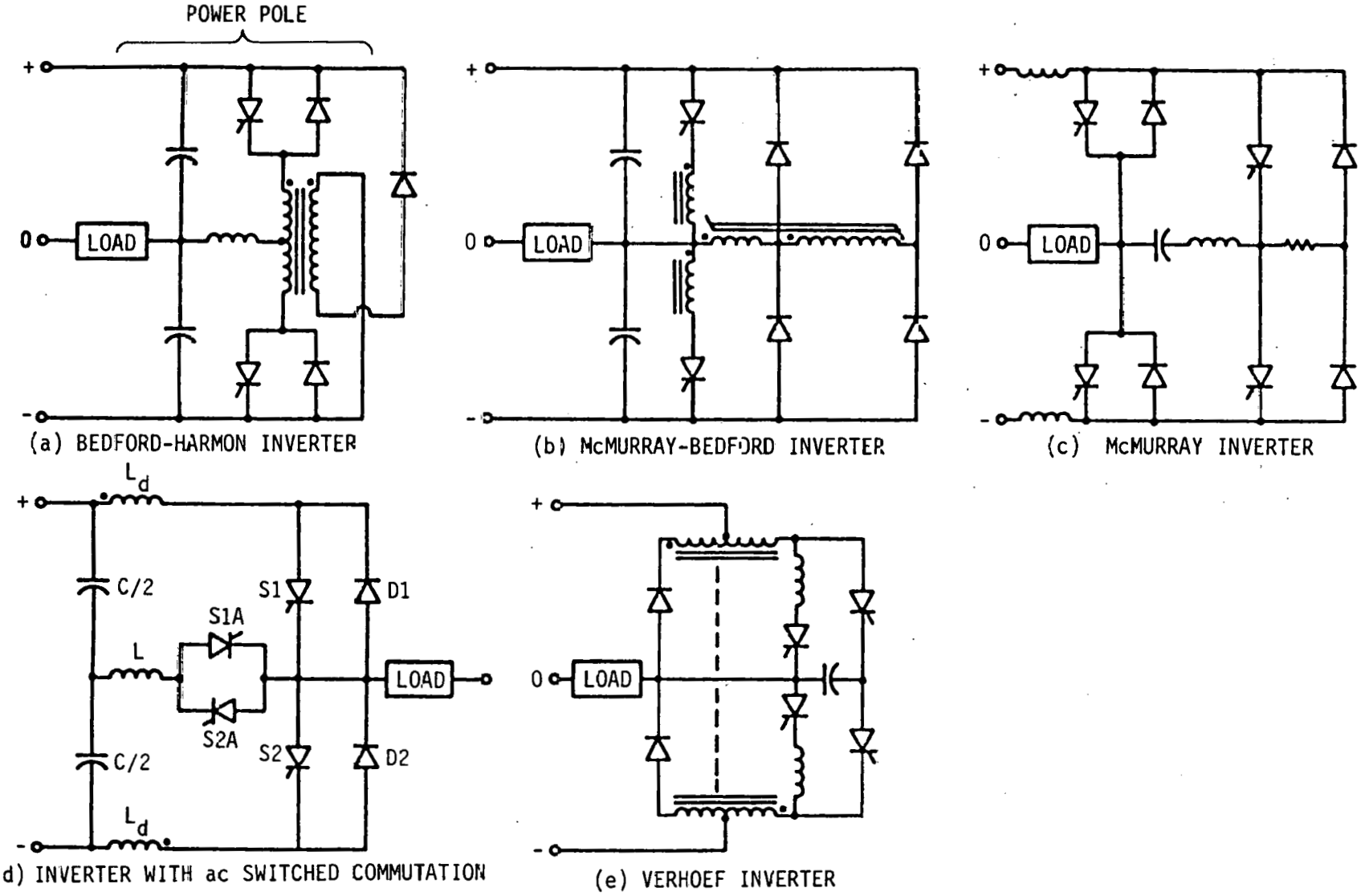


Figure 6-8. Alternate Commutation Circuits for Voltage-Fed Inverters (see Reference 6-16)

generally reflects lower reliability. As an example, the McMurray-Bedford inverter (Figure 6-8b) uses fewer thyristors than the McMurray inverter (Figure 6-8c). Table 6-1 provides a comparison of inverter circuit designs for the same duty. The object of including this table is to show that different circuit design approaches require different thyristor ratings, capacitor ratings, and inductor ratings. In addition, energy losses differ according to the design used. Increased energy loss will reduce inverter efficiency. The McMurray inverter in Figure 6-8c uses a greater number of switching thyristors but lower kVA of commutating capacitors (Table 6-1) and inductors than the McMurray-Bedford inverter in Figure 6-8b.

The inverters of Figure 6-8a and 6-8b operate on the basis that the triggering of a thyristor will turn off the complementary thyristor. This occurs from the induced voltage in the connected commutation reactor resulting from discharging of a commutation capacitor. The other three inverter poles shown use auxiliary commutaton that utilizes an auxiliary thyristor to insert a capacitor to turn off the associated power-switching thyristor.

These inverter poles are used in a multiplicity of inverter applications, including photovoltaic inverters. They can be configured for single-phase or three-phase operation. Single-phase operation may use from one to two power poles whereas three-phase operation must use at least three power poles. The McMurray inverter (Figure 6-8c) is used extensively in intermediate and large photovoltaic PCSs.

6.4 WAVESHAPING AND VOLTAGE REGULATION

6.4.1 Sinusoidal Pulse-Width Modulation (PWM)

6.4.1.1 Voltage Regulation of PWM Inverters. Voltage regulation of PWM inverters is accomplished by varying the on-to-off time of the switching power semiconductors (see Figure 6-2a). A simplied representation of this method is shown in Figure 6-9 for PWM control of a square wave. This method is applicable to the waveforms shown in Figures 6-2b through 6-2d. The average voltage for 1/2 cycle of operation of Figure 6-2b at terminals A, B, assuming no inverter losses, will be:

$$V_{AB} = V_{dc}$$

for the PWM waveform, where t_1 and t_3 are variables that change with desired output voltage. The resultant average voltage for 1/2 cycle of operation will be:

$$V_{AB} = V_{dc} \times \frac{t_1}{t_2}$$

While this discussion is for a single-phase bridge inverter, it is also applicable to a three-phase inverter.

Table 6-1. Comparison of Inverer Circuit Designs for Same Duty (see Reference 6-6)

Circuit	Bedford Harmon	McMurray Bedford	McMurray	Transformer Verhoef	Transformer Coupled
Total commutating capacitance, μF	275	266	56.8	81	105
Total dc inductance, μH	29.8	55.3	2.95	10.5	47.3
ac (or di/dt limiting) inductance, μH	0.895	(0.85)	2.95	(4)	1.58
Time for worst necessary commutation, μs	349	414	66.8	60.0	381
Time for worst redundant commutation, μs	48.8	523	69.2	91.5	0
Peak thyristor current, A	2097	2155	1754[a]	1217[a]	1667[a]
Peak main thyristor voltage, V	568	568	480	460	790
Peak auxiliary thyristor voltage, V	---	---	560	860	615
Max trapped energy, J	17.9	26.6	0.74	0	17.6
Max inevitable loss, J	2.31	0.47	0.74	0	0
Max energy in inductance, J	9.1	32.1	4.54	9.06	8.3
Max total extra I^2t in reactor windings, A^2s	580	943	---	165	[b]

[a] In auxiliary thyristor.
[b] Probably about the same as in the Bedford-Harmon circuit.

6.4.1.2 Analog Voltage Pulse-Width Modulation. Figure 6-10 shows a technique of analog PWM waveform generation. A symmetrical triangular timing pulse is compared to a sinusoidal reference at 60-Hz utility system frequency. Power switching occurs when the sine wave intersects the triangle wave, thereby producing the PWM waveform. These waveforms shown in Figure 6-10a are for the respective power poles of a two-power pole inverter (see Figure 6-2a). The harmonic content of the output waveform is a function of the frequency of the triangular timing pulse. High switching frequency consistent with good semiconductor utilization provides a minimum output filter. The resultant ac output waveform of the power poles of Figure 6-2a is shown in Figure 6-10b. PWM voltage regulation can be provided as described in Section 6.4.1.1 (References 6-19 and 6-20).

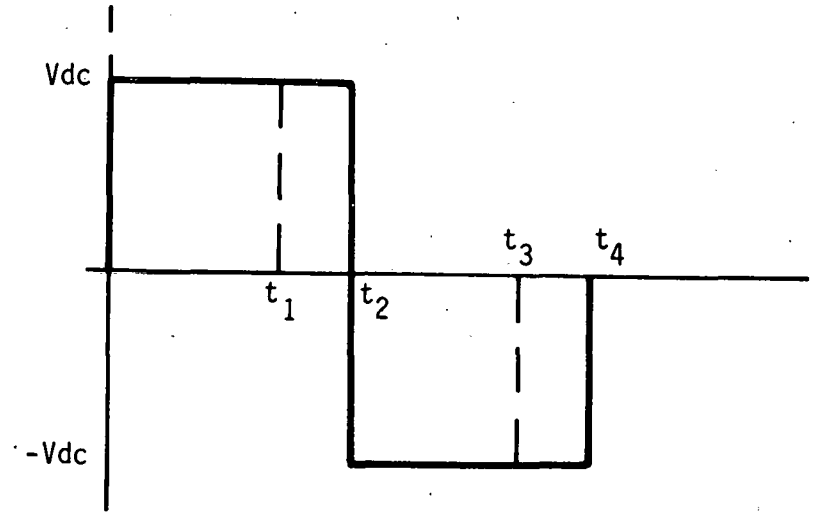


Figure 6-9. Voltage Control Pulse-Width Modulation (PWM)

6.4.1.3 Digital PWM (Programmed Waveform). Figure 6-11 shows a programmed waveform technique used for waveform generation (see References 6-13 and 6-19). The waveform shown is for a single power pole. The resultant inverter output of a two-pole, single-phase inverter would be the effective differential output of the two-power poles. The description of waveform generation is similar to that of the analog PWM generation with the exception that the reference sine wave is replaced with a digitally synthesized waveform reference. The digitally synthesized pattern of positive and negative pulses is stored by usage of large-scale integrated (LSI) circuits such as the programmable read-only memory (PROM). These pulses are selected to eliminate unwanted low-order harmonics. Again, because the digitally derived waveform approximates a sine wave due to the elimination of low-frequency harmonics, minimum output filtering is required. With the large-scale integration (LSI) for waveform generation and control and the availability of high-speed transistors, thyristors, and GTOs for power switching, the digitally PWM method offers many advantages. This technique is used in all sizes of inverter systems. The advantages of PWM systems are in filter and magnetic component reduction, allowing for process-intensive inverter designs that are cost- and performance-effective. Programmed waveform generation inverters can run at frequencies of one-third to one-tenth of the analog PWM inverters. As a result, many advanced technology inverter systems will use the programmed waveform inverter approach.

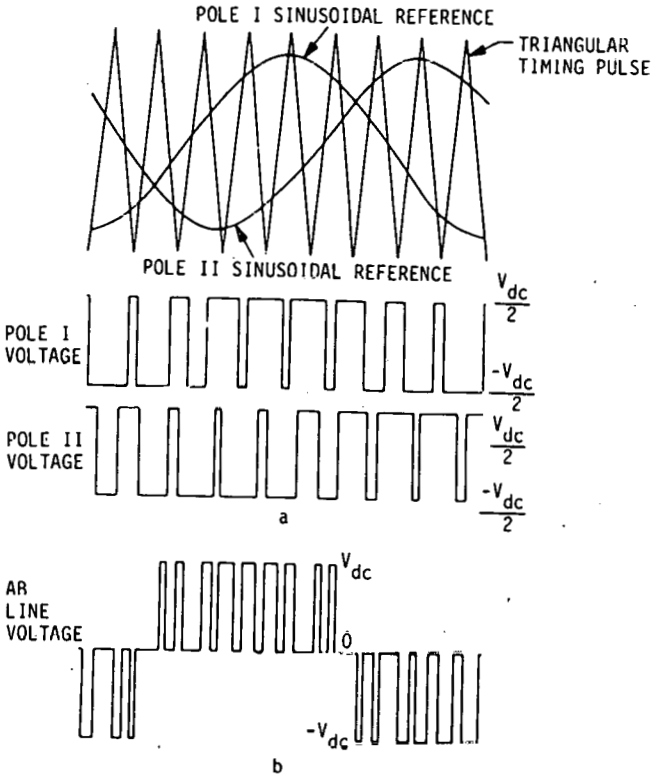


Figure 6-10. Sinusoidal Analog Pulse-Width Modulation (PWM) (Reference 6-9)

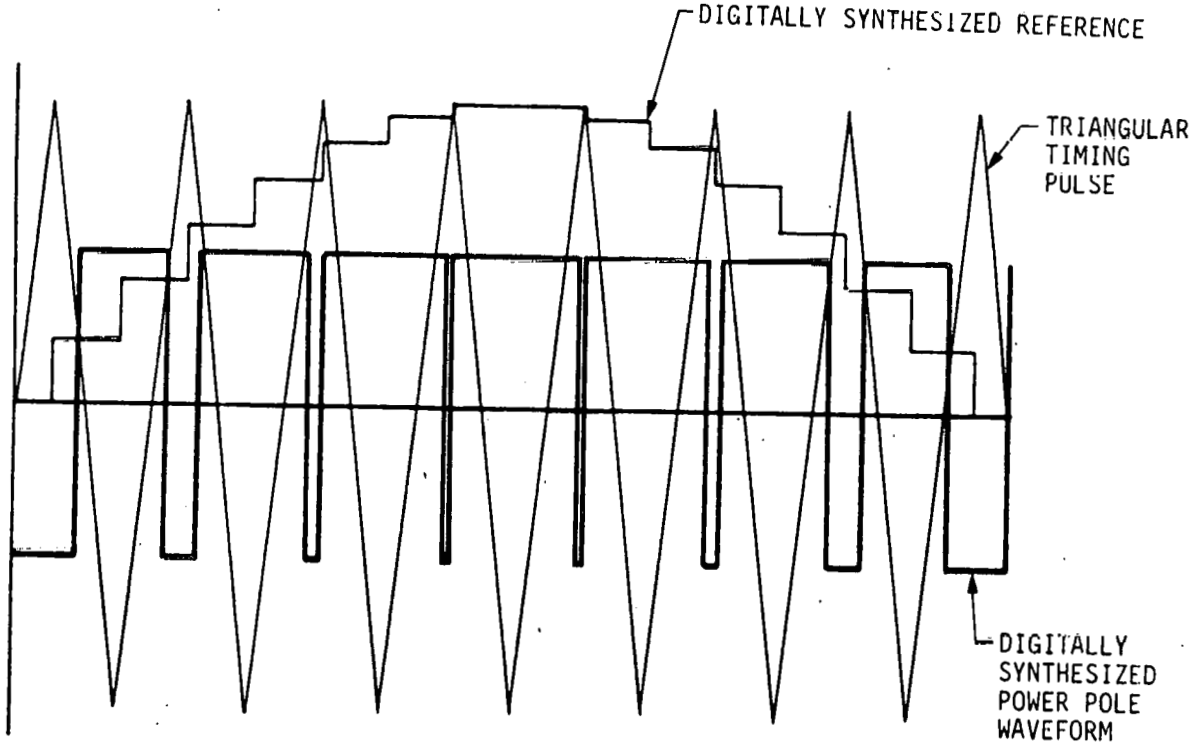


Figure 6-11. Sinusoidal Digital Pulse-Width Modulation (Reference 6-6)

6.4.1.4 Current-Band, Pulse-Width Modulation. Current-band, PWM control, sometimes called current-programmed mode, is shown in Figure 6-12. In the current-band, PWM control, a reference signal that is internally generated and is a composite of the desired load current is compared to the sensed-load current. When the difference between the sensed-load current and generator signal exceeds the control-band limits, the power semiconductors are switched as required (see Figure 6-2). Inverter switching keeps the load current within the sinusoidal required output and control-band limits. Switching occurs whenever the load current reaches the control-band limits. This method provides peak-current or fault-current sensing that can provide instantaneous power semiconductor protection (see References 6-10 and 6-15).

6.4.2 Synthesized-Waveform Inverters

6.4.2.1 Stepped-Waveform Inverter. Figure 6-13 shows a basic six-pulse thyristor inverter. The switching elements may also be transistors or GTOs. The switch firing order and resultant output voltage waveforms are shown. The output line-to-line voltage has no harmonic voltages that are multiples of the second and third harmonics. Waveform harmonic content is shown in Table 6-2 with the first harmonic being the fifth. This type of inverter is commonly used for ac motor control and may be used for photovoltaic systems by the addition of output ac filters similar to that shown in Figure 6-5. Voltage control may be accomplished by PWM control.

6.4.2.2 Multiple-Step, Waveform Inverters. With the use of two six-pulse inverters (see Figure 6-13) that are phase-shifted, improved harmonic output waveform and voltage regulation are possible. This method is shown in Figure 6-14 wherein two three-phase stepped inverter are phase shifted 30 deg from each other, each producing output waveforms as shown in Figure 6-13 (see References 6-16 and 6-21).

This waveform will have no harmonic components that are multiples of the second, third, fifth and seventh (harmonics = $12n \pm 1$ $n = 1,2,3 \ldots$). The first harmonic component will be the eleventh. Voltage regulation is accomplished by adjusting the phase relationship between the two stepped waveform inverters. Because voltage control increases the harmonic content of the output voltage, output filters or increased numbers of stepped-wave inverters may be used for harmonic reduction. An example of this is shown in Section 7, Figure 7-25. In this figure, 12 power poles are used and stepped for harmonic reduction. They are phase-shifted to provide voltage regulation.

There are numerous alternate methods of stepped waveform synthesis, one of which is shown in Figure 7-24 (see Reference 6-4). In this figure, 3 three-phase bridge inverters are used that are phase-shifted 20 deg from each other for harmonic reduction. Voltage control is accomplished by PWM (Reference 6-22).

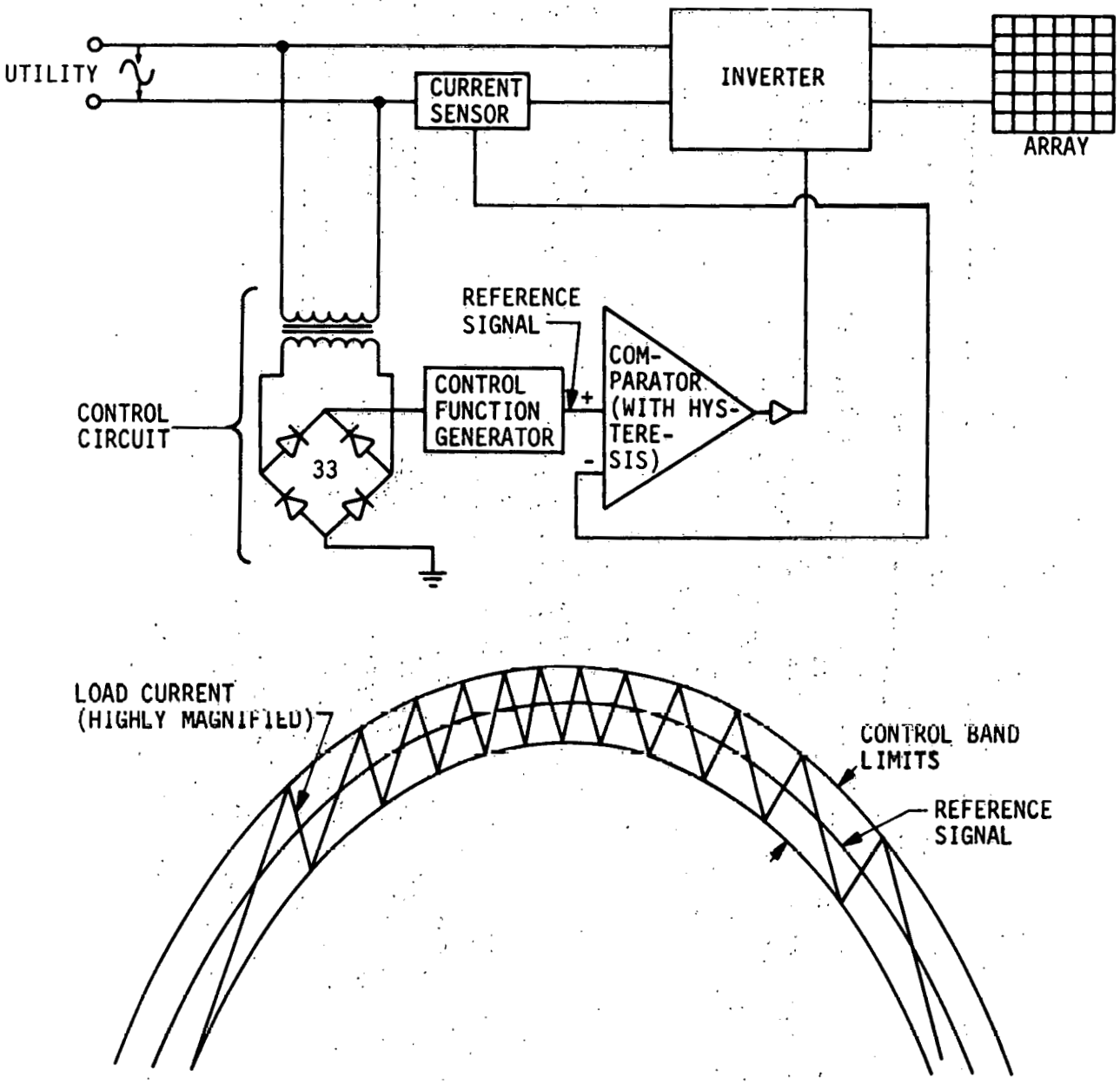


Figure 6-12. Principle of Current-Band, Pulse-Width Modulation Control (see Reference 6-10)

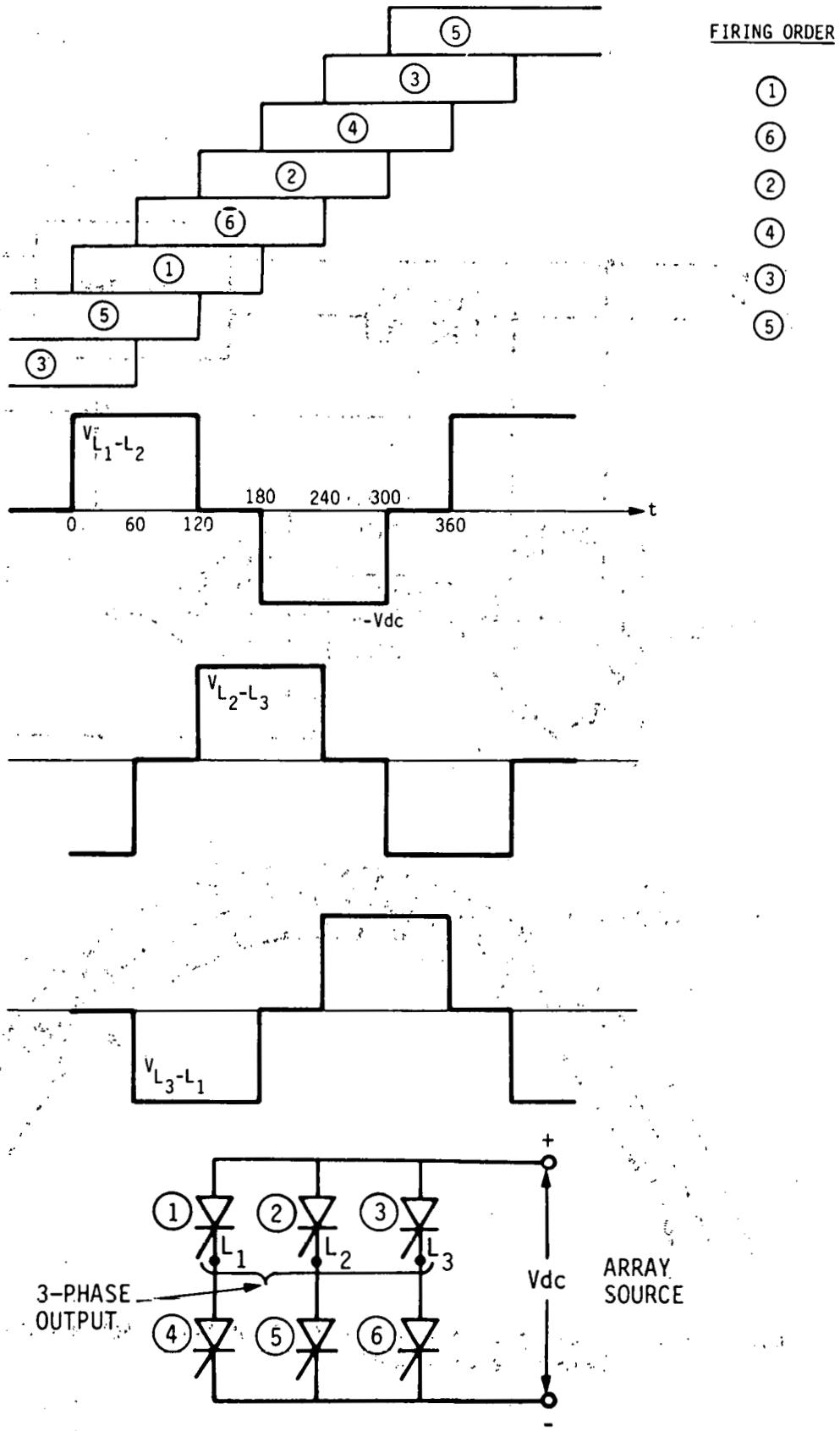


Figure 6-13. Synthesized Waveforms of a Three-Phase, Six-Pulse Inverter

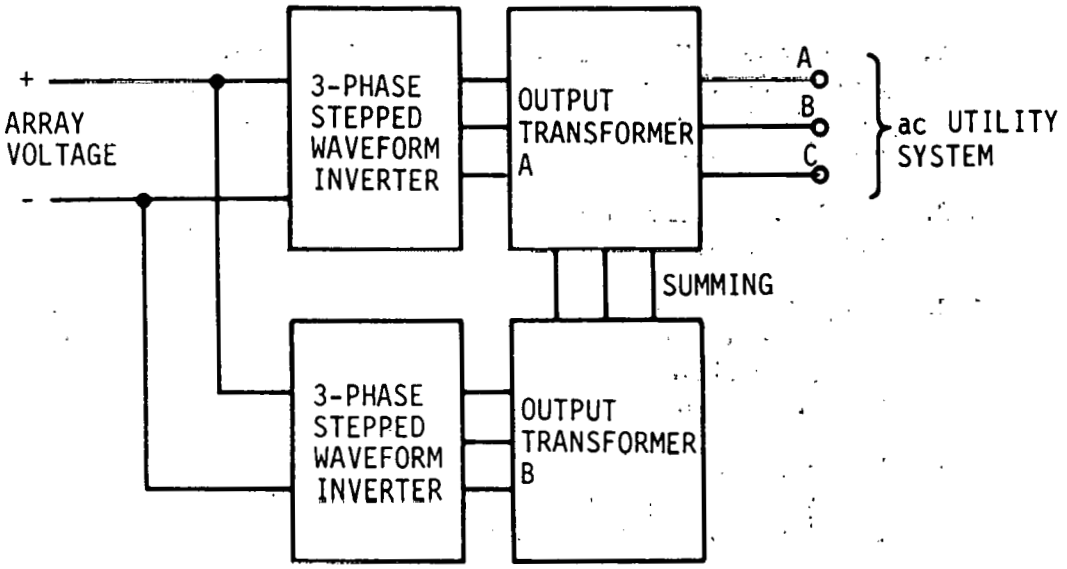


Figure 6-14. Block Diagram of a Stepped Waveform Inverter

Table 6-2. Waveform Harmonic Content

Harmonic	Percent
5	20
7	15
11	9
13	8
Total	30.9

[a] Harmonics = $6n \pm 1$, $n = 1,2 \ldots$

[b] $\text{Percent} = \frac{100}{\text{Harmonic}}$

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SECTION 7

CHARACTERISTICS OF STATE-OF-THE-ART AND ADVANCED POWER INVERTER TOPOLOGIES

Various topologies of inverters that are available for application in PV systems are discussed in this section. The topologies reviewed were selected out of a pool of the commercially available, breadboard-proven or only conceptually conceived inverter circuits. The selected circuits are reviewed in order of the deliverable power, i.e., according to kilowatt size (small, intermediate, and large) and are generic in nature. Appendix C provides a matrix of PCS manufacturers, characteristics, kW sizes, performance, efficiencies, and costs. The sizes detailed are from small to large units.

Two different types of inverters are being used in utility interactive photovoltaic power conditioners: line-commutated and self-commutated. There are advantages and disadvantages in both types of systems. Both systems can be designed to provide a somewhat comparable performance.

Most line-commutated systems without output filters have low power factor ratings and inject high levels of harmonic currents into a utility system. Line-commutated inverters with comparable performance to self-commutated inverters generally require output filters that approximate a large percentage of the kVA rating of the power conditioner. The effect of these large filter elements and harmonics on a utility system under heavy PV penetration levels is presently unknown.

The most effective inverter will be determined by costs, performance, and efficiency tradeoffs. The marketplace will ultimately determine which is the preferred design.

7.1 SMALL INVERTERS (1 to 15 kW)

Small inverters are residential-size units intended to link the solar source with the utility for the parallel system operation. Ratings of the units do not exceed 15 kW. Inversion is single-phase, with ac output of 240 V.

There is a strong trend toward the use of transistors instead of thyristors for power switching; however, some thyristor inverters are still being produced and installed. Emergence of the GTO thyristor has created new opportunities that are beginning to be exploited. Selected configurations will be reviewed.

7.1.1 Transistorized Single-Bridge Inverter (see Section 6.3.1)

Figure 7-1 shows a typical transistor-bridge inverter (References 7-1, 7-2). Each of the power switches (Q1 through Q4) consists of two

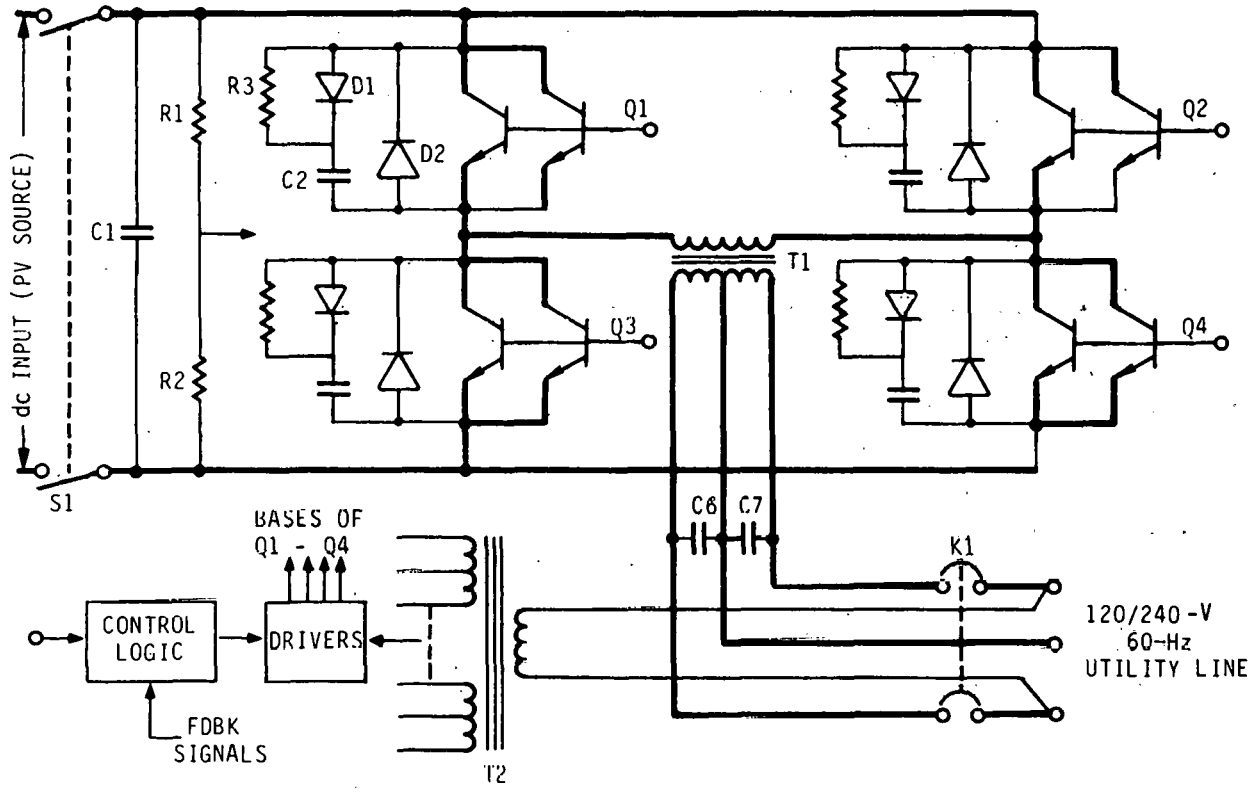

Figure 7-1. Single-Phase Transistor Bridge Inverter

parallel-connected power transistors. An output power transformer, T1, is used to match the dc-source voltage level to the utility voltage level and provides electrical isolation between the two sources.

Inverter circuitry can be electrically isolated at both ac and dc interfaces by disconnect, S1, and contactor, K1. Auxiliary transformer T2 powers the control logic and drives of the power transisors. Power transformer T1 isolates the array and inverter from the utility line.

Fast switching power transistors permit use of high-frequency modulation (see Reference 7-1 and Section 6.4), such as pulse-width modulation (PWM) or digital PWM for the purpose of generating a nearly sinusoidal current. To produce the 0- to 180-deg section of the 60-Hz waveform, Q1 will stay fully on and Q4 will alternate on and off at a high repetition rate.

The on-to-off-time duty cycle of Q4 will vary as shown in Figure 7-2 during this interval. At zero or small angles, the duty cycle is low. The duty cycle increases until a maximum duty cycle is reached at 90 deg; then the duty cycle decreases until it reaches minimum at 180 deg. The process is repeated wherein Q2 stays full on and Q3 is alternately turning on and off at high modulating frequency to form the 180- to 360-deg section of the 60-Hz waveform.

Choice of the modulating frequency varies from one design to another. For example, modulating at 540 Hz or at 9 x 60 Hz eliminates all odd harmonics below the 9th; thus, the 3rd, 5th and 7th harmonics are suppressed. Modulation at 3060 Hz (51 x 60 Hz) eliminates all harmonics below the 51st. In all cases, due to circuit imperfections, total elimination is not always achieved.

The higher the modulating frequency the greater are the switching losses. On the other hand, the higher the modulating frequency the less filtering is required. For example, in the case of the bridge inverter shown in Figure 7-1, where relatively high frequency is used for PWM, the output filtering is accomplished by using the leakage inductance of the T1-transformer and capacitors C6 and C7 to create the low-pass filter suppressing the high-frequency harmonic currents.

A single-bridge inverter using four power transistors can presently handle only about 4 to 5 kW of power. Higher power rating can be achieved by paralleling transistors. Paralleling of the bipolar junction transistors (BJTs) presents some problems, as discussed previously. Although paralleling of individual bridges is feasible, it is cumbersome because forcing two bridges to share the power equally requires additional provisions within the logic configuration. A typical commercially available unit that operates in excess of 2,000 Hz delivers 4 kW and requires minimum ac harmonic filtering.

An example of the PCS ac output is shown in Figure 7-2. E_{ac} is the programmed pattern ac output voltage, and V_{ac} is the PCS output voltage. The difference in the two waveforms is the filtering action of the built-in inductance in the transformer T_1 and output capacitors C6, C7 (see Figure 7-1). ϕ_{ac} is the phase relationship between the generated patterned waveform and the PCS output voltage.

7.1.2 Transistorized Dual-Bridge Inverter (see Section 6.4.1.3)

The two-bridge configuration (Figure 7-3) provides an interesting concept: the two ac outputs are connected in series rather than in parallel. This forces the output currents of two bridges to be equal; therefore, two bridges share the demand equally (see Reference 7-1).

The PV source dc input is connected to two bridges that are connected in parallel. On the output side the ac power from each bridge output is delivered to the primaries of two identical transformers. Each transformer has two separate secondaries. Two sets of secondaries are connected in series, each providing a 120-V output. Jointly they yield an output of 240 V.

The wave pattern applied to the bases of the individual transistors (see Figure 7-3) is shown in Figure 7-4. It is the case of a multi-pattern PWM. The wave pattern A-B represents the waveform at the output terminals of the first bridge, where the pattern C-D identifies the output of the second bridge. These two patterns also differ. The series-connected transformer secondaries add these two patterns (A-B) + (C-D), offering a symmetrical replica of a sinusoidal waveform perturbed by the harmonics.

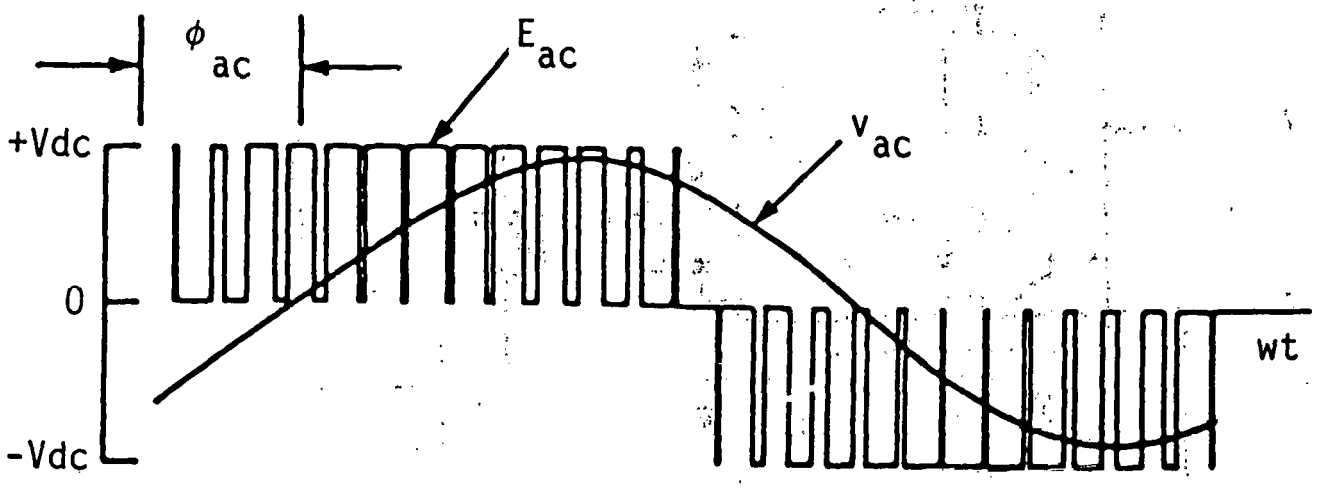

Figure 7-2. Relationships Between E_{ac}, V_{ac} and $_{ac}$

These patterns are not fixed; they continuously vary under influence of the two servo loops. The first loop controls the phase angle relation between the utility's line voltage and the current delivered by the inverter into the line. They should be in phase. To achieve that, the line voltage and line current are fed into the logic, where their phase-relation is identified. In a case when they are not in phase, the phase angle generates an error signal that causes the timing of the pulses to be modified, until a zero error is achieved.

The second loop controls the dwell time between the individual high-frequency pulses. Increasing the dwell time causes a decrease in the amplitude of the composite voltage waveform of Figure 7-4 and results in the reduction of the amplitude of the line current.

7.1.3 Gate Turn-off, Half-Bridge Inverter

Use of gate turn-off (GTO) thyristors climinates the need for paralleling the power transistor switches. It is possible to build 10-kW, residential-size inverters of the configuration shown in Figure 7-5, using two GTO switches (see Reference 7-2).

The GTO half-bridge inverter (see Figure 7-5) may offer a cost-saving option. Two GTOs are used to switch output line Y from positive to negative, while the line X remains at a constant, half-voltage level. This results in an ac waveform across points X, Y.

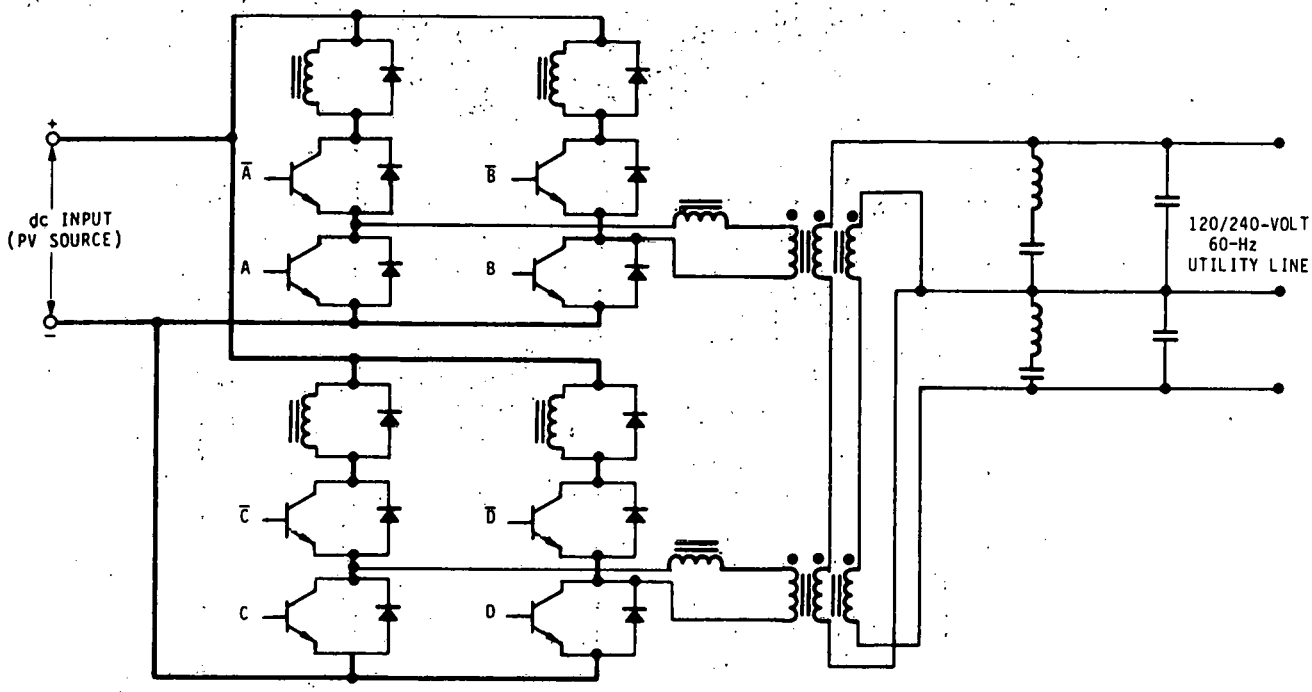

Figure 7-3. Transistorized, Dual-Bridge Inverter

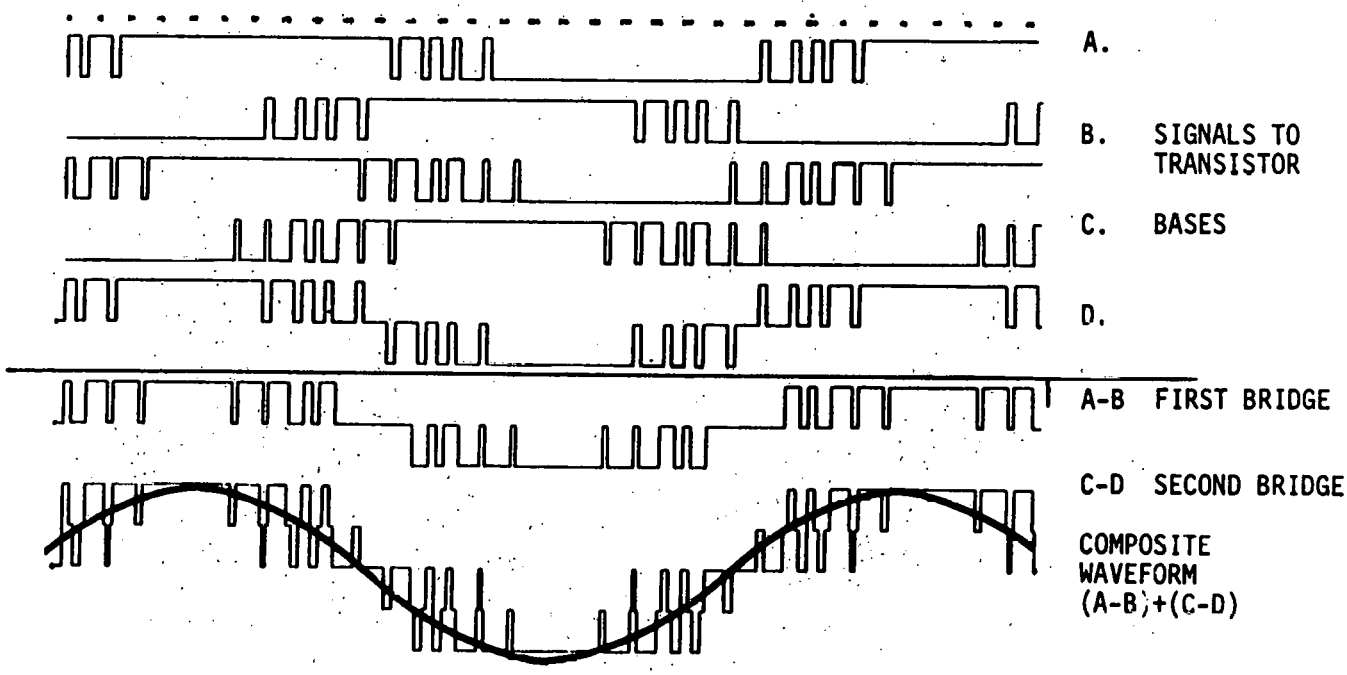

Figure 7-4. Wave Pattern of a Dual-Bridge Inverter

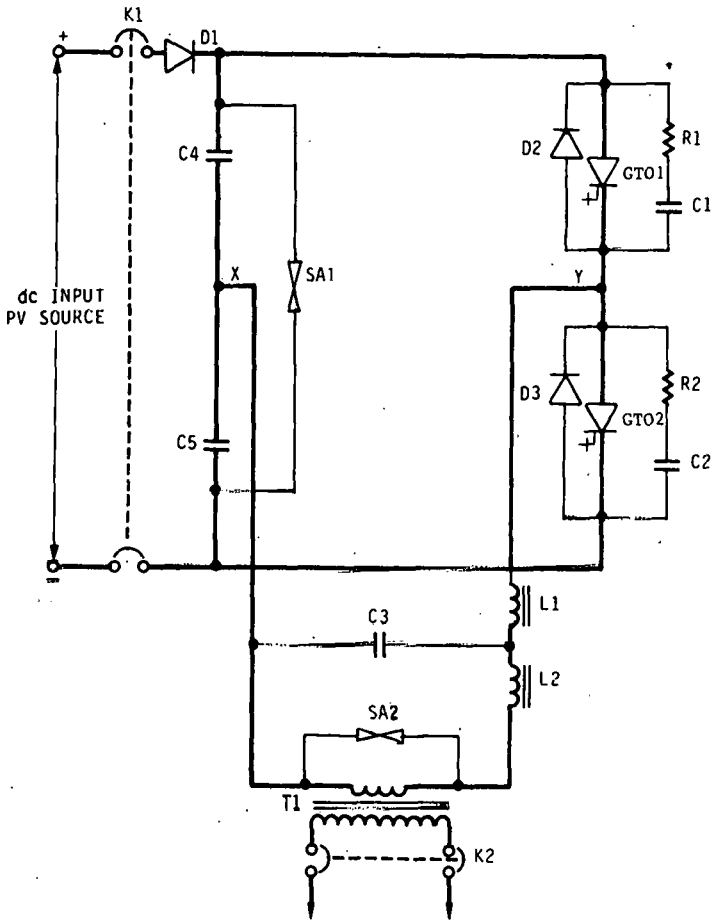

Figure 7-5. Conceptual Design for a 5-kW Unit

Because the voltage swing between points X and Y is reduced to the half value (point X is at 1/2 of the array voltage) of that of the full-bridge version (see Figure 7-1), for the same value of the power ratings each of the GTOs carries twice the current of the transistors (Q1 through Q4 in Figure 7-1). The existing sizes of the GTOs can comfortably handle the required currents.

The GTO, half-bridge circuit of Figure 7-5 would require higher current GTOs compared to full-bridge circuit.

Pulse-width modulation used in Figure 7-2 or the multipattern PWM of Figure 7-4 can be used for the logic of the GTO inverter. Because the GTO thyristor switching time is slower than the equivalent power transistor, the modulating frequency of this configuration may have to be lower than in the previous cases. Reduction of the modulating frequency, where GTOs are used, will result in some additional harmonic currents that must be filtered out. An output filter (L_1, L_2, C_3), shown in Figure 7-5, takes care of this requirement.

7.1.4 High-Frequency Link Utility Interactive Inverter (see Section 6.4.1.4)

The configuration of Figure 7-6 offers a promise for improving the overall conversion efficiency, reducing the overall unit size, and reducing the overall manufacturing cost (Reference 7-3). This improvement occurs due to major size and cost improvement due to the reduction in the isolating transformer T_1, compared to a 60-Hz output transformer. This is accomplished by operation of the inverter at high frequencies above the audible band.

The power converter consists of a high-frequency inverter (Q1-Q4); a high-frequency power transformer; a dc rectifier (D1-D4); and a utility-interactive, transistor self-commutated power inverter (Q5-Q8). Microprocessor logic is utilized to generate a sinusoidal current and provide the required control functions.

A power circuit block diagram is shown in Figure 7-7. Also included are the computer-generated, simplified current and voltage waveforms along the signal transmission path.

The operation of the PCS can be summarized as follows: The high-frequency current mode PWM-inverter (see Figure 7-6) generates high-frequency voltage pulses modulated with a 60-Hz sinusoidal wave. This voltage, after being rectified, is inverted and used to feed the ac power into the utility lines. The line current (Figure 7-8) exhibits a high-frequency ripple that is attenuated by filtering after high-frequency rectification.

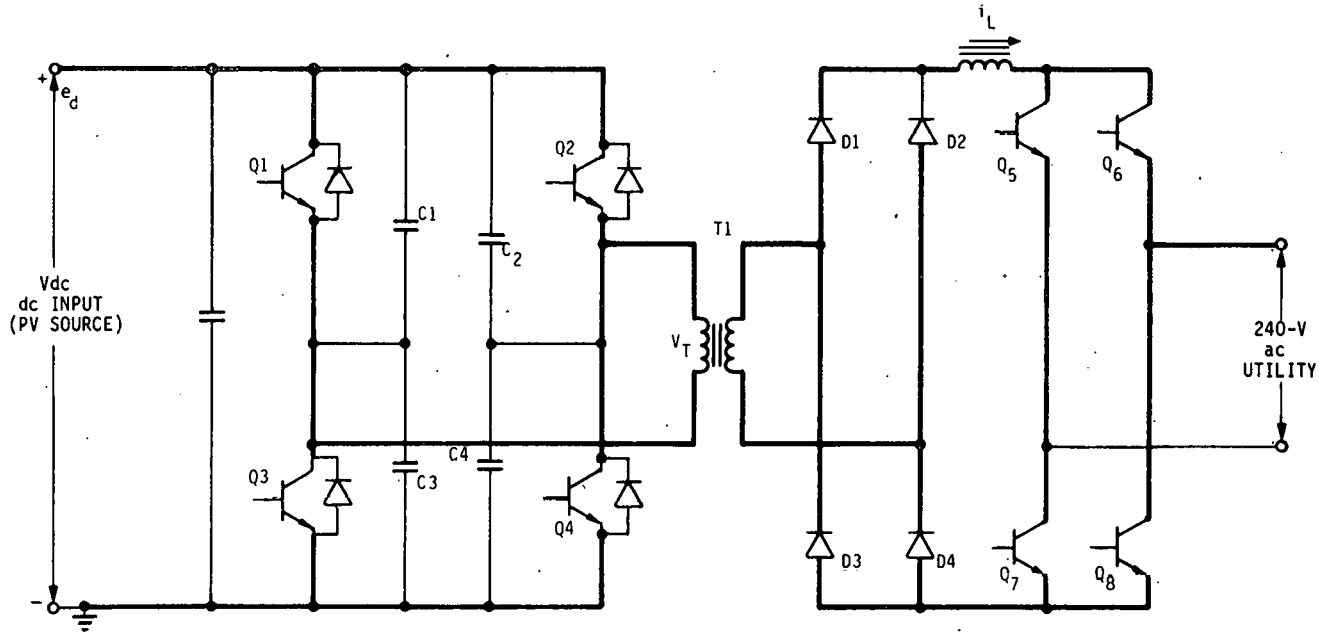

Figure 7-6. Utility Interactive Power Converter with a High-Frequency Transformer Link

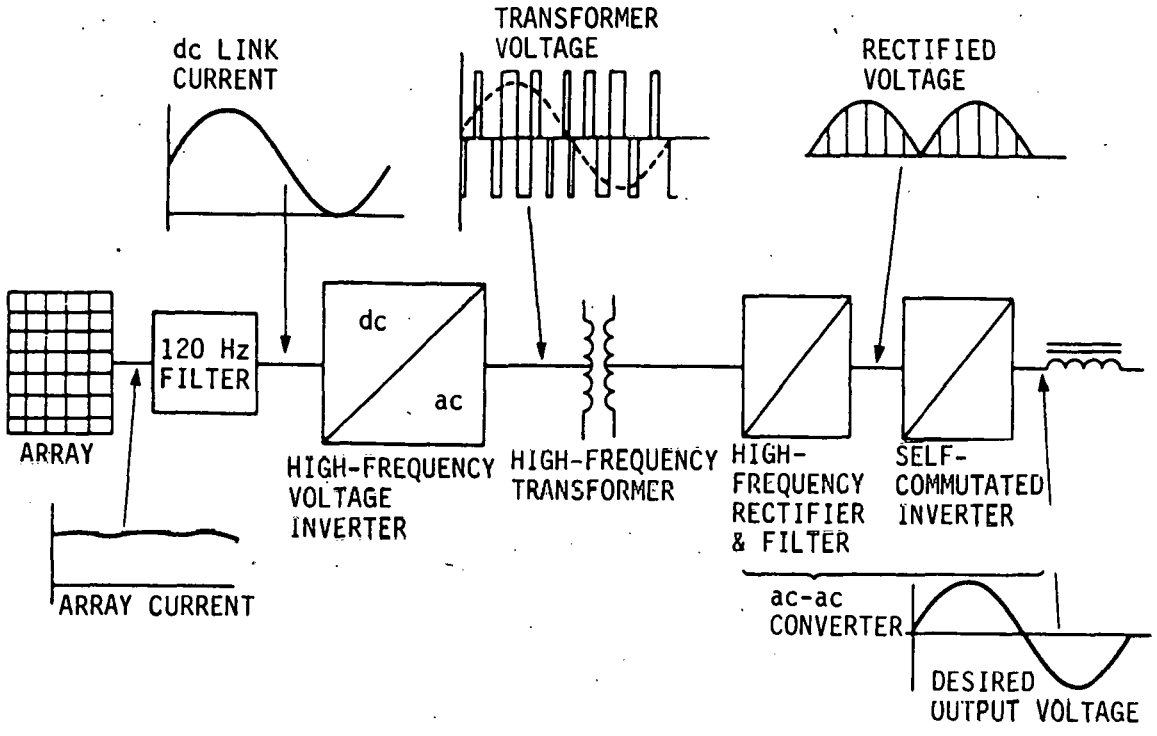

Figure 7-7. High-Frequency Link with Controlled Voltage (see Reference 7-3)

If a major component failure occurs in the utility tie inverter (Q5-Q8), then the high-frequency PWM inverter Q1-Q4 will instantly electronically turn off. The utility tie contactor is then actuated, and the system is electrically disconnected both from the array and the utility. The system will also turn off if, during a fault, dc current is injected into the utility system.

7.1.5 Thyristor Bridge, Line-Commutated Inverter

The line-commutated inverters belong to the family of current-fed inverters (see Section 6.3.4). They are characterized by a high input source impedance, consisting of a L-C half section filter. The inverter is a current-fed, line-commutated type. The inverter behaves as a current source. The voltage at the output terminals is proportional to the driving point impedance looking into the terminals of the utility (Reference 7-4).

Inverters of this type use thyristors for switching power. No special inverter commutation circuitry is required because the utility voltage is used to extinguish the thyristors, thereby simplifing the circuitry considerably. A major deficiency of this inverter is the inability of wave shaping by means of high-frequency modulation. Because pulse modulation is not feasible, the current waveform contains considerable harmonics that must be removed

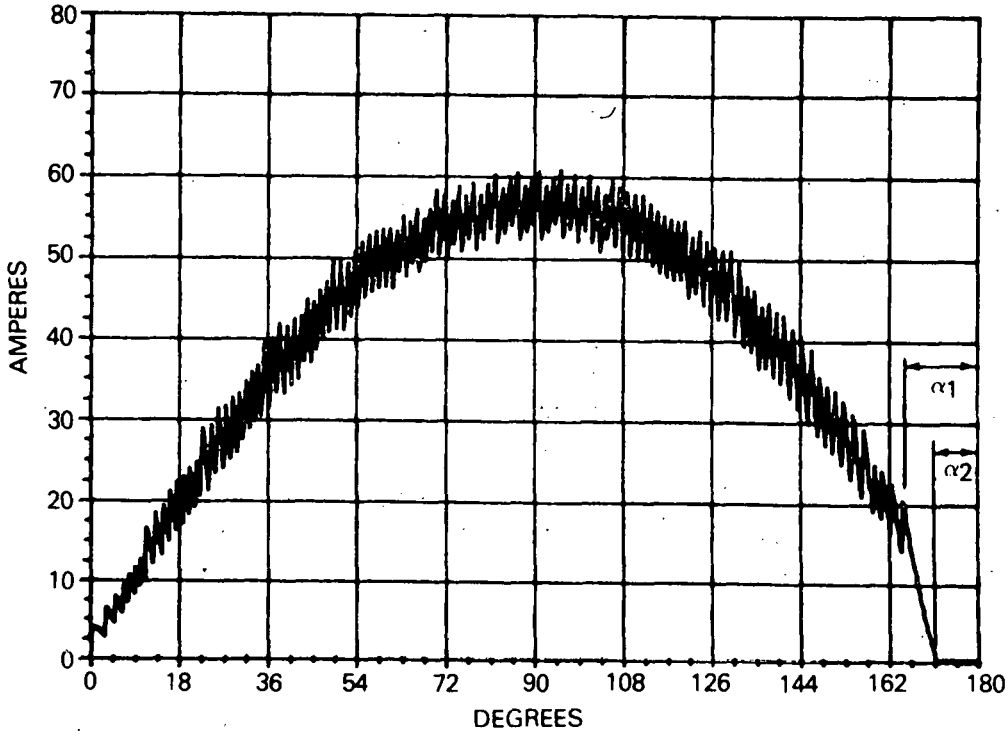

Figure 7-8. Line Current for a 4-kW Inverter (see Reference 7-3)

by filtering, thereby raising the overall cost. Furthermore, the value of the power factor (PF) varies with the load, becoming rather poor at lighter loads (Figure 7-9). The power factor and harmonics levels are also affected by array voltage levels and utility voltage levels.

It is possible to improve the power factor by means of the ac line capacitors. The dashed line of Figure 7-9 shows the improvement obtained by means of a large-size capacitor. If correction of the PF is necessary, the parts count and cost rises. A typical inverter configuration is shown in Figure 7-10. Four power thyristors, SCR1 through SCR4, form a single-phase bridge. They are fired by pulses derived from the logic and turned off by the back electromotive force of the utility line.

The input filtering is accomplished by L1 - C1, which suppresses the even harmonic currents and prevents them from circulating in the PV array. It should be noted that excessive ripple will reduce the array energy efficiency. The L2, C2 trap at the output may be used to filter the third-harmonic currents and provide power factor correction. The ac-line choke L3 provides additional filtering of the waveform of the current delivered to the utility and may be used to limit utility current and notching during commutation.

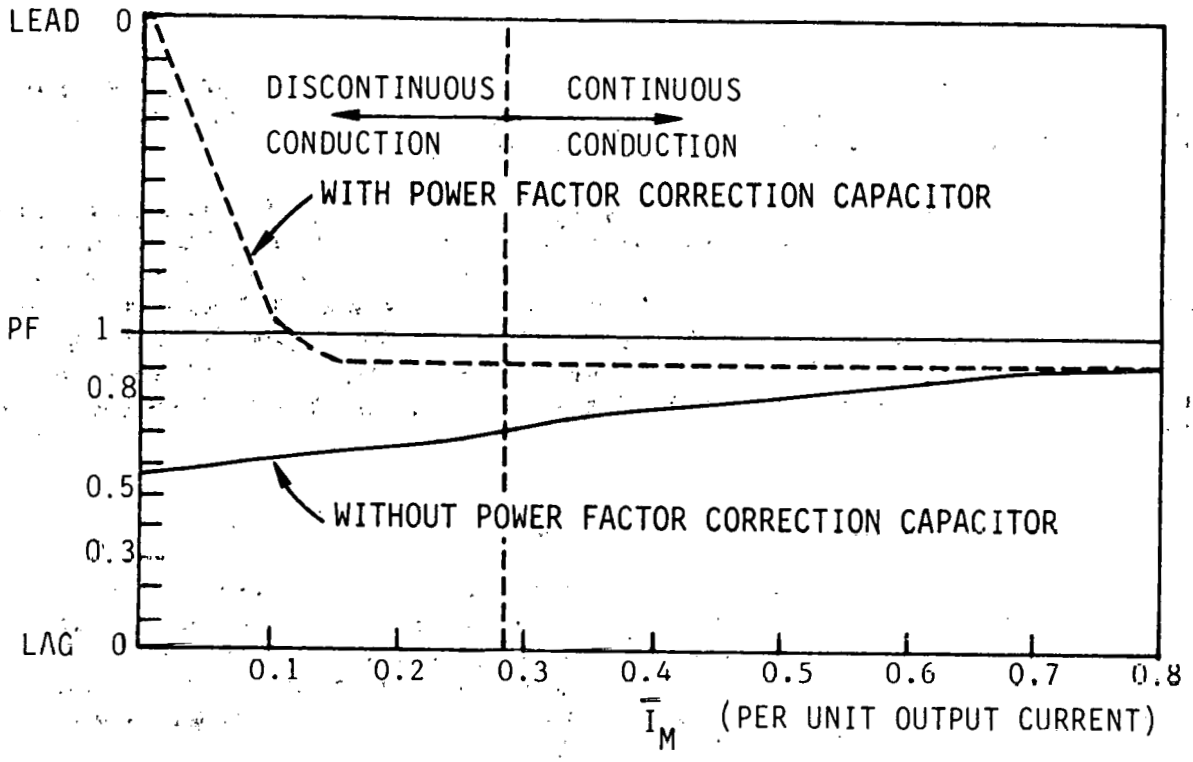

Figure 7-9. Power Factor versus Per-Unit Output Current

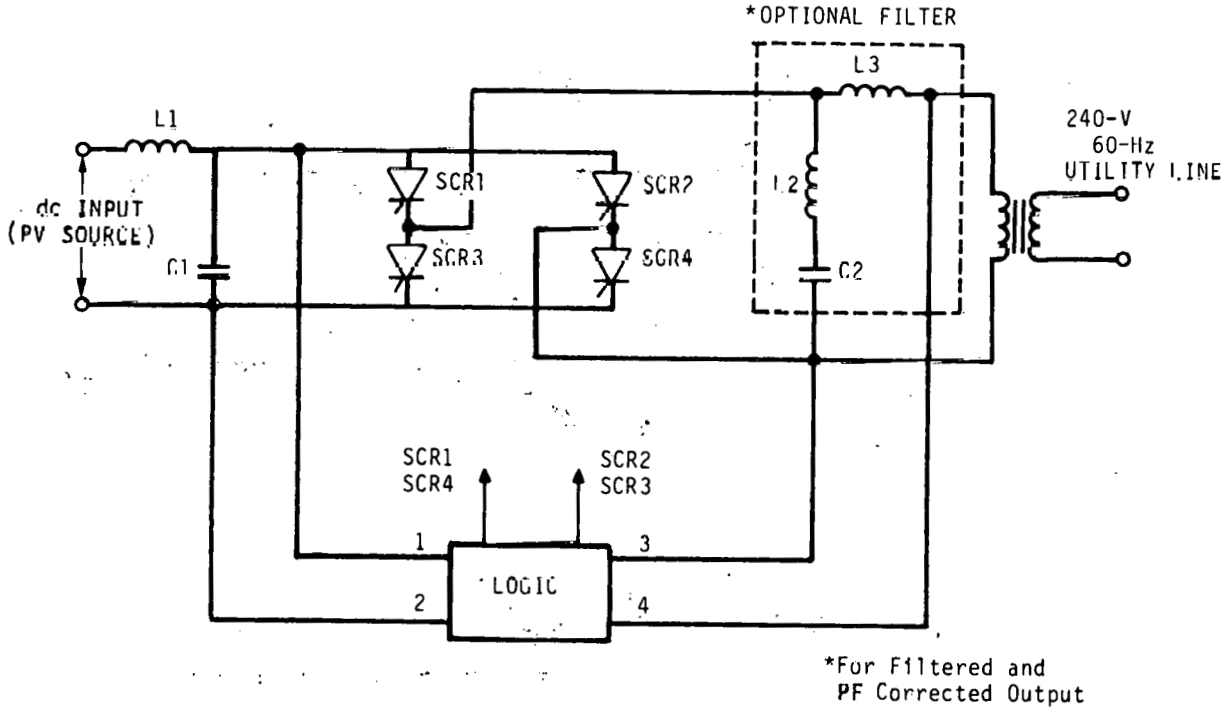

Figure 7-10. Diagram of a Line-Commutated Single-Phase Thyristor Inverter

The waveform of the output current changes with changes of the source voltage, utility voltage, and loading. When the optional filter (see Figure 7-10) is used, the current waveform is improved.

Figures 7-11 and 7-12 show typical waveforms of a standard line-commutated inverter without an output filter. The waveforms shown are the line-voltage, ac line current and dc line current. It should be noted that there is considerable ac line current waveform difference between that shown in Figure 7-11 at full load and Figure 7-12 at 25% load. An indication of harmonic current levels for a particular unit is shown for a design with an input dc voltage of 200 V, input inductor 0.012 H, and output inductor 510 μH (Table 7-1).

7.1.6 dc/dc Converter Controlled Transistor Bridge Inverter

The deficiencies of the line-commutated, unfiltered inverter configuration described above, i.e., a poor wave shape of the output current and a poor power factor, can be overcome by introducing a front-end modulation of the dc power delivered to a self-commutated power inverter using transistors in the output bridge. This concept of power conversion is performed by a high-frequency chopper (see Reference 7-3).

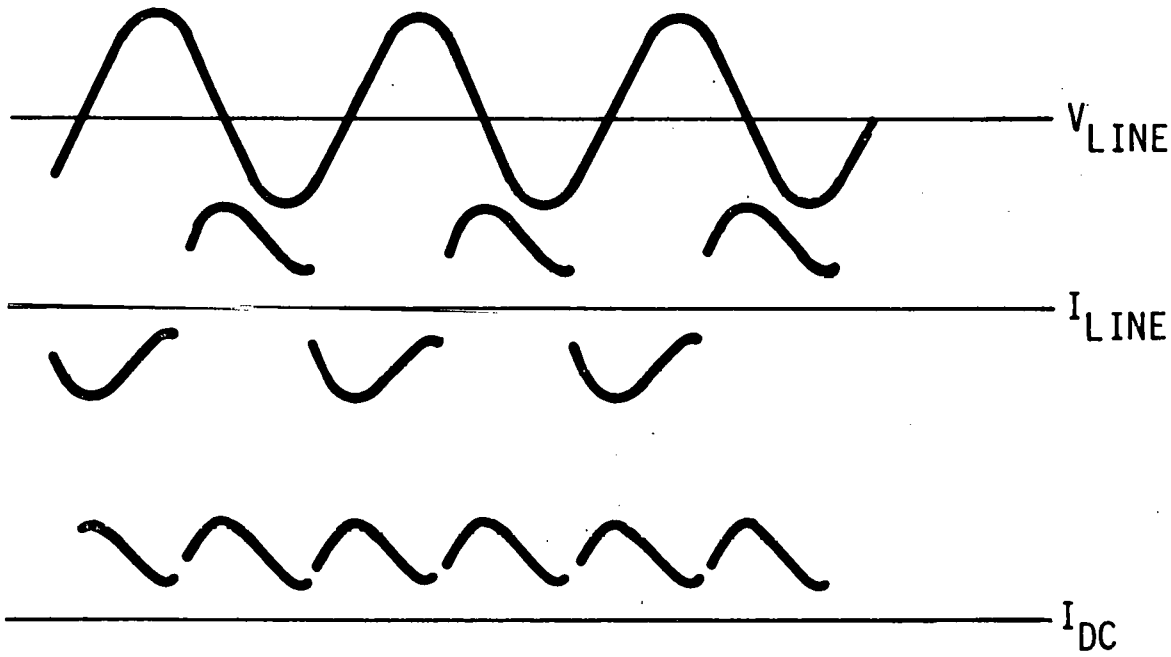

Figure 7-11. Typical Line-Commutated Inverter at Full Load

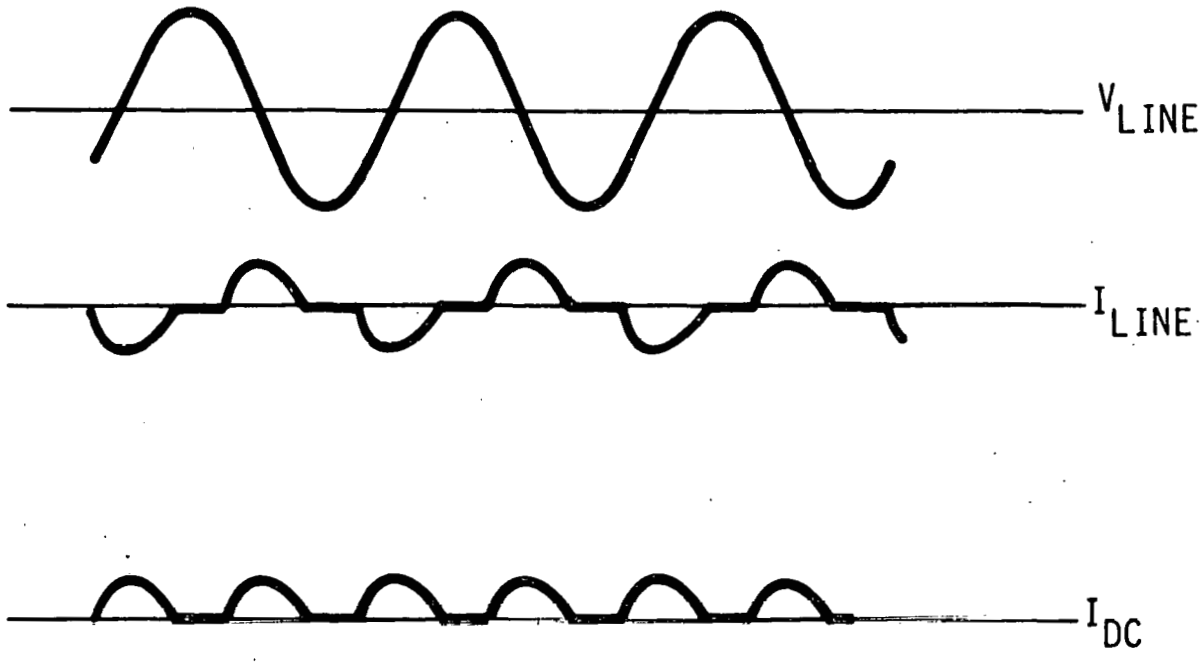

Figure 7-12. Typical Line-Commutated Inverter at 25% Load

Table 7-1. Harmonic Current Output for Line-Commutated Inverter

Frequency	Amperes
60	41.0
180	7.8
300	4.2
420	2.9
540	2.2
660	1.8
780	1.5
900	1.3

Several approaches of the dc/dc converter-inverter configuration are feasible. One of the available approaches is shown in Figure 7-13.

To produce the 0- to 180-deg part of the 60-Hz current waveform, the transistors Q2 and Q5 are turned on by energizing their bases. Also, at the same time, the base drive is applied to transistors Q1. The flow of current is initiated. Starting of the current flow is synchronized with the line voltage zero crossing to keep them in phase and create a unity power factor source.

The high-frequency is performed by a transistor chopper Q1. Q1 pulse width modulates the dc voltage which, with the aid of L, generates unidirectional half-sinusoidal current pulses (see Figure 7-13).

It should also be mentioned that thyristors in place of transistors (Q2 - Q5) may be used for dc-to-ac inversion. Thyristor inversion for this application has limited use under narrow utility voltage range.

Transistors Q2 - Q5 invert these unidirectional sinusoidal current pulses into full-wave ac current. The amplitude of the output current is controlled by varying the pulse width of the base drive of Q1.

Protection against failure of inverter transistor $Q_2 - Q_5$ is secured by turning off Q1 and opening the output contactor.

7.2 INTERMEDIATE INVERTERS (15 to 1000 kW)

Inverters in the intermediate size range are intended for photovoltaic systems use for various industrial, commercial, and agricultural customers. They will be operating in parallel with the utility. The inverter output power will be delivered at 208 V or 480 V, 3-phase, 60 Hz. Certain applications require a utility interface at 3 kV or above.

The majority of the commercially available inverters use thyristors for power switching. Some advanced configurations, which include GTOs and power transistors, are presently being evaluated for efficiency, reliability, and cost. Some of the commercially available or proposed concepts are reviewed in the following sections.

7.2.1 Thyristor-Powered Inverters

Both line- and self-commutated topologies are available. Both 6-pulse and 12-pulse bridge-type inverters are offered. The 12-pulse system improves the wave shape by providing 12 steps per cycle (one step every 30 deg). Most of the configurations use a three-phase bridge as a building block, but three single-phase bridges, operating with a displacement angle of

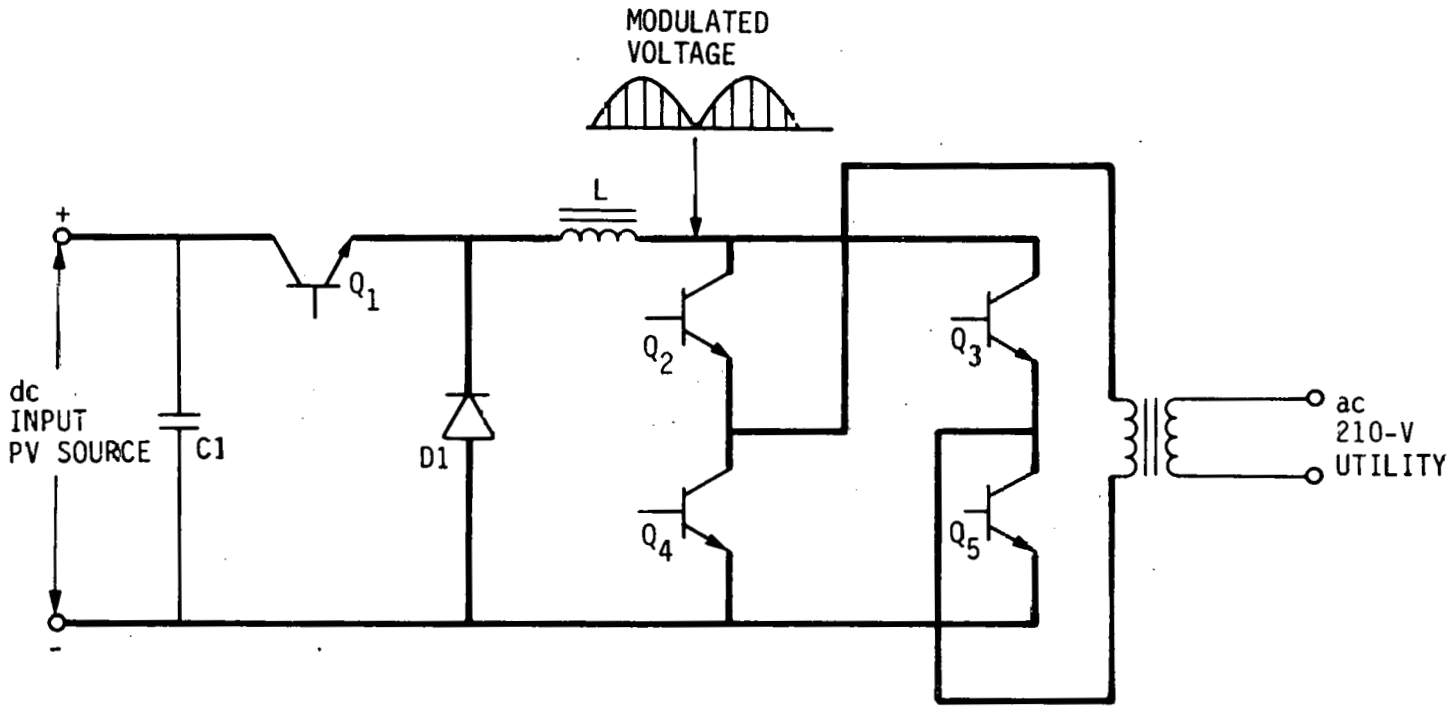

Figure 7-13. High-Frequency, Chopper-Controlled Transistor Inverter Without Transformer

120 deg are also utilized to deliver three-phase power. The reason for using the latter configuration is the possibility of increasing the delivered power without paralleling devices and to have individual phase-voltage and phase angle control of the output voltage.

7.2.1.1 Six-Pulse, Line-Commutated Inverters (see Section 6.3.4). A single three-phase bridge is employed to convert the dc power from the PV array into ac power for the utility. The six-power thyristors of the bridge are fired by gate pulses, whereas the turn-off is accomplished by reversal of the utility line voltage (see Section 6.3.4). The line-commutated inverter belongs to the category of current source inverters. The dc line inductor (Figure 7-14) determines the wave shape of the utility line current. The isolation transformer provides a voltage match between the PV source and the utility grid and also permits grounding of one side of the PV array. An optional ac filter consists of an L-C half section and may be used to reduce injected harmonic ac line current.

The configuration is characterized by simplicity, light weight, and low cost. The first higher harmonic currents present in the output are 5th and 7th. The harmonic current level is dependent on inverter design. Current harmonic distortion may be in excess of 20%.

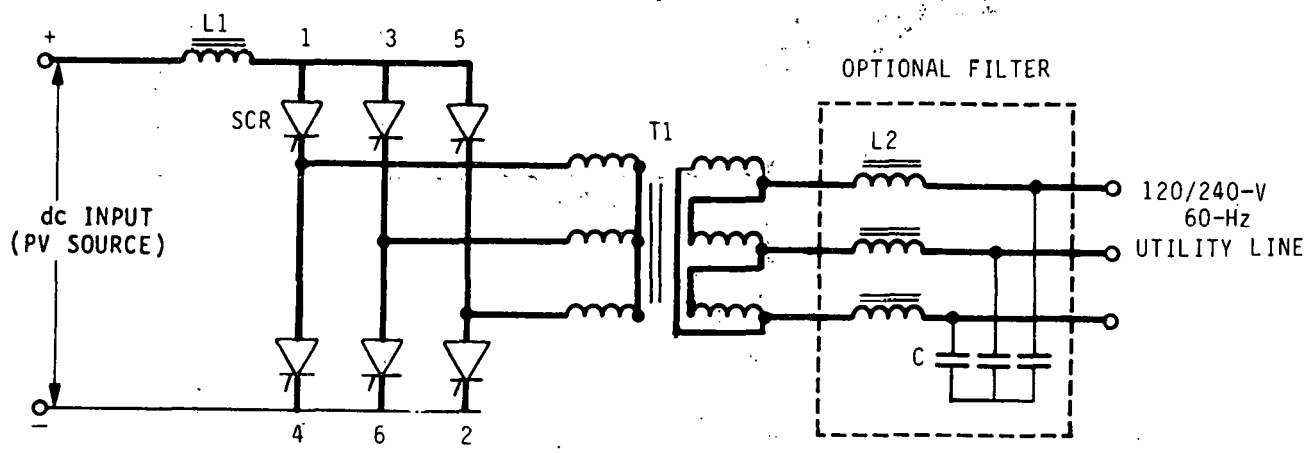

Figure 7-14. Line-Commutated, Three-Phase Inverter

The control of the delivered power is achieved by phase angle control of the firing point of the thyristor when the current pulse is initiated. The inverter current flow continues for 120 deg. At the firing of the next thyristor, current flow is transferred to the next phase. Depending upon the angle at which the current leads the voltage, the power factor (PF) changes as the firing angle is changed. The PF for such inverters is generally below 0.7 and will vary with load, array voltage, and utility voltage.

The phase relationship of the output current with the utility voltage determines the amount of reactive load absorbed from the utility. Deterioration of the PF at the reduced energy levels is shown in Figure 7-9.

Correction of the PF may be achieved by using the optional filter (see Figure 7-14). The PF correction capacitors may be switched in and out in steps, reflecting the need for keeping the PF under control for the total anticipated range of loads.

7.2.1.2 Twelve-Pulse, Self-Commutated Inverter (see Section 6.3.6). The two three-phase bridge inverters (Figure 7-15) operate at a 30-deg phase displacement to create a twelve-pulse inverter system (Reference 7-5).

A balanced three-phase inverter inherently cancels all harmonics that are a multiple of two and three. When two inverter outputs are added with a phase difference of 30 deg and amplitude ratio of 1:3, the fifth and seventh harmonics are also cancelled. The first harmonic present is the eleventh. The thyristors are force-commutated so that the inverter can be used both for utility or stand-alone operation.

Control of the output power is accomplished by varying the relative phase position of the firing angle of both inverters. The secondaries of two transformers are series connected. The star plus zigzag connection contributes to a reduction of harmonics.

A low-pass, T-section ac filter is used at the output for suppression of harmonic current. Also, in the case of parallel operation with the utility, the series reactor is deployed as a tie reactance needed for reducing the effects of utility line voltage unbalance, helping to suppress the line surges and facilitating smoother control of the power flow.

7.2.2 Transistorized Inverters

Although transistor topologies have gained acceptance at the residential power level, they are not yet generally considered for intermediate-size power systems. Continuing progress with high-power, low-cost transistors raises the possibility that transistor topologies will be viable at

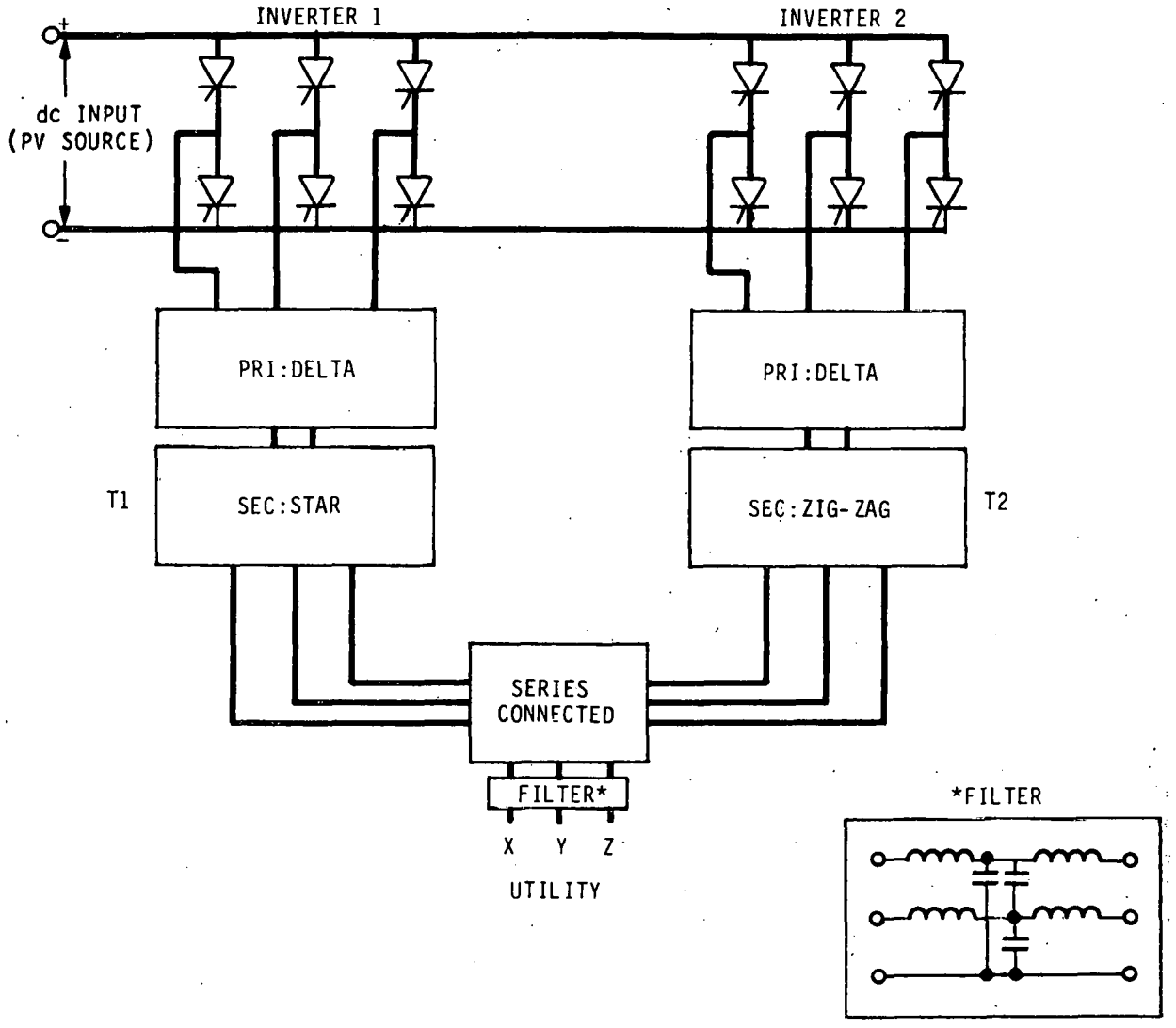

Figure 7-15. A Twelve-Pulse Inverter Using Two Three-Phase Bridges

intermediate power levels. Analysis by General Electric Company (see Reference 7-3) and United Technologies Corporation (see Reference 7-6 and 7-7) indicate that transistor-based systems offer improved costs and efficiency compared with their thyristor counterparts.

The use of fast-switching transistors will permit the implemention of high-frequency modulation, thus reducing the harmonic content with substantially less filtering than their thyristor counterparts.

The high-frequency switching rate varies from one design to another. One manufacturer proposes to use transistor current limits to set the switching pattern for their PWM system. When the ac transformer current

rises above a preset limit, the base drives of a set of transistors is switched off and the other pair is switched on until the current falls below the limit and the original transistors are turned on again. Such a scheme will have a varying number of switchings per second, depending upon the operating conditions. Under nominal conditions, 4420 switchings per second occur. However, this rises to 5160 or falls to as low as 4200 switchings per second under other conditions. A second manufacturer proposes to use a varying, high-frequency switching rate proportional to dc input voltage that meets the ac harmonic specification. The range of switching rate lies between 1.4 kHz at 350 Vdc to 2.7 kHz at 500 Vdc.

7.2.2.1 Transistorized, Pulse-Width Modulated, Six-Pulse Inverter. One method of implementation of a pulse-width modulated, six-pulse inverter is shown in Figure 7-16 (Reference 7-6).

This proposed scheme uses three transistor power poles with a total of six transistors. Higher power rating is accomplished by paralleling of transistors. This circuit configuration is commonly used in ac motor speed control. High-frequency operation of the power transitors produces a current output waveform with very low harmonic distortion. This is accomplished with a minimum of filtering using inductors L_A through L_C. Waveform synthesis and voltage control is provided by PWM operation of the inverter.

An alternate proposed method of inversion (see Reference 7-7) is accomplished by means of three single-phase bridges (Figure 7-17). Three single-phase transformers are used rather than one three-phase unit. While simplifying production and servicing, this alternate approach increases the total size and weight of the transformer magnetics.

At present, paralleling of transistors is needed for high-power systems to provide the required rating. The use of six power poles rather than three, as used in a case of a single three-phase bridge, raises the comparative power handling capabilities. This configuration provides a six-pulse waveform that eliminates the fifth and seventh harmonic. Higher harmonics are suppressed by PWM (see Section 6.4), which also serves the purpose of controlling the inverter output voltage for power-factor control.

7.2.2.2 Transistorized, Twelve-Pulse Inverter. A proposed twelve-pulse, six single-phase bridge configuration (Figure 7-18), is electrically equivalent to the one shown in Figure 7-15 but uses twice the number of power switches that are required for two three-phase bridges. The power handling capability is thus doubled. A different method of driving the power switches is used. In the thyristor system shown in Figure 7-15 the control is achieved by controlling the phase angle at which the thyristors were fired, whereas control of the power transistors of Figure 7-18 is achieved by high-frequency

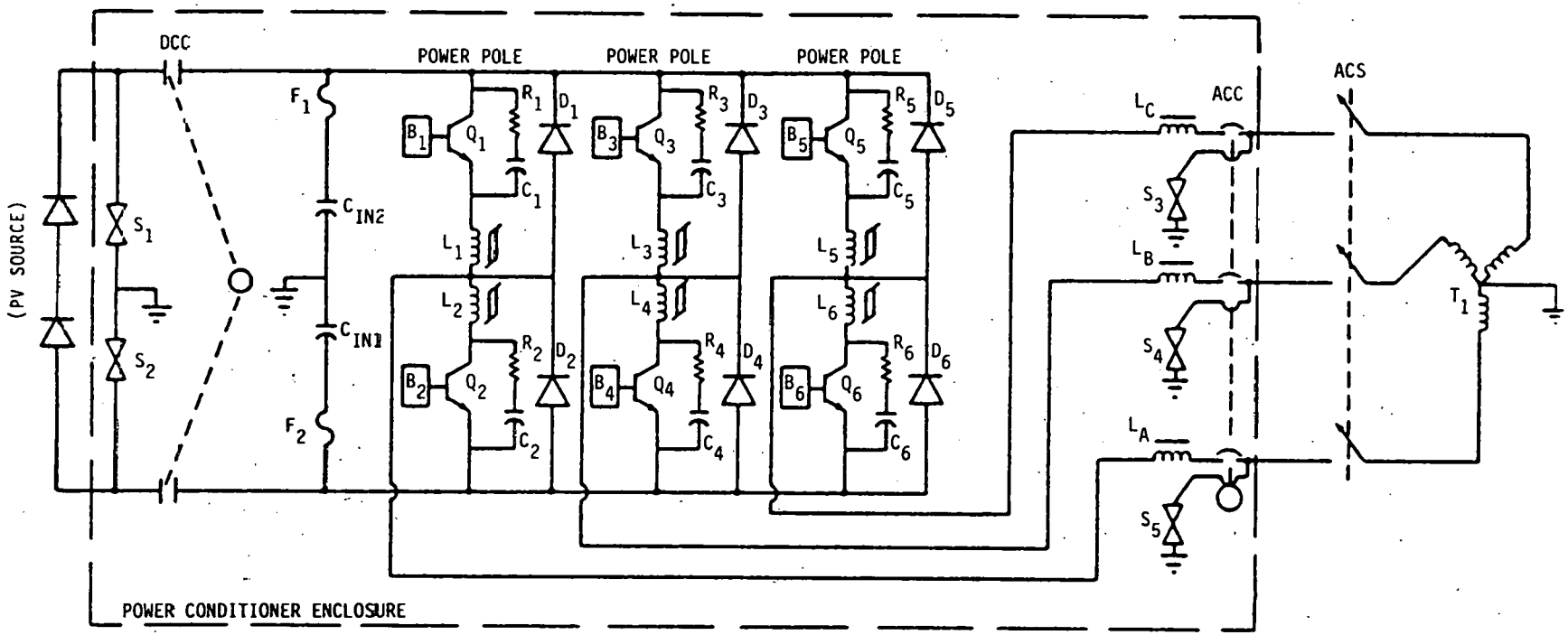

Figure 7-16. Six-Pulse, Pulse-Width Modulated Inverter (see Reference 7-6)

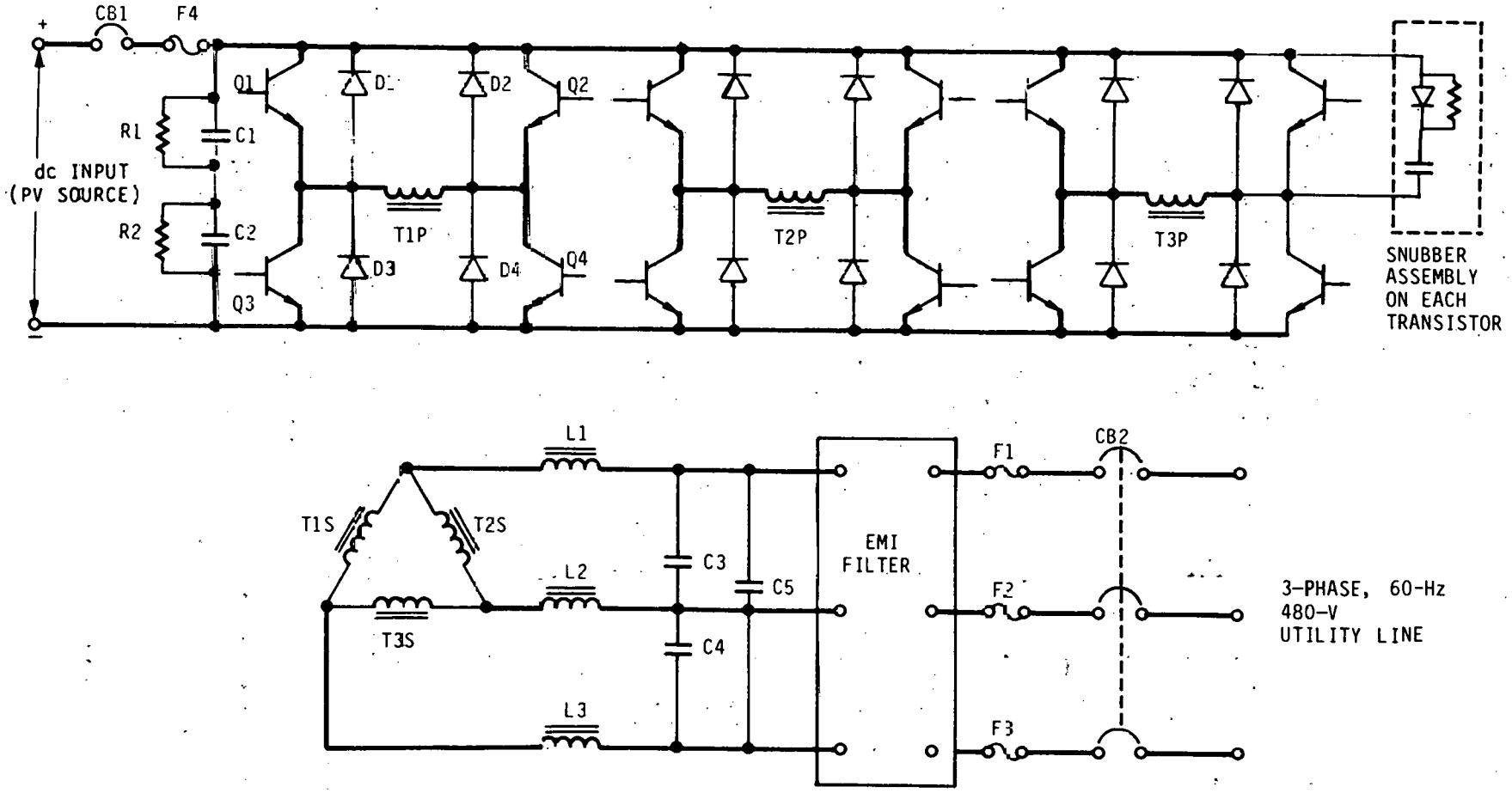

Figure 7-17. Pulse-Width Modulated, Six-Pulse Inverter Using Transistors (see Reference 7-7)

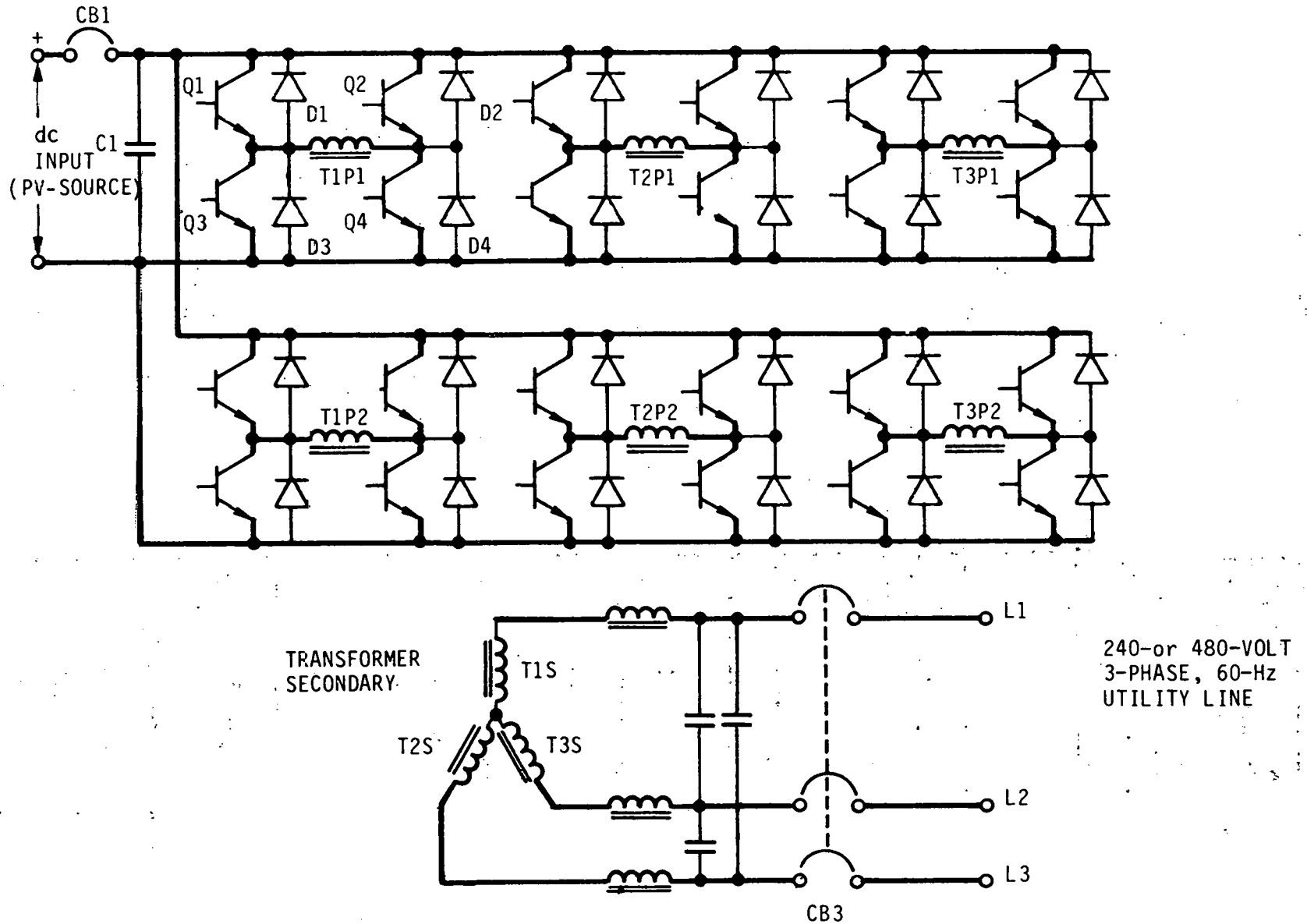

Figure 7-18. Transistorized 12-Pulse Inverter with Pulse-Width Modulation (see Reference 7-7)

modulation techniques. Consequently, the higher harmonics that appear in the output are suppressed by modulation techniques rather than by filtering. Voltage control for this circuit configuration is accomplished by PWM operation (see Reference 7-7).

7.2.3 Inverters Using Gate Turn-off Thyristors

Inverter implementation for the circuits description in Section 7.2.2 can be accomplished by interchanging the noted transistors to gate turn-off devices (GTOs). A typical schematic of a voltage source GTO inverter is shown in Figure 7-19 (Reference 7-8).

The Darlington connected power transistors, General Electric type D67DE, are rated at 500 V/80 A, whereas gate turn-off thyristors rated at 2500 V/800 A are reported to be commercially available in Japan (Hitachi GFT 1000D25). A single GTO could be used in each pole in place of two or possibly three parallel connected power transistors that may be required in each pole. The result is a lower parts count with the potential of higher reliability. It should be noted that the forward voltage drop of a GTO is greater than that of a power transistor; consequently, the efficiency may be slightly lower. There is a substantial interest in GTO inverters with possible reliability, performance, and cost improvements compared to thyristor and transistor designs.

7.2.4 Hybrid Inverters

Hybrid inverters use a combination of different power semiconductors to accomplish inversion. Hybrid topology inverters, which combine thyristor with self turn-off devices such as transistors, FETs, and GTOs may have merit for medium-size PV systems. The hybrid configuration would use thyristors as main power handling switches and the self turn-off devices as commutation switches.

Compared with thyristor topologies, such configurations may be more efficient and less costly because of reduced losses and lower costs of the commutation circuit. Compared with GTO circuit configurations, hybrid topologies will have advantages of cost and efficiency; compared with transistor topologies, they will have an advantage of improved ruggedness, reduced switching losses, overload capability, and lower total device cost.

A 60-kW GTO commutated, six-pulse thyristor three-phase bridge inverter is being developed at the Jet Propulsion Laboratory for a medium-size PV application (Figure 7-20). In this configuration the commutation of all power thyristors is accomplished by means of a single GTO. Each of the six main thyristors is back-biased during the interval of GTO conduction. T1 serves as a current sourcing input inductor and as a transformer. Saturating inductors L1 through L3 isolate the feedback diodes from the thyristors during the commutation interval, thereby allowing thyristor turn-off. The three output legs are connected to a conventional star/delta transformer (T2).

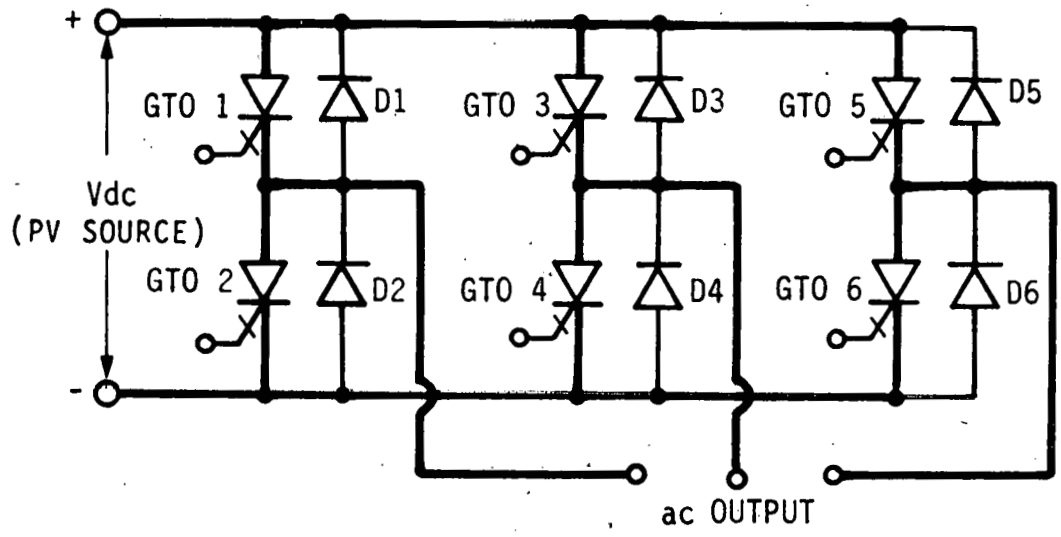

Figure 7-19. Voltage Source Inverter with GTO Switches (see Reference 7-8)

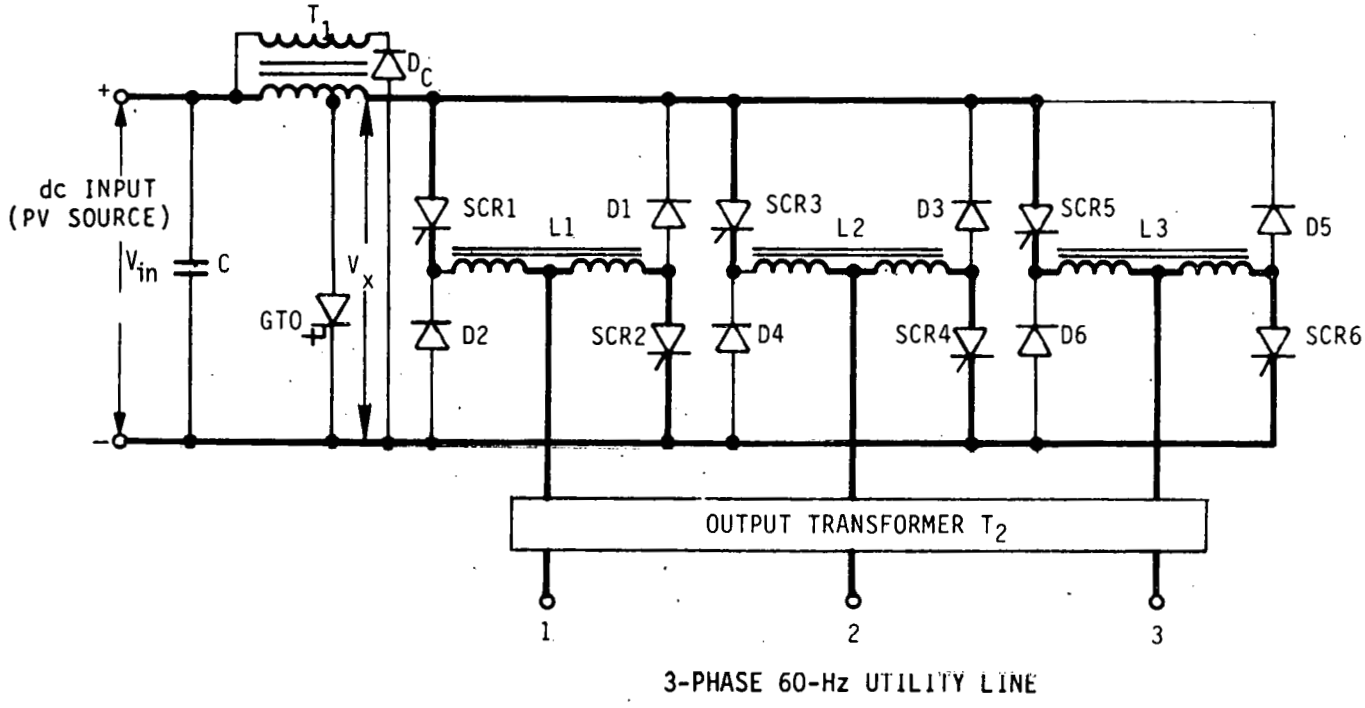

Figure 7-20. A GTO Commutated, Six-Pulse Thyristor, Three-Phase Bridge Inverter

The theory of operation can be summarized as follows.

When the GTO fires, V_x goes negative by autotransformer action of T1. This causes all six thyristors to become reverse biased. When the GTO is turned off, V_x becomes positive and all ungated thyristors remain off. Inductors L_1-L_3 isolate antiparallel diodes during commutation. Energy build-up in T_1 is returned to the dc bus capacitor C via diode Dc.

Cost advantages of this arrangement result from the lower cost of thyristor drive circuits as compared with GTO and transistor counterparts. Efficiency advantages derive from: (1) reduced forward drop of thyristors compared with an all GTO system; (2) reduced snubbing losses as compared with transistor system; and (3) significant reduction in commutation componentry compared to conventional thyristor systems.

7.3 LARGE INVERTERS (ABOVE 1 MW)

Large inverters are used to provide the power conversion for photovoltaic systems for small generating stations that will partially supply power to small communities or become part of the dispersed power generation system of the future.

The power inverter consists of one or more high-power bridges of a three-phase variety. Thyristors for high-power applications are paralleled to increase the inverter power handling capability. Paralleling of the individual power conditioner units may also be used if increased power is required. Equalizing the loading of two units operating in parallel is accomplished by electronic control of the individual inverter outputs.

Both line-commutated and self-commutated inverters are presently being designed, operated, and evaluated. Line-commutated performance in the existing high voltage dc (HVdc) transmission converter stations has been judged adequate and its reliability has been high. Self-commutating inverter systems have been extensively used in uninterruptible power supplies, photovoltaic systems and ac motor speed control. Well engineered systems have proven reliabilty of 50,000 hours mean time between failure (MTBF). Comparative systems have similar costs and efficiency. Several of the advanced topologies have potential for low cost and high efficiency compared to state-of-the-art designs.

7.3.1 Six-Pulse, Line-Commutated 1-MW Inverter (see Section 6.3.4)

This configuration (Figure 7-21 and see also Section 6.3.4) uses one three-phase bridge to generate 1 MW of ac power. Two thyristors (SCR1 and SCR2) are connected in parallel; small aircore inductors L1 and L2 safeguard against the possibility of one of the two thyristors failing to turn on. For

example, if the SCR2 has fired prior to the SCR1, L2 secures that the voltage across A-B will remain high during the time that the current through SCR2 rises to its maximum value. The SCR1 thus has a chance to turn on. Once conducting, both devices share the load equally. The power factor can be kept to a specified value by connecting a suitable number of PF correcting capacitors at the utility terminals.

In one application of a 1-MW photovoltaic installation at the Arco Solar Lugo site, the power factor is adjusted by switching in-or-out power factor correction capacitors with electromechanical switches (by Garrett Corporation). In another application of a 3-MW MHD installation (by Westinghouse in Butte, Montana), the power factor is adjusted by electrical means using a subsystem termed a VAR generator. In this case, smooth and continuous power factor control is accomplished by a combination of thyristors, inductors, and capacitors. Thyristors effectively adjust the amount of inverter filter capacitance, thereby keeping the total system power factor at a specification level. The higher harmonics (5, 7, 11, 13th) are trapped by output LC shunts, resonating at 300, 420, 660, and 780 Hz.

For the above 1-MW application, protection against a shoot-through[1] in the case of a temporary loss of the utility is accomplished by means of the high-speed dc circuit breaker (CB). The breaker is capable of interrupting the current flow within 6 ms; the buildup of current during this period is limited by the line inductor L and to the array overload capacity, which is approximately 120% of rated array current. An alternate approach (used in the above 3-MW application) to inverter protection is to use a static interrupter, which interrupts the applied dc voltage during inverter fault conditions.

7.3.2 Twelve-Pulse, Line-Commutated Inverter (see Section 6.3.4)

Currently a twelve-pulse, line-commutated inverter is under development and construction (by Windworks, Inc.) for photovoltaic station application at the Sacramento Municipal Utility District (SMUD). This inverter will interface with an array at a voltage level 500 Vdc and will interface with the utility at 12 kV (see Figure 6-6). One six-pulse, line-commutated inverter is connected to a delta-wye, three-phase transformer; and the other six-pulse inverter is connected to a delta-wye transformer. The result is a twelve-pulse inverter with the attendant harmonic and power factor improvement over a six-pulse, line-commutated inverter. Output filtering using tuned traps are used for harmonic current reduction. The capacitors in these traps also are used to improve system power factor.

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[1] Two inverter thyristors on at the same time across the dc bus.

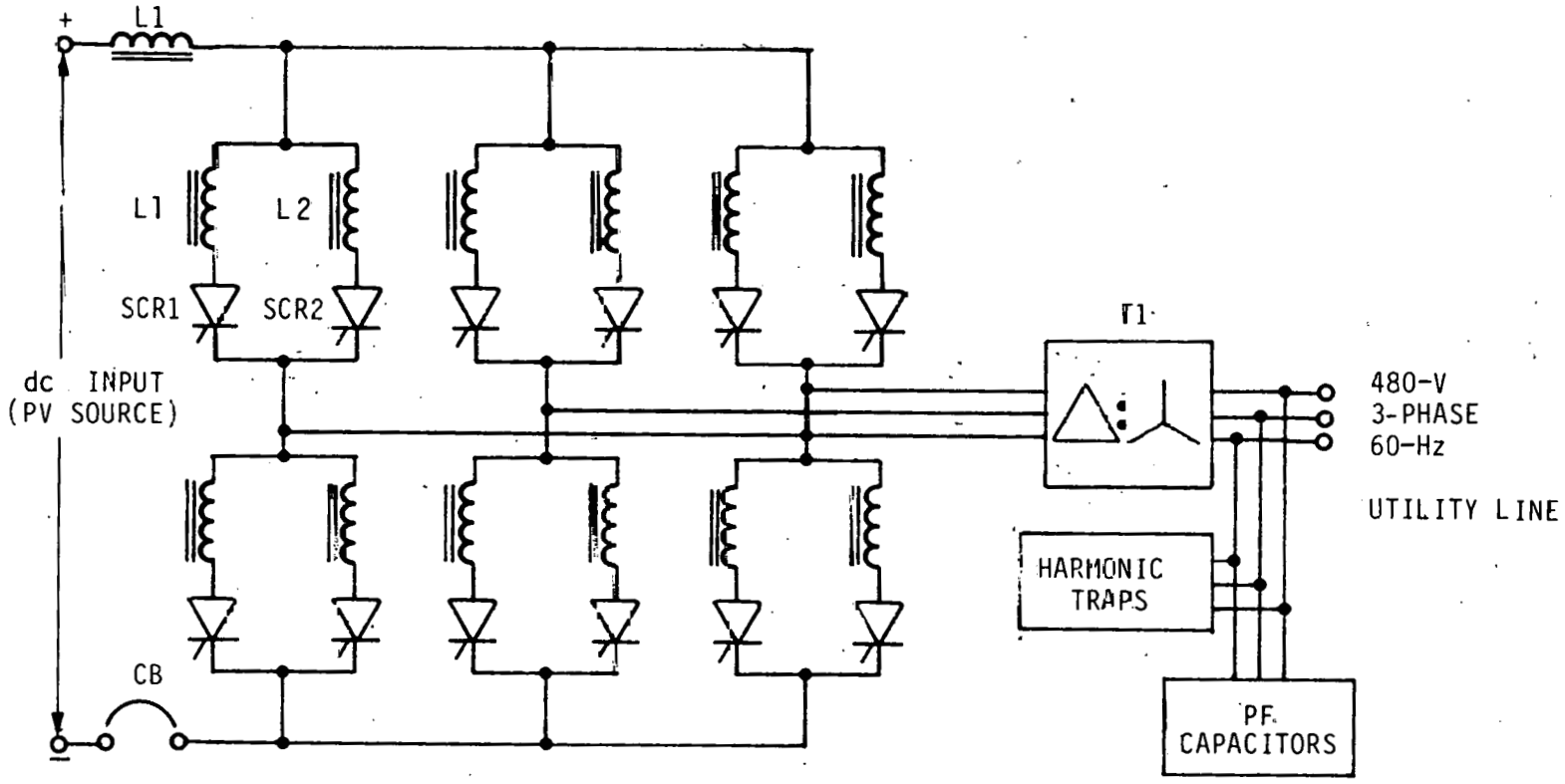

Figure 7-21. Six-Pulse, 1-MW, Line-Commutated Inverter with Power-Factor Correction

7.3.3 Twelve-Pulse, Self-Commutated, 500-kW and 750-kW, Thyristor Inverter (see Section 6.3.6)

Two 500-kW, twelve-pulse, self-commutated inverters have been operating in a 1-MW photovoltaic installation at the ARCO Solar Lugo Installation in Hesperia (by Helionetics Corp.). Multiple 750-kW units are being installed for a 16-MW system at the ARCO Solar Carrisa Plains Installation, with initial installed capacity of 6 MW. These units will be similar electrically to the above except parallel modules will be 750 kW each.

The inverter (Figure 7-22) belongs to the family of voltage source inverters, with a large capacitor C across the dc bus. Six single-phase bridges are employed to generate 500 kW or 750 kW of power, without any paralleling of thyristors.

Forced commutation is not dependent on the utility line for turn-off of the thyristors, as is the case for line commutation. This provides an additional degree of freedom and permits the power flow regardless of interface voltage levels without affecting the power factor. The inverter is capable of operating at near unity power factor; the power factor, which remains constant for all power levels, can be made adjustable providing for lagging, unity, or leading power factor operation.

Single-phase transformers are used because each bridge feeds one primary, as shown in Figure 7-22. Each secondary consists of three windings, wound in a 4:3:1 ratio. All these windings are interconnected in series to form a single composite star. Harmonic reduction is accomplished by waveform synthesis similar to that described in Section 6.4.2.

The total harmonic distortion for all loads remains under 2%, due to the selected method of interconnection of the transformer secondaries and L-C filtering at the output.

Control of the output power is achieved by adjusting the phase relationship between the inverter and utility voltage. Power factor control is provided by adjustment of the inverter output voltage.

7.3.4 4.8-MW, Self-Commutated, Eighteen-Pulse Inverter

A 4.8-MW, ac fuel cell electric power generator was designed and manufactured by the Power Systems Division of United Technologies Corporation (UTC) under a jointly sponsored program with the U.S. Department of Energy (DOE) and the Electric Power Research Institute (EPRI) (see Reference 7-9). The system will be operated by Consolidated Edison Company of New York, Inc., under contract with DOE.

The 4.8-MW PCS contains three 3-phase inverter bridges (Figure 7-23) constituting an 18-pulse inverter. These bridges are operated so that common phases have a 20-deg electrical phase relationship, permitting cancellation of output voltage harmonics up to the seventeenth harmonic by way of low-voltage harmonic reduction transformers. Series reactors are

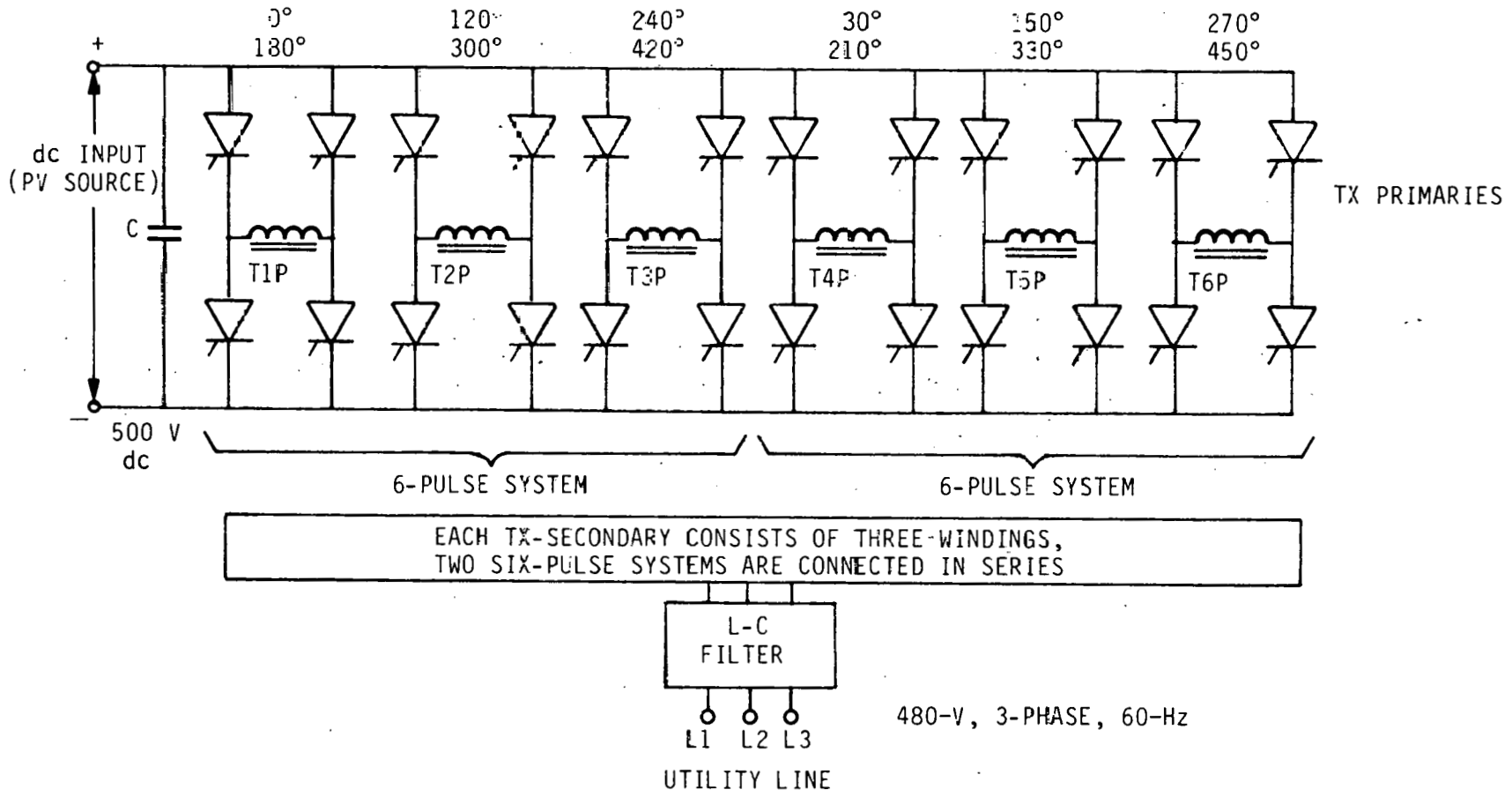

Figure 7-22. Twelve-Pulse, 500-kW Thyristor Inverter

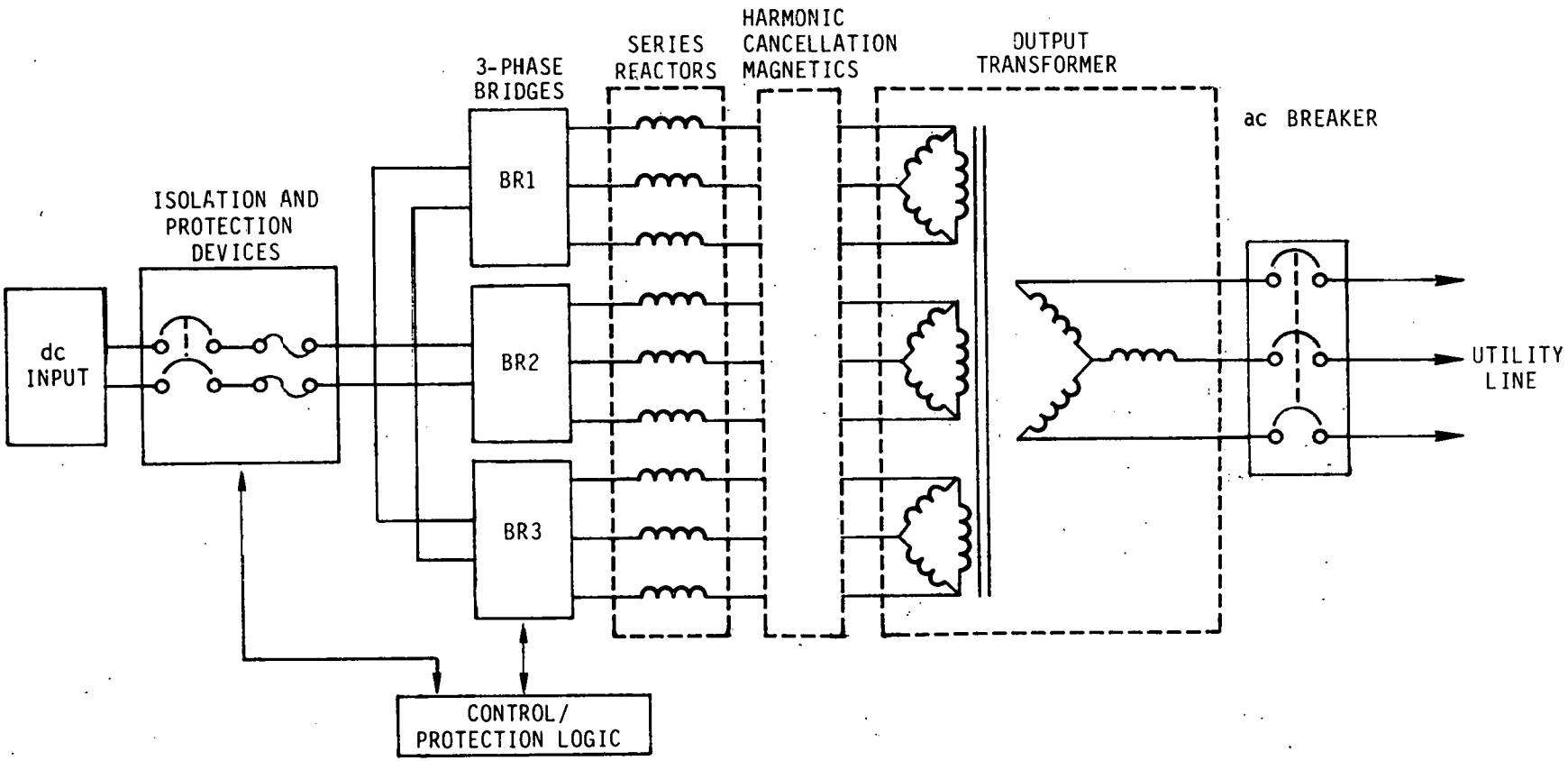

Figure 7-23. Schematic of a 4.8-MW Self-Commutated Inverter

approximately 0.22 per unit, and frequency of inverter thyristor switching is at 180 Hz. The inverter operates in parallel with the utility; interconnection is implemented at the primary feeder level of 13.8 kV. The inverter is equipped with the force-commutation circuitry that permits continuous electronic power factor control without power factor correction capacitors. The inverter power pole used in this application is of the auxiliary-commutated type shown in Figure 6-8d.

The self-commutated inverter is basically a voltage source in series with an impedance. Thus, when operated in parallel with a utility network, the basic principle for control of real and reactive power flow is identical to that of a conventional rotating generator (see Appendix A).

The inverter is paralleled to the utility line through a series tie reactance. The real power flow is controlled by adjusting the phase of the inverter voltage in relation to the utility line voltage, and the reactive power flow is controlled by adjusting the magnitude of the inverter output voltage in relation to the utility line voltage.

7.3.5 5-MW, Chopper-Controlled, Line-Commutated, Twelve-Pulse Inverter (see Reference 7-10)

A 5-MW photovolttaic fuel cell power conditioning subsystem is in initial design and development stages by the Westinghouse Advanced Energy Systems Division of Westinghouse Corporation. The initial conceptual efforts are under a jointly sponsored program with the U.S. Department of Energy and the Electric Power Research Institute (EPRI).

The basic inverter uses a 12-pulse current-sourced, line-commutated inverter (see Sections 6.3.4, 7.3.2 and Figure 7-24). To overcome the low power factor and high current harmonic levels of the conventional line-communtated inverter, a dc/dc converter (Figure 7-24) is added between the photovoltaic/fuel cell source and the twelve-pulse inverter. Multiple paralleled dc/dc converters using GTO devices are used to reduce source or array ripple and to reduce converter inductor size. The objective of adding the dc/dc converter is to adjust the dc voltage so that the relationship with the utility line voltage is fixed and at a level which provides inverter operation, simulating the characteristics of twelve-pulse rectifier operation. This allows operation at high power factor levels and low harmonic current injection into the utility. In addition, the dc/dc converters can be used to interrupt an inverter "lock on" (two thyristors on at the same time across the dc bus).

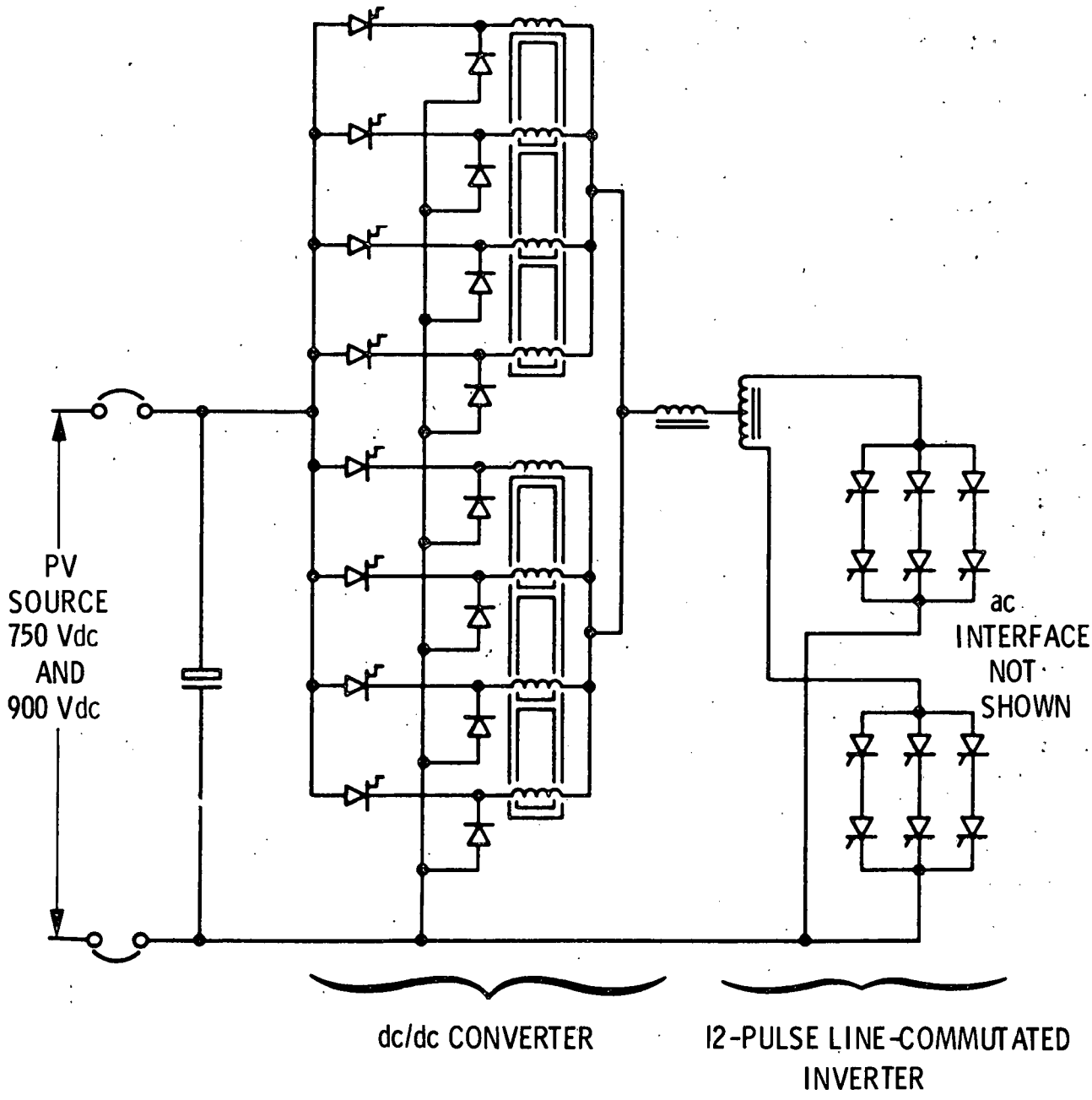

Figure 7-24. 5-MW Photovoltaic Inverter: dc/dc Converter-Controlled, Line-Commutated, 12-Pulse Inverter (see Reference 7-10)

7.4 REFERENCES

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SECTION 8

NEEDED RESEARCH AND OPPORTUNITIES FOR DEVELOPING IMPROVED POWER CONDITIONING SUBSYSTEMS

Power conditioning subsystem technology has advanced rapidly in recent years. As experience has been acquired, various requirements for PCS cost, performance, safety, and utility integration have surfaced. The current understanding of these requirements and their implications for PCS design are detailed in this section of the document. Experience has shown that acceptable integrated operation can be expected with proper PCS design; however, there are still unknowns in the design of a utility interactive power conditioner subsystem.

Specific progress has been made in the areas of small single-phase power conditioner subsystem technology. The results of U.S. Department of Energy and industrial-supported activities have produced power conditioner subsystems with unusual characteristics and performance for residential utility interactive PV systems. Many of these power conditioner subsystems use microprocessor control and have what may be constituted a "brain." They do not require the usual synchronizing and protective relaying that are essential for conventional cogeneration and dispersed energy systems connected to the utility line. These units were developed to provide this intelligence by internal electronic means to reduce PCS costs because conventional synchronizing and protective relaying would have increased PV system costs excessively. Thus, there are today a number of commercially available, small power conditioner subsystems that electronically synchronize to the utility, provide electronic under and over voltage and frequency protection; and electronically disconnect the PV system from the utility line under out-of-tolerance utility line conditions. All this is accomplished without the use of electromechanical relays and sensors. All sensing and control is accomplished reliably by electronic means without the use of electromechanical relays. Currently, many small commercially available and developmental power conditioner subsystems are under intensive engineering test and evaluation at the Sandia National Laboratory (SNL).

It is apparent that static and dynamic voltage and frequency changes on the utility system can seriously affect PCS design. Audible noise is also a concern because most small photovoltaic power conditioners may be installed inside a residence or in a critical work area. To meet adequate cost and electrical performance requirements, there are serious concerns in meeting various safety codes to guarantee the safety of users as well as PCS maintenance and utility personnel. A detailed description is provided of the current open issues and concerns that remain for the power conditioner subsystem designer to consider.

8.1 STANDARDS, GUIDELINES, AND SPECIFICATIONS

Standards, guidelines, and specifications are needed to inform manufacturers, utilities, and consumers about the specifics of adequate

performance, characteristics, and safety concerns related to the design, manufacture, and installation of power conditioning subsystems (see References 8-1 through 8-5).

Insolation characteristics over an operational day will vary in different parts of the United States. Power conditioning efficiencies at full or part loads do not necessarily reflect energy efficiency of the power conditioner with specified insolation profile. Thus, the energy efficiency for power conditioners will vary in different parts of the United States.

Different types of arrays such as flat plates, concentrator arrays, and tracking flat-plate arrays will have power output characteristics that will differ from each other even though operating in the same environment. Power conditioning efficiencies, either at full load or part loads, are predicated upon power conditioning design. Thus, one power conditioner may have a high efficiency at full load and only a modest efficiency at one-quarter load. Another power conditioner may be designed for high efficiency at a three-quarter load and a somewhat lower efficiency at full load. The net effect is that power efficiency may in fact not reflect the important significant function of a power conditioner, which is to process the maximum amount of energy available. It is suggested that a figure of merit be determined for each power conditioner that will relate the available insolation characteristics (in a particular region where the PCS will be used) to the PCS energy efficiency. This will allow the system designer and/or the consumer to choose a power conditioner for a specific PV system by proper tradeoff of power conditioning cost and energy efficiency of the power conditioner.

Because of discrepancies in available documents, there is substantial confusion in determining design practice by system designers and power conditioning manufacturers in determining acceptable functional and safety requirements and performance parameters. Acceptable terms of design and integration for one region of the country may be unacceptable in another region. Currently, there are various national and international groups whose objectives include the development of standards, guidelines, and specifications. There are proposed modifications for the 1984 National Electrical Code (NEC) relating to photovoltaic integration that, if approved, will be in Section 690 of the Code. There are also various activities in the Institute of Electrical and Electronic Engineers (IEEE) Photovoltaics Power Conditioning Subcommittee, both in the area of power conditioning recommended practice and power conditioning testing recommended practice. The IEEE Photovoltaic System Subcommittee has promulgated a trial standard for integration of small and intermediate photovoltaic systems into a utility.

There are currently no acceptable standards or requirements for electromagnetic interference (EMI) and radio frequency interference (RFI) for power conditioning subsystems. Current field testing by the National Bureau of Standards reflects that most of the units tested interfered with AM-band radio operation, indicating the need for EMI filters for the PCS. Development of EMI and RFI standards and guidelines would assist power conditioning manufacturers to determine requirements for acceptable operation of power conditioning subsystems.

Currently, there are no definitive design guidelines for power conditioning subsystems. However, some of these activities have had substantial efforts to date (see References 8-3, and 8-6 through 8-8).

8.2 OPPORTUNITIES TO REDUCE COST AND INCREASE EFFICIENCY OF POWER CONDITIONERS

Acceptable photovoltaic power conditioning subsystem hardware can be defined as hardware that satisfies the performance and safety needs of a photovoltaic utility interactive installation. There are various concerns relating to the design and development of such power conditioning subsystem hardware that affect safety, performance, and cost. The optimum design configuration of a power conditioning subsystem would reflect low-cost and acceptable performance. Such factors as the dc array voltage, harmonics, power factor, and safety also affect cost and performance; therefore, they also have a direct impact on power conditioning design.

8.2.1 Power Conditioning Subsystems

Transformerless power conditioning subsystems have potential advantages over systems that contain isolation transformers. Transformers add substantially to the cost and size of the power conditioner as well as to a reduction of power conditioning subsystem efficiency. Transformerless systems can also reduce audible noise. The questions that must be answered for transformerless systems are:

(1) Can the projected changes in the National Electrical Code that require array grounding or equivalency be met effectively? From a safety point of view, is it necessary to ground the array?

(2) Can a transformerless system be operated with multiple PV sources on a single distribution transformer without affecting the other connected photovoltaic systems?

(3) Can ground fault detectors be integrated effectively within the context of acceptable transformerless design?

(4) Can the injection of direct current into the utility distribution transformer be prevented?

(5) Can transformerless PCSs be interconnected with a utility without affecting utility operation and maintenance?

A number of these questions have been addressed by JPL under contract to SNL (Reference 8-6).

8.2.2 Development of Cost- and Performance-Effective, Intermediate Power Conditioning Systems

Most medium-size power conditioning systems available in the United States today reflect designs that were developed 10 to 15 years ago. These designs are characterized as highly material-intensive rather than process-intensive (the use of semiconductors replacing magnetic and capacitor functions). There are basically two types of intermediate power conditioners that are commercially marketed for photovoltaic needs. The first type is primarily modified, uninterruptible power supplies. These self-commutated power conditioners can provide a high quality of power with appropriate circuit design. The second type is line-commutated power conditioners. Line-commutated systems with equivalent harmonic and VAR performance of self-commutated systems (reflecting some of the standards being promulgated) require substantial filtering to provide acceptable harmonic and power factor performance.

With advanced semiconductor components there is an opportunity to develop new circuit configurations that reduce PCS cost and improve performance. The new circuit configurations will allow for process-intensive designs instead of material-intensive designs (large magnetic and capacitor structures) for medium-size power conditioners.

With the development of advanced circuit topologies, power losses and costs associated with filters and line- and self-commutated inverters can be materially reduced. In addition, costs and power losses associated with commutation circuitry in self-commutated systems can be substantially reduced. These cost and power loss reductions can provide for power conditioner subsystems of substantially improved cost, efficiency, and performance.

8.2.3 Development of Cost- and Performance-Effective, Large Power Conditioning Systems

Large power conditioners used for present-day central-station-type photovoltaic systems use designs that are basically modified uninterruptible power supplies (UPS) or line-commutated inverters with filtering. In both cases, costs are substantially beyond the desired levels consistent with low photovoltaic systems costs ($35 to $60/kW compared to $10/kW). Apart from the lack of large-scale PCS production, the reason for this relatively high cost is primarily due to the material-intensive rather than process-intensive designs. This is due to the relatively low switching speeds resulting in costly filter configurations that reflect material-intensive designs. In addition to costly filter configurations, self-comutating inverters require commutation circuitry needed for circuit implementation. Commutation circuitry adds materially to cost and complexity of both state-of-the-art and advanced designs. At present, there are no advanced-technology (without commutation circuitry and large output filters), low-cost, large power conditioning systems that are available commercially and that have a proven operational track record.

The cost and performance of large power conditioners is limited by the availability of new, advanced semiconductors with improved switching speeds. Thus, with newly developed semiconductors, large power conditioning subsystems that reflect process-intensive designs with low cost and high performance should be possible. Several important questions must be addressed. Can commutation components be eliminated for self-commutated designs? What is an acceptable array dc voltage for minimum levelized energy cost? What new design opportunities exist for very large PV systems (above 50 MW)?

Needed research concerning minimum cost system design is underway at Sandia National Laboratories at Albuquerque (SNLA) and their subcontractors to establish the appropriate dc operating voltage and optimal circuit topologies for central station power conditioners. These new circuit topologies, both line- and self-commutation types, offer a potential of substantial cost reduction and efficiency improvement compared to state-of-the-art systems.

8.2.4 Impacts of Advanced Semiconductor Devices on Power Conditioner Design

The new, advanced, high-power semiconductor devices that are becoming available and that will impact PCS design are high-voltage, high-current transistors; high-speed, high-voltage, gate turn-off control rectifiers; and induction-type thyristors (high-speed, high-voltage, high-current devices). Several of the major power conditioning research organizations under contract to the Department of Energy have indicated that advanced, megawatt-size power conditioner implementation PCS should be oriented toward the use of gate turn-off devices for next generation PCS hardware. At present, there are no medium- or high-power inverters using GTOs available in this country in either the UPS, photovoltaics, or other dispersed-storage and generation markets. Advanced devices such as the GTOs and induction thyristors are available commercially in Japan, but not from American manufacturers. The Japanese are producing high-power power conditioners using GTOs. The United States is behind Japan in manufacturing and using GTOs. There is substantial interest in GTO devices by American semiconductor manufacturers, and possibly this will result in development and manufacturing capability.

8.2.5 Impacts of Advanced Magnetic Materials on Power Conditioner Design

New magnetic materials such as amorphous steels have become available that can materially improve power conditioning design efficiency. Experimental results indicate substantial efficiency improvements. Initially, implementation will occur in the smaller-size magnetics area, but the real advantage for these magnetic materials will be in the medium- and large-size power conditioners.

Can these new magnetic materials be integrated in designs so that they can be manufactured in an economical and practical method to satisfy the needs of photovoltaic power conditioners?

8.2.6 Harmonic Current Effects on PV Filter Components

Many applications of utility interactive PV power conditioners use parallel filters, including inductors and/or capacitors. In such designs, the filter elements will not only absorb harmonic currents that are produced by the power conditioner but also will absorb harmonic currents from the utility lines. As a result, the current requirements of filter components may be substantially greater than that specified for operation with a utility interactive photovoltaic system with negligible harmonic line voltages operations. The impact of randomly placing the filter components across the utility line, without concern for the effect of additional heating that may occur due to both power conditioning harmonics and line harmonics, may be excessive and cause undue failure in the power conditioning subsystem.

Research to determine the power spectrum and magnitude of harmonics on existing utility lines would be of significant value to designers of power conditioner filters. This would assist PCS designers to consider the effect of utility-line harmonics on filter component selection and sizing.

8.2.7 Power Conditioner Self-Excitation

Under conditions of normal utility operation there will be conditions in which voltage is reduced or removed for a period of time. In addition to this, the utility feeder recloser may open and close several times in a normal operating sequence. When a feeder line is opened, any connected generator should be immediately disconnected from the utility line. This is required to prevent utility line disturbances or failure due to the reapplication of feeder voltage. In addition, the line may have been disabled for maintenance purposes, and if a connected generator is operating, utility personnel may be endangered.

If a power conditioner self excites and reapplication of utility voltage occurs out of phase of the self-excited generator voltage, large surges of current will flow. This large, out-of-phase current may damage components of the power conditioner. When there is a utility disconnect, the power conditioner must turn off immediately under all conditions of load and in the presence of other connected generators. Although this design requirement is understood, the best approach to meeting it has not been determined. Several manufacturers are doing development and testing of residential PCSs to meet this need. Sandia National Laboratories and various utilities are also conducting intensive testing with positive results reported.

8.3 SAFETY ISSUES

Unless appropriate requirements are established within the existing framework of product safety standards, building and electrical codes, and utility codes, it will be difficult to obtain the necessary approval from the utility or local code enforcement officials for installation of photovoltaic power conditioner subsystems.

Safety is, therefore, a critical concern for the power conditioning and photovoltaics industry. For power conditioners, fire and electrical hazards must be controlled. Control of these hazards is the subject of the Underwriter Laboratories (UL) draft specification on photovoltaic power conditioners. Currently the UL document is in draft form and has not been issued. In addition, no photovoltaic power conditioners have been submitted to the UL to be qualified and listed for residential or intermediate use.

It is important that PV systems connected to a utility system should not cause any safety hazard to either the PV source owners or to utility personnel. The safe installation of residential, commercial, and industrial electrical systems is guided by the National Electrical Code (NEC), which is published by the National Fire Protection Association (NFPA) every 3 years. The current code does not address photovoltaics. It is anticipated that revisions to the NEC (1984) will emphasize the unique aspects of photovoltaics and address those concerns that could result in an unsafe installation. Some issues of concern are grounding of PV arrays and the PCS, electrical isolation (through a transformer) of the PV system from the utility system, and disconnection of the PV array from the PCS and the PCS from the utility during times of maintenance. These and other issues directly related to safety must be thoroughly analyzed and included in any revision of the code.

8.3.1 Effect of Array Grounding on Ground-Fault Indicators, Circuits, and Protective Circuit Operation

Array grounding or equivalency is required by code. Code requirements relate to small and intermediate systems. Large utility systems do not necessarily follow national electrical code with regard to grounding. In large systems major grounding design concerns are protection of personnel, protection of equipment, and safety.

Arrays may be positive- or negative-ground or center-tap ground (see Reference 8-4). There is reason to believe that the National Electrical Code, when approved , will allow for equivalency of grounding with approved photovoltaic power conditioners. Currently, large systems use either low-resistance, center-tapped ground or high-resistance, center-tapped ground. Due to the various grounding methods, it is unknown whether available ground-fault detectors, protective circuits, interrupters, and conventionally designed power conditioning logic circuits will operate reliably (see Reference 8-3).

8.3.2 Effect of Array Grounding on PCS Logic Circuits and Protective Circuit Operation

Due to various possibilities of grounding, it is desirable for the PCS logic to be designed so that it does not require a firm connection to the array ground. The PCS logic should be designed electrically off ground to preclude the possibility of either injected noise interference or ground loops due to attachment of instruments to measure logic functions. While the National Electrical Code at this point does not require the use of ground

fault detectors either for the array or for the inverter output, it is apparent that they will be used for large array systems for safety purposes and more reliable operation. Problems are not anticipated with systems that have internal electrical isolation transformers. The problem of using either ac or dc ground-fault detectors arises when transformerless systems are designed. Designs for transformerless systems or code-approved PCS with equivalency of grounding should include provisions for ground-fault detectors.

8.4 PCS ARRAY/INTERCONNECTION DESIGN FACTORS

Various factors affect the efficient extraction of energy from the array. Factors other than those that affect energy production (insolation levels, wind, temperature, and array degradation) are:

(1) Inverter ripple.

(2) Power extraction control methods.

(3) The ratio of power conditioner rating to array rating.

8.4.1 Effects of Inverter Ripple on Array Energy Delivery

Excessive array ac ripple due to the inverter can affect array energy extraction by reducing effective array energy output. There have been several curves published that quantify the loss in energy production to ripple level (Reference 8-7). These curves have been used by various designers of power conditioning equipment and by groups writing specifications for power conditioning design. The validity of these curves should be verified by testing.

8.4.2 Power Extraction Control Methods

Two methods of power extraction have been basically detailed for photovoltaic systems. One method tracks the maximum power point of the array I-V curve. The other method operates the array at fixed voltage. With maximum-power tracking, the operating range of the array voltage operation depend on conditions prevailing at the site. A voltage range of $\pm 15\%$ is the maximum over which the power conditioner will generally be required to operate. This voltage range may be substantially reduced at the expense of small reductions in array delivered power. With fixed-voltage operation, the power conditioner nominally operates at a specified fixed-voltage exclusive of turn-on voltage and open-circuit voltage. With either method of operation, it is necessary for the power conditioner to be able to protect itself under array open circuit conditions and to bring the array into operation when the power available from the array exceeds the tare losses. In other words, even in a fixed-voltage operation system the array must be brought back to the nominal voltage even though it is operating at some higher voltage. Hence, closed-loop control is required for either method of operating. Theoretically, maximum-power tracking should provide higher energy extraction than

fixed voltage operation. Although some initial attempts to use maximum-power tracking power conditioners have been disappointing, several are available that perform well.

Research is needed to characterize the spectrum of noise on the dc power signal from arrays of different sizes in different geographic locations. This is required to assist the designer of maximum-power trackers in determining the signal-to-noise ratio of the sensed signal. This basic data combined with new tools for designing maximum-power trackers in the presence of noise will allow maximum-power tracking PCSs to reach the potential. Whether this in fact is an improvement over fixed-voltage operation will ultimately require empirical data on both cost, PCS sizing, efficiency, and reliability. Additional field engineering evaluation is required to determine the effectivity of the different maximum-power trackers and evaluating the differences of maximum-power tracker operation and fixed-voltage operation.

8.4.3 Power Conditioner to Array Size Ratio

Inverter design and requirements will be affected if it is required to process less than 100% of the energy developed by the array at nominal operating voltage. The ability to process less than 100% of the array can be economically desirable. Unless firm system design decisions are established for energy extraction, the PCS selection may be larger, more costly, and less efficient that that required for the application. Design procedures are needed that will allow power conditioner size to be selected in a manner that minimizes the cost of power production.

8.5 FACTORS RELATING TO UTILITY INTEGRATION (see References 8-8 and 8-9).

8.5.1 Utility System Voltage Range and Voltage Unbalance Effect on PV Power Conditioner Design and Cost

System unbalance voltage relates to three-phase systems and is defined as the difference in voltage between phase voltages in a three-phase system. Distribution utility system voltage ranges are provided by ANSI standards. In general, central-station systems have a narrow band of voltage variation compared to medium systems (References 8-8 through 8-10).

Excessive voltage unbalance can cause problems with power conditioning operation, component overheating, and nuisance tripping of power conditioning protective devices. Utility system voltage range will affect the power conditioning cost according to the range required by specification.

Voltage range is specified by ANSI standards. In numerous cases ANSI standards are exceeded in actual practice. The power conditioner output transformer should be designed to encompass operation over the full range of actual operating voltage and voltage unbalance. This will relate to a power conditioner output transformer that is larger than that required under ANSI

requirements, resulting in greater transformer losses and lower power conditioning efficiency. Voltage unbalance in the three-phase system will reduce the power handling capability of the power conditioner compared to that of balance voltage operation. The unbalanced voltages will force unbalanced line currents to flow because the power conditioner output is designed to a maximum current level. One phase may have maximum current whereas other phases may have lower levels of current. The result of this is reduced power output of a power conditioner compared to the name plate rating. To obviate effects due to unbalance voltage, increased line tie reactance is desired or tighter control by the utility on its unbalance specification. Voltage ranges for utilities specified in ANSI standards are often exceeded in practice. Better information on actual voltage ranges and the degree of voltage unbalance experienced could be of help in minimizing power losses and the cost of PCS components. Ultimately the cost to the utility for improving its voltage regulation needs to be traded off against the cost of PV system accommodating voltage deviation and unbalance. While ultimately important, this type of research is site specific.

8.5.2 Voltage Regulation and Reactive Compensation

Utilities must maintain the voltage at the customer's terminals with limits specific in tariff schedule offered to the customer. Historically, radial distribution systems were designed for one-way flow of electrical power from the distribution substation to the load via the distribution feeder, lateral, distribution transformer, secondaries, and the customer's service line. With one-way flow, the logical primary feeder design (to permit maximum loading and area coverage) assigns the maximum limit (e.g., 125 V) to the customer nearest to the source (distribution substation) and the lowest limit to the customer farthest from the substation. Figure 8-1 is a single-line diagram of a residential feeder showing feeder components and location of the first and the last customer. To ensure that these voltage limits are maintained, there are several methods of regulating the voltage such as load tap-changing transformers, induction and step regulators, and switched capacitors (both shunt and series). All of these methods control or affect the flow of reactive power over the system (see Reference 8-8).

When PV systems, however, are connected to the utility distribution system, the problem of proper voltage regulation is complicated for several reasons:

(1) In present-day distribution systems with the flow of power in one direction only, it is much easier to ensure that the above conditions are met. It is necessary to analyze the one-way power flow on a radial distribution system to determine the voltage levels and I^2R losses within the system. With distributed PV sources on the system, such an analysis could become quite complicated. With reference to Figure 8-1, one can no longer assign the maximum allowable voltage limit (125 V) to the customer electrically nearest to the source. The obvious solution is that the power flow

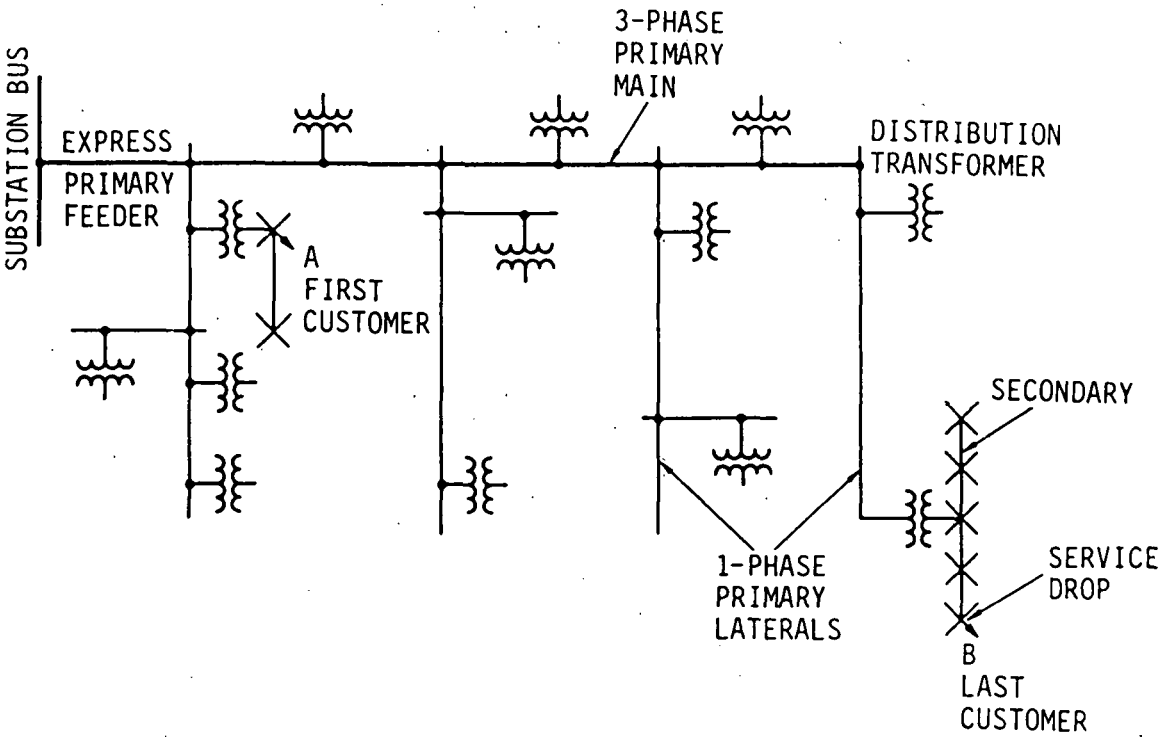

Figure 8-1. Residential Feeder Showing Feeder Components and Location of First and Last Customer

analysis would have to be done by using computer codes like the ones the utilities use for the analysis of their transmission systems. Better models will need to be developed for the PV systems, voltage regulators, and the loads.

(2) Line-commutated converters operate at lagging power factors. In other words, they draw reactive volt amperes (VARs) from the system. The utility system must be in a position to supply the additional VARs and the VARs needed to satisfy the load requirements. Because most of the real power demand of the loads is met by the PV systems, the utility system is left with supplying large amounts of reactive power but very little real power during high insolation levels. Thus, the system VARs will be greater than the real power (watts) seen by the utility system besides causing some secondary concerns such as higher I^2R losses and overloading of distribution system components. For line-commutated, small-, and medium-size systems with either individual or multiple users of the interconnected distribution, transformer voltage at out-of-tolerance conditions may occur. At the point of interconnection, the out-of-tolerance voltage is dependent upon distribution

transformer reactance. The higher the reactance, the greater the problem. This problem could be alleviated by using power factor correction capacitors at either the power conditioner output or at distribution voltage levels. Placement of capacitors is critical because resonances can develop. Care must be exerted in PCS filter design and utility power factor correction design to take into account low insolation conditions because overvoltages might be experienced at the point of interconnection on the system. A self-commutated inverter can be operated at a unity power factor or possibly even a leading power factor. At this stage, however, it is not clear that a unity power factor converter is the answer because the ratio of volt amperes to watts at the substation would still be rather high. Further research is required, particularly to determine the effects on voltage (load voltage limits and regulations) at the point of interconnection of the PV system to the utility.

8.5.3 Stability

Stability in the control theory sense refers to the ability of the control system to direct the system to a desired equilibrium state following a disturbance of any external stimulus. Source or system stability is defined as the ability of an individual or multiple PV systems (with different circuit designs) connected to the utility system to maintain operation without large fluctuations in voltage, power, etc., such as might result from improper controls or disturbance generated on a utility line. The assumption here is that the individual or multiple PV system power rating is far less than the feeder capacity.

Any such fluctuations in output parameters could cause nuisance tripping of the PV source following a disturbance. In some cases, it could also cause damage to the PV system. Any undesirable interaction between various PV systems connected to the same distribution system could cause nuisance tripping at the lateral feeder or substation level, causing unnecessary outages to customers. It could also result in damage to customer equipment connected to the system.

Currently, Purdue University, under contract with SNL, is studying single and multiple systems stability when interconnected to a utility system under steady-state, dynamic, and fault conditions.

8.5.4 Harmonics

The term "harmonics," as used in this document, is the maximum amount of voltage and/or current harmonics produced by a PV system (at its terminals) when connected to a utility power system. Harmonics (both current and voltage) have many undesirable effects associated with them. Excessive harmonics can cause problems with the utility power system with connected loads and with communication equipment (see Reference 8-9 and 8-11 and Appendix B).

Many sources of harmonics already exist on utility distribution systems. In general, devices with nonlinear operating characteristics produce harmonics. Some examples are transformer magnetizing currents, arc furnaces and welders, thyristor-controlled devices, and rectifiers.

PV sources connected to the grid will add to the level of harmonics on the system. Of the various types of dc-to-ac conversion alternatives available, two approaches commonly used by power conditioning systems produce different types of harmonics. The current-fed, line-commutated inverter produces current harmonics while the voltage-fed, force-commutated inverter produces voltage harmonics. In both cases, the level of harmonics is dependent on the characteristics of the inverter and the utility system impedance.

The set of harmonics frequencies produced by either type of converter is a function of the switching design and can be classified into the following categories:

(1) Characteristic harmonics: These harmonics are produced if ideal switchings occur within the inverter.

(2) Uncharacteristic harmonics: These harmonics are of the order other than (1) above that are caused from unbalanced line voltages, noise in the electronic circuits controlling the switching, and interactions of characteristics harmonics and fundamental currents in non-linear portions of the system.

(3) High-frequency harmonics: These harmonics in the tens of kHz range are produced due to semiconductor switching in the inverter.

The undesirable effects of harmonics are summarized below. No effort is made to isolate effects from voltage or current harmonics because they are essentially duals of each other, i.e., one produces the other.

(1) Overheating of capacitor banks due to lower impedance to higher order harmonics.

(2) Overheating in rotating machines and transformers. Harmonics influence motor torque also, but this effect is not thought to be signficant.

(3) Interference with utility ripple and carrier-current systems.

(4) Interference with voice communication (telephone interference).

(5) Overvoltage due to resonance.

(6) Instability in converter controls.

(7) Malfunctioning of protective relays.

(8) Errors in metering real and reactive energy.

(9) Malfunctioning of connected loads, such as computers.

The risk that any of the above undesirable effects of harmonics will manifest themselves depends largely on the characteristic of the utility and its connected load. Power conditioner designers currently face a great deal of uncertainty concerning the level of harmonics that are tolerable in given application.

One solution would be the establishment of a standard limit on harmonics for power conditioners. The IEEE Photovoltaic Systems Subcommittee has developed a trial standard (draft) for the interconnection of PV systems to a utility. This draft standard recommends harmonic levels of current to be under 5% and that harmonic voltage levels to be under 2% (THD) when connected to a specified utility impedance.

Research is needed to finally establish standards that balance the risk of problems with the cost of limiting harmonics. The research would involve determining the maximum allowable harmonic limits at any point on the system and translation of this number into an allowable harmonic injection (voltage or current) at the terminals of the converter. This limit would depend on the characteristics of the distribution system, background harmonic level from other sources on the system and, most importantly, to the penetration level (both local and system-wide) of PV sources. System simulation and field measurements are a necessary part of this research.

8.6 REFERENCES

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APPENDIX A

REACTIVE POWER FLOW

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The following discussion examines the relationship of power delivered to the utility by the PV system and reactive power required by the PV system from the utility. Conventional line-commutated inverters require reactive volt amperes from the utility and operate over a range of lagging power factors that are substantially below unity. Most self-commutated inverters by internal voltage control can be made to operate over a broad range of leading and lagging power factors, including unity. A mathematical explanation of the factors that determine PCS reactive VAR requirements and its associated resultant power factor is as follows.

Consider steady-state interaction between a single-phase (residential) PV system and the utility. Figure A-1 shows such an interaction while Figure A-2 shows corresponding vector diagram. Assume that the effect of harmonics is ignorable, the resistance in the circuit is small, and the total reactance is x. If the utility voltage V is used as a reference and the inverter voltage with respect to this reference is $E\angle\theta$, then the current,

$$I = \frac{E\angle\theta - V\angle 0}{jx} = \frac{E}{x}\angle\theta - 90^\circ - \frac{V}{x}\angle -90^\circ = \frac{E}{x}\sin\theta + j\frac{(V - E\cos\theta)}{x} \quad (1)$$

Therefore, in-phase component of I, $I_p = \frac{E}{x}\sin\theta$

and quadrature component of I, $I_q = \frac{V - E\cos\theta}{x}$

Volt-ampere, S_s, supplied by the inverter (source):

$$S_s = P_s + jQ_s = E\angle\theta \cdot I^* \quad (2)$$

where * indicates mathematical conjugation of a complex number and the subscript, s, refers to source.

On simplifying,

$$P_s = \frac{EV}{x}\sin\theta \quad (3)$$

$$Q_s = \frac{E(E - V\cos\theta)}{x} \quad (4)$$

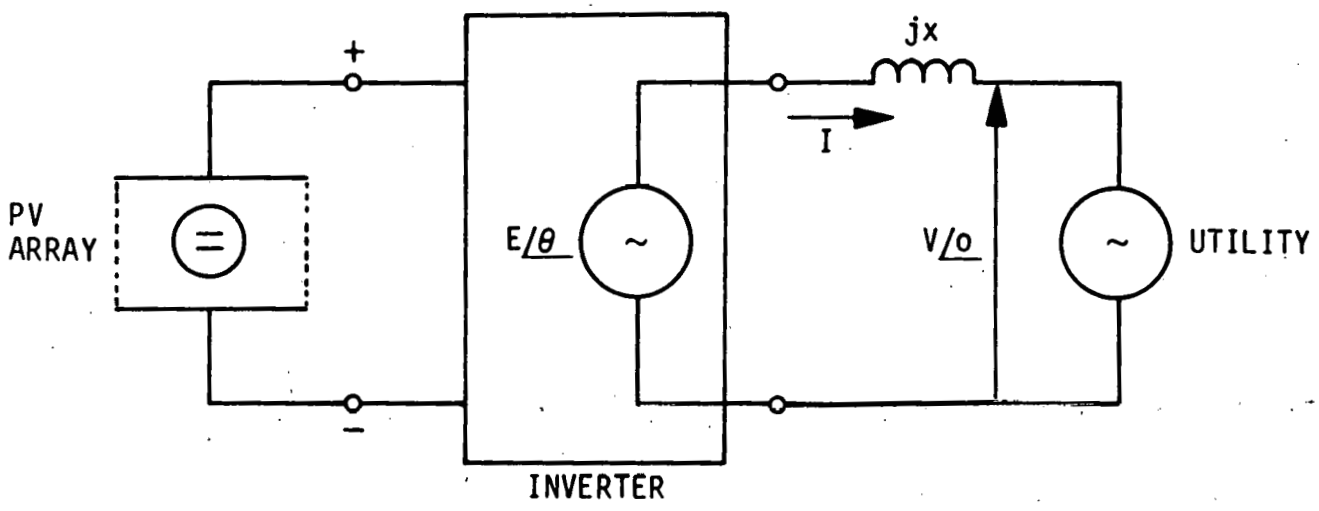

Figure A-1. A Simplified Representation of Photovoltaic System and Utility Interaction

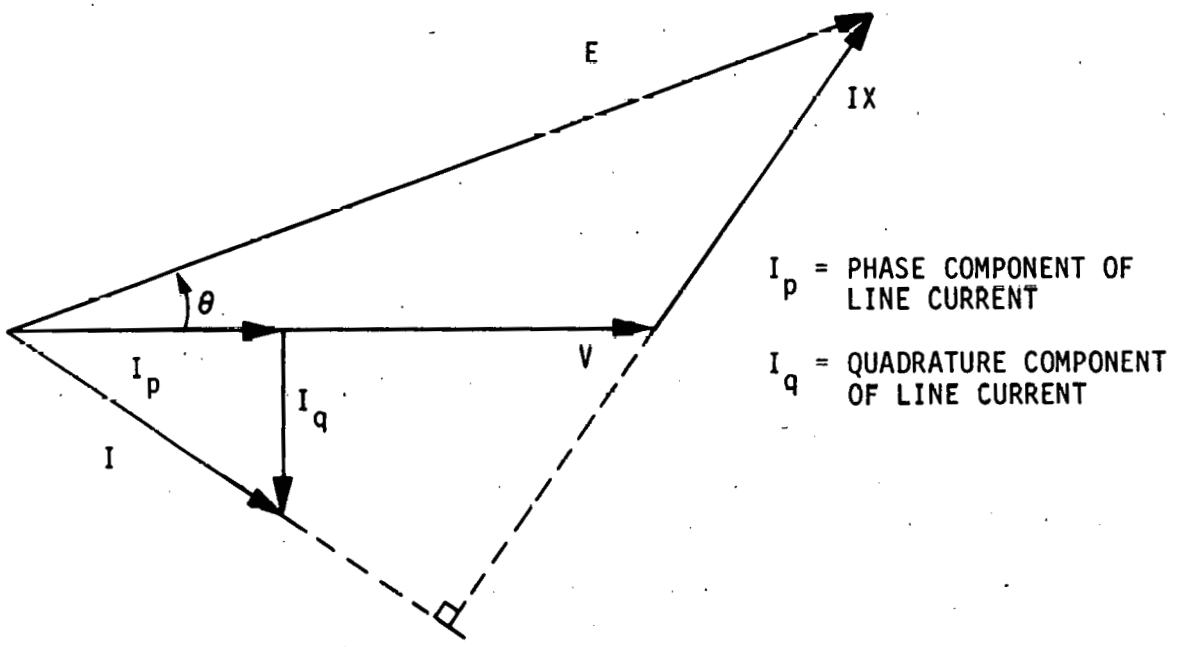

Figure A-2. Vector Diagram for Circuit Shown in Figure A-1

Clearly, $Q_s<o$ or $Q_s>o$ according as $E<V \cos \theta$ or $E>V \cos \theta$, respectively.

$$I_p = \frac{E}{x} \sin \theta \tag{5}$$

$$I_q = \frac{V-E \cos \theta}{x} \tag{6}$$

$$\text{and } |I| = \left(I_p^{\,2} + I_q^{\,2}\right)^{\frac{1}{2}} = \frac{(E^2 + V^2 - 2EV \cos \theta)^{\frac{1}{2}}}{x} \tag{7}$$

Inverter power factor = $\cos(\theta + \tan^{-1} \frac{QS}{P_s})$, lagging.

Volt-amperes, S_r, received by the utility:

$$S_r = P_r + jQ_r = V \angle \theta . I^*$$

therefore, $P_r = \frac{EV \sin \theta}{x} = P_s$

$$Q_r = \frac{EV}{x} \cos \theta - \frac{V^2}{x} = \frac{V(E \cos \theta - V)}{x}$$

Reactive power loss in the line,

$$Q_{loss} = \Delta Q = Q_s - Q_r = \frac{E^2 + V^2 - 2EV \cos \theta}{x} = |I|^2 x$$

Power factor at the utility = $\cos \left(\tan^{-1} \frac{I_q}{I_p}\right) = \cos (\tan^{-1} \frac{Qr}{Pr})$, lagging

It is important to note that the power flow to the utility is adjusted by changing the relative phase angle θ between the inverter voltage and the utility voltage. Therefore, to meet real power demand of the load, the angle θ may be such that the inverter may require VARs. Increasing the phase angle θ will increase the IX drop for the same value of V and E. As a result, I increases along with Q_{loss}, $|I|^2x$. The possibility of VAR demand by the PV system is an operational constraint on the utility.

Similar analyses can be carried out for other conditions, and the effects due to resistance or harmonics current flow can be determined.

APPENDIX B

THEORY OF HARMONIC DISTORTION

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The presence of harmonics in the source voltage and current affects the performance of a network in terms of load voltage, line current, and power factor. The following discussion examines effects of harmonic currents and voltage generated by a photovoltaic system connected to a utility system. Consider a simple circuit as shown in Figure B-1 and assume that the circuit consists of linear and lumped elements and that the principle of superposition holds.

$$\text{Let } V_s(t) = \sum_{n=1}^{\infty} \sqrt{2}\, V_n \sin(nwt) \text{ be the source voltage}$$

where

V_n = RMS value of its nth harmonic component
ω = fundamental radian frequency

Therefore, circuit impedance due to the nth harmonic voltage component

$$Z_n = (r + R) + jn(w\ell + wL) = (r + R) + jn(x + X) \tag{1}$$

where x and X are fundamental frequency reactances due to the line inductance, ℓ, and the load inductance, L, respectively. r and R are line and load resistances, respectively, that are assumed constant at all harmonic frequencies.

Therefore, current $i_n(t)$ due to the nth harmonic voltage component,

$$i_n(t) = \frac{\sqrt{2}\, V_n}{[(r + R)^2 + n^2(x + X)^2]^{1/2}} \sin(nwt - \phi_n) \tag{2}$$

where

$$\text{phase angle, } \phi_n = \tan^{-1}\left[\frac{n(x + X)}{r + R}\right] \tag{3}$$

$$\text{Total current, } i(t) = \sum_{n=1}^{\infty} i_n(t) = \sum_{n=1}^{\infty} \frac{\sqrt{2}\, V_n}{[(r+R)^2 + n^2(x+X)^2]^{1/2}} \cdot \sin(nwt-\phi_n)$$

$$= \sum_{n=1}^{\infty} \sqrt{2}\, I_n \sin(nwt - \phi_n) \tag{4}$$

where I_n is the RMS value of current due to the nth harmonic voltage. It can be shown that:

$$\text{RMS value of } i(t) = I = \left(\sum_{n=1}^{\infty} I_n^2 \right)^{1/2} \tag{5}$$

but RMS value of fundamental frequency current,

$$I_1 = \frac{\sqrt{2}\, V_1}{[(r + R)^2 + (x + X)^2]^{1/2}} \tag{6}$$

Therefore, total harmonic distortion, THD, defined as

$$= \frac{1}{I_1} \left(\sum_{n=2}^{\infty} I_n^2 \right)^{1/2} = \left[\sum_{n=2}^{\infty} \left(\frac{I_n}{I_1} \right)^2 \right]^{1/2} = \left[\sum_{n=1}^{\infty} \left(\frac{I_n^2 - I_1^2}{I_1^2} \right) \right]^{1/2} \tag{7}$$

RMS voltage across the load

$$V_L = \sum_{n=1}^{\infty} \frac{\sqrt{2}\, V_n (R^2 + n^2 X^2)^{1/2}}{[(r + R)^2 + n^2 (x + X)^2]^{1/2}} \tag{8}$$

$$\text{Power delivered to the load, } P_L = I^2 R = R. \sum_{n=1}^{\infty} I_n^2 \tag{9}$$

$$\text{Load power factor} = \frac{P_L}{V_L . I} \tag{10}$$

Fundamental frequency load power factor, $\cos \phi_1$, is related to power and current at fundamental frequency by the equation:

$$P_1 = V_L . I . \text{Cos } \phi = I_1^2 . R \tag{11}$$

For the same load power, $P_1 = P_L$, the load power factor can be obtained using Equations (10) and (11).

$$\text{Load power factor} = \frac{I_1}{I} \cdot \cos \phi_1 \qquad (12)$$

But from Equations (5) and (7)

$$\frac{I^2}{I_I^2} = 1 + THD^2$$

or

$$\frac{I}{I_1} = \left(1 + THD^2\right)^{1/2}$$

Therefore, using Equation (12)

$$\text{Load power factor} = \mu \cos \phi_1 \qquad (13)$$

where μ = distortion factor = RMS value of the fundamental component of the load (or line) current divided by the RMS value of the total load (or line) current, or

$$\mu = \frac{I_1}{I} = \frac{1}{(1 + THD^2)^{1/2}} \qquad (14)$$

ϕ_1 is also the angle between the source voltage and the fundamental component of the load (or line) current. Therefore, $\cos \phi_1$ is also called displacement factor or fundamental component power factor.

If the effect of harmonic summation on the utility grid is to be analyzed, each PV source interconnected with the grid has to be mathematically represented, and individual harmonic currents have to be computed to determine the total harmonic current injection into the grid. Figure B-2 depicts such an approach. Knowing open-circuit voltages of all PV sources and their Thevenin's impedances, the problem of determining total harmonic currents is equivalent to calculating values of individual harmonic currents and finding their summation. It should be noted, however, that the total harmonic content depends on two factors: (1) the harmonics produced by each inverter and (2) the total impedance presented by the utility and the connected loads at harmonic frequencies.

At this time, there is only limited data base available to provide sound engineering foundation for the setting of harmonic voltage limits. A total current harmonic content of 5% of fundamental value and a total harmonic voltage content of 2% appears to be an acceptable limit at the present time (References 4-5, 4-6).

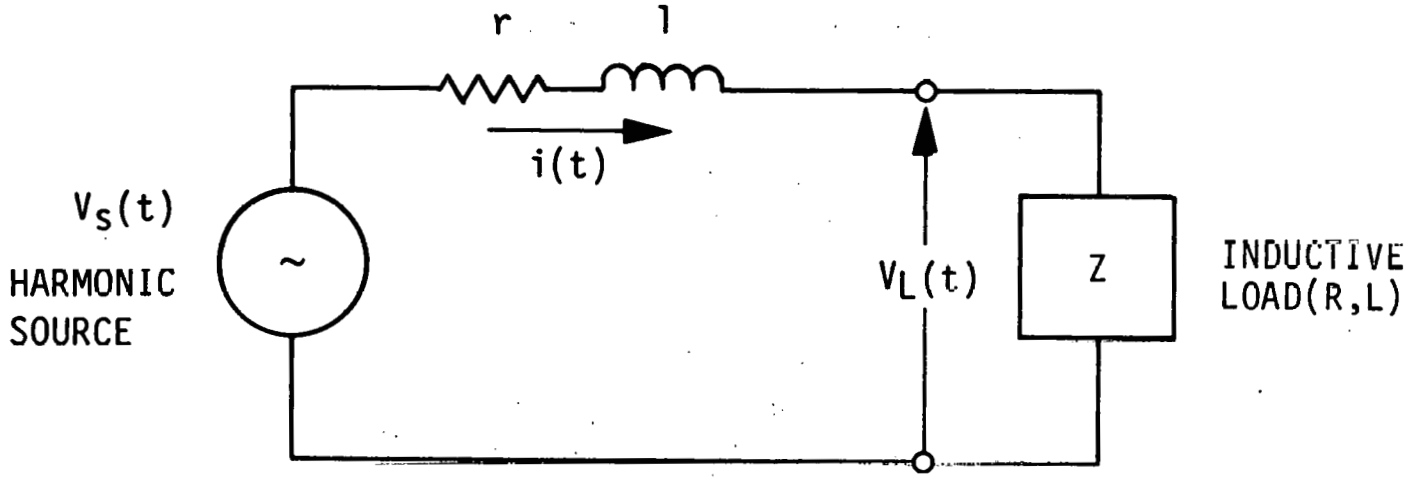

Figure B-1. A Circuit Showing an Impedance Load-Connected to a Harmonic Source through an Inductive Line

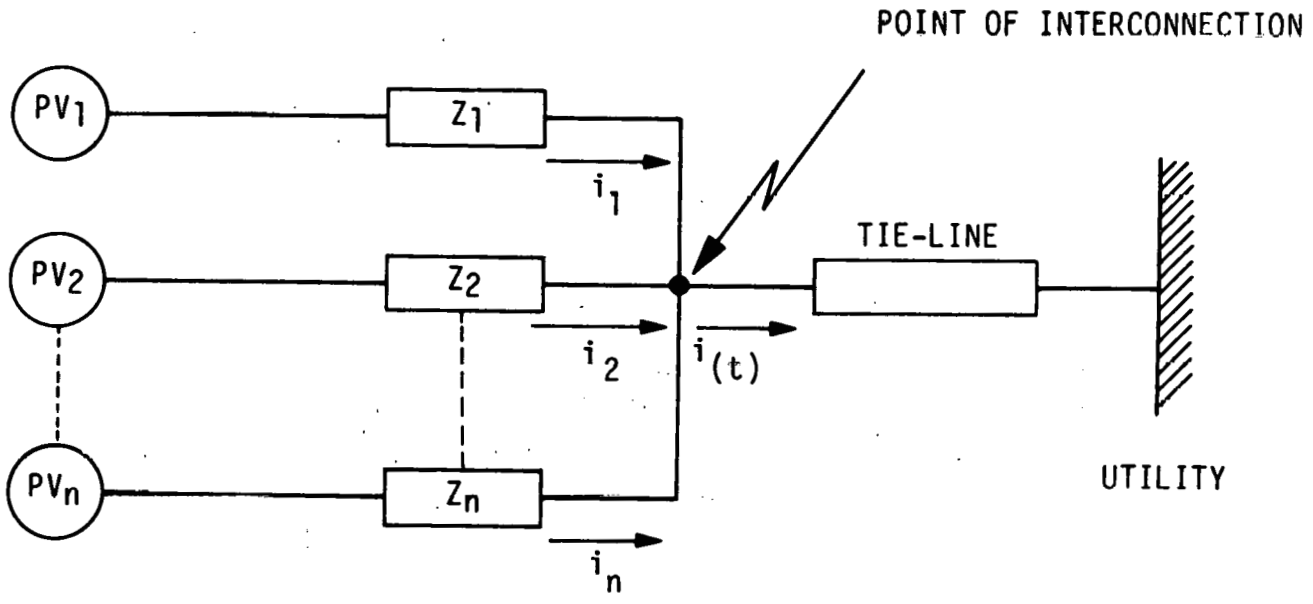

Figure B-2. Harmonic Summation on the Utility Grid

APPENDIX C

POWER CONDITIONERS

AVAILABLE FOR PHOTOVOLTAIC APPLICATIONS

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MANUFACTURER ADDRESS TELEPHONE NUMBER	TRADE NAME & POWER RANGES SINGLE PHASE UNITS	TYPICAL MODEL MAIN FEATURES OPTIONS & WEIGHT/POWER RATIO	INPUT (VOLTS dc)	OUTPUT (VOLTS ac)	EFFICIENCY PERCENT	OUTPUT CURRENT WAVEFORM & HARMONIC DISTORTION	POWER FACTOR	ARRAY VOLTAGE CONTROL	WEIGHT (LBS) SIZES (INS) W X D X H COSTS ($)
Abacus Controls, Inc. P.O. Box 893 Somerville, NJ 08876 (201) 526-6010	"Sunverter" 2kW to 10kW	Model 463-4-200 5kW Stand-Alone (SA) Utility Interactive (UI) Battery Option Available 53#/kW	150-240 200 Nominal	120/240	87% and Greater Above 1/5 load	Sine Wave <5% @ Full Power	Fixed at .98 in UI, Load Responsive in SA Mode	Auto tracks Pilot Cell Except in Battery Mode	320# 6kW 24x30x52 Free Standing $9400
American Power Conversion Corp. 89 Cambridge Street Burlington, MA 01803 (617) 273-1570	"Sunsine" 2kW 4kW	Model UI-4000 4kW - UI Only SA in FY83 30#/kW	210-300 230 Nominal	240	90% at Full Load	Sine Wave <5% @ Full Pwr	Unity Only	Auto tracks for Max. dc	118# 13x10x24 Wall Mount $7950
Alpha Energy Systems 7038 Convoy Court San Diego, CA 92111 (619) 292-7811	"Solar Inverter" 3kW	Model SI-3000, kW UI Battery Compatible SA Optional 13#/kW	38-58 48 Nominal	120/240	90% and Greater Above 1/2 Load	Sine Wave <5% @ Full Pwr	Accommodates Pwr Factor of .98 Lead or Lag	Auto tracks for Max. ac Pwr.	39# 10x7x14 Wall Mount $3000
Advanced Energy Corp. 14933 Calvert Street Van Nuys, CA 91411 (213) 782-2191	No Trade Name .5kW to 4kW	Model 4048 4kW SA Only Battery Compatible 31#/kW	38-58 48 Nominal	120/240 Regulated ∓2%	80% and Greater Above 1/2 Load	Quasi Sine Wave >15% (Optional Filter)	Load Responsive .7 Lag to Unity	Battery Dependent	125# 20x10x24 Wall Mount $2795
Acheval Wind Elect. 361 Aiken Street Lowell, MA 01854 (617)453-0874	"Silci" 1kW to 12kW	Model 225/10kW 10kW - UI Only 10#/kW	200-225	240	95% and Greater Above 1/10 Load	Quasi Sine Wave >15%	.6-.7 Lagging	Fixed at Factory	95# 15X8X24 Wall Mount $2400
Best Energy Systems P.O. Box 280, Rt.1 Necedah, WI 54646 (608) 565-7200	"Best" .5kW to 12kW	Model M36-3800 3.8kW - SA Only Battery Compatible 39#/kW	31.5 - 43 36 Nominal	120/240	90% and Greater Above 1/4 load	Quasi Sine Wave >15%	Load Responsive .7 Lag to .7 Lead	Battery Dependent	147# 21x10x22 Free Stndg Mnt or Wall $2887
Helionetics, Inc. 17312 Eastman Street Irvine, CA 92714 (714) 546-4731	"DECC" 2kW to 12kW	Series 61289-3 6kW - UI Only 33#/kW	170-230 200 Nominal	120/240	92% or Greater Above 1/2 Load	Sine Wave 2% of Rated Current	Factory Set for Unity Has sw. to Select Leading	Auto tracks for Max. ac Power	200# 21x17x23 Free Standing Cost N/A
Soleq Corp. 8969 N. Elston Avenue Chicago, IL 60646 (312) 792-3811	"Soleq" 1.5kW to 48kW	SWI-112-6K-60 6kVA SA Only Battery 83#/kW	98-140	120/240	90% and Greater Above 1/2 Load	Sine Wave <5%	Load Responsive .7 Lag to .7 Lead	Battery Dependent, Auto Option Available	500# 30x17x30 Free Stndg $10658
Windworks, Inc. Rt.3, P.O. Box 44-A Mukwonago, WI 53149 (414)363-4088	"Gemini" 2kW to 15kW	SI-40-24V-31 8kW UI Only 20#/kW	100-200	240	95% and Greater Above 1/2 Load	Quasi Sine Wave >15% 5% with filter	.8 Lagging @ F.L. .65 Lag @1/4 F.L. Unity with filter	Array Voltage Field Adjustable	160# 24x12x30 Wll Mt Isltn XFMR 130# 12x10x19 $9384

*In this survey, the costs given are current as of November 1982

Compiled at Sandia National Laboratories from Manufacturers' Information - November 1982
F. B. Brumley - Div. 2364

Figure C-1. Power Conditioners Available for Residential Photovoltaic Applications *

*U.S. GOVERNMENT PRINTING OFFICE:1984 -746 -081/2612 REGION NO. 4

MANUFACTURER ADDRESS TELEPHONE NUMBER	POWER RANGES	TYPICAL MODEL MAIN FEATURES & WEIGHT/POWER RATIO	INPUT (VOLTS dc)	OUTPUT (VOLTS ac) All are 3φ	EFFICIENCY PERCENT	OUTPUT CURRENT WAVEFORM & HARMONIC DISTORTION	POWER FACTOR	ARRAY VOLTAGE CONTROL	WEIGHT (LBS) SIZE (INS) W X D X H COSTS $kW
Abacus Controls, Inc. P.O. Box 893 Somerville, NJ 08876 (201) 526-6010	18 to 30kW	30kW Model Utility Interactive (UI) Stand alone (SA) (self-comm) 50#/kW	160 - 240	277/480 3 or 4-Wire	90% Above 40% Load	Sinewave 60 HZ or 50 HZ <5% at Full Power	Fixed at .98	Automatic Tracking	1500#(60 HZ) 1600#(50 HZ) 48x30x72 $1500/kW
Garrett Corporation Airesearch Mfg.Co.Div. 2525 W.190th Street Torrance, CA 90509 (213) 512-4091	200kW to 2.5MW	200kW Airesearch Model SA Only (self-comm) Battery Compatible 40#/kW	350 - 575	277/480 4-Wire	91% at Full Load 87% a t Half Load	Quasi Sinewave ±.1HZ <5% (with Filter)	.95 Lead to .8 Lag	Automatic Tracking (Optional) or Array Voltage Fixed at Factory	800# 90x30x108 $800/kW
Hellonetics, Inc. 17312 Eastman St. Irving, CA 92714 (714)546-4731	75kW to 500kW	DECC Model 61264 75kW UI & SA (self-comm) 60#/kW	200 - 280 400 Max	277/480 3-Wire	93% at Full Load 92% at Half Load	Sinewave <3% at Full Pwr	.98 Adjustable	Automatic Tracking	4500# 84x76x36 $1000/kW
Nova Electric Mfg.Co. 263 Hillside Ave. Nutley, NJ 07110 (201) 661-3434	50kW	Model 30k 30kW UI & SA (self-comm) 100#/kW	100 - 600	277/480 4-Wire	90% at Full Load 85% at 1/2 Load	Sinewave 2%	.8 Lead to .8 Lag	Voltage Field Adjustable	3000# 30x30x72 $1000/kW
Power Systems & Control 1730 Lanvale Ave. Richmond, VA 23330 (804) 355-2803	250kW	250kW Model UI & SA (self comm) 60#/kW	260 - 465	480 Vac 3-Wire	92% at Full Load 88% at 1/4 Load	Sinewave <3.5%	Fixed at Unity	Automatic Tracking	15,000# 180x79x39 Cost by negotiations
United Technologies P.O. Box 109 So. Winsor, CT 06074 (203) 727-2210	40kW to 1MW	40kW Model SA (self-comm) UI with Grid Connect Option" 25#/kW	130 - 260	120/208 Vac 4-Wire	92% at Full Load	Sinewave	.85 Lag at Full Load	Automatic Tracking (optional)	1000# 48x41x22 Contr. Negotiations Only
Westinghouse Elec. Corp. P.O. Box 989 Lima,OH 45802 (419)266-3159	62.5kVa	AV1-623 62.5kVa UI & SA Battery compatible (self-comm) 30#/kW	200 - 300 350 Max	120/208 Vac 4-Wire	91% @ Full Load 88% @ 1/4 Load	Sinewave 5% Max 1% any Single Harmonic	.9 Lead to .7 Lag	Automatic Tracking up to 300V at Input	1830# 33x33x82 $1150/kW
Windworks, Inc. Rt. 3, P.O. Box 44-A Mukwonago, WI 53149 (414) 363-4088	50kW to 1MW	Model S6-125-480-31 50kW UI Only (line-comm)	200 - 400	480 Vac 3-Wire	95% at Full Load 80% at 1/10 Load	Quasi-Sine 10% at Full Power	.85 Lag at Full Load	Array Volt is field adjustable Max. Pwr Tracking Option Available	Wt & Size Unavailable $400/kW

*Prices given are estimates. Actual per kW cost will vary with options, number of units purchased time of order & market factors.

Compiled from manufacturer's information at Sandia National Laboratories - November 1982
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Figure C-2. Power Conditioners (15 WE to 1 MW) Available for Photovoltaic Applications*