Physical and electrical properties of noncrystalline Al_2O_3 prepared by remote plasma enhanced chemical vapor deposition

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Noncrystalline Al_2O_3 dielectric films have been synthesized by remote plasma enhanced chemical vapor deposition (RPECVD) and deposited on (i) H-terminated Si(100) and (ii) on SiO_2 prepared by remote plasma assisted oxidation and RPECVD on Si(100) substrates using organometallic source gases injected downstream from a He/O_2 plasma. Chemical composition and morphology of the Al_2O_3 films and their interfaces have been studied by Auger electron spectroscopy (AES), Fourier transform infrared spectroscopy, nuclear resonance profiling (NRP), and x-ray diffraction (XRD). Previous studies in which Al_2O_3 was deposited by thermal CVD, rapid thermal CVD, (RTCVD), direct PECVD, and physical vapor deposition generally resulted in relatively thick SiO_2 or Al-silicate interfacial layers which impact adversely on the highest attainable capacitance. In line AES and NRP indicate the as-deposited RPECVD films are fully oxidized on deposition, and their interfaces can be chemically abrupt with Si oxide or Al silicate interfacial layers that are no more than 0.6 to 0.8 nm thick. However, these relatively abrupt interfaces do not ensure good device performance. Electrical measurements indicate negative fixed charge on the order of 10^{12} charges/cm^2. The fixed charge resides at the Al_2O_3 interface, and can be moved away from the silicon substrate by deposition of a thin, ~1–2 nm, intermediate layer of RPECVD SiO_2. © *2001 American Vacuum Society.* [DOI: 10.1116/1.1379316]

I. INTRODUCTION

As device dimensions are scaled according to the 1999 Technology Roadmap for Semiconductors,[1] the equivalent gate oxide thickness, EOT, must decrease below about 1.5 nm. At this thickness of SiO_2, the direct tunneling current for a one volt potential drop across the oxide is >1 A/cm^{-2} and begins to reduce the ratio of on- to off-state current in a field effect transistor. To reduce the off-state leakage currents due to tunneling through silicon dioxide and maintain a capacitance equivalent to what is obtained with a SiO_2 dielectric with a physical thickness of 1.5 nm and below, alternative high-*k* dielectrics are being investigated (see Refs. 2, 3, and references therein). These high-*k* alternative dielectrics will yield the required levels of EOT for device scaling at larger physical thickness, thereby providing a materials pathway for reducing the tunneling current. Other factors such as conduction band offset energies also play a role in determining the tunnel leakage, and these generally decrease with increasing *k*.

Recently aluminum oxide has been the focus of several studies. Klein *et al.*[4] studied the deposition of Al_2O_3 with a chemical vapor deposition (CVD) growth method. Their work reports evidence for a silicate layer at the interface between the Al_2O_3 film and silicon substrate as measured by nuclear resonance profiling (NRP) and x-ray photoelectron spectroscopy (XPS). Gusev *et al.*[5] reported work on atomic layer CVD (ALCVD) Al_2O_3 where they investigated both the physical and electrical properties of the deposited films. Based on NRP, medium energy ion scattering, (MEI) and high-resolution transmission electron microscopy results, they showed it was possible to deposit Al_2O_3 on H-terminated silicon substrates without forming an interfacial oxide or silicate layer.

Transistors with an equivalent gate oxide thickness of 0.96 nm with Al_2O_3 oxide as the gate dielectric material have been fabricated by Chin *et al.*[6] These devices indicated $D_{it} \geqslant 3\times{}^{10}$ cm^{-2} and a positive flat band shift, indicating interfacial negative fixed charge. Buchanan *et al.*[7] reported work on *n*-MOSFETs formed by ALCVD Al_2O_3 with 0.08 μm gate lengths. They also observed a negative fixed charge for devices with an equivalent oxide thickness of 1.3 nm.

This article focuses on noncrystalline thin films of Al_2O_3 and its physical and electrical properties. The dielectric constants of these films are approximately 9 (Ref. 3), and based on the dielectric constant ratio of ~2.4 between Al_2O_3 and SiO_2, dielectric films can be at least two times thicker for the same capacitance. However, recent XPS measurements have indicated that the band offset energy between the conduction bands of Si and Al_2O_3 is about 2.1 eV, or about 1 eV lower

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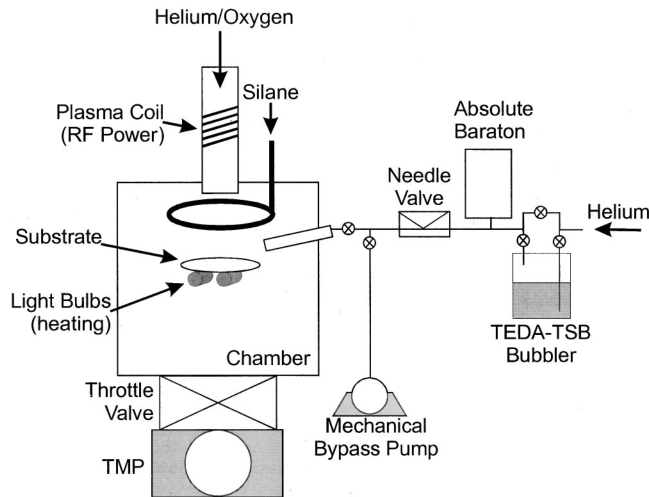

FIG. 1. Physical configuration of the RPECVD deposition chamber is shown.

than for SiO_2 and Si.[8] Based on the tunneling through a simple trapezoidal or rectangular barrier, this reduces the amount of direct tunneling current reduction to what is attainable with a physical thickness reduction corresponding to an effective *k*-value (based on a 3.15 eV offset) of about 7.5. This is still technologically significant and therefore of interest in the device community.

II. EXPERIMENTAL METHODS

Aluminum oxide was deposited using a remote plasma enhanced CVD (RPECVD) technique.[9] The aluminum source is a liquid metal organic, triethyldialuminum tri-sec-butoxide (TEDA-TSB),[10] contained in bubbler setup. The carrier gas is helium. The pressure in the bubbler is held at 30 Torr and is maintained by closed loop control using an absolute baratron and a needle valve (Fig. 1). The temperature of the bubbler assembly is held at 75 °C by a silicone oil bath. The setup and operation of the bubbler is described in Ref. 11. The aluminum source vapor is injected into the chamber through a heated injector assembly located to the side of the sample.

A mixture of helium and oxygen is excited by 30 W of rf power at 13.56 MHz and is injected directly above the substrate. The substrate is held at 300 °C in order to desorb any organic molecules from the surface. The pressure in the chamber is controlled to 0.3 Torr. 2% silane, SiH_4, in He is injected via a ''showerhead'' ring below the plasma tube, and replaces the TEDA-TSB flow for the deposition of SiO_2 films.

For electrical measurements, field isolation metal–oxide–semiconductor (MOS) capacitors were fabricated on 0.06–0.08 Ω cm boron doped Si, and 0.02–0.05 Ω cm phosphorous doped Si substrates. Prior to the Al gate metal contact evaporation, the samples were annealed at 800 °C for 30 s using an AG Associates minipulse rapid thermal annealer. As will be discussed, annealing at 900 °C results in the crystallization of the Al_2O_3 film, so that after the 800 °C anneal the Al_2O_3 films remain amorphous. It has been shown for SiO_2 films deposited by RPECVD, that a rapid thermal anneal at a temperature of ~900 °C for approximately 30 s to 1 min is necessary to promote structural and chemical relaxation of the film,[12] so that the anneal for Al_2O_3 is not optimized for a low defect density the Si–SiO_2 that is used in some of the electrical measurements. A 30 min post metallization anneal in a forming gas mixture of 10% H_2 in N_2 at 400 °C concluded the sample preparation.

The films for the Fourier-transform infrared spectroscopy (FTIR) and x-ray diffraction (XRD) characterizations were >100 nm thick and were annealed with the same rapid thermal annealer temperature-time cycles as the MOS capacitors. Auger electron spectroscopy (AES) was preformed *in situ*. Interrupting the deposition every 10 s and scanning with AES, we were able to investigate the formation of the aluminum oxide and silicon substrate interface.

The Al_2O_3 interfaces with HF last, H-terminated Si, and with SiO_2 interfacial layers were investigated using resonant NRP.[13] The narrow, isolated resonance at 404.9 keV[14] in the cross section curve of the $^{27}Al(p,\gamma)^{28}Si$ nuclear reaction was used to obtain Al concentration depth distributions. The measured excitation curves, i.e., gamma-ray yield versus incident proton energy, in the vicinity of the resonance energy were converted into concentration profiles using the SPACES program,[15] which is based on stochastic theory of energy loss of ions in solid. By measuring the excitation curves for thin and thick aluminum films, the nuclear reaction resonance at 404.9 keV was determined to be narrower than 40 eV. A sample geometry with a tilt 65° with respect to the incident beam, was used to increase depth resolution. Several factors contribute to the quantitative aspects of depth resolution: (i) the extremely narrow nuclear reaction resonance at 40 eV, (ii) the significant energy loss of 405 keV protons in Al_2O_3, approximately 380 $keV\,mg^{-1}\,cm^{-2}$, if a density of 3.98 $g\,cm^{-3}$ is assumed, (iii) the low energy spread of the proton beam (a Gaussian lineshape with approximately 80 eV full width at half maximum (FWHM) at the resonance energy of 405 keV), as provided by the 500 keV HVEE ion implanter at Porto Alegre, Brazil, and (iv) an effective thickness magnification factor of 2.4 due to the tilted geometry. The ultimate resolution is limited by energy straggling and angular multiple scattering processes. In the present study, the depth resolution was estimated to be 0.4–0.5 nm near the surface, which degraded to about 0.6 to 0.8 nm near the buried Al_2O_3 interface.

The silicon profiles were determined by NRP using the narrow, isolated resonance approximately 414 keV ($\Delta R = 100$ eV) for the $^{29}Si(p,\gamma)^{30}P$ nuclear reaction.[13–15] Using a tilt angle of 60° sample the depth resolution is 0.7 nm at sample surface, which degrades to approximately 1.0 nm at a depth of 8.0 nm into the film. The excitation curves and the profiles determined by SPACES simulations are shown in Figs. 3 and 4.

The capacitance–voltage measurements were performed by a HP 4284A LCR meter at 1 MHz. The current–voltage measurements were preformed by a HP 4140B voltage

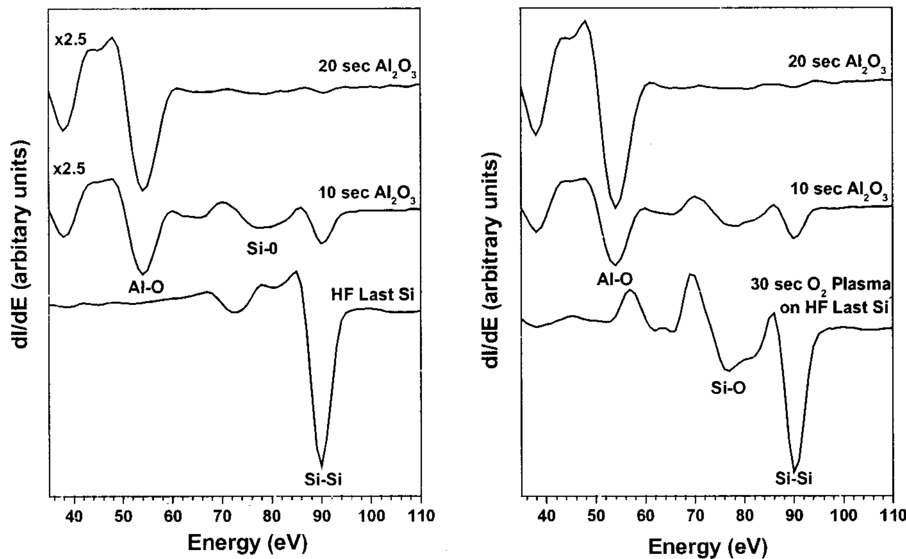

FIG. 2. AES of aluminum oxide deposition on HF last silicon and 0.6 nm of silicon dioxide on HF last silicon are presented.

source with a picoammeter and voltage ramp of $dV/dt = 0.05$ V/s. Both types of measurements were preformed at 25 °C in a light tight box.

III. EXPERIMENTAL RESULTS AND DISCUSSION OF THE REDUCED DATA

A. Interface formation: AES and NRP

The AES spectra are shown in Fig. 2 display the evolving chemical composition and bonding at the Si interface and within the deposited Al_2O_3 thin film. The left-hand side plot is for Al_2O_3 deposited directly on HF last, H-terminated Si. The right-hand side plot is for Al_2O_3 deposited on 0.6 nm of SiO_2 that was formed by remote plasma assisted oxidation, i.e., exposing the HF last silicon for 30 s to active O atoms and metastable molecules extracted from a remote He/O_2 plasma discharge. The thickness of the interfacial SiO_2 layer was determined by comparing the relative amplitudes of the Si–O (76 eV) and the Si/Si (91 eV) AES features.[16]

After the deposition of Al_2O_3 for 10 s of the two AES spectra in Fig. 2 are essentially the same. In particular, the ratio of the intensities of the Si–O and Si–Si features indicates that approximately 0.6 nm of SiO_2 was formed during the initial stages of the Al_2O_3 deposition on to HF last Si. In addition, the lineshape of the Al–O feature at ~55 eV does not change with increasing deposition time. It is a single peak and located at an energy consistent with aluminum bonded to oxygen.[17] From this, we can conclude the Al atoms are not bonded to Si atoms at the interface, and that the Al is fully oxidized throughout the deposited film.

NRP independently demonstrates that Al_2O_3 interface on HF last Si is abrupt, with the spread of Al atoms into the interfacial Si oxide layer being less than 0.6–0.8 nm, the limiting resolution of the NRP measurement. This estimate is based on the spread of the proton beam within the film. Figure 3 is the NRP study for the deposition of Al_2O_3 directly onto HF last Si. The lower traces with the experimental points are the gamma ray yield data, and the upper portions of Fig. 3 display the calculated and normalized concentrations of Al and Si as a function of depth;[13–15] the normalized concentrations are 1.0 for both Al_2O_3 and bulk Si.

For the deposition of Al_2O_3 on the HF last Si, there is an abrupt drop in the Al concentration followed by a rapid onset of the Si concentration. If we take the intersection of the Al and Si concentrations as the where, the location of the plane where the interfacial layer begins, then the bulk Si concentration is reached in <1.0 nm. There are essentially no changes in the experimental data or in the Al and Si concentrations after annealing at 800 °C. This means there is no detectable intermixing of the Al_2O_3 and SiO_2 and the transition regime remains abrupt.

Figure 4 contains NRP data and Al and Si concentrations for the deposition of Al_2O_3 onto a RPECVD SiO_2 layer. The shoulder in the Si concentration profile indicates the thickness of the SiO_2 layer, ~2 nm. There are changes in the abruptness of the Al profile before and after the 800 °C anneal indicating the intermixing of the deposited Al_2O_3 and SiO_2 films. Since the two traces in Fig. 4 come from different regions of the same wafer, and since the deposited Al_2O_3 were not of uniform thickness across the entire wafer, the extent of the mixing is best estimated from the changes in the abruptness of the interfacial profiles of both the Si and Al atoms. Based on this subjective analysis of the profiles, the internal transition layer thickness is of the order of 1 nm, or approximately three molecular layers, thick.

B. Bulk oxide characterization

Bulk characterization was carried out using FTIR and XRD. The films for these studies were >100 nm thick. The features in the FTIR spectra are bond specific and give information of coordination as well, whereas the XRD spectra can be used to determine the onset of crystallization, i.e., the transition from a noncrystalline or amorphous film to a crystalline or partially crystallized film. Based on FTIR and

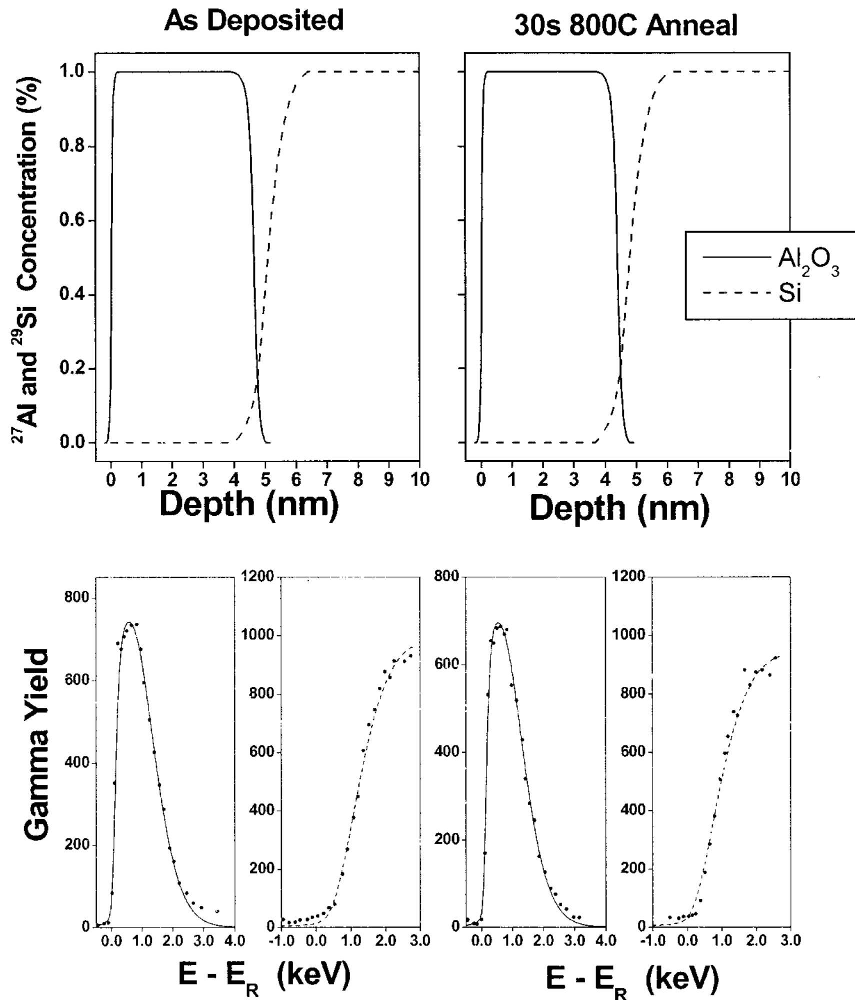

FIG. 3. NRP for Al_2O_3 on HF last silicon is shown where the scale is normalized to Al_2O_3 and bulk silicon.

XRD data shown in Figs. 5 and 6, we observe that after the 900 °C anneal, the coordination of the Al atoms has changed, and the film has crystallized.

Figure 5 displays two FTIR spectra for an as-deposited film and for a film annealed at 900 °C. FTIR spectra of films annealed at 600, 700, and 800 °C were essentially the same as that of the as-deposited film and are not displayed in Fig. 5. The features in the FTIR spectra after the 900 °C are in the spectral regime of features previously identified in crystalline Al_2O_3 in the corundum structure.[18] The broad feature in the as-deposited film results from both Al and O atom motions, whereas the sharper feature in the 900 °C spectrum is due mostly to O-atom motion. The shift of the spectrum to lower wave numbers is consistent with (i) an increase in the average coordination of the Al atoms from ~4.5 in the noncrystalline state,[19] to 6 in the corundum or α-Al_2O_3 structure, and (ii) an increase in the ionic character of the bonding that accompanies the increase in average coordination of the Al and O atoms.

For as-deposited films, and those annealed up to 800 °C, there are no sharp features in the XRD spectrum (see Fig. 6); however, a diffraction peak associated with crystalline Al_2O_3 appears at about 40° after the 900 °C anneal, which corresponds to the (110) plane for corundum Al_2O_3.[18] The broad feature at about 70° is due to Si.

C. Electrical characterization

Field isolation MOS capacitors were made on n-type and p-type Si(100) substrates with carrier concentrations in the mid $10^{17}\,cm^{-3}$ range. RPECVD Al_2O_3 was used as the gate dielectric and was deposited onto four different interfaces (i) HF last, H-terminated Si, (ii) 0.6 nm SiO_2 prepared by remote plasma-assisted oxidation via a He/O_2 plasma, (iii) 1.2 nm of deposited RPECVD deposited SiO_2, and (iv) 2.2 nm of RPECVD deposited SiO_2.

$C-V$ measurements were performed at 1 MHz, and the data in Fig. 7 was analyzed using a fit program that performs a least squares fit routine and yields values of flat band voltage and oxide thickness normalized to the dielectric constant of SiO_2.[20] Samples deposited on the HF last silicon had flat band voltages that were shifted positively for increasing thickness for both p-type and n-type Si substrates, i.e., in so-called n-MOS and p-metal–oxide–semiconductor capacitor structures where n and p, respectively, refer to the minority carriers in the p-type and n-type substrates (this notation

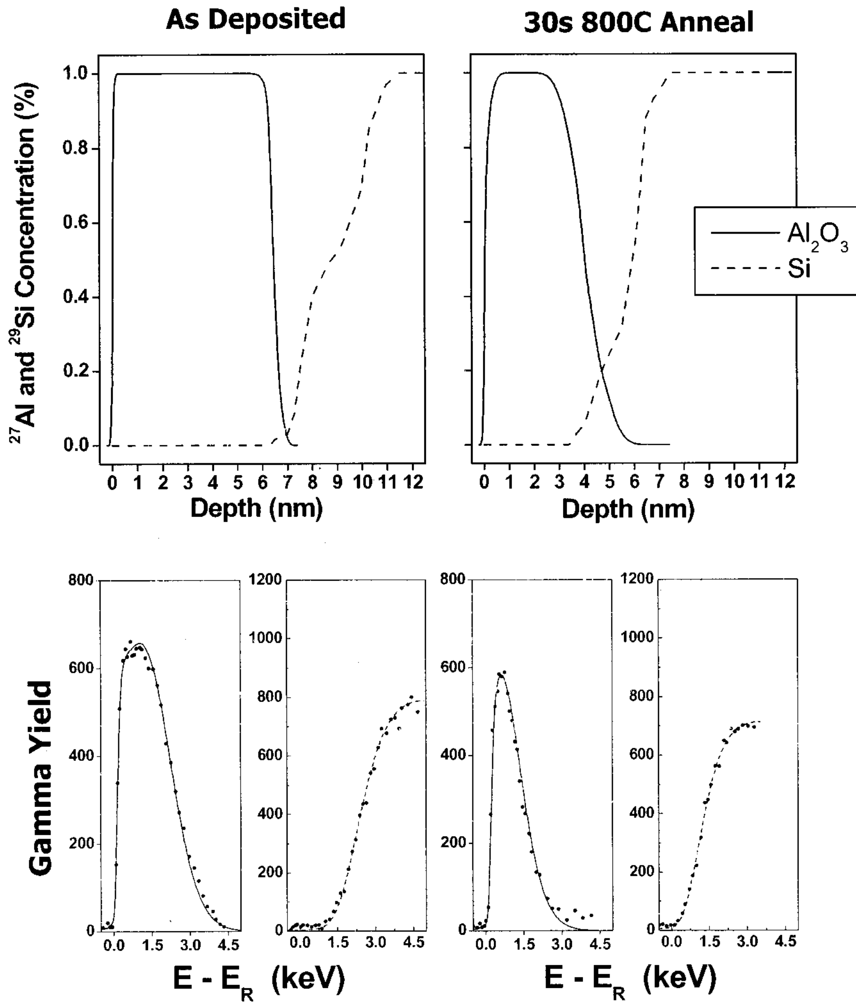

FIG. 4. NRP for Al_2O_3 on 2.2 nm of silicon dioxide deposited on HF last silicon is shown where the scale is normalized to Al_2O_3 and bulk silicon.

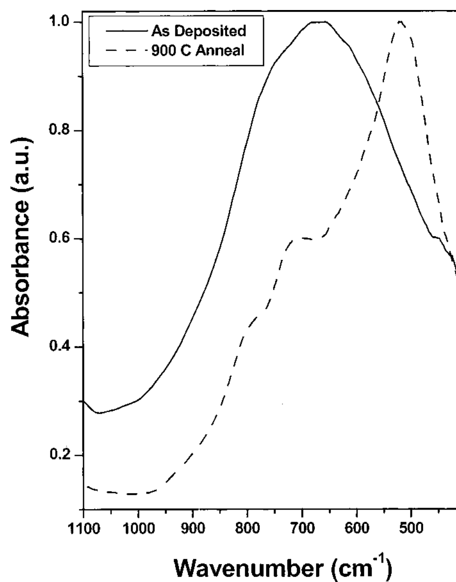

FIG. 5. FTIR for >100 nm of aluminum oxide on silicon before and after a 900 °C anneal.

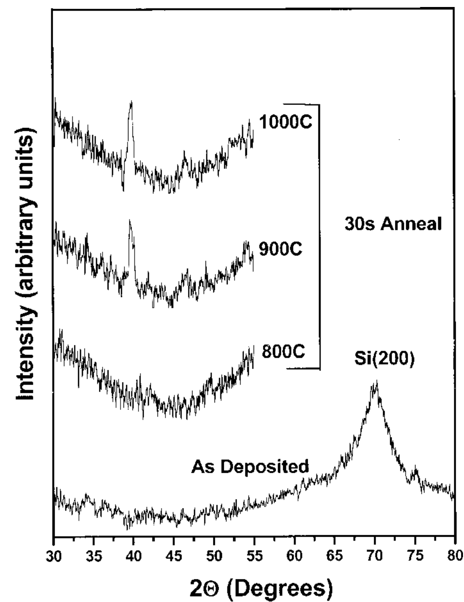

FIG. 6. XRD for aluminum oxide on Si(100) is presented.

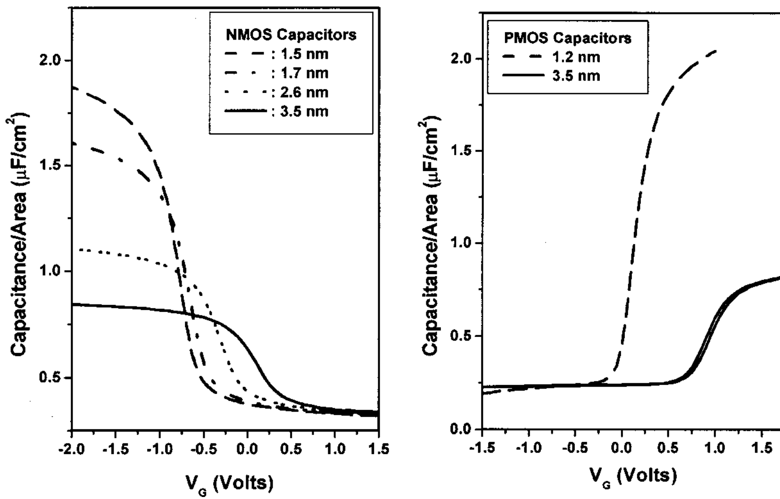

FIG. 7. $G-V$ data for aluminum oxide on HF last silicon are presented.

is the convention for field effect transistor devices, where the channels for carrier transport are formed by substrate inversion).

Figure 8 presents plots of the flat band voltage as a function of EOT of the Al_2O_3 portion of the gate dielectric [see Eq. (1)]. The EOT for the Al_2O_3 portion of the composite dielectric was obtained by subtracting 0.6 nm from the total EOT. This subtraction was based on the AES and NRP data for the HF last depositions, and on experimental data that indicated that the fixed charge levels at the remote plasma-processed Si–SiO_2 interfaces were at most in the mid $10^{10}\,cm^{-2}$. The flat band voltages for reference n-MOS and p-MOSCAPs with SiO_2 interfaces were equal to within experimental error of ~0.05 V, to the metal–semiconductor work function differences for the silicon substrates and Al gate electrodes. The flat band voltage—EOT data have been fit with straight lines consistent with the analysis to be presented. The y-intercept in this fit is the metal–semiconductor work function difference, Φ_{ms}, and the slope indicates the fixed charge at the interface between the Al_2O_3 portion of the stacked dielectric and the interfacial layer.[21]

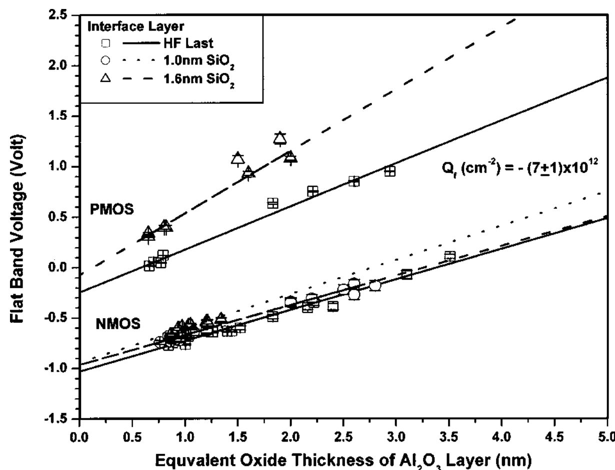

FIG. 8. Flatband voltage as a function of the aluminum oxide EOT is shown.

The slopes, obtained from the fits to the n-MOS and p-MOSCAPs correspond to negative fixed interfacial charge densities of $-7.0\pm1.0\times10^{12}/cm^{-2}$. The values of Φ_{ms} are consistent with the work function difference between Si and the Fermi level position in the doped Si substrates. This analysis places the fixed charge the interface between the SiO_2 and the RPECVD Al_2O_3 layer. By varying the thickness of the SiO_2 layer deposited between the Si substrate and the Al_2O_3 layer, the position of the fixed charge can be confirmed. Before discussing the data for these stacked dielectrics, the solution to Poisson's equation is presented.

By using Poisson's equation, the potential due the interfacial charge can be calculated, and be subtracted from the work function difference, Φ_{ms}, which is the flat band voltage in the absence of fixed charge, and the flat band voltage, V_{FB}, can be then be calculated as in Eq. (1);[21]

$$V_{FB}=\Phi_{MS}-\frac{q}{\epsilon_0\cdot k_{SiO}}\cdot\left[Q_{SiO}\cdot\left(d_{SiO}+\frac{k_{SiO}}{k_{AlO}}\cdot d_{AlO}\right)+Q_{AlO}\cdot\frac{k_{SiO}}{k_{AlO}}\cdot d_{AlO}\right]. \quad (1)$$

Q_{SiO} is the charge located at the Si–SiO_2 interface, and Q_{AlO} is the charge located at the internal dielectric interface between the SiO_2 interface layer and the RPECVD Al_2O_3 layer. ϵ_0 is the permitivity of free space, k_{SiO} and k_{AlO}, are, respectively, the dielectric constants of SiO_2 and Al_2O_3, 3.8 and 9.0, and d_{SiO} and d_{AlO} are, respectively, the physical thicknesses of the SiO_2 and Al_2O_3 constituent layers of the stacked dielectric. Equation (1) can be rearranged and written in terms of the contributions to V_{FB} in which d_{SiO} and d_{AlO} are the scaling variables, as in Eq. (2);

$$V_{FB}=\Phi_{MS}-\frac{q}{\epsilon_0\cdot k_{SiO}}\cdot\left[Q_{SiO}\cdot d_{SiO}+(Q_{SiO}+Q_{AlO})\cdot\frac{k_{SiO}}{k_{AlO}}\cdot d_{AlO}\right]. \quad (2)$$

If the flat band shift is plotted as a function of aluminum oxide thickness, then fixed charge residing at the Si–SiO_2 interface will affect both the slope and the y-intercept value. If the charge is only at the internal SiO_2–Al_2O_3 dielectric interface then only the slope will be affected; i.e., the slope will be proportional to Q_{AlO}, and the intercept with Φ_{ms}.

Figure 8 presents the flat band voltage-EOT plots for n-MOS and p-MOSCAPs. From n-MOS data, the slopes and y-intercepts for varying amounts of SiO_2 are the same to within experimental error as the respective slopes and y-intercepts or the HF last devices with 0.6 nm of interfacial SiO_2. The p-MOS data exhibit changes in both slope and y-intercept as compared to the HF last devices.

The NRP results indicated a mixing of Al_2O_3 and the RPECVD SiO_2 after the 800 °C anneal. This is mixing is confirmed in the $C-V$ results from a reduced value in the EOT for aluminum oxide on RPECVD silicon dioxide. The measured EOT of the device should be a weighted addition of the silicon dioxide and aluminum oxide as in Eq. (3);

$$\mathrm{EOT}=T_{\mathrm{ox}}(\mathrm{SiO_2})+\frac{k_{\mathrm{SiO_2}}}{k_{\mathrm{Al_2O_3}}}*T_{\mathrm{ox}}(\mathrm{Al_2O_3}). \tag{3}$$

Analysis of MOSCAPs on p-type and n-type Si substrates with the same deposition times as those in Fig. 8 resulted in gate oxides with physical thicknesses, respectively, of 1.2 and 2.2 nm. For the SiO_2–Al_2O_3 stacks the EOT was extracted from the $C-V$ data. The thickness of the SiO_2 portion of the dielectric was then subtracted from EOT to give contribution due to the Al_2O_3 layer. If d_{SiO} values of 1.2 and 2.2 nm were used to calculate the thickness of the Al_2O_3, the resultant Al_2O_3 layer thicknesses were significantly thinner compared to that of an equivalent Al_2O_3 deposited on the HF last Si. Instead, thicknesses of 1.0 and 1.6 nm were required to attain aluminum oxide thickness that corresponded well to HF last devices. This effect is presumed to result from a mixing of the SiO_2 and Al_2O_3 layers that determined from the resonant NRP studies (see Fig. 4). When SiO_2 is mixed with higher dielectric materials, the effective dielectric constant of the resulting material is always higher than that of SiO_2.[22]

Figure 9 indicates current density–voltage, $J-V$, data for n MOS and p MOSCAPs, for substrate accumulation. The primary features of the leakage current in Fig. 9, is an asymmetry in the $J-V$ trances for equivalent EOT and bias. This is attributed to an inherent asymmetry in the band alignment and resulting band bending (see Fig. 10). For n MOSCAPs, the current is injected from the gate and the semiconductor bands bend down providing a large barrier that reduces direct tunneling. In the p MOSCAPs, the current is injected from the substrate, the semiconductor bands bend up providing a smaller tunneling barrier for an equivalent bias and EOT. This inherent difference in barrier heights results in an increased current density for p MOSCAPs.

IV. SUMMARY

The AES spectra of Fig. 2 indicate only one Al feature. The energy of this peak in the AES spectra indicates that the Al atoms are bonded only to oxygen, and that there is no detectable silicide (Al–Si) or metal–metal (Al–Al) bonding. The AES spectra of Fig. 2 and the NRP of Fig. 3 indicate that when Al_2O_3 is deposited by RPECVD at 300 °C on HF last, H terminated Si, this is accompanied by approximately 0.6 nm of SiO_2 being formed subcutaneously at the Si–dielectric interface. NRP further indicates that the interface of the Al_2O_3 film with this subcutaneously formed SiO_2 layer is abrupt to within ~0.4–0.6 nm as deposited, and after an 800 °C anneal. Analysis of $C-V$ data for n MOSCAPs and p MOSCAPs for the HF last Al_2O_3 depositions are consistent

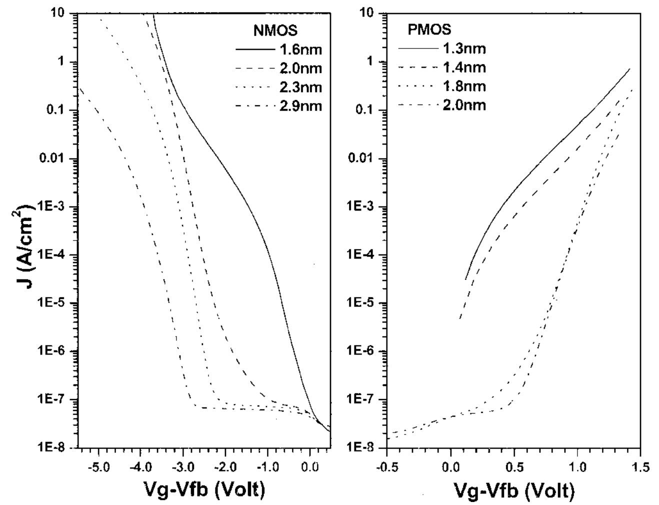

FIG. 9. Leakage current density vs $Vg-Vfb$ is presented.

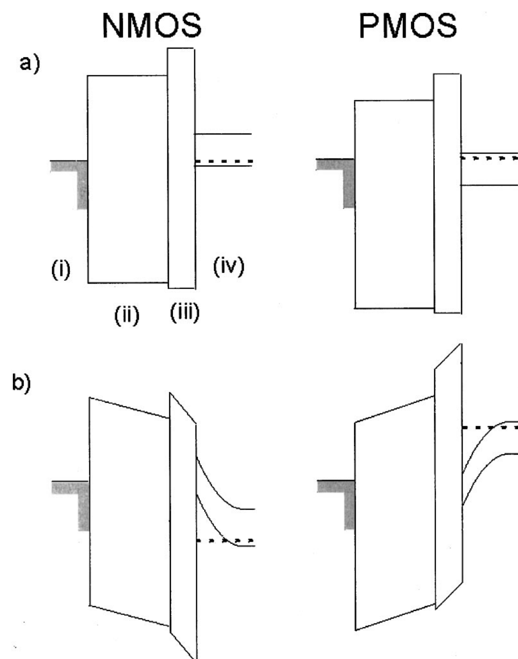

FIG. 10. Ideal band bending for n- and p-MOS devices is presented where (i) aluminum gate metal, (ii) aluminum oxide layer, (iii) silicon dioxide interfacial layer, and (iv) silicon substrate. (a) Flat band condition. (b) Accumulation condition where both are biased with an equal magnitude of gate voltage. For n MOS, the device experiences gate injection and for p MOS there is substrate injection.

with a stacked dielectric structure which includes ~0.6 nm of SiO_2 between the Si substrate and the Al_2O_3 film.

The analysis of $C-V$ data, in particular the variation of flat band voltage as a function of the Al_2O_3 contribution to EOT, indicates negative fixed charge, of the order of $6-8 \times 10^{12}\,cm^{-2}$ at the interface between the Al_2O_3 layer and the subcutaneously formed SiO_2 interface. It is possible to move this charge further away from the Si substrate by depositing a thicker layer of SiO_2 by RPECVD, prior to the Al_2O_3 deposition.

The fixed negative charge is consistent with a model for the local atomic bonding of noncrystalline Al_2O_3 that has two different bonding environments for the Al atoms;[23] (i) a tetrahedrally coordinated Al site that has a net negative charge, and (ii) and octahedrally coordinated site in which the Al has a charge of $3+$. The negatively charged Al atoms can bond directly to the O atoms of the SiO_2 interfacial and this is the arrangement that is responsible for the negative fixed charge. The tetrahedral arrangement with a negatively charged Al is unique, and essentially all of the other transition metal oxides studied to date display fixed positive charge at their interfaces with Si or SiO_2.[23] Temperature dependent $C-V$ measurements indicate electron traps in the immediate vicinity of the Si–dielectric interface;[24] the trapping sites may be intrinsic and associated with the octahedrally-coordinated Al. Finally, $J-V$ data for substrate accumulation shows a marked asymmetry between n-MOSCAP and p-MOSCAP devices. This has been attributed to inherently asymmetric band bending in stacked dielectric structures.

Finally, a few comments will be made relative to thermal stability and changes in bonding that take place at crystallization. The FTIR and XRD results indicate that the Al_2O_3 films are amorphous as deposited at 300 °C, but are crystallized after an anneal at 900 °C. These observations are for films that are considerably thicker than those used in devices, and additional experiments must be made to determine if there are no changes in the effective crystallization temperatures of these thinner layers. The changes in the FTIR spectrum are consistent with an increase in the Al atom coordination after crystallization. The shift to lower wave number is also consistent with an increase in k from about 9 in the noncrystalline films to 11 in the crystalline films. In general, alloys of Al_2O_3 and SiO_2 or Ta_2O_5 will have a higher effective crystalline temperatures, and this has been observed in experiments we have performed on $Al_2O_3-Ta_2O_5$ pseudobinary alloys prepared by remote plasma deposition.

ACKNOWLEDGMENTS

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[1]Semiconductor Industry Association, International Technology Roadmap for Semiconductors: 1999 Edition (http://public.itrs.net).
[2]J. Robertson, J. Vac. Sci. Technol. B **18**, (2000).
[3]G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[4]T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Mayer, C. C. Hobbs, R. I. Hedge, I. J. R. Baumvol, and G. N. Parsons, Appl. Phys. Lett. **75**, 4001 (1999).
[5]E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, Appl. Phys. Lett. **76**, 176 (2000).
[6]A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, Tech. Dig. VLSI Symp. 16 (2000).
[7]D. A. Buchanan *et al.*, Tech. Dig. Int. Electron Devices Meet. 223 (2000).
[8]S. Miyazaki, J. Vac. Sci. Technol. B (submitted).
[9]T. Yasuda, Y. Ma, S. Habermehl, and G. Lucovsky, J. Vac. Sci. Technol. B **10**, 1844 (1992).
[10]R. G. Gordon, K. Kramer, and X. Lui, Mater. Res. Soc. Symp. Proc. **446**, 383 (1997).
[11]S. D. Hersee and J. M. Ballingall, J. Vac. Sci. Technol. A **8**, 800 (1990).
[12]B. J. Hinds, F. Wang, D. M. Wolfe, C. L. Hinkle, and G. Lucovsky, J. Vac. Sci. Technol. B **16**, 2171 (1998).
[13]I. J. R. Baumvol, Surf. Sci. Rep. **36**, 166 (1999).
[14]S. E. Hunt and W. M. Jones, Phys. Rev. **89**, 1283 (1953).
[15]I. Vickridge and G. Amsel, Nucl. Instrum. Methods Phys. Res. B **45**, 6 (1990).
[16]H. Niimi, K. Koh, and G. Lucovsky, Proc.-Electrochem. Soc. **12**, 623 (1996).
[17]L. E. Davis, N. C. MacDonald, P. W. Palnberg, G. E. Raich, and R. I. Weber, *Handbook of Auger Electron Spectroscopy*, 2nd ed. (Physical Electronics Industries, Inc. Eden Pairie, MN, 1976).
[18]JCPDS-ICDD, Newton Square, PA, 1993.
[19]B. Rayner, H. Niimi, R. Johnson, R. Therrien, G. Lucovsky, and F. Galeener, *Proceedings of the Characterization and Metrology for USLI Technology* (American Institute of Physics, Melville, NY, 2000) (in press).
[20]J. R. Hauser and K. Ahmed, AIP Conf. Proc. **449**, 235 (1998).
[21]D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).
[22]G. Lucovsky and G. B. Rayner, Jr., Appl. Phys. Lett. **77**, 2912 (2000).
[23]G. Lucovsky, J. C. Phillips, and M. F. Thorpe, *Proceedings of the of Characterization and Metrology for USLI Technology* (American Institute of Physics, Melville, NY, 2000) (in press).
[24]R. S. Johnson and G. Lucovsky (to be published).