Physical and Predictive Models of Ultrathin Oxide Reliability in CMOS Devices and Circuits

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Invited Paper

***Abstract*—The microelectronics industry owes its considerable success largely to the existence of the thermal oxide of silicon. However, recently there is concern that the reliability of ultra-thin dielectrics will limit further scaling to slightly thinner than 2 nm.**

This paper will review the physics and statistics of dielectric wearout and breakdown in ultrathin SiO_2-based gate dielectrics. Electrons or holes tunneling through the gate oxide generate defects until a critical density is reached and the oxide breaks down. The critical defect density is explained by the formation of a percolation path of defects across the oxide. Only $<1\%$ of these paths ultimately lead to destructive breakdown, and the microscopic nature of these defects is not known. The rate of defect generation decreases approximately exponentially with supply voltage, below a threshold voltage of about 5 V for hot electron-induced hydrogen release. However, the tunnel current also increases exponentially with decreasing oxide thickness, leading to a decreasing time-to-breakdown and a diminishing margin for reliability as device dimensions are scaled. Estimating the reliability of the dielectric requires an extrapolation from the measurement conditions (e.g., higher voltage) to operation conditions. Because of the diminished reliability margin, it has become imperative to try to reduce the error in this extrapolation. Long-term (>1 year) stress experiments are now being used to measure the wearout and breakdown of ultrathin (<2 nm) dielectric films as close as possible to operating conditions. These measurements have revealed the details of the voltage dependence of the defect generation rate and critical defect density, allowing better modeling of the voltage dependence of the time-to-breakdown. Such measurements are used to guide the technology development prior to the manufacturing stage. We then discuss the nature of the electrical conduction through a breakdown spot and the effect of the oxide breakdown on device and circuit performance. In some cases, an oxide breakdown does not lead to immediate circuit failure, so more research is needed in order to develop a quantitative methodology for predicting the reliability of circuits.

***Index Terms*—Dielectric breakdown, MOSFETs, reliability.**

I. Introduction

THE microelectronics industry, including the Internet and the telecommunications revolutions, owes its success largely to the existence of the thermal oxide of silicon, i.e., silicon dioxide (SiO_2). A thin layer of SiO_2 forms the insulating layer between the control "gate" and the conducting "channel" of the transistors used in modern integrated circuits. As circuits are made more dense, all the dimensions of the transistors are reduced ("scaled") correspondingly [1], so that nowadays the SiO_2 layer thickness (t_{ox}) is 2 nm or less, and the reliability of such ultrathin oxide layers has become a major concern for continued scaling.

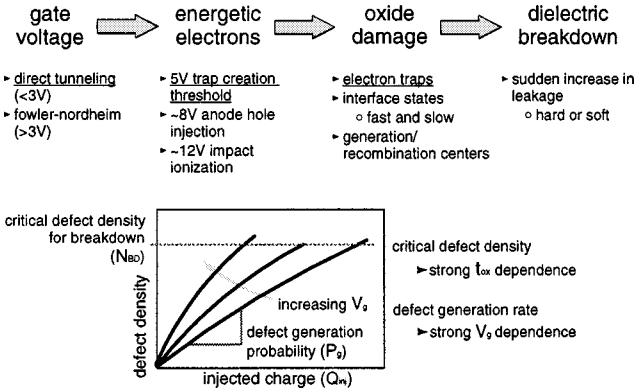

Fig. 1. Mechanism of defect generation to breakdown.

The reliability of SiO_2, i.e., the ability of a thin film of this material to retain its insulating properties while subjected to high electric fields for many years, has always been an important issue and has been the subject of numerous publications over the last 35 years [2]–[6], since the realization that SiO_2 could be used as an insulating and passivating layer in silicon-based transistors [7], [8]. Oxide reliability and the experimental methods for accelerated testing have been the subject of earlier review papers [9]–[18].

For the relatively thick (>10 nm) oxides used in earlier technologies, the breakdown mechanisms are actually fairly complex, and the detailed understanding of the intrinsic reliability has only come about in the more recent past, as manufacturing processes have matured and high-quality MOSFET samples incorporating a wide range of oxide thickness have become available for scientific study [19]. The essential elements of our present understanding are illustrated in Fig. 1. When a voltage is applied across the gate oxide, an electron current will flow if the gate voltage (V_g) is high enough and/or the oxide is thin enough. For thick oxides, the current is controlled by Fowler–Nordheim tunneling [20], [21], while for thin oxides ($t_{ox} \lesssim 3$ nm) at voltages below about 3 V (corresponding to the barrier height between n-type silicon and the SiO_2) the current is due to direct quantum-mechanical tunneling. The

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electrons flowing across the oxide will trigger several processes depending on their energy. At least three defect generation mechanisms have been identified: impact ionization and anode hole injection occur at higher voltages, leading to hole trapping and hole-related defect generation [19], [22]. The lowest energy process so far identified, which dominates at the voltages where present MOSFETs operate, is the so-called "trap creation" process attributed to hydrogen release from the anode [23] with a threshold gate voltage of about 5 V. This process continues in the subthreshold region even at operating voltages, down to 1.2 V or lower [24], [25].

As a consequence of the reaction of the released mobile hydrogen [23], [26]–[30], a variety of defects such as electron traps, interface states, generation/recombination centers in the substrate, positively charged donor-like states, etc., gradually build up in the oxide. For breakdown, it is believed that bulk traps are the most important [31]–[34]. Eventually, enough damage builds up to the point where the oxide breaks down destructively. Breakdown is defined experimentally as a sudden increase in conductance, often accompanied by current noise.

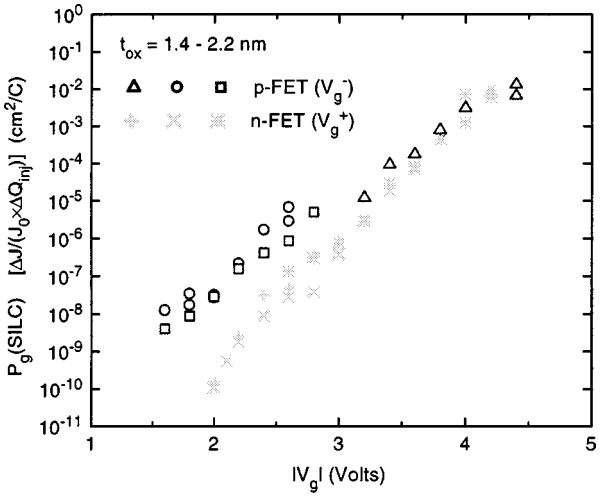


Fig. 2. Comparison of the defect generation probability (P_g) for holes (p-FET) or electrons (n-FET).

II. Physical Models for Defect Generation

The evidence for hydrogen involvement in defect generation and breakdown is circumstantial but strong. Already in the 1970s it was suggested that hydrogen would play a major role in the growth of SiO_2 and in radiation processes in this material [35], [36]. The evidence up to 1989 for hydrogen's role in the trap creation process has been reviewed by DiMaria [23]. Since that time, it was shown that exposure of bare SiO_2 films to atomic hydrogen radicals, in the absence of any electric field, will produce electrically active defects essentially identical to those produced by electrical stress or radiation [26], [37]–[51]. Paramagnetic interface defects [38], [39], [48], [50] (the P_b centers, which are Si dangling bonds at the Si/SiO_2 interface), diamagnetic interface defects (fast and slow interface states) [37], [38], [40]–[43], [45]–[50], and bulk electron traps [44] are produced. The desorption rate of hydrogen from Si surfaces was measured as a function of incident electron energy [52] and showed a dependence remarkably similar to the voltage dependence of the trap generation process [23], [25]. However, a major perceived stumbling block to the general acceptance of the "hydrogen model" for breakdown has been the apparent lack of any isotope effect for the breakdown process [53] compared to the large effect observed for hydrogen/deuterium desorption and for channel hot electron-induced interface degradation [54]. This may have recently been resolved by the observation [55], [56] of a significant isotope effect on the stress-induced flat-band voltage shift and stress-induced leakage current (SILC), which is a measure [44], [57], [58] of the bulk traps which ultimately relate to breakdown. A significant isotope effect on trap generation and oxide breakdown in deuterated oxide has also been reported earlier [59].

Two other physical models for breakdown have been widely discussed in the literature. The first is the anode-hole injection (AHI) model, which claims that breakdown is caused by holes which are injected from the anode contact [60], [61]. This model derived considerable support from a comprehensive theoretical treatment of anode hole injection by surface plasmon excitations, decaying into electron–hole pairs in the silicon gate [62], [63], and experimental data showing the expected dependence on anode material [62], [64]. The original concept was a variant of earlier models [3], [4], [6] postulating a positive feedback mechanism for current runaway, caused by the field-enhancement due to the trapped holes. The main experimental evidence in support of this was a constant value of the hole fluence to breakdown as a function of oxide field [60] $Q_p \approx 0.1$ C/cm^2, where the injected hole flux is obtained from the substrate hole current using n-FETs biased in inversion, although it was later shown that Q_p decreases for t_{ox} less than about 6 nm [61] and that the constancy of Q_p does not hold at temperatures below 300 K [65]. The AHI model is commonly associated with a time-to-breakdown (T_{BD}) dependence on oxide field of the form $T_{BD} \propto \exp(\text{-constant}/E_{ox})$ (referred to as the "$1/E$ model") [66], but since this dependence comes mostly from the form of the Fowler–Nordheim current it is not an essential element of the physical model and would not be expected to hold in the direct tunneling regime [67].

According to the plasmon model calculations [62], the gate voltage threshold for positive charge generation by hole trapping due to AHI is 7–8 V for FETs with n^+-poly gates, and this was confirmed experimentally [22]. Thus, this mechanism may not be able to account for the substrate currents measured at lower voltage. A recent modification of the AHI model [68], [69] proposes that a weaker minority carrier ionization process [70] is responsible for hole injection and defect generation at low voltages. This mechanism will be operative for electron injection into a p-type material or hole inversion layer, and was observed for n-FETs with low gate doping when the n-poly gate inverted [34]. The modified model can successfully fit the measured slope of T_{BD}-versus-voltage at high fields [67], [69] but cannot account for the absolute magnitude of the defect generation rate. Since the hole current at low voltage (e.g., 2–3 V) in this model is at least 12 orders of magnitude lower than the primary electron current [68], the defect generation rate per hole must be very much greater than the rate per injected electron. However, direct measurement of the rate of defect generation by holes transporting through an SiO_2 layer [71], [72] shown in Fig. 2 gives values comparable to the generation rate due to

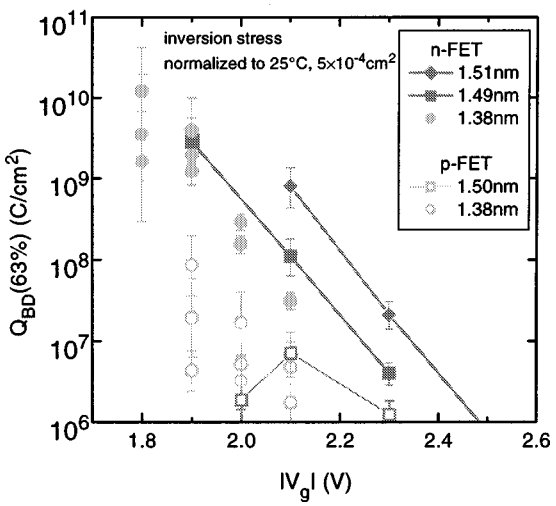


Fig. 3. Charge-to-breakdown measurements on p-FETs and n-FETs under inversion conditions.

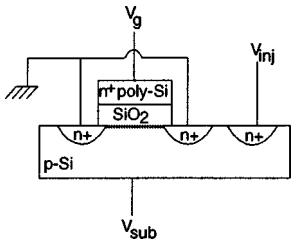
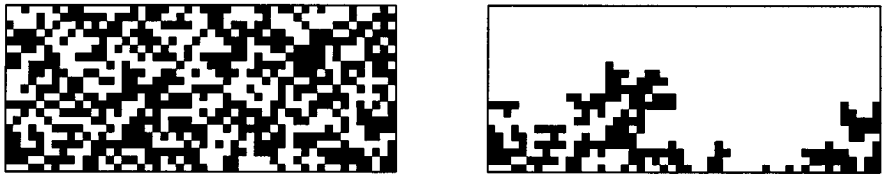


Fig. 4. Device structure for SHE injection.

electrons and many orders of magnitude less than what is required by a minority carrier mechanism. (See the next section for the definition of P_g.) Charge-to-breakdown measurements using substrate hot hole injection [73], [74] and on p-FETs at low bias [72] (Fig. 3) have also shown that the hole fluence to breakdown, Q_p, is as large as eight orders of magnitude greater than the value used in the AHI model, consistent with the measured defect generation rate. The data in Fig. 3 indicate that p-FET breakdown may be the limiting factor at low voltage, contrary to the usual idea [75] that n-FETs should represent the worst case. The AHI model has also been criticized on the basis that the measured substrate currents at low voltage may have other origins besides hole tunneling through the oxide, including generation-recombination processes in the substrate [22] and photoexcitation due to photons generated by hot electrons in the gate [22], [76]. Other kinds of defect generation, especially donor-like interface states which give interfacial positive charge, or bulk neutral traps which cause an increase in the leakage current, can be easily mistaken for trapped holes in the oxide [19], [22], [44]. In cases where holes due to AHI are clearly observed (i.e., above 7–8 V) [22] there is no correlation with breakdown [19], [77].

The other widely cited breakdown model is the "thermochemical" model, or "E-model," which proposes that defect generation is a field-driven process and that the current flowing through the oxide plays at most a secondary role. The development of this model from its origin in the mid 1980s through the late 1990s has been reviewed by McPherson [78], [79]. Briefly, the model considers the interaction of the applied electric field E with the dipole moments associated with oxygen vacancies (weak Si–Si bonds) in SiO_2. The activation energy required for bond breakage is lowered by the dipolar energy, leading to a quantitative prediction for the field dependence of the activation energy for dielectric breakdown (or equivalently, the temperature dependence of the field acceleration factor) which agreed well with experiment [80]–[82]. McPherson also showed [78] that allowing for a distribution of energies of the weak bonds could account for a wide range of observations of the temperature- and field-dependence of SiO_2 breakdown times, since the defect which dominates the breakdown process may change depending on stress conditions. However, it was also observed that for very thin oxides ($t_{ox} \lesssim 4$ nm) the breakdown times are no longer a function of only the field, but are strongly decreasing with thickness at the same oxide field [79], [83]. The decreasing breakdown times are consistent with the increasing direct-tunneling leakage currents in the ultrathin oxides. It was proposed that the strong increase in current leads to an increase in hole injection (presumably by the same mechanism as in the AHI models discussed above), and that these holes are trapped at oxygen vacancies further reducing the activation energy for bond rupture [79], [83]. Other attempts to unify the AHI and thermochemical models by treating these as parallel competing mechanisms have been published [84]–[86].

The E-model has attained widespread acceptance, largely on the basis that, empirically, the $T_{\rm BD}$ data appear to follow an exponential dependence on field [80]–[82], [87]–[90] including an experiment of 3-yr duration at oxide fields down to 5.3 MV/cm on 9-nm films [91]. However, it must be pointed out that the exponential dependence on field is not proof of the validity of the particular physical model. Probably the strongest evidence against the thermochemical model comes from substrate-hot-electron (SHE) injection experiments [92], [93]. In this experiment, using a specially designed n-FET structure [94] (see Fig. 4), a forward-biased n^+ diffusion in the p-type substrate is used to inject electrons toward the inversion layer at the Si/SiO_2 interface. The inversion layer is maintained by keeping the gate positively biased relative to the source and drain (both held at ground). A negative substrate bias accelerates the injected electrons, and the injector current can be controlled independently of both the substrate and gate bias by varying the magnitude of the forward bias applied across the injector junction. The substrate voltage controls the maximum electron energy incident on the Si/SiO_2 interface, and for a sufficiently high substrate bias so that some electrons are injected over the energy barrier into the oxide, the gate voltage additionally controls the energy of the electrons incident on the gate–oxide interface. In these experiments, it was found that the charge-to-breakdown ($Q_{\rm BD}$) is strongly dependent on the substrate bias, even though the oxide field is held fixed [93]. Therefore, $Q_{\rm BD}$ correlates with the electron energy not the oxide field. This was also demonstrated for conventional Fowler–Nordheim stress by varying the doping of the anode [34], [95]. The SHE experiments also showed that $T_{\rm BD}$ is inversely related to the current density [93], again showing that breakdown is dominated by the effect of the energetic electrons and not the field in the oxide. The same conclusion was arrived



(a) (b)

Fig. 5. Schematic of the percolation model. (a) Occupied sites $(p_0 = 0.5)$. Two-dimensional simple cubic lattice with uniform 50% occupancy. "Defects" are represented by dark squares. (b) Cluster #1, connects to bottom face. Starting from the same defect distribution as in (a), only those occupied sites which connect to the bottom face via nearest neighbors are kept. Note the use of periodic boundary conditions in the horizontal dimension. For this sample size and defect density, there is no breakdown path connecting the bottom face to the top face, but connecting paths would exist if the sample were made thinner or wider. This schematic shows a small (21×50) sample in two dimensions. The actual calculations were performed in three dimensions using a larger sample.

at based on measurements of the effect of varying the gate doping [34], [75], [96].

III. The Critical Defect Density

The idea of damage building up to a critical level has been a key insight in leading to a predictive model of oxide reliability. The concept is not novel: for example, in 1983, resonant tunneling via defect states was proposed as a mechanism leading to breakdown, [97] and in 1986 it was proposed that defect generation ("wear out") above some threshold concentration would lead to a new conduction path resulting in oxide breakdown [98]. Nor does the concept depend in any way on the physics of defect generation, whether hydrogen-induced or otherwise: the field-driven model [78], [79], [83] (E-model) also assumes a critical density of broken bonds in order to induce electric breakdown and thermal runaway, and the field dependence of trap generation has been used to support this model [99]. The most recent version of the AHI model [69], [100] likewise adopts the viewpoint that holes create some (unspecified) form of defect which eventually leads to a critical conduction path.

Beginning in the early 1990s, it was reported that in a large variety of oxide thickness stressed over a wide range of voltages, the charge-to-breakdown $(Q_{\rm BD})$ is inversely related to the initial rate of defect generation for most stress conditions [19], [88], [101]–[103]. Extending this to thinner samples, the thickness dependence of oxide breakdown was explained as resulting from a thickness-dependent number of defects $(N^{\rm BD})$ required to trigger breakdown [24]. The thickness dependence of $N^{\rm BD}$ was explained in terms of a simple percolation model [24], [31]–[33].

The relationship between the charge-to-breakdown $(Q_{\rm BD})$, the critical defect density $(N^{\rm BD})$, and the defect generation probability per injected electron density $(P_g \equiv qdN/dQ)$ is

$$N^{\rm BD} = \frac{1}{q}\int_0^{Q_{\rm BD}} P_g\, dQ \tag{1}$$

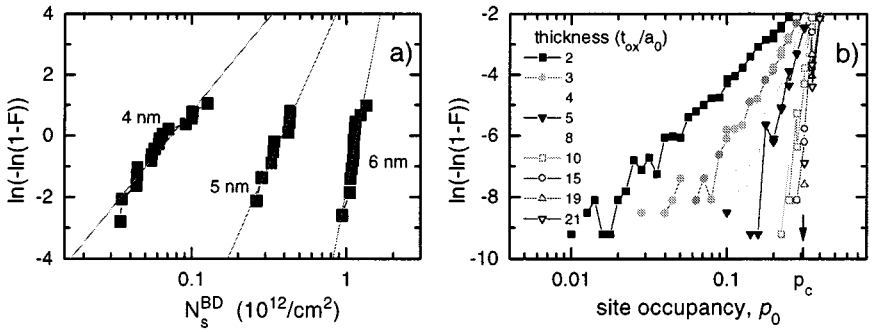
where q is the magnitude of the electron charge. When the defect generation is first order in the electron fluence, then

$$Q_{\rm BD} = qN^{\rm BD}/P_g. \tag{2}$$

(It is commonly observed that the defect density N is a sublinear power-law function of the injected charge Q. However, observed over a sufficiently wide range of fluence, the full dependence is typically sigmoidal, with a linear region bracketed by sublinear portions at low and high fluence [72], [104]. If the low-fluence background is subtracted, a linear behavior is found independendent of stress conditions. At higher fluence (near breakdown) the saturation may be due to measurement technique, and the underlying defect generation probably continues in proportion to the fluence [105].)

The concept of a critical defect density was quantitatively examined by Suñé *et al.*, [106] who showed that it leads to the correct statistical behavior. This was not a predictive model since $N^{\rm BD}$ was treated as a fitting parameter. Later, Degraeve [31] formulated the percolation model in which breakdown is envisioned as the formation of a connecting path of defects, as a result of random defect generation throughout the insulating film. This explains the thickness dependence of $N^{\rm BD}$ as a geometrical/statistical effect, by which a connecting path of defects is more likely for thinner films.

The percolation concept, and the origin of the thickness dependence of NBD, is schematically illustrated by the computer simulation [33] in Fig. 5. According to this model, breakdown can occur only when a connecting path of traps is formed across the gate oxide, forming a conducting path from the substrate to the gate. The probability of forming such a connecting path ("percolation path") with randomly generated defects throughout the oxide bulk is computed as a function of defect density and oxide thickness. For a given defect density, the formation of a percolation path is more likely for thinner oxides. Conversely, as the oxide is made thinner a percolation path can form with some probability at a lower average defect density than is necessary in a thick oxide. In the simulation, we start by placing defects (black squares) randomly throughout the sample [Fig. 5(a)], and then discard all defects which are not part of a cluster that is attached (via nearest neighbors) to one face of sample [Fig. 5(b)]. It does not matter at which face we begin when the percolation cluster is found, because if a site is part of a cluster which connects the two faces of the sample, then it will be counted regardless of which side we start from. It would be computationally redundant to separately examine the opposite cluster extending from other face of the sample, because this cluster cannot touch the first face unless the first cluster also spans the sample. (Note the use of periodic boundary conditions in the lateral direction, i.e., edge effects are avoided by treating the sample as if it were a cylinder made by connecting the left and right ends.) For the particular



(a) (b)

Fig. 6. (a) Weibull plot of the cumulative failure (F) distributions of measured defect density at breakdown, for p-FETs with oxide thickness from 4 to 6 nm under positive gate bias Fowler–Nordheim stress. The lines are first order least squares fits. (b) Weibull plot of the calculated cumulative failure (F) distributions for percolation on a 3-D simple cubic lattice as a function of site occupation fraction p_0, with normalized thickness as a parameter. The Weibull function is normalized to a unit area a_0^2, the defect cross-sectional area. The classical percolation threshold is indicated by p_c.

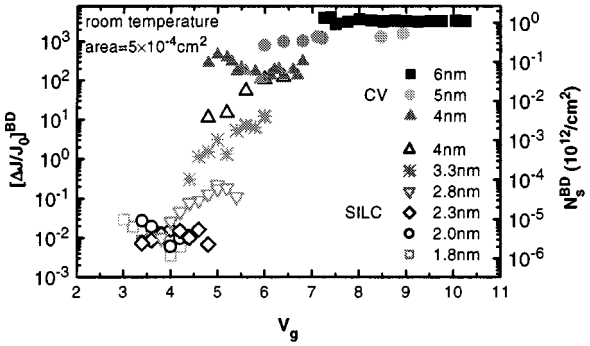


Fig. 7. Critical defect density at breakdown. Filled symbols from CV, open symbols from SILC. The CV and SILC data are normalized to their average values at 5 nm.

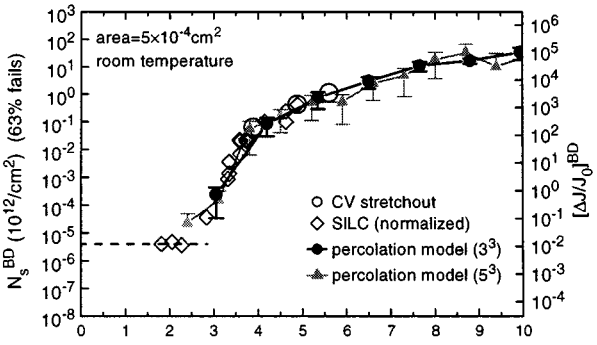


Fig. 8. Critical defect density for breakdown as a function of oxide thickness. The CV and SILC data are normalized at 5 nm. The fit to the percolation model is shown.

defect density illustrated in Fig. 5, there is no percolation path connecting top to bottom of the sample, and therefore we have not reached breakdown. However, breakdown would have occurred at this density if the sample were thinner, i.e., thinner than the extent of the cluster in Fig. 5(b). As the defect density is increased, the percolating cluster extends deeper into the sample until at some critical density it will touch the opposite face. Also, even for the same defect density and thickness, if the sample were made wider (corresponding to a larger device area), there is a finite probability of locally finding a cluster that does span the thickness. Thus, this rather simple model accounts nicely for all the statistical features of oxide breakdown including thickness and area dependence.

Fig. 6 shows the cumulative failure (F) distributions for N^{BD} calculated from this model [33] along with experimental data [24]. The data are capacitance voltage (CV) measurements of the interface state density. Although it was stated earlier that the bulk traps control breakdown, the interface state generation parallels the bulk defects. For both theory and experiment, the slope of the failure distribution is an increasing function of sample thickness and the curves shift with thickness. The slope of the failure distribution is an important parameter used in reliability estimations, as will be discussed in a later section of this paper.

The measured critical defect density at breakdown is shown in Fig. 7 as a function of stress voltage, with thickness as a parameter [77]. Each point in this figure represents the final defect density extrapolated to breakdown for an individual sample. In addition to CV measurements (used for oxides with $t_{\mathrm{ox}} \geq 4$ nm), this figure includes SILC data. In SILC measurements, the relative increase in current in the direct tunneling range below 3 V is expressed as $\Delta J/J_0$ where J_0 is the initial current density in the as-fabricated device. This quantity is proportional to the density of generated neutral electron traps [44]. Thus, N^{BD} from SILC measurements is in units of $\Delta J/J_0$. The critical defect density was taken as the value of $\Delta J/J_0$ immediately prior to the first soft or hard breakdown. However, for high fluence (i.e., near breakdown) and especially for low stress voltages, the SILC tends to saturate with increasing stress duration [44], [105]. This may limit the usefulness of SILC as a direct measure of N^{BD}. The two vertical scales in Fig. 7 have been adjusted to match the average values obtained using the two measurement techniques on the 5-nm sample, from which we obtain [33] the relation $N_s(\mathrm{cm}^{-2}) \approx 3 \times 10^8 \Delta J/J_0$. This is consistent with the value found [44] for bulk the neutral traps, where $N_n(\mathrm{cm}^{-2}) \approx 1.25 \times 10^8 \Delta J/J_0$.

The thickness dependence is the dominant effect on N^{BD}, but there may be some V_g dependence as a second-order effect. The observed V_g dependence may be partly attributed to the measurement technique, since CV and SILC data on the same 4-nm sample show different dependencies. In Fig. 8, we plot the average N^{BD} value as a function of t_{ox}. N^{BD} drops by a factor of $\sim 10^5$ from 6 to 3 nm, and then reaches a plateau below 3

nm. These features are fully explained by a percolation model [33] shown by the filled symbols. The fit is described by two parameters, which are adjusted to give a consistent fit to both the data above 3 nm and the plateau below this thickness. The two parameters are the defect diameter (hopping distance) a_0 and the probability (f) that a percolation path triggers destructive breakdown. For $t_{ox} < a_0$, the percolation model predicts that the thickness dependence will vanish because only one "defect" is required to form a connecting path across the oxide. Therefore, the plateau region is $t_{ox} < a_0$, and N^{BD} in the plateau corresponds to one active defect in the area of the sample. In terms of absolute defect density, using the SILC normalization discussed earlier the plateau value below 3 nm corresponds to a constant number equal to 2000 defects in the 5×10^{-4} cm^2 area of each sample, suggesting that each percolation path has a probability of about 10^{-3} of initiating a destructive breakdown event. In other words, only a fraction $f \sim 10^{-3}$ of the defects are "active" or "effective" in causing breakdown. This might result from the different energy levels of defects, or from their different physical or chemical nature. The idea that there exists some special subset of defects which trigger breakdown has been independently suggested from the electron microscopy observation of breakdown patterns [107] where it was found that the density of "weak spots" is ~1% of the defect density at breakdown.

The value of the defect "size" obtained from the N^{BD} data is $a_0 \approx 3$ nm. This is believed to correspond physically to the electrical sphere of influence of a point defect, e.g., a tunneling distance or trapping cross section. Other authors obtained smaller values for the defect diameter (1.6–1.8 nm) based on fitting to the distribution of breakdown times [31] or resistances [108].

One component of the percolation model is that N^{BD} is relatively independent of how the oxide is stressed. This has been the assumption whenever N^{BD} measurements at elevated voltage have been used to project oxide reliability down to operating conditions [104], [109]–[113]. Several experiments have supported this assumption, using various measurements of the defect density including interface states, trapped charge, and stress-induced leakage. [24], [32], [93], [114]–[118]. On the other hand, several groups have reported measurements showing a decrease in N^{BD} as the stress voltage is reduced using 3–5-nm oxides [77], [119]–[121]. This observation could have a significant effect on the reliability projections for such oxides.

In order to measure N^{BD} at lower voltage, i.e., closer to actual operating conditions, it has been necessary perform long-term reliability experiments on bonded chips. Other long duration stress experiments have been performed [91], [122] using thicker oxides. Fig. 9 shows SILC measurements performed for more than 1 year at 2.4 V using n-FETs with $t_{ox} = 2.2$ nm. The horizontal dotted lines in this figure indicate roughly the 10%, median, and 90% values of $\Delta J/J_0$ at breakdown for the higher stress voltages. The 2.4-V stress shows breakdown events occurring at statistically significant higher values of N^{BD}. Fig. 10 shows the cumulative distributions for N^{BD} this sample. For stress voltage ≥ 2.8 V, the N^{BD} distributions are nearly coincident, consistent with the assumption that N^{BD} is independent of V_g. For lower voltages, however, the distributions shift toward higher values of N^{BD}.

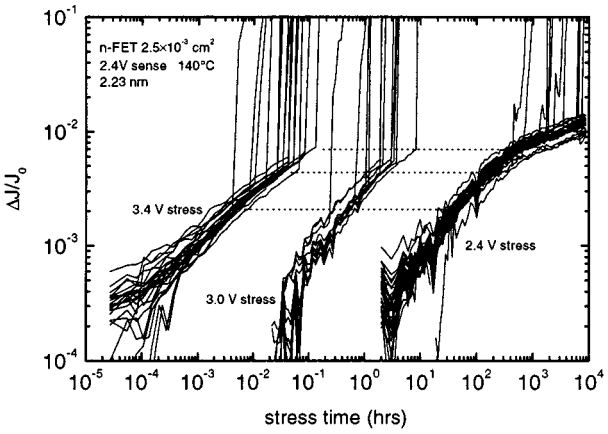


Fig. 9. Long-term stress data, showing SILC data to breakdown for three different stress voltages.

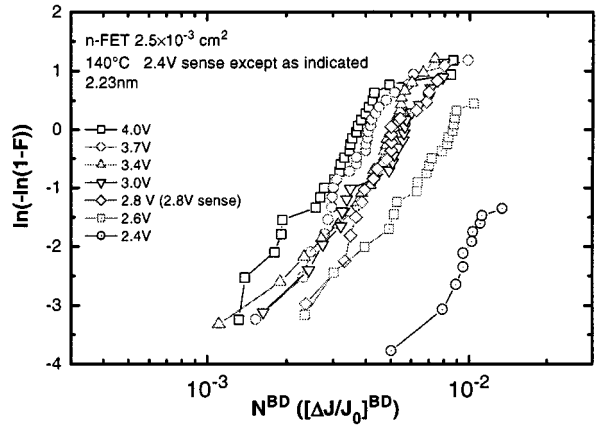


Fig. 10. Weibull plot of the critical defect density distributions at various stress voltages for 2.2-nm oxide.

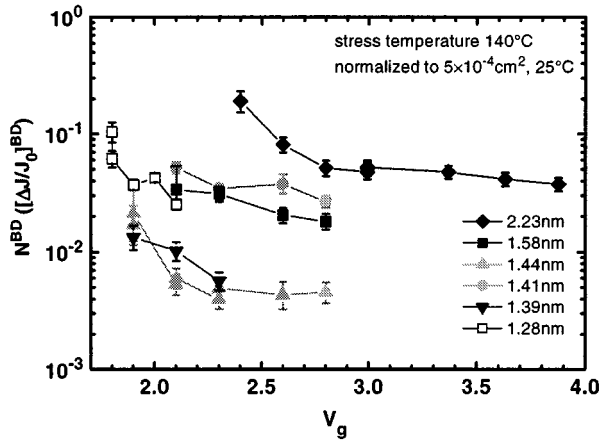


Fig. 11. N_{BD} versus stress voltage for various ultrathin oxides.

In Fig. 11 is plotted the characteristic (63rd percentile) values of N^{BD} versus the gate voltage during stress (V_g) for the same sample as in Figs. 9 and 10 as well as some thinner oxide samples. The oxide thickness is estimated from the accumulation capacitance including quantum mechanical corrections, but it must be admitted that the quoted values are uncertain to at least ± 0.1 nm. Error bars in N^{BD} reflect the statistical uncertainty,

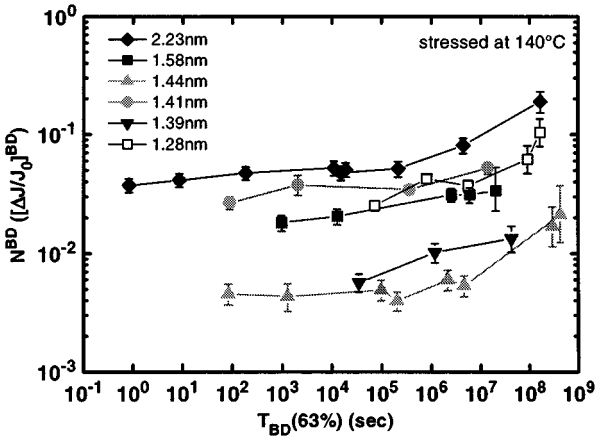


Fig. 12. $N_{\rm BD}$ versus stress time for various ultrathin oxides.

and in some cases at the lowest voltages only ∼10% of the samples had failed and therefore $N^{\rm BD}$ is estimated using the initial fail data and the statistical distributions from higher voltages. In this figure, the $N^{\rm BD}$ values have been normalized to a reference area of 5×10^{-4} cm^2 using Weibull statistics, taking the Weibull slope from data such as those in Fig. 10. The Weibull slope (discussed in more detail later) and $N^{\rm BD}$ are only weakly dependent on $t_{\rm ox}$ in this range. It can be observed that $N^{\rm BD}$ tends to *increase* with reducing V_g. In Fig. 9, it can be seen that the SILC tends to saturate at long times, i.e., the increase in SILC becomes sublinear in time for low voltage. A tendency for SILC to exhibit a saturating behavior at low stress voltage has been reported previously [44], [105]. In spite of this tendency, the ultrathin oxide samples stressed at lower voltage reach a higher average value of $\Delta J/J_0$ before breakdown. Therefore, while the measured $\Delta J/J_0$ may underestimate $N^{\rm BD}$, the observed increase at low voltage is real and correlates with an increase in charge-to-breakdown at low voltage [123].

Although the data in Fig. 11 show a trend for $N^{\rm BD}$ to increase as V_g is lowered, there does not appear to be a universal behavior as a function of V_g. For example, for the 2.23-nm oxide, $N^{\rm BD}$ starts to increase below 2.8 V, while for the 1.44-nm oxide the increase in $N^{\rm BD}$ is not seen until V_g is reduced below ∼2.2 V, and the 1.28-nm oxide shows no increase in $N^{\rm BD}$ even for V_g as low as 1.9 V. In Fig. 12, the same data have been replotted as a function of the breakdown times ($T_{\rm BD}$) instead of the stress voltage. $T_{\rm BD}$ is a function of $V_g, t_{\rm ox}$, and device area. In this figure, $T_{\rm BD}$ is the projected value to 63% failure for cases where not all samples have reached breakdown. Note that, in this figure, $N^{\rm BD}$ is again normalized to a constant reference area, but $T_{\rm BD}$ is not normalized, i.e., the x-axis values reflect the actual time under stress. Here we see that the data show a universal trend, wherein $N^{\rm BD}$ starts to increase for stress times longer than about 10^6 s (∼10 days). The long stress times necessary to see this effect would preclude its observation in most experiments. For the 1.28-nm oxide at 1.8 V (open squares), devices with two different areas were tested, which when plotted against V_g result in different values of $N^{\rm BD}$ even after area normalization (Fig. 11). However, smaller area devices have a longer lifetime, which accounts for the higher value of $N^{\rm BD}$ as shown in Fig. 12.

A voltage-dependent $N^{\rm BD}$ could arise from several sources. The percolation path, which has been modeled in zero field [31], [33] to obtain the fit shown in Fig. 8, could be weakly field-dependent. The formation of the percolation path, i.e., the generation of new defects, could depend on the local field produced by the other defects [124], [125]. This would lead to more directed paths at higher voltage, so that the average defect density to form a connecting path across the sample would be reduced. However, according to the idea that the stress time, not the voltage, is responsible for the increase in $N^{\rm BD}$, the data may be interpreted in terms of the defect "effectiveness" (the fraction f of "active" defects) which was introduced [33], [107], [121] to describe the probability that a defect, or percolation path, can trigger breakdown. For long stress times, a greater defect density is required to trigger breakdown, contrary to the assumption that $N^{\rm BD}$ should be independent of the stress condition. The observation of reduced defect effectiveness for very long duration stress experiments may imply that defects undergo a slow relaxation that reduces their ability to participate in breakdown. It must be emphasized, however, that the final runaway stage of destructive breakdown, whereby a percolation path leads to catastrophic failure, is still not fully understood.

IV. Defect Generation Rate

Extensive work in the 1980s revealed the existence of the so-called "2-eV trap creation threshold" (electron energy measured with respect to the bottom of the SiO_2 conduction band) for defect creation by hot electrons in SiO_2 [23]. For thick oxides, electrons in the conduction band obtain this average energy for oxide fields greater than about 2–4 MV/cm. In the thin oxides which are of current interest, for which electron transport is ballistic or quasi-ballistic, the threshold corresponds to a gate voltage of about 5 V for Fowler–Nordheim tunneling through the 3-eV potential barrier at the Si/SiO_2 interface. For voltages below threshold, it was shown [24] that the defect generation rate depends only on the absolute value of the gate voltage (V_g), independent of substrate or gate doping or polarity. Recent work using the SILC to measure P_g has given the somewhat surprising result that 2 eV is not a hard threshold [25], [119]. Instead, there is a subthreshold trap generation process that decreases exponentially below 5 V. This is shown in Fig. 13, where the SILC and CV data have again been normalized to each other using the same relation as described above for $N^{\rm BD}$.

Fig. 13 includes data from a variety of oxide thicknesses and processes, including "standard" thermal SiO_2 grown in O_2, oxides grown in N_2O, and oxides grown on N_2-ion-implanted (N_2-I/I) substrates, indicating the relative insensitivity of P_g to the oxidation process. P_g is also observed to be independent of stress voltage polarity. For each oxide thickness, it is possible to measure P_g over only a limited range of V_g, in order to keep the measurements within an experimentally accessible time scale. Plotting overlapping ranges of V_g obtained using oxides of different thickness shows a universal exponential behavior of P_g as a function V_g, independent of $t_{\rm ox}$. Using substrate hot electron (SHE) and channel hot electron (CHE) stress, it is possible to obtain much greater hot electron flux at the interface, permitting measurements of P_g at low electron energy even for thick

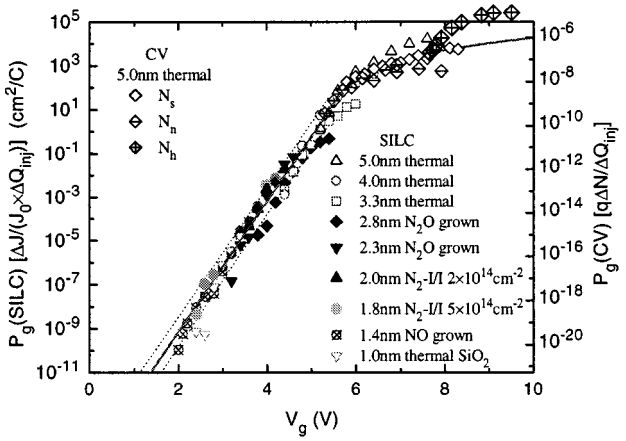


Fig. 13. Defect generation probability measured from SILC (P_g (SILC)) and CV stretch-out (P_g (CV) and N_S), and electron and hole trapping rates (N_n and N_h, respectively), as a function of stress voltage for various oxides.

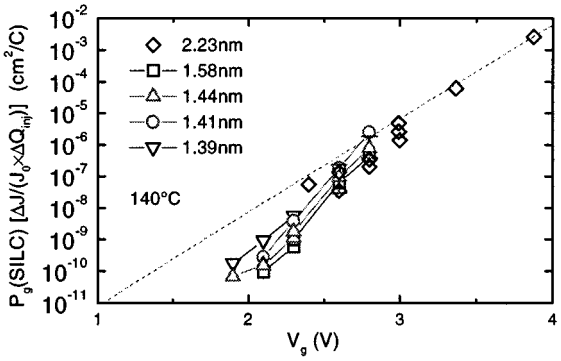


Fig. 14. Detail of P_g data from long-term stress experiments, showing deviation from purely exponential behavior.

samples. Using these techniques, it has been shown [25], [126], [127] that defect generation by hot electrons impinging on the substrate–oxide interface follows the same dependence on energy as that from Fowler–Nordheim injection through the oxide, and that the exponential V_g dependence extends at least as low as 1.2 V [127].

A remarkable and unexpected feature of the data of Fig. 13 is that there is no hard threshold voltage below which the generation rate drops faster than the exponential trend. In particular, there is no large discontinuity or change in slope at the transition from Fowler–Nordheim to direct tunneling at about 3 V. This is contrary to earlier suggestions [128], [129] that breakdown would be strongly suppressed in the direct tunneling regime and strongly suggests that the relevant energy scale is the electron energy in the anode, which is the poly-silicon gate or the silicon substrate depending on injection polarity. Although the rate of defect generation decreases approximately exponentially with supply voltage below a threshold voltage of about 5 V for hot electron-induced hydrogen release, detailed measurements [123], [127] have found an inflection in the voltage dependence of P_g between 2–3 V. This is shown in Fig. 14. Taken together, the complete measurements of P_g and N^{BD} can explain in detail the voltage and thickness dependence of Q_{BD} in ultrathin gate oxides, shown in Fig. 15(a).

In addition to the interface state (N_s) and bulk electron trap (N_n and SILC) densities, Fig. 13 also includes data on hole trapping (N_h) showing the anode hole injection threshold at $\sim$7.5 V. [22] The offset between this threshold and the lower trap creation threshold clearly establishes the subthreshold tail as being related to the trap creation (hydrogen release) process and not anode hole injection.

Measured over a sufficiently wide range of stress conditions, neither T_{BD} nor Q_{BD} will obey any simple "law" such as exponential dependence on $E, 1/E$, or V_g, as has been commonly assumed in reliability extrapolations. Without the simplifying assumptions of a voltage-independent N^{BD} and a purely exponential voltage dependence of P_g, it becomes more difficult to extrapolate reliability to operating voltage. The steeper V_g dependence of P_g between 2–3 V can easily lead to an overly optimistic T_{BD} projection if data are limited to this range. Likewise, projection of data from higher voltages without knowing the complete V_g dependence may lead to more pessimistic projections. Moreover, according to the idea that N^{BD} increases for long stress duration, breakdown is a time-dependent as well as voltage-dependent phenomenon. Care must be taken when interpreting Q_{BD} or T_{BD} data to separate the voltage- and time-dependent effects.

V. Lifetime

Although Q_{BD}, defined as the time-integrated current density that flows through the oxide until breakdown occurs, is the physically meaningful quantity, the quantity of interest for an electronic component is the failure rate, which can be derived from the lifetime or time-to-breakdown, T_{BD}. For constant voltage stress, this is related to Q_{BD} by the relation

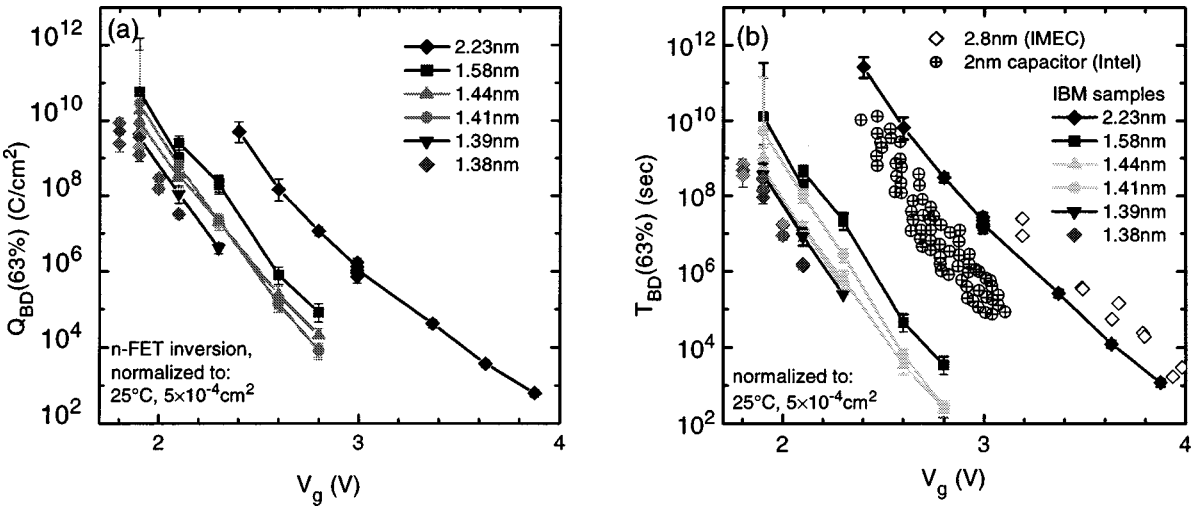
$$\int_0^{T_{\mathrm{BD}}} J\,dt = Q_{\mathrm{BD}} \tag{3}$$

where J is the instantaneous value of the current density. For thin oxides, the current is nearly constant until breakdown (in marked contrast to thicker oxides, where electron trapping and/or hole trapping cause large changes in the current during stress), therefore

$$T_{\mathrm{BD}} = Q_{\mathrm{BD}}/J. \tag{4}$$

The tunnel current density increases exponentially with decreasing oxide thickness [104]. Therefore, from (4), T_{BD} decreases exponentially with decreasing $t_{\mathrm{ox}} \lesssim 3$ nm even though Q_{BD} [Fig. 15(a)] is only slightly thickness-dependent in this range due to the weak thickness dependence of N^{BD}. The measured T_{BD} data are shown in Fig. 15(b). This implies a rapidly diminishing margin for reliability as device dimensions are scaled. Fig. 15(b) also shows that data from different labs [112], [123], [130] are in reasonable agreement, taking into account the differences in oxide thickness, indicating little dependence on processing for state-of-the-art facilities.

It is commonplace in the microelectronics industry to specify an operating life of ten years, i.e., to guarantee a specified (usually small) failure rate over a 10-yr period. First the T_{BD} data



(a) (b)

Fig. 15. (a) $Q_{\rm BD}$ data from long-term stress experiments on ultrathin oxides. (b) $T_{\rm BD}$ data from long-term stress experiments, and published data from other labs. All data have been scaled to a reference area using Weibull statistics and to room temperature.

such as those in Fig. 15(b) must be projected from the high percentiles where experimental data are collected to low percentiles desired for the product failure rate. Second, a lifetime correction must be made from the small-area test structures to the total gate oxide area of a chip. Both of these projections depend on the shape of the breakdown distribution, which must be known for accurate reliability estimates.

The statistics of gate oxide breakdown are described using the Weibull distribution [5], [31], [131]–[134]

$$F(x) = 1 - \exp[-(x/\alpha)^{\beta}] \tag{5}$$

which is an extreme-value distribution in $\ln(x)$ and is appropriate for a "weakest-link" type of problem. Here F is the cumulative failure probability, i.e., the population fraction failed by age x, where x can be either charge or time. The characteristic life α is the 63.2th percentile, and β is called the slope parameter or Weibull slope. Plotting

$$W \equiv \ln[-\ln(1-F)] \tag{6}$$

against $\ln(x)$ yields a straight line with slope β (see Fig. 16).

Gate oxide failure is a weakest-link type of problem because failure of the whole chip is defined by the failure of the first individual device, and a device fails if any small portion of the gate area of the device breaks down. From elementary statistics, if the probability of any one unit failing is p then the probability of any one of N independent units failing is

$$F = 1 - (1-p)^{N} \tag{7}$$

so that

$$\ln[-\ln(1-F)] = \ln N - \ln[-\ln(1-p)]. \tag{8}$$

The Weibull plot [(6)] thus has the extremely useful property that if the area is increased by a factor N then the curve shifts vertically by $\ln(N)$. Fig. 16 illustrates this effect schematically. If the desired low failure rate is $F_{\rm chip}$ over the product lifetime $T_{\rm life}$ for the total gate area $A_{\rm ox}$ on the chip (point indicated by the asterisk in Fig. 16), this is equivalent to a higher failure rate $F_{\rm test}$ in time $T_{\rm test}$ on the test structures with area $A_{\rm test}$, where from Fig. 16 we can obtain

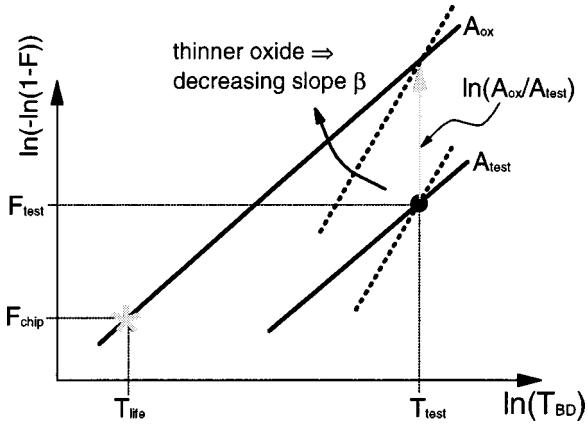


Fig. 16. Procedure for extrapolation to small failure rate and chip area, illustrating the effect of Weibull β on area scaling and failure rate projection.

$$\frac{T_{\rm life}}{T_{\rm test}} = \left(\frac{A_{\rm test}}{A_{\rm ox}}\right)^{1/\beta} \left(\frac{\ln(1-F_{\rm chip})}{\ln(1-F_{\rm test})}\right)^{1/\beta} \approx \left(\frac{A_{\rm test}}{A_{\rm ox}}\frac{F_{\rm chip}}{F_{\rm test}}\right)^{1/\beta}. \tag{9}$$

The appropriate β to use in (9) is the one corresponding to the projected operating voltage. The assumption is generally made that β is independent of V_g. This equation is used to scale measured breakdown times to the expected product lifetime, or equivalently to estimate the chip failure rate from test structure measurements. Since $F_{\rm chip} < F_{\rm test}$ and typically $A_{\rm test} < A_{\rm ox}$, then $T_{\rm test} > T_{\rm life}$ by this equation, therefore it is always necessary to measure the test structure under accelerated stress conditions (voltage and temperature). Understanding the voltage dependence is the major reason for investing the time to obtain long-term stress data as shown in Fig. 15, and is the reason so much attention is paid to the physical model for trap generation and breakdown, as discussed above [135], [136].

There is no guarantee in practice that actual failure distributions will be perfectly linear on a Weibull plot, and other distributions could in principle be more appropriate [133]. Nonetheless, a study of 900 samples [135] clearly supported the Weibull distribution down to a failure rate of 10^{-3}. In the simplest case, the presence of multiple failure modes such as extrinsic failure caused by processing defects will lead to bi- or multi-modal distributions with varying slope. A subtler problem can arise from nonuniformity of $t_{\rm ox}$, which will lead to variations in $Q_{\rm BD}$ because of the thickness dependence of the critical defect density and will cause further variation in $T_{\rm BD}$ because of the thickness dependence of the tunnel current. This will lead to distortion and curvature of the Weibull plot [137], [138]. Such issues can seriously complicate the otherwise rather straightforward projections. Curvature in the Weibull plot usually indicates a problem such as extrinsic failure modes or nonuniformities that need to be dealt with before the data can be reliably interpreted.

From the previous discussion, it can be seen that an important parameter for reliability projections is the Weibull slope β. A key advance was the realization that β is a function of $t_{\rm ox}$, becoming smaller as $t_{\rm ox}$ decreases [24], [31], [33]. The thickness variation of the Weibull slope of the $Q_{\rm BD}$ distribution stems from the properties of $N^{\rm BD}$ and is a statistical property of the percolation model for $N^{\rm BD}$. It is an intrinsic property of the breakdown of ultrathin oxides and does not imply that the breakdown mechanism is changing. A smaller β means greater sensitivity to the area and failure rate extrapolations and gives more pessimistic projections via (9), so this is a crucial issue for predicting breakdown of ultrathin oxides. It is often difficult to obtain an accurate value of β from a direct measurement of the failure distribution, because of thickness variations and statistical uncertainty [139]. In order to circumvent these difficulties, Wu [135], [140] adopted the area scaling relation of (9) in order to obtain accurate values.

Fig. 17 shows schematically how the failure rate and area projections each reduce the maximum operating voltage allowable for a particular reliability specification. The effects are greater for thinner oxides, because of the lower value of β. In addition, the operating temperature must be taken into account, since $T_{\rm BD}$ and $Q_{\rm BD}$ are strongly temperature-dependent especially for $t_{\rm ox} \lesssim 3$ nm [77], [141], [142].

VI. Functional Reliability

The preceding discussion has shown how the reliability margin for gate oxide breakdown has been drastically reduced as a consequence of device scaling. Published models [69], [104], [111], [112], [123] have indicated that, for the oxides used in the past with $t_{\rm ox} \gtrsim$ 3–4 nm, intrinsic gate oxide reliability has probably not been a real issue. However, the time is near when it will no longer be possible to meet reliability specifications for ultrathin gate oxides, although the exact point when this will happen is the subject of considerable debate. At present, predicted reliability "limits" for the gate oxide thickness range from less than 1.5 nm [69] to 2.8 nm [111], [112]. Even if the smallest estimates were correct, the latest international roadmap for the industry [143] anticipates that $t_{\rm ox} \sim 1$ nm will be needed by 2005 for 60–70-nm gate lengths (90-nm lithography node) operating at $\sim$1 V in order to meet the desired performance targets. One way this might be achieved is by replacing the SiO_2 with another dielectric with a higher dielectric constant, such as metal oxides, metal silicates, and epitaxial perovskites. This avenue is being aggressively pursued but faces large hurdles, as neither the materials science nor the electrical properties of these materials are understood nearly as well as for SiO_2. A more conservative approach is to used nitrided oxides, which have shown somewhat improved reliability characteristics compared to pure SiO_2 [144], [145].

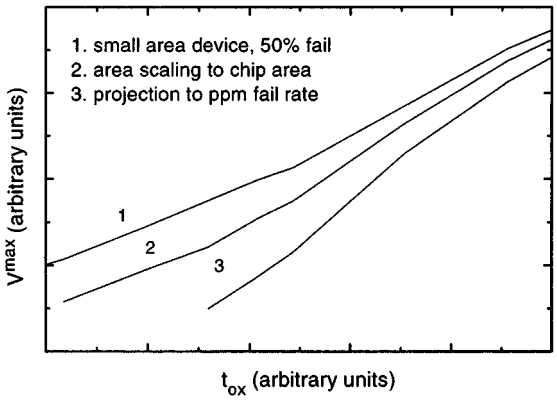


Fig. 17. Schematic illustration of the effect of area and failure rate projections on the maximum operating voltage as a function of oxide thickness.

Up to now, the definition of oxide breakdown has generally been the first event marked by a discrete jump in leakage current. Some researchers have pointed out, however, that often the magnitude of this jump is not great enough to completely destroy the functionality of a transistor, much less that of an entire circuit [146]–[148]. It has been suggested that the definition of breakdown which we have been using, although *physically* a correct signature of the formation of a conducting path across the insulator, may not be the appropriate *practical* criterion for product reliability specification. Most work up to now has focused on the understanding of the defect generation leading to breakdown. If product reliability is to be assured, it will be necessary to focus more attention on understanding the nature of the conduction after breakdown [149]–[159] and on the impact of this conduction on device and circuit functionality.

A. Soft Breakdown

The so-called "soft" breakdown (SBD) or "quasi-breakdown" was first reported [160]–[162] in 3–4-nm oxides subjected to either constant-current [161], [162] or constant-voltage [160] stress. After first showing a uniform degradation in the form of SILC, the oxides exhibited a sudden jump to a fluctuating (noisy) current with high leakage at low voltage. The SBD phenomenon has recently been thoroughly reviewed [158] and so we will only highlight certain aspects here.

The fact that the *I–V* characteristic after SBD merges with the prebreakdown Fowler–Nordheim characteristic at higher voltages distinguishes this mode from the destructive, or "hard" breakdown (HBD). The latter type is probably a result of thermal damage [158] when sufficient energy is deposited during the breakdown transient [107], [163]–[174]. There is probably some confusion in the literature over the precise

characterization of breakdown events as "soft" or "hard" because of the lack of a precise definition and because for some experimental conditions the detection of one or the other breakdown mode may be difficult. For example, when testing a large-area structure or a very thin oxide where the initial current is larger than the breakdown current, a "soft" event could be missed, or a "hard" event could be interpreted as soft. Initially, it was argued [175] that SBD is a precursor of HBD, i.e., that an SBD spot will become hard after some time. This view was not consistent with a later statistical analysis of data [176] showing that the distribution of breakdown times is independent of whether they are soft or hard, and that an HBD which occurs after an SBD is a random event uncorrelated with the first SBD spot. It was also shown that SBD and HBD follow similar area dependence [177] but the temperature dependence and voltage dependence were found to be different [178] or the same [179] in different laboratories. The similar light emission spectral characteristics of SBD and HBD [180] also support the idea that they are related phenomena, differing only in the size of the breakdown spot. This conclusion has been questioned in turn by a different analysis of data [181] finding subtle differences in the parameters describing both the statistical distributions and the voltage dependence of SBD and HBD.

Soft breakdown is the most common mode for a constant-current stress, while hard breakdown may occur during constant-voltage stress [182]. The soft breakdown is a localized spot, which can be shown by measuring the area dependence [153], [158], [160], [161], [181] or by viewing the optical emission [17], [161], [181], [183]. The size of this spot is 10^{-14} to 10^{-12} cm^2 [158]. Several soft breakdown events, occurring in different spots, may sometimes be seen in large-area devices prior to a hard breakdown [153], [155], [158], [160], [175], [184]. In addition, the SBD current voltage *(I–V)* characteristic is independent of the oxide thickness at least down to 3 nm, within a band of observed curves [153], [155], [158], [185]. In contrast to the "hard" breakdown (HBD) which shows a roughly linear (ohmic) *I–V* characteristic of resistance $\sim$10 kΩ if the damage region remains localized and does not propagate, [107], [158] the SBD *I–V* characteristic is a power-law with an exponent of 3–6, [149], [150], [158], [186] although it maybe better described by an exponential voltage dependence [159]. The SBD voltage dependence can be explained by a quantum point contact model [151], [153]–[156], [158], [159], although other models have been proposed as well [149], [150], [187]–[190]. The point contact model can account for both SBD and HBD within a single framework as two limiting cases, depending only on the lateral size of the breakdown spot which determines the energies of the subbands in the conduction path [158].

Simultaneous with the jump in gate current after SBD is a large increase in the substrate hole current (for the case of n-FETs biased in inversion) [161], [189]–[192] and the p-channel hole tunneling current (for p-FETs in inversion) [174], [188]–[190]. For the n-FET case, this was attributed to valence band tunneling or back-injection of holes generated in the anode, but a recent study found that the spectral characteristics of the light emission from breakdown spots is similar to that generated by hot carriers in the channel of a MOSFET, suggesting that the substrate current is dominated by impact ionization in the space charge region of the channel near the breakdown spot [180].

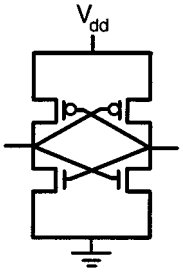


Fig. 18. Basic SRAM storage cell.

B. Device Breakdown

It was suggested early on [161] that the SBD leakage at low voltage would be too large for device applications and therefore SBD should be regarded as oxide failure. In addition, the appearance of large fluctuations in the direct tunneling current led to the consensus that SBD should be identified as the dielectric breakdown [162], [193]. This view was not questioned until others [146] claimed that gate current noise was the *only* detectable effect of SBD on n-FETs fabricated with a 2-nm gate oxide and that there was no correlated degradation in either the threshold voltage (V_T) or transconductance (g_m). It was therefore suggested that SBD would not cause device or circuit failure in many applications [146]. However, Pompl *et al.* [194] and others [135], [138], [195], [196] later showed that SBD will cause a significant increase in the transistor-off current if the breakdown spot is in the drain region, which is increasingly likely in short-channel devices. This will be referred to as "device breakdown." In a study of the channel length- and width-dependence of device breakdown in n-FETs stressed at 4.1 V, Wu [135], [177] showed that, for short-channel devices (0.2-μm channel length), the distribution of oxide breakdown times for the first breakdown event coincides with the distribution of device breakdown times, whereas for longer channels (10 μm) the device breakdown occurs some time after the first soft breakdown. After a "hard" breakdown, the device is clearly nonfunctional by any ordinary criterion, exhibiting a negative drain current when the gate-to-drain leakage exceeds the normal transistor on current [194]. However, even a hard breakdown may not completely destroy circuit functionality: Kaczer *et al.* [197] showed that in some cases a circuit may be able to survive an oxide breakdown that previously would have been assumed to be catastrophic.

In a CMOS circuit, the stress conditions on a transistor gate are not the same as the typical experimental conditions used to study reliability. A circuit does not usually subject a gate to either a constant-voltage or a constant-current stress, which are the two types of stress typically employed, but rather to a current-limited stress in which the current through a breakdown spot is limited by the saturation on-current (Idsat) of a complementary transistor in series [172]. Fig. 18 shows the situation for an SRAM cell consisting of two cross-coupled inverters. Not all circuits will fall into this category, for example some gates

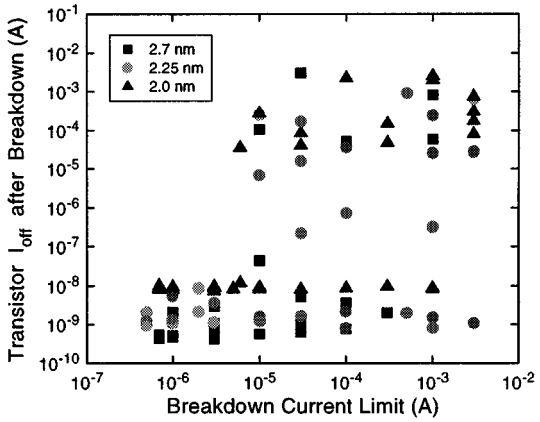


Fig. 19. The n-FET off current $(I_{\rm off})$ after breakdown versus the value of the breakdown current limit.

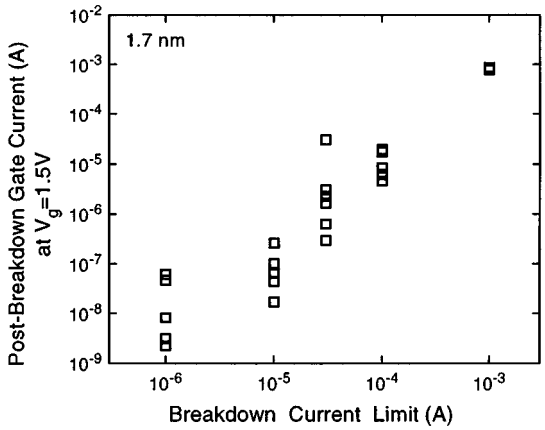


Fig. 20. The post-breakdown conduction measured at $V_G = 1.5$ V as a function of the stress compliance level.

will be driven by a low-impedance clock, but SRAM occupies a large fraction of the area of many chips and therefore it is a useful place to begin an investigation of circuit reliability. In the SRAM cell, the gate oxides are not connected directly to the power supply. The n-FET gates are connected via p-FETs, and the p-FET gates via n-FETs. Compared to a typical constant voltage source, the small transistor in series has much higher impedance, a much lower current capability, and a lower capacitive loading. To simulate the stress that gate oxides experience during circuit operation, Linder [172] purposely limited the post-breakdown current using the compliance setting of a voltage source or by inserting a transistor between the voltage source and device under test. The compliance level could be set to emulate the saturation current of the drive transistor. In order to prevent this from being a simple constant current stress, the initial stress current must be significantly less than the current limit, necessitating the testing of small area devices.

The n-FET off current $(I_{\rm off})$ after breakdown is plotted versus the value of the current limit in Fig. 19. For a current limit less than $\sim$10 μA, the off current remains small after oxide breakdown, while higher current limits resulted in a wide range of $I_{\rm off}$ values [172]. Thus it appears that small current limits (corresponding to very small p-FET drivers) halt the breakdown event such that the transistors may still be operational. Toriumi [173], [174] similarly showed that increasing the circuit time constant, by inserting an inductive impedance in series with the device, will reduce the severity of the breakdown, without affecting the breakdown time, and Lombardo *et al.* have observed that the breakdown becomes softer at low inversion layer density [198]. This shows that the nature of the breakdown spot is influenced by the circuit environment of the device, which in turn may affect the overall projected reliability of a circuit.

Fig. 20 shows the post-breakdown conduction measured at $V_g = 1.5$ V as a function of the stress compliance level [172]. Again there is a transition at about 10^{-5} A compliance, corresponding to a series resistance of $\sim 10^5$ Ω. Below this value, the n-FET leakage remains below 10^{-7} A, but for higher current limits the leakage increases more rapidly. The compliance level of 10^{-5} A corresponds to Idsat of a small p-FET, such as might be used in an SRAM cell. For fast logic circuits, p-FET Idsat values of $\sim 10^{-4}$ A are likely, in which case the n-FET post-breakdown leakage will average $\sim 10^{-5}$ A. At this level of leakage, the voltage drop across the p-FET channel in Fig. 18 after n-FET oxide breakdown is expected to be $\sim$0.1 V. This amount of voltage droop can probably be tolerated by most logic circuits. However, there is a distribution of post-breakdown leakage levels [108], [156], [158], [170], [171], [186] so it is likely that some circuit failures will occur as a result of oxide breakdown. The overall effect of SBD on circuit performance is still an open question since many different circuit elements are used in practice and some may be more sensitive than others to noise and voltage margins.

Even if devices survive after an initial breakdown event, the subsequent stress on the damaged oxide can lead to erratic behavior and a progressive degradation of the device characteristics [135]. Thus, it would be premature to disregard oxide breakdown as a factor in circuit reliability. Much more research will be needed in order to formulate a complete methodology for the quantitative prediction of device and circuit reliability.

VII. Conclusion

In this paper, we have reviewed the physics and statistics of dielectric wearout and breakdown in ultrathin SiO_2-based gate dielectrics. Electrons or holes tunneling through the gate oxide generate defects until a critical density is reached and the oxide breaks down. A percolation model can explain the critical defect density and the thickness dependence of the Weibull slope. Some fundamental aspects are still unknown, e.g., the microscopic nature of the defects and what factors determine how a percolation path leads to breakdown. The rate of defect generation decreases approximately exponentially with supply voltage, below a threshold voltage of about 5 V for hot electron-induced hydrogen release. There is strong evidence for the role of hydrogen in defect creation, but other models, specifically the thermochemical and AHI models, are also in widespread use. Some aspects of these models are not in accord with certain experimental data, and so more experimental and theoretical work will be required for a complete understanding.

The direct tunneling current increases exponentially with decreasing oxide thickness, leading to a decreasing time-to-breakdown and a diminishing margin for reliability as device dimen-

sions are scaled. Estimating the reliability of the dielectric requires an extrapolation from the measurement conditions (e.g., higher voltage) to operation conditions. Because of the diminished reliability margin, it has become imperative to try to reduce the error in this extrapolation. Long-term (>1 year) stress experiments are now being used to measure the wearout and breakdown of ultrathin (<2 nm) dielectric films as close as possible to operating conditions. From measurements over a wide range of stress conditions, we find that neither $T_{\rm BD}$ nor $Q_{\rm BD}$ will obey any simple "law" such as exponential dependence on $E, 1/E$, or V_g, as has been commonly assumed in reliability extrapolations. Thus, it becomes more difficult to extrapolate reliability to operating voltage.

The nature of the electrical conduction through a breakdown spot will have a significant bearing on the degree to which the oxide breakdown affects device and circuit performance. The definition of oxide breakdown has generally been the first event marked by a discrete jump in leakage current. However, sometimes the magnitude of this jump may not be great enough to completely destroy the functionality of a transistor, much less that of an entire circuit. The "hardness" of breakdown is influenced by several factors, including the circuit in which the oxide is used. Conversely, different circuits will have various degrees of sensitivity to erosion of noise and voltage margins resulting from oxide breakdown, so more research is needed in order to develop a quantitative methodology for predicting the reliability of circuits.

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