Physical Design Automation for 3D Chip Stacks – Challenges and Solutions

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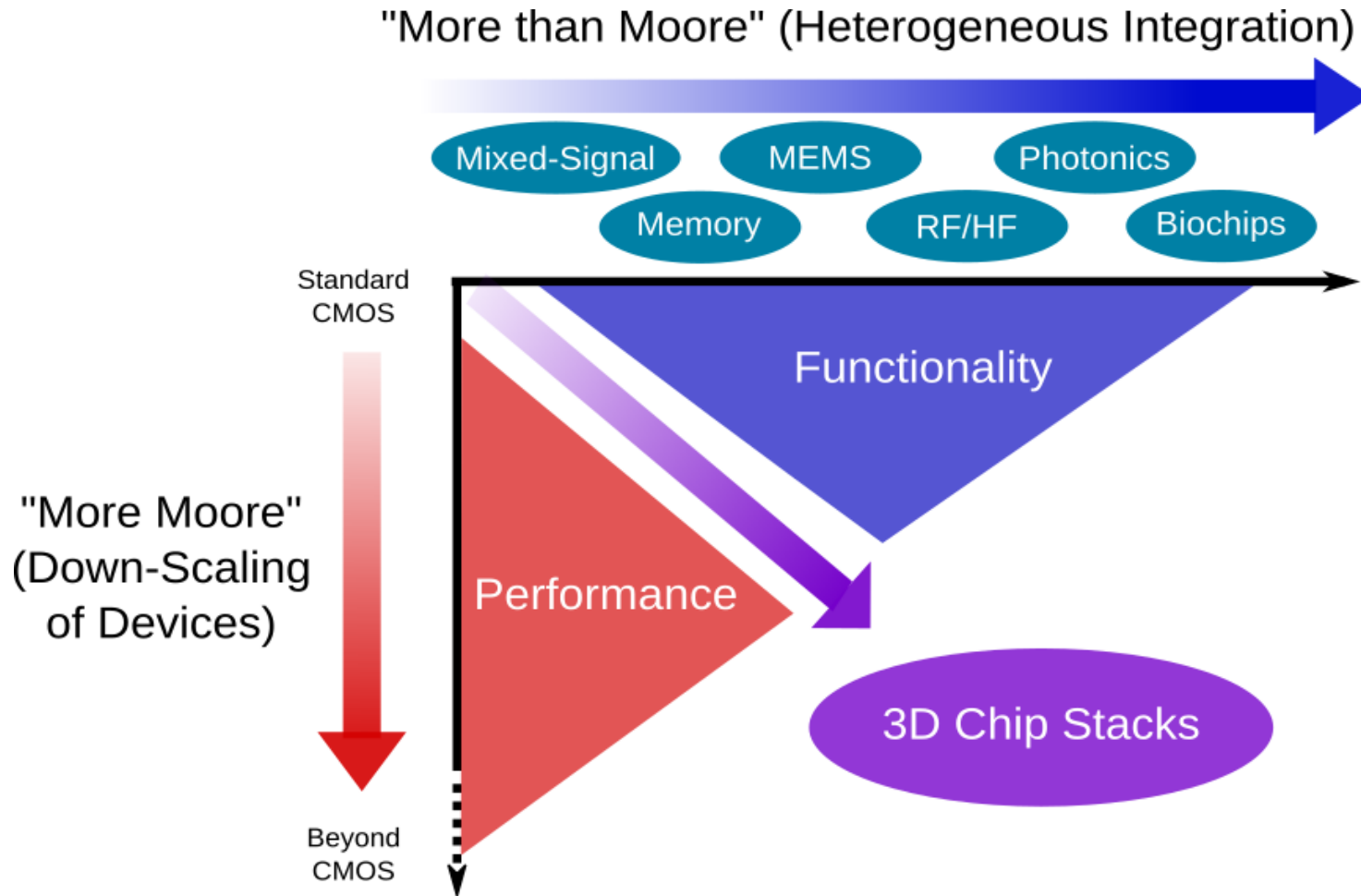
TwinLab "3D Stacked Chips"
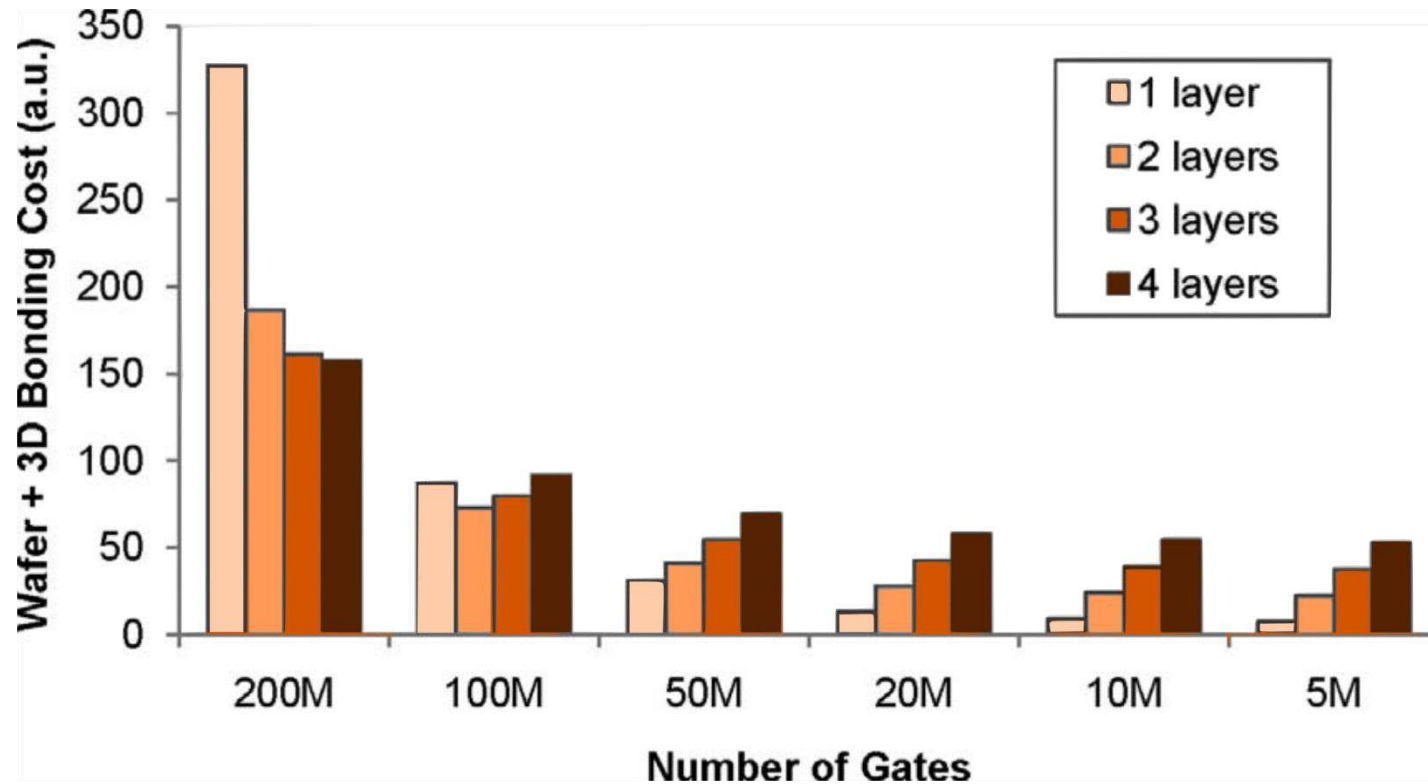Masdar Institute and TU Dresden

ISPD 2016, April 4

Outline

1. Introduction: Motivation and 3D Chip Stacking Options

2. Classical Challenges – Aggravated but Solvable

3. Novel Design Challenges and Emerging Solutions

4. Summary

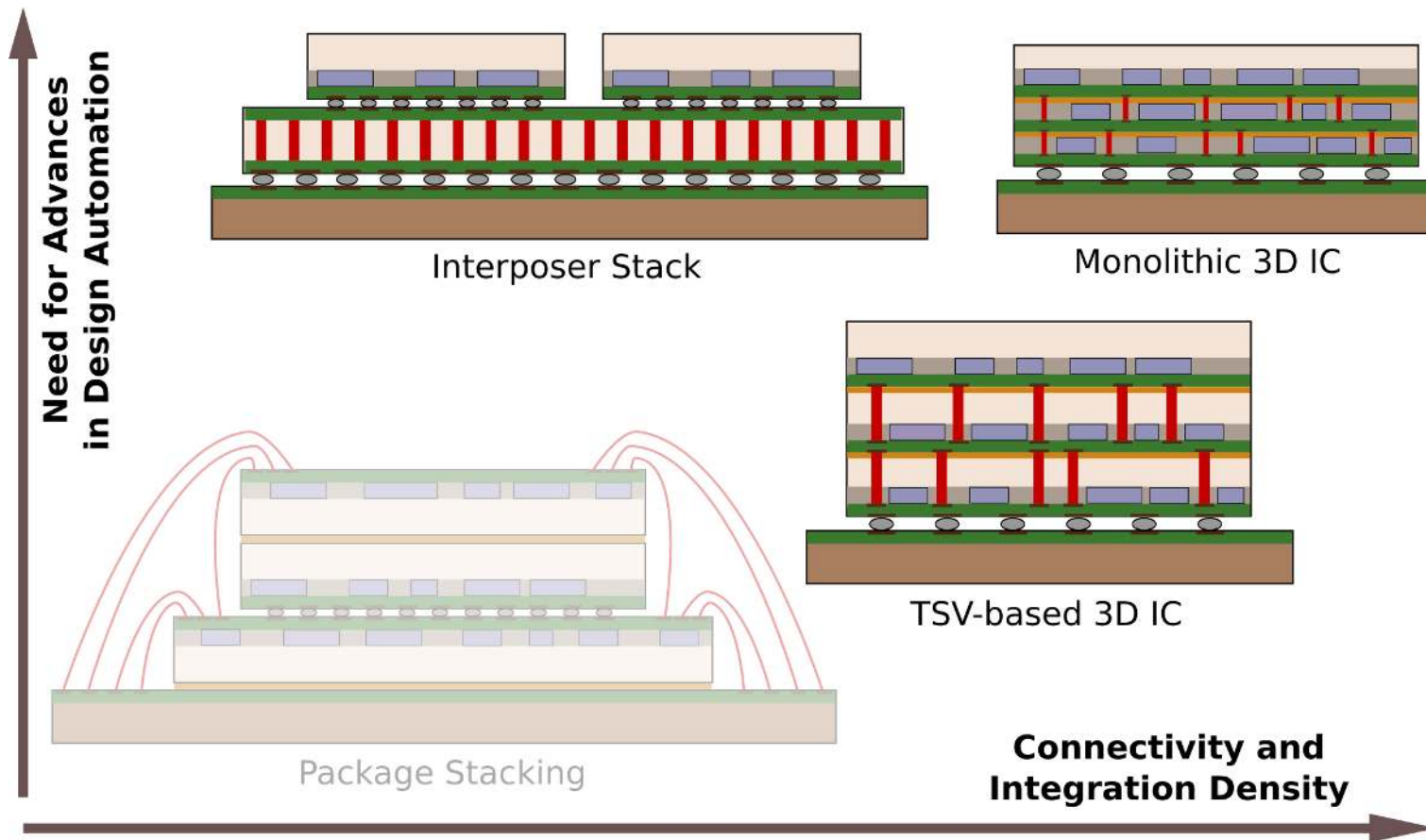# 3D Chip Stacks: Meeting Trends for Modern Chip Design

3D Chip Stacks: Cost Benefits

Dong, X.; Zhao, J. & Xie, Y. "Fabrication Cost Analysis and Cost-Aware Design Space Exploration for 3-D ICs" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2010, 29, 1959-1972

J. Knechtel, J. Lienig "Physical Design Automation for 3D Chip Stacks – Challenges and Solutions," Proc. of the ACM 2016 Int. Symposium on Physical Design (ISPD'16), Santa Rosa, CA, pp. 3-10, April 2016

3D Chip Stacking Options

Interposer Stack

Monolithic 3D IC

TSV-based 3D IC

Package Stacking

Need for Advances in Design Automation

Connectivity and Integration Density

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Power Delivery and Thermal Management

⚠ For *d* dies, approx. *d*-fold power density than 2D chips
  - Large current to be delivered without excessive noise
  - Large heat to be dissipated

🟢 Arrangement of TSVs
  – Distribute PG TSVs
  – Align TSVs for better heat dissipation

clustered P/G TSV location   distributed P/G TSV location
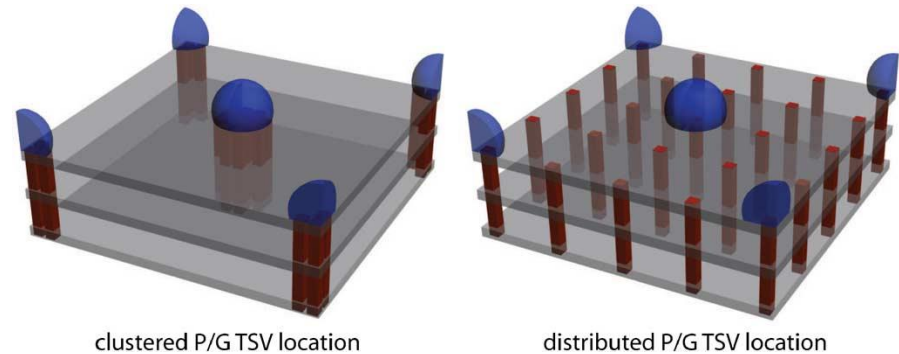
Healy, M. B. & Lim, S. K. "Distributed TSV Topology for 3-D Power-Supply Networks" Trans. VLSI Syst., 2012, 20, 2066-2079

🟢 Dedicated 3D PDNs
  – Synchronize synthesis of PG grids among all dies

🟢 Low-power, thermal-aware design

🟢 Technological measures: decap dies, multiple power supplies, microfluidic channels, etc.

Clock Delivery

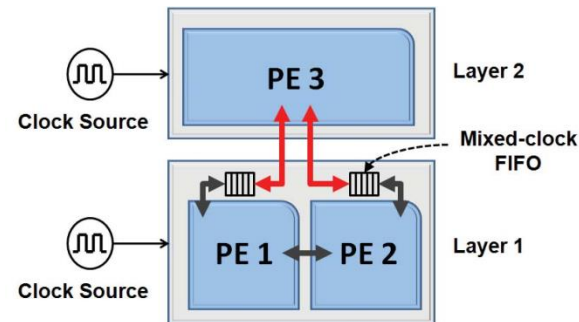⚠ **Reliable, uniform and high-speed delivery across multiple dies**

➡ **Redundant and/or array arrangement of clock TSVs**
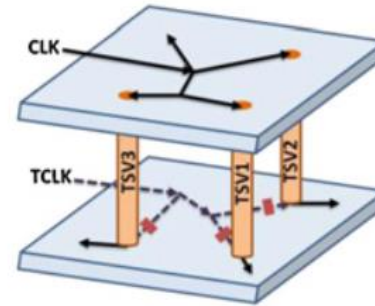
Lung, C.-L. et al. "Through-Silicon Via Fault-Tolerant Clock Networks for 3-D ICs" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 1100-1109

➡ **Multiple clock domains**
   – Mitigate inter-die variations
   – Enable testability

Garg, S. & Marculescu, D. "Mitigating the Impact of Process Variation on the Performance of 3-D Integrated Circuits" Trans. VLSI Syst., 2013, 21, 1903-1914
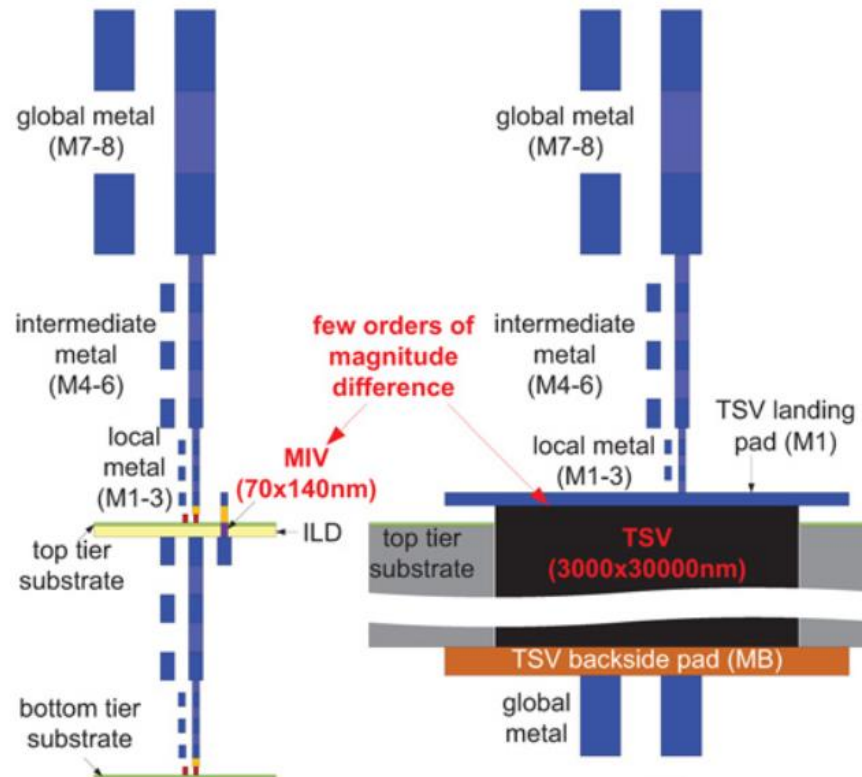
➡ **Dedicated 3D clock-network synthesis**
   – Account for vertical interconnects' impact on timing (variations)
   – 3D extension of effective techniques such as MMM and DME

Partitioning and Floorplanning

⚠️ Traditional 2D metrics not sufficient

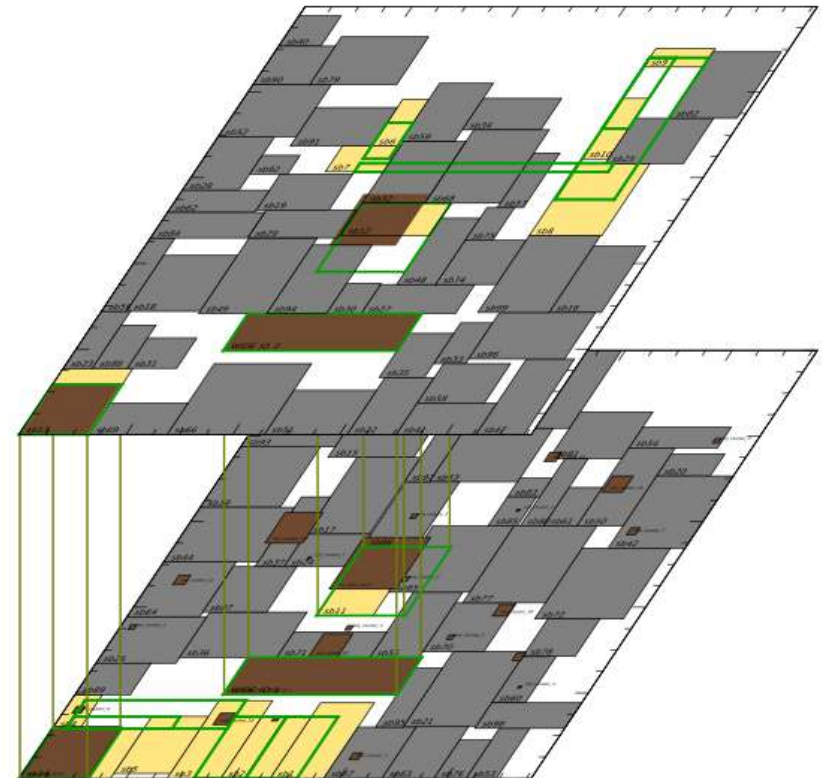➡️ Technology-aware partitioning; not min-cut

Lee, Y.-J. & Lim, S. K. "Ultrahigh Density Logic Designs Using Monolithic 3-D Integration" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 1892-1905

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Partitioning and Floorplanning

⚠️ Traditional 2D metrics not sufficient

▶️ Technology-aware partitioning; not min-cut

Knechtel, J.; Young, E. & Lienig, J. "Planning Massive Interconnects in 3D Chips" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 1808-1821

▶️ Multi-objective floorplanning
- Thermal management
- Stress management
- PDN-noise management
- Interconnects-aware timing
- Co-arrangement of modules and global interconnects
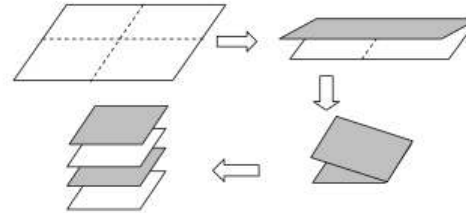
▶️ Fast, holistic and accurate design evaluation

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10

Placement

⚠ Placement throughout the 3D domain is complex

▶ **Folding-based placement**
  – Practical for monolithic ICs

Cong, J.; Luo, G.; Wei, J. & Zhang, Y. "Thermal-Aware 3D IC Placement Via Transformation" Proc. Asia South Pacific Des. Autom. Conf., 2007, 780-785

▶ **Analytic placement**
  – Solving systems of equations either for 2.5D or 3D domain
  – Complex; requires clustering and coarsening, global smoothing, etc.

▶ **Hierarchical placement**
  – A framework for GP, DP, legalization
  – Not restrictive; analytical placer etc.
  – Co-placement of TSVs
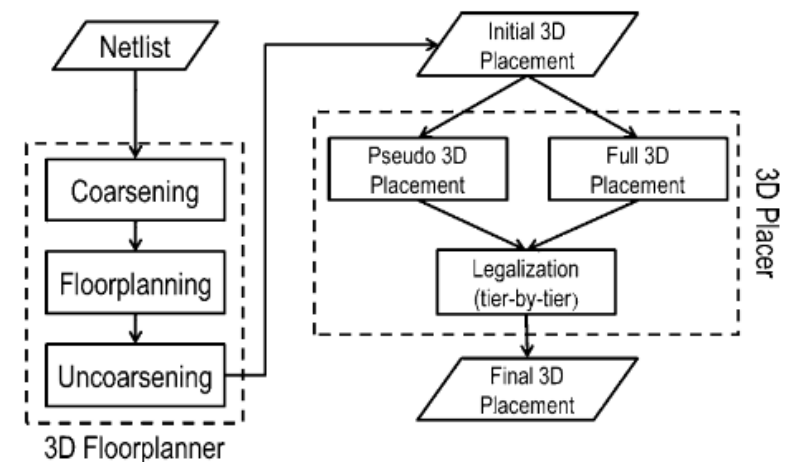
Luo, G.; Shi, Y. & Cong, J. "An Analytical Placement Framework for 3-D ICs and Its Extension on Thermal Awareness" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 510-523

Routability Estimation and Routing

⚠️ Nets may span across multiple dies; heterogeneous topologies

➡️ Analytic and heuristic estimation
   – Extended HPWL and routing graphs
   – Interconnects models, with TSV parameters, buffer emulation etc.
   – Probabilistic models, used for routability-driven paritioning or placement
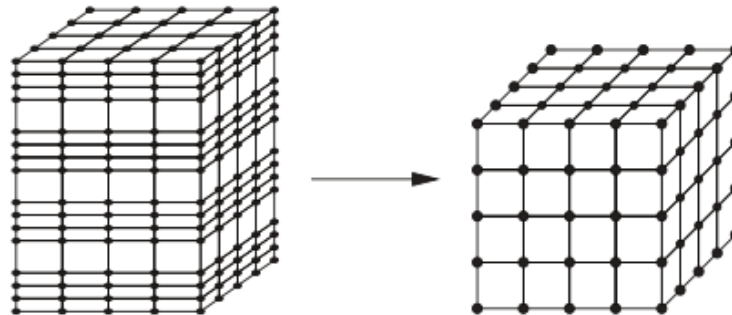

Fischbach, R.; Lienig, J. & Meister, T. "From 3D circuit
technologies and data structures to interconnect prediction"
Proc. Int. Workshop Sys.-Level Interconn. Pred., 2009, 77-84

Routability Estimation and Routing

⚠ Nets may span across multiple dies; heterogeneous topologies

➡ Global routing
  – TSV-based 3D ICs: 3D Steiner trees, thermal analysis, (re)arrange TSVs
  – Interposer stacks: 3D NoC design; challenging for heterogeneous stacks
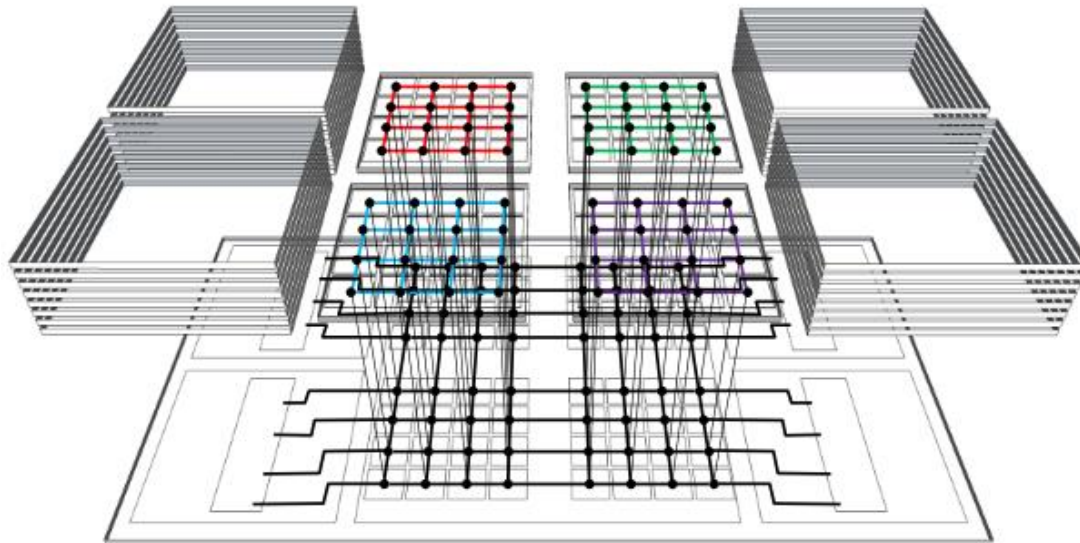
Loh, G. H.; Jerger, N. E.; Kannan, A. & Eckert, Y. "Interconnect-Memory Challenges for
Multi-chip, Silicon Interposer Systems" Proc. MEMSYS, 2015, 3-10

Routability Estimation and Routing

⚠ Nets may span across multiple dies; heterogeneous topologies

➡ Global routing
- TSV-based 3D ICs: 3D Steiner trees, thermal analysis, (re)arrange TSVs
- Interposer stacks: 3D NoC design; challenging for heterogeneous stacks

➡ Detailed routing: not fundamentally different once vertical and global interconnects are planned for

Testing

⚠ Multiple testing requirements; pre-bond and post-bond testing

▶ Tailored fault models and at-speed testing, e.g., ATPG considering TSV-induced thermo-mechanical stress

▶ Standard for testing architecture: IEEE P1838
  - Test access based on IEEE 1149.1
  - Die wrapper register like IEEE 1500
  - Internal debugging via IEEE P1687

Marinissen, E. J. "Status Update of IEEE Std P1838" Proc. Int. Workshop Testing 3D Stack. Integr. Circ., 2014
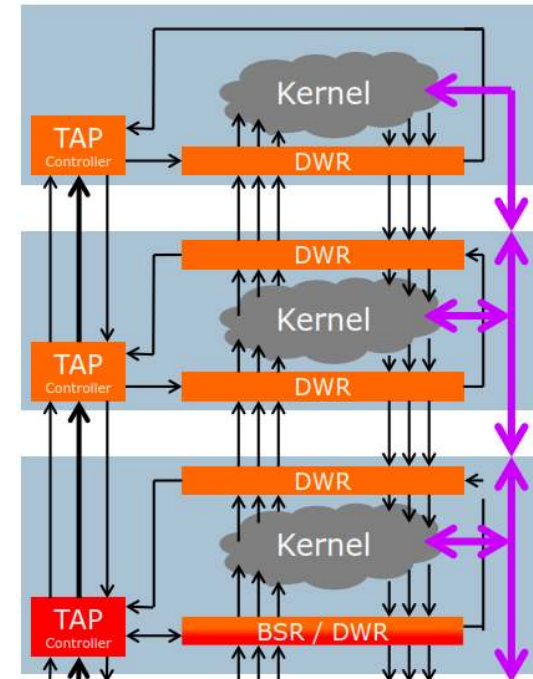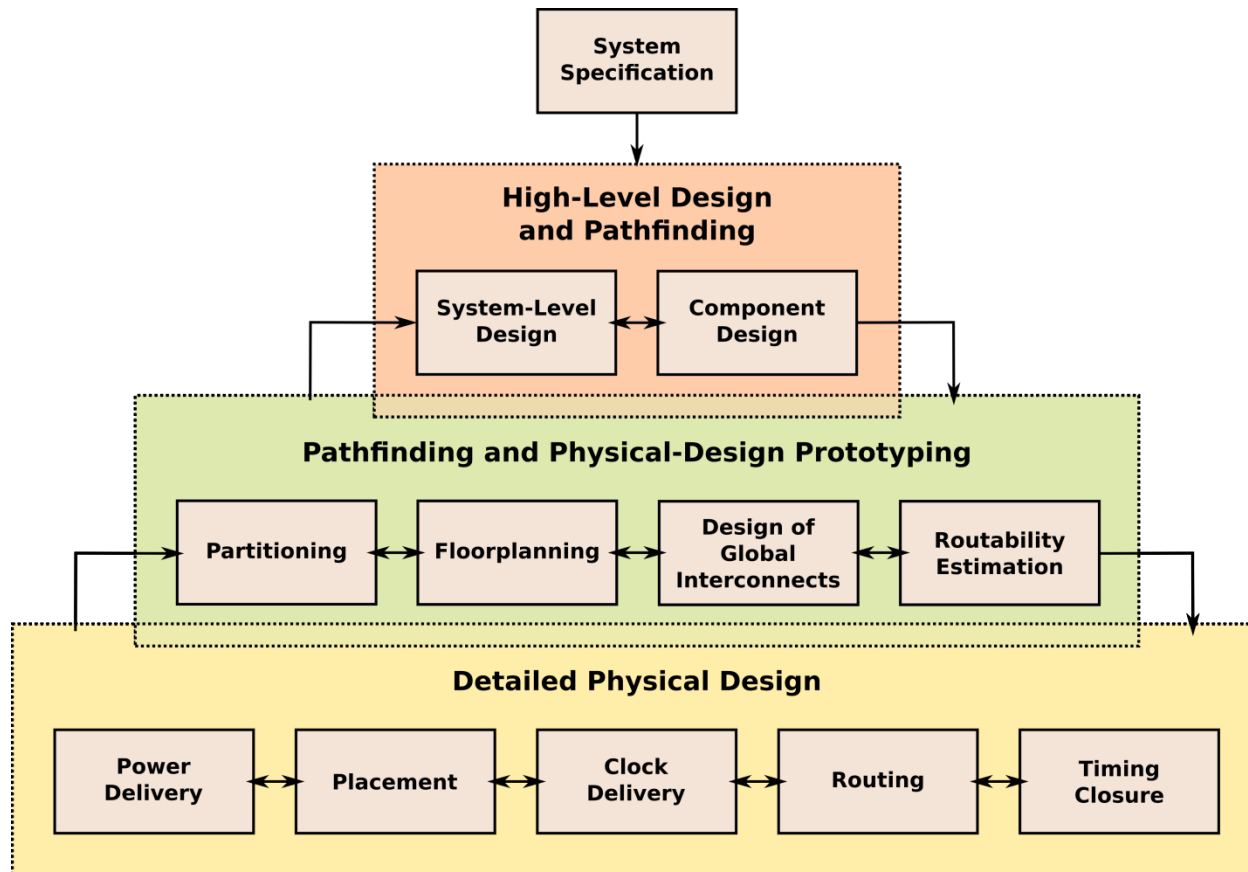
15

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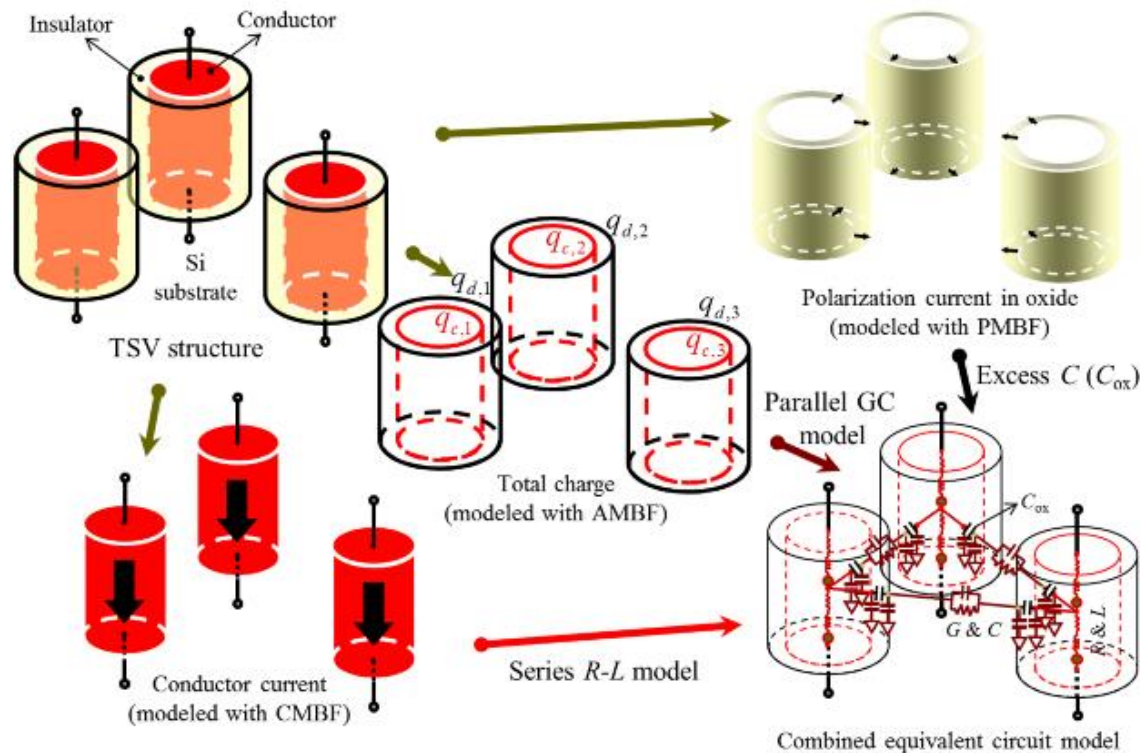
High-Level PD: Pathfinding and Chip-Package Co-Design

1. Derive components from high-level descriptions
2. Prototyping: generate and evaluate "coarse" layouts

17

High-Level PD: Pathfinding and Chip-Package Co-Design

1. Derive components from high-level descriptions
   – Abstracted, modular components, e.g., RTL modules
   – Parameterizable multi-port components for TSVs, bumps, etc.

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1. Derive components from high-level descriptions
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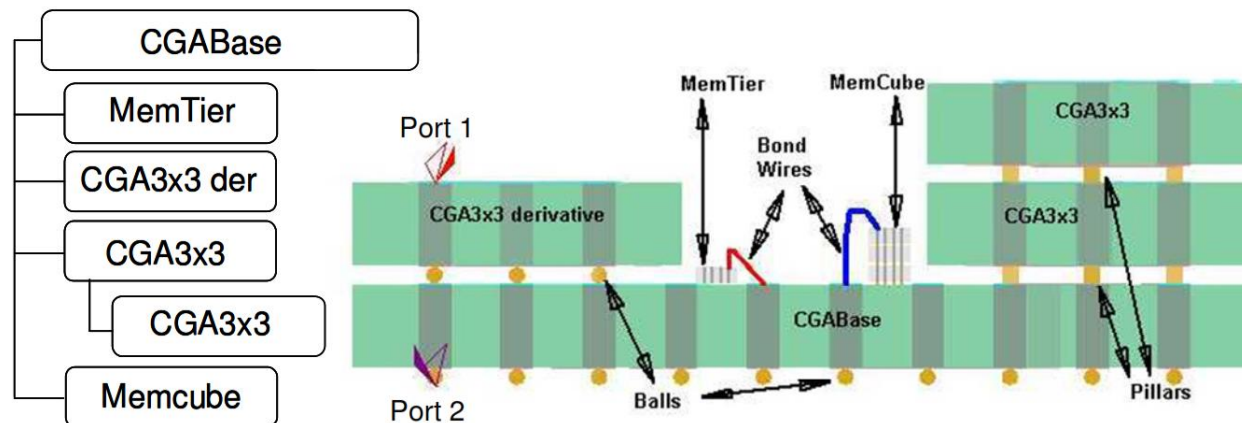   – Parameterizable multi-port components for TSVs, bumps, etc.

2. Prototyping: generate and evaluate "coarse" layouts
   – Explore different stacking and technology options
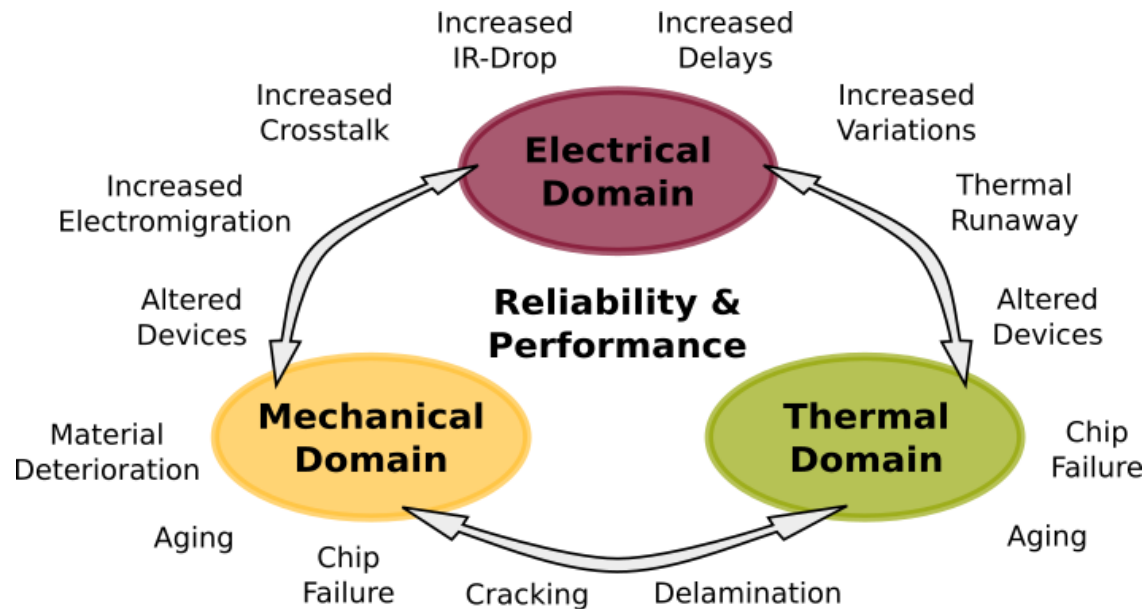   – Annotate stack and modules with simulation feedback; management of multi-physical effects

Martin, B.; Han, K. & Swaminathan, M. "A Path Finding Based SI Design Methodology for 3D Integration" Proc. Elec. Compon. Technol. Conf., 2014, 2124-2130

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19

Multi-Physics Simulation

⚠ Strong coupling of physical domains in 3D stacks

→ Scalable simulation techniques, linking across different design levels

Multi-Physics Simulation

⚠ Strong coupling of physical domains in 3D stacks

Schneider, P.; Reitz, S.; Wilde, A.; Elst, G. & Schwarz, P. "Towards a Methodology for Analysis of Interconnect Structures for 3D-Integration of Micro Systems" DTIP, 2007, 162-168

➡ Scalable simulation techniques, linking across different design levels
  ➡ From fine-grain to abstracted, high level simulation
  ➡ Model generation, network simulation, superposition etc

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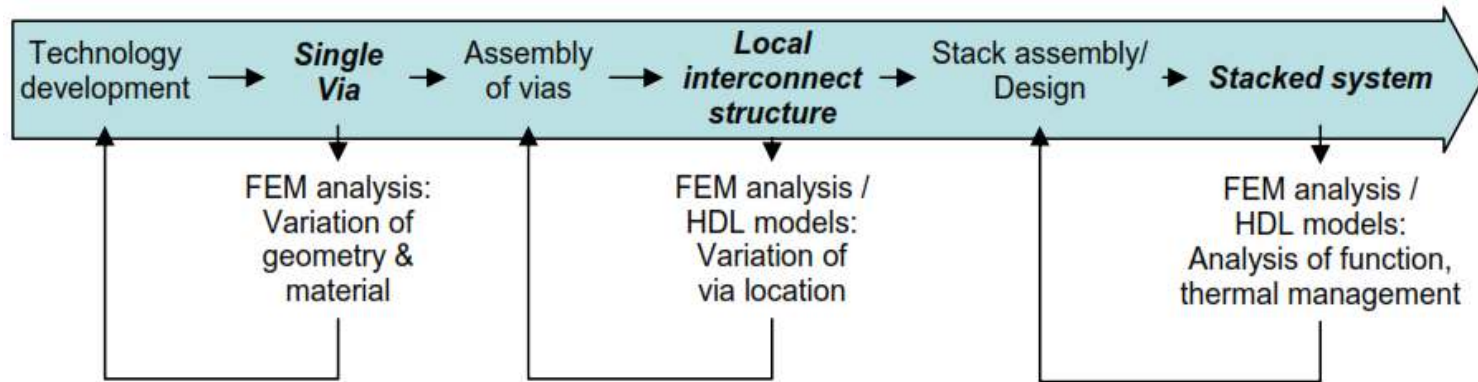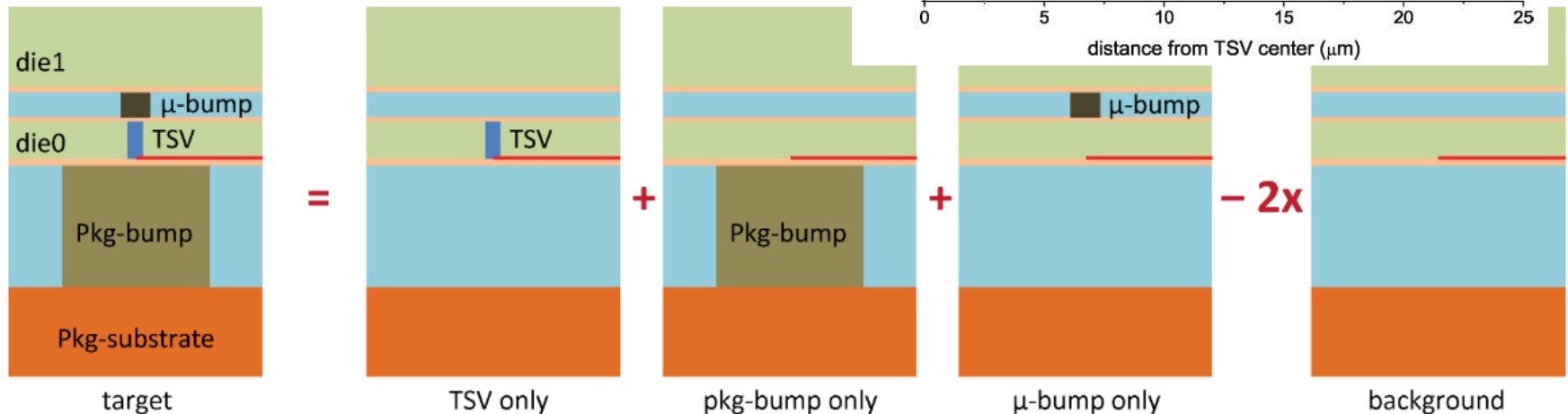
Multi-Physics Simulation

⚠ ## Strong coupling of physical domains

Jung, M.; Pan, D. Z. & Lim, S. K. "Chip/Package Mechanical Stress Impact on 3-D IC Reliability and Mobility Variations" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 1694-1707


➡ ## Scalable simulation techniques, linking across different design levels
   ➡ ### From fine-grain to abstracted, high level simulation
   ➡ ### Model generation, network simulation, superposition etc

Design Standards and File Formats

⚠️ Lack of standards and file formats for data exchange hinder commercial adoption

➡️ Multiple standards for memory integration; mass production of memory stacks
  – Wide I/O, High Bandwidth Memory (HBM), Hybrid Memory Cube (HMC)

➡️ Assembly design kit (ADK)
  – Exchange of design data, manufacturing steps, material properties etc.
  – Streamlining interaction of tools and verification for whole stack
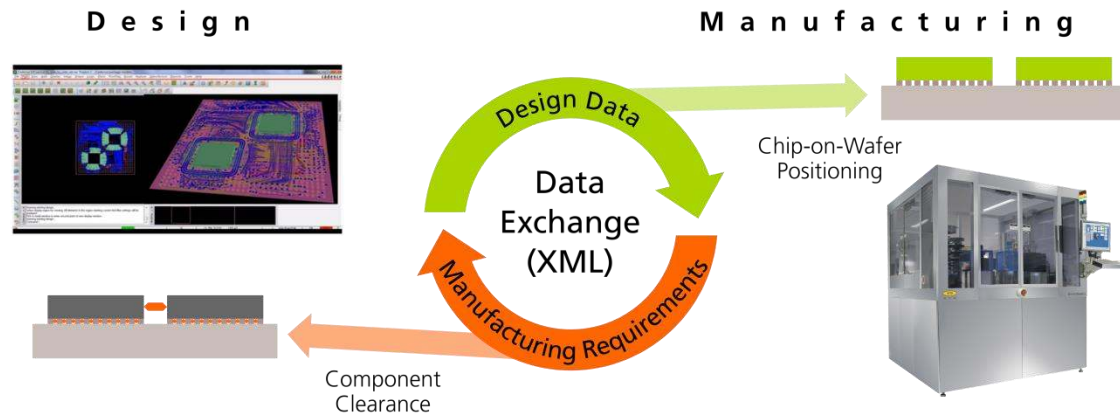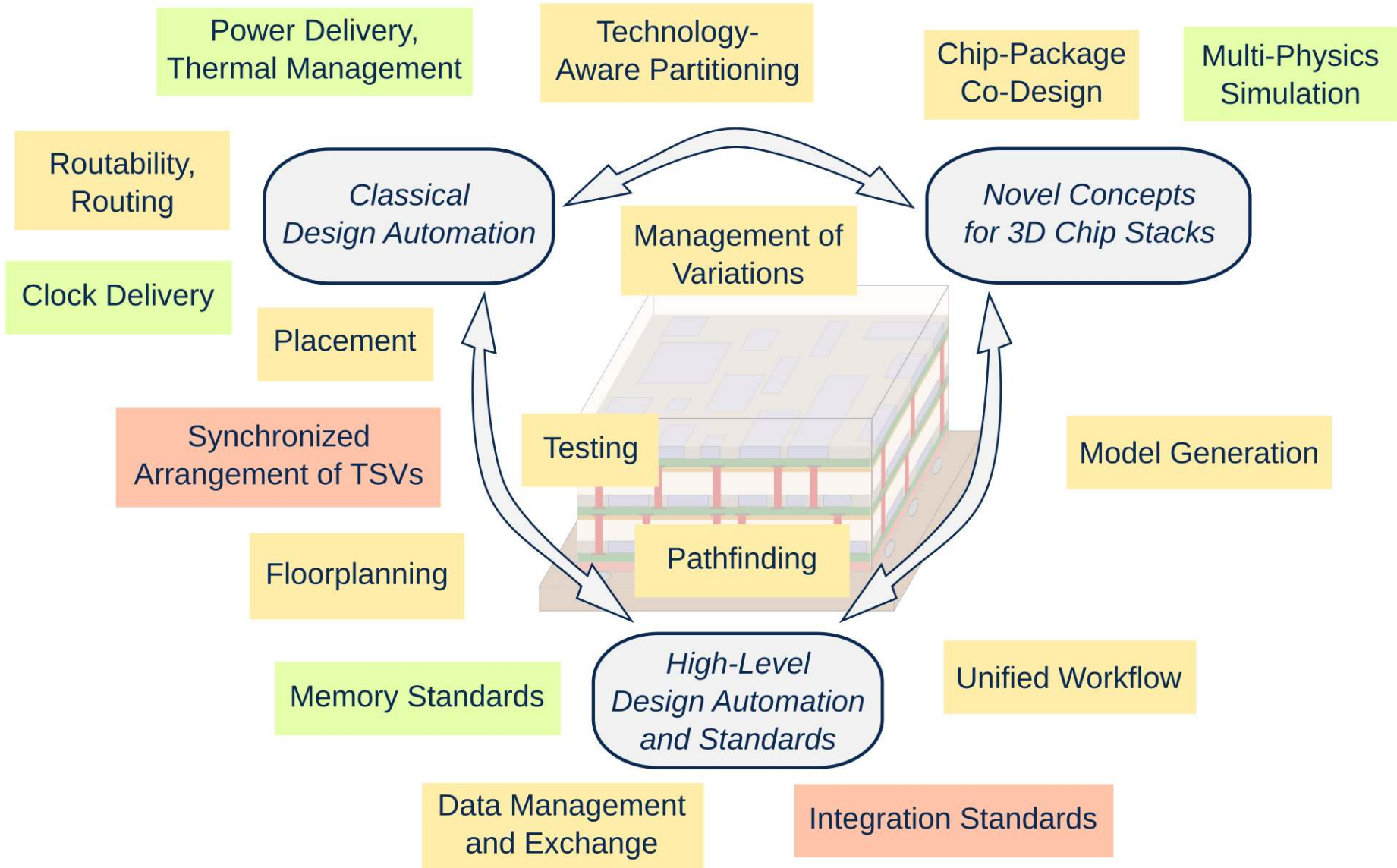

Heinig, A. & Fischbach, R. "Enabling automatic system design optimization through Assembly Design Kits" Proc. 3D Sys. Integr. Conf., 2015, TS8.31.1-TS8.31.5

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24

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➜ Comprehensive overview, more than 100 references

➜ http://dx.doi.org/10.1145/2872334.2872335