Physical Insights on Nanoscale FETs Based on Epitaxial Graphene on SiC

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***Abstract*— Epitaxial graphene on SiC substrate is a promising channel material for FETs because it can possibly overcome two main problems of graphene-based devices: the fabrication process is suitable for large-volume manufacturing, and the material exhibits an appreciable semiconducting gap of 0.26 eV. We present an analytical model of a nanoscale FET based on epitaxial graphene on SiC, and assess the achievable performance in the case of fully ballistic transport. Our model also allows us to conduct an exploration of the design parameter space. We observe that the main aspect undermining the performance of graphene FETs on SiC is the still limited energy gap, that has two main consequences: on the one hand it allows band-to-band tunneling at the drain side when the device is in the off state, therefore limiting the achievable $I_{\rm on}/I_{\rm off}$ ratio; on the other hand the injection of holes in the channel, when the device is biased in subthreshold, increases the channel quantum capacitance and can severely degrade the subthreshold slope. We show that an $I_{\rm on}/I_{\rm off}$ ratio of 60 and a subthreshold slope of 150 mV/decade are obtained for a ballistic device without lateral confinement and for a supply voltage of 0.25 V. We also show that performance can be largely improved if accumulation of holes in the channel is inhibited or suppressed (by allowing a limited degree of inelastic scattering) up to a very interesting $I_{\rm on}/I_{\rm off}$ ratio close to 10^4.**

I. Introduction

Graphene has attracted the attention of the scientific community since its isolation in 2004 [1], [2], due to its exceptional physical properties, such as an electron mobility exceeding more than 10 times that of silicon wafers [3], and in view of its possible applications in transistors [4] and in sensors [5].

However, as far as its possible use as a channel material in electron devices is concerned, graphene presents the problem of being a semi-metal, i.e. a zero-gap material. For this reason, several attempts have been made to open an energy gap in graphene. Lateral confinement is one possibility [4], [6] that allows to obtain very interesting device behavior [7], but has the drawback of requiring prohibitively narrow ribbons and single-atom precision. Bilayer graphene exhibits a gap in the presence of a perpendicular electric field, but the range of applicable bias is not sufficient to obtain a satisfactory behavior in terms of $I_{\rm on}/I_{\rm off}$ ratio [8], [9].

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Recently Zhou *et al.* [10] have experimentally demonstrated, through angle-resolved photo-emission spectroscopy measurements, that a graphene layer, epitaxially grown on a SiC substrate, exhibits a gap of about 0.26 eV. The gap is probably due to breaking of the symmetry between the two sublattices forming the graphene crystalline structure, as confirmed by recent density functional calculations [11], [12]. The fabrication method is also very interesting from the point of view of manufacturability. Such an energy gap would require an armchair nanoribbon with a width smaller than 3 nm, or nanotubes with diameter smaller than 2 nm.

Still, the energy gap is significantly lower than that of channel materials typically used in electron devices: the main problem resides in interband tunneling, which can severely limit the minimum achievable current when the device is in the off state.

In this work we present a semi-analytical model of a ballistic FET with a channel of epitaxial graphene grown on a SiC substrate, where the band structure, the electrostatics, thermionic and tunneling currents are carefully accounted for. On the basis of our model, we assess the achievable device performance through an exploration of the device parameter space, and gain understanding of the main aspects affecting device operation.

II. Model

A. Band Structure

We adopt the Tight Binding Hamiltonian for single layer graphene on SiC that was proposed by Zhou *et al.* [10]:

$$H = \begin{pmatrix} m & tf(\mathbf{k}) \\ tf^*(\mathbf{k}) & m \end{pmatrix} \tag{1}$$

where t is the in-plane hopping term, equal to 2.7 eV, $m = 0.13$ eV is an empirical parameter introduced to reproduce the energy band gap and $f(\mathbf{k})$ is

$$f(\mathbf{k}) = 1 + e^{-ik_y\frac{\sqrt{3}a}{2}}\left[e^{-ik_x\frac{3a}{2}} + e^{-ik_y\frac{\sqrt{3}a}{2}}\right], \tag{2}$$

with $a = 0.144$ nm the carbon-carbon distance. The valence and conduction bands, calculated from the diagonalization of the TB Hamiltonian, read:

$$E_{\pm}(k_x, k_y) = \pm\sqrt{m^2 + t^2|f(\mathbf{k})|^2}. \tag{3}$$

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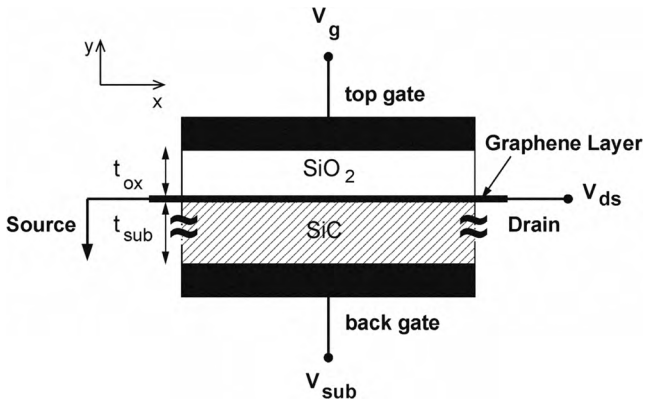

Fig. 1. Schematic cross section of a graphene on SiC transistor. The black line between SiO_2 and SiC oxide represents the graphene plane acting as device channel.

Now, in the six Dirac points of the graphene Brillouin zone, where $f(\mathbf{k})$ is zero, $E_{\pm} = \pm m$ and therefore a finite energy gap $E_g = 2m$ is obtained.

B. Vertical Electrostatics

The device under consideration, depicted in Fig. 1, is a transistor with a channel of epitaxial graphene on a SiC substrate of thickness $t_{sub} = 100$ nm, with a top gate separated by a SiO_2 layer of thickness t_{ox}. In Fig. 2 we have sketched the band edge profiles along the transport direction $\hat{x}$, where E_{Ci} and E_{Vi} represent the conduction and valence band edges, respectively, in the three different regions denoted by i=S, D, C (Source, Drain, Channel). Source and drain contacts are n^+ doped, with molar fraction α_D, which translates into an energy difference A between the electrochemical potential μ_S (μ_D) and the conduction band edge E_{CS} (E_{CD}) at the source (drain) contact. Let us note that

$$E_{CC} = E_g/2 - q\phi_{ch} \quad ; \quad E_{VC} = -E_g/2 - q\phi_{ch}, \tag{4}$$

where q is the absolute electron charge and ϕ_{ch} is the self-consistent potential in the central region of the channel. The potential is fixed to zero at the source and to V_{ds} at the drain contact, while it is imposed by the vertical electrostatics in the center of the channel. From evanescent mode analysis [13], we obtain an exponential expression for the potential profile connecting each contact to the central region of the channel, defined by the characteristic length λ, that — assuming $t_{sub} \gg t_{ox} \gg t_{ch}$ — reads:

$$\lambda \approx \left(t_{ox} + \frac{t_{ch}}{2}\right)\frac{2}{\pi}, \tag{5}$$

where t_{ch} is the effective separation between the interfaces of the SiO_2 and SiC layers, for which assume $t_{ch} = 1$ nm [4]. Exploiting the Gauss theorem we can write the surface charge density in the central part of the channel as a function of ϕ_{ch}

$$Q = -C_g\left(V_g - V_{FBt} - \phi_{ch}\right) - C_{sub}\left(V_{sub} - V_{FBb} - \phi_{ch}\right), \tag{6}$$

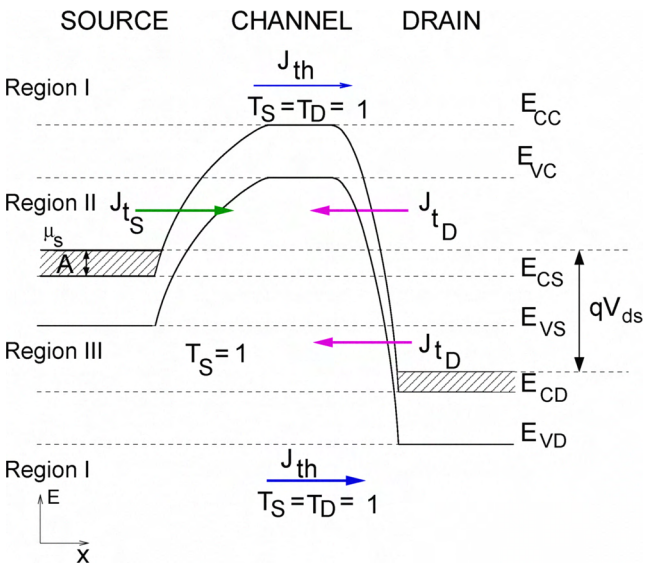

Fig. 2. Profile band structure along the transport direction. The dashed lines separate the energy region in which it is possible to have thermionic current (J_{th}), tunneling current from source to channel (J_{tD}) and tunneling current from drain to channel (J_{tS}).

where $C_g = \epsilon_{SiO_2}/t_{ox}$ ($C_{sub} = \epsilon_{SiC}/t_{sub}$) is the capacitance per unit area between the channel and the top gate (back gate), V_g (V_{sub}) is the top gate (back gate) voltage, V_{FBt} (V_{FBb}) is the flat-band voltage of the top gate (back gate), which we set to -0.4 eV. We consider ballistic transport with complete phase randomization along the channel. The assumption of phase randomization is particularly important in the evaluation of the density of states in the channel valence band, because it allows us to neglect the effect of resonances.

As an example, for the bias considered in Fig. 2, we can distinguish three transport regions:

- *Region I—Thermionic transport*: $E > E_{CC}$ or $E < E_{VD}$. The occupation factor in the channel is the half sum of the two Fermi-Dirac distributions for S and D.
- *Region II—S and D interband tunneling*: $E_{CS} < E < E_{VC}$. The occupation factor in the channel at energy E is obtained from the balance of source and drain tunneling currents (J_{tS} and J_{tD} in Fig. 2).
- *Region III—D interband tunneling*: $E_{CD} < E < E_{VS}$. The occupation factor in the channel is obtained from the balance of source injection and drain tunneling.

An analogous analysis can be done for different bias conditions. The charge per unit area in the channel can be expressed as [14]

$$\begin{aligned} Q \;=\; & \frac{q}{4\pi^2}\Bigg\{ -\int_{BZ}\frac{1}{T^*}\left[T_S\left(2-T_D\right)f(x_S^e) + \right. \\ & \left. T_D\left(2-T_S\right)f(x_D^e)\right]dk_x dk_y + \\ & \int_{BZ}\frac{1}{T^*}\left[T_S\left(2-T_D\right)f(x_S^h) + \right. \end{aligned}$$

$$T_D\,(2 - T_S)\,f(x_D^h)]\,dk_x dk_y \Bigg\}, \quad (7)$$

where $x_S^e \equiv (E_+ - q\phi_{ch} - \mu_S)/kT$, $x_D^e \equiv (E_+ - q\phi_{ch} - \mu_D)/kT$, $x_S^h = (\mu_S - E_- + q\phi_{ch})/kT$, $x_D^e = (\mu_D - E_- + q\phi_{ch})/kT$ and $T^* = T_S + T_D - T_S T_D$. T_S (T_D) is the transmission probability of the interband barrier at source (drain). T_S is zero in the source band gap and 1 when there is no barrier between source and channel, when a barrier is present T_S is computed within the WKB approximation, assuming k_y conservation due translational invariance along the y direction:

$$T_S(E, k_y) = \exp\left\{-2\int_{x_1}^{x_2} |\Im(k_x^{E,k_y}(x))|dx\right\}, \quad (8)$$

where x_1 and x_2 are the classical turning points and

$$\Im\left[k_x^{E,k_y}(x)\right] = -\frac{2}{3a}\ln(\Delta + \sqrt{\Delta^2 - 1}), \quad (9)$$

with

$$\Delta = \frac{(E - E_c(x, k_y))^2 - m^2 - t^2 - 4B^2t^2}{4Bt^2}. \quad (10)$$

Here $E_c(x, k_y)$ represents the profile of the conduction band edge between channel and the source contact for a fixed k_y, and $B = \cos\frac{\sqrt{3}ak_y}{2}$. The same approach is repeated for T_D.

C. Current

The total current density can be expressed as [14]

$$J_{tot} = \frac{q}{4\pi^2}\left\{\int\int \frac{T_S T_D}{T^*} v_x\left[f(x_S^e) - f(x_D^e)\right]dk_x dk_y + \int\int \frac{T_S T_D}{T^*} v_x\left[f(x_S^h) - f(x_D^h)\right]dk_x dk_y\right\} \quad (11)$$

where v_x is the group velocity obtained from the energy dispersion relation.

III. Results

In order to evaluate the possible performance of the SiC-graphene FET, we compute the transfer characteristics by varying three device parameters: donor molar fraction at the contacts α_D (and therefore parameter A), oxide thickness t_{ox} and drain-source voltage $V_{ds} = (\mu_S - \mu_D)/q$.

First, let us consider Fig. 3, where the transfer characteristics are plotted for $V_{ds} = 0.1$ V and $V_{ds} = 0.25$ V, for different doping levels of the contacts. Increasing the doping causes an increase of both the maximum current, due to an improved capacity of the source to inject electrons, and the minimum current, because a lower gate voltage is needed to shut off the thermionic current, which is associated to a larger electric field at the drain and therefore to larger interband tunneling. From Fig. 3 we draw the indication that by reducing doping at the contacts we improve the current dynamics.

Let us note that, when the source-drain voltage exceeds the gap of the semiconducting channel ($V_{ds} > 0.3$ V), the characteristics drastically degrade, since the tunneling current becomes comparable with the thermionic current, and hole accumulation in the channel inhibits channel control from the gate. This effect is made more severe by our assumption of ballistic transport and of no carrier recombination.

In Fig. 4 we highlight the effect of V_{ds} on the subthreshold slope: in Fig. 4(a) we plot the device transfer characteristics for different V_{ds}, while keeping a donor molar fraction of $\alpha_D = 6.5 \times 10^{-4}$, corresponding to $A = 0.01$ eV. The main visible effect of an increase of V_{ds} is a gradual decrease of the subthreshold slope from 72 mV/dec to 202 mV/dec. The reason is simply related to the increased injection and accumulation of holes in the channel with increasing V_{ds}, which implies an increased quantum capacitance of the channel and therefore a reduced control of the channel potential from the gate voltage.

The increase of oxide thickness t_{ox} has mainly two effects, which can be associated to a reduction of the capacitive coupling between gate and channel: it increases the subthreshold slope S (as shown in Fig. 4(b)), and the opacity of tunneling barriers (i.e. a larger λ). The former effect is more evident for $V_{ds} = 0.25$ V, where the quantum capacitance is larger, instead S is almost constant at about 75 mV/dec for $V_{ds} = 0.1$ V.

Fig. 5 represents the $I_{\rm on}/I_{\rm off}$ ratio as a function of t_{ox} for $V_{ds} = 0.1$ V and $V_{ds} = 0.25$ V, calculated for two different gate voltage ranges $\Delta V_g = 0.25$ V and $\Delta V_g = 0.5$ V. From the point of view of a digital circuit operation, we conclude that the optimal parameters are an oxide thickness $t_{ox} = 1$ nm and an α_D lower than 4×10^{-3}. Indeed, choosing $V_{ds} = \Delta V_g = 0.25$ V, we obtain an $I_{\rm on}/I_{\rm off} = 60$, as can be deduced from Fig. 5(b). The result is not sufficient for digital integrated circuits, but is one order of magnitude larger than that obtained with other means except lateral quantum confinement.

In addition, a promising possibility comes from the observation that a larger current ratio (in excess of 10^4) can be obtained for $\Delta V_g = 0.5$ V and $V_{ds} = 0.1$ V (Fig. 5(b)). The advantage of low V_{ds} is the fact that accumulation of holes is suppressed, so that we can obtain a steep subthreshold slope. This means that if a way can be found to suppress accumulation of holes, also at larger V_{ds}, the performance can be significantly improved.

For example, non-idealities can be of help: a degree of inelastic scattering and electron-hole recombination in the channel can somewhat reduce the maximum current, and at the same time strongly suppress accumulation of holes in the channel. This aspect needs to be further investigated, also from the experimental point of view.

IV. Conclusion

In this work we have investigated the performance of a ballistic transistor based on epitaxial graphene on a SiC substrate with an analytical model. We have shown that a sub-threshold slope of ≈ 150 mV/decade and an $I_{\rm on}/I_{\rm off}$ ratio of about 60 can be obtained, with a supply voltage of 0.25 V. The limiting factor for this kind of device is represented by the small voltage drop applicable to the fully ballistic transistor, being limited by the energy gap (0.26 eV) of semiconducting material. A steeper subthreshold behavior ($S = 72$ mV/decade) can be obtained

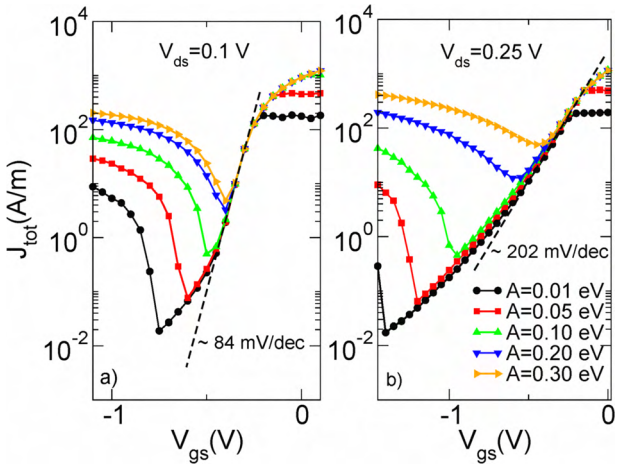

Fig. 3. Transfer characteristics for $V_{ds} = 0.1$ V (a) and $V_{ds} = 0.25$ V (b), with doping parameter $A = 0.01, 0.05, 0.1, 0.2, 0.3$ eV corresponding respectively to α_D of 6.5×10^{-4}, 4×10^{-3}, 9.3×10^{-3}, 2.3×10^{-2}, 4.3×10^{-2}, $t_{ox} = 2$ nm.

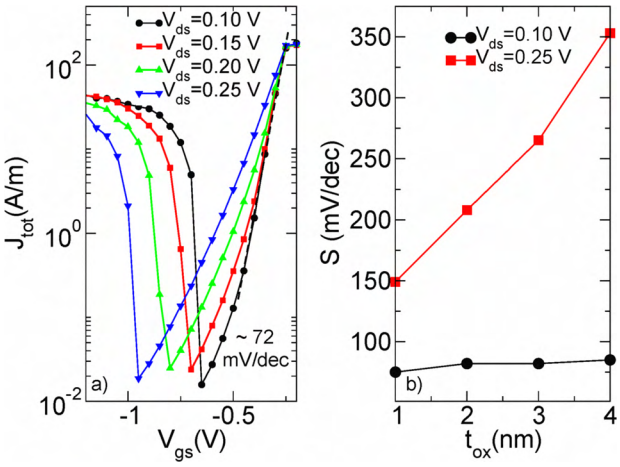

Fig. 4. (a) Transfer characteristics for different V_{ds}, $A = 0.01$ eV corresponding to α_D of $= 6.5 \times 10^{-4}$, $t_{ox} = 1$ nm. (b) Sub-threshold slope for $V_{ds} = 0.1, 0.25$ V.

for smaller $V_{ds} = 0.1$ V, when the accumulation of holes is inhibited, and a larger current ratio in excess of 10^4 can be obtained for a gate voltage window of 0.5 V. In conclusion we believe that graphene on SiC is worth of further investigation as a channel material for FETs, focusing especially on the mechanisms capable to suppress hole injection also at larger V_{ds}. Already now it seems is one of the few promising possibilities to obtain a significant $I_{\rm on}/I_{\rm off}$ ratio without resorting to prohibitive lithography.

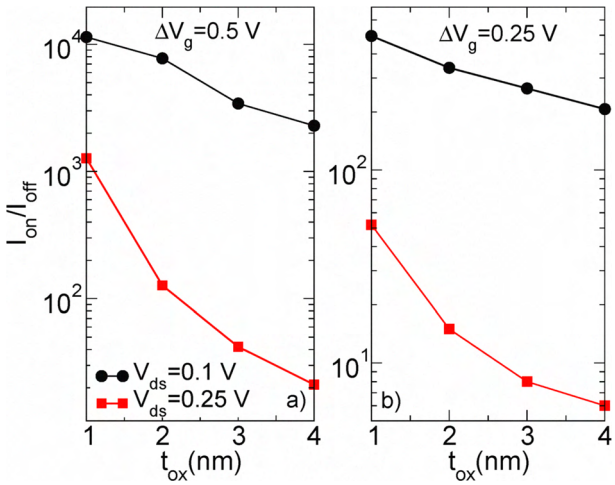

Fig. 5. $I_{\rm on}/I_{\rm off}$ ratio calculated calculated for two different gate voltage ranges ΔV_g: (a)$\Delta V_g = 0.5$ V and (b)$\Delta V_g = 0.25$ V.

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