PHYSICAL PACKAGING AND ORGANIZATION OF THE DRIFT CHAMBER ELECTRONICS SYSTEM FOR THE STANFORD LARGE DETECTOR*

G. M. Haller, M. L. Freytag, G. Mazaheri, J. Olsen, and L. Paffrath

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94309

Abstract

In this paper the logical organization, physical packaging, and operation of the drift chamber electronics for the SLD at SLAC is described. The system processes signals from approximately 7,000 drift wires and is unusual in that most electronic functions are packaged on printed circuit boards within the detector. The circuits reside on signal-processing motherboards, controller boards, signal-transition boards, power-distribution boards, and fiber-optics-to-electrical conversion boards. The interaction and interconnection of these boards with respect to signal and control flow are presented.

I. INTRODUCTION

The SLD [1–5] is a high-energy physics detector built to study fundamental particles and forces at the e^+e^- Stanford Linear Collider. The detector is optimized to measure positions, momenta, energies, and types of particles at energies near the rest energy of the Z^0 particle. The vertical section of a quadrant of the SLD is shown in fig. 1. Figure 2 is an isometric view of the detector showing the locations of the Central and Endcap Drift Chambers which form one of the major subsystems of the SLD [1]. The Central Drift Chamber (CDC) measures particle coordinates by drift time and charge division, and dE/dx for particle identification. This is accomplished by recording the waveforms of the current pulses induced on the sense wires of the chamber with subsequent extraction of time and amplitude information. The CDC consists of 5,120 sense wires that are grouped in eight-wire vector cells [1,2]. A total of 640 vector cells are arranged in ten superlayers surrounding the interaction point. The four Endcap Drift Chambers (EDC) comprise approximately 500 drift wires each and extend the tracking coverage of the SLD to 97% of 4π.

Performance and space requirements led to a novel design for the SLD drift chamber electronics system. Most of the electronic components are packaged within the SLD magnet volume, as opposed to external electronics support racks, in order to minimize noise pick-up, capacitive loading of the signals, and cable plant volume. Figure 2 shows the location of the electronic boards on both end faces of the CDC and on the circumference of the endcap chambers. The signals from the sense wires are processed on motherboards [6,7] each comprising up to

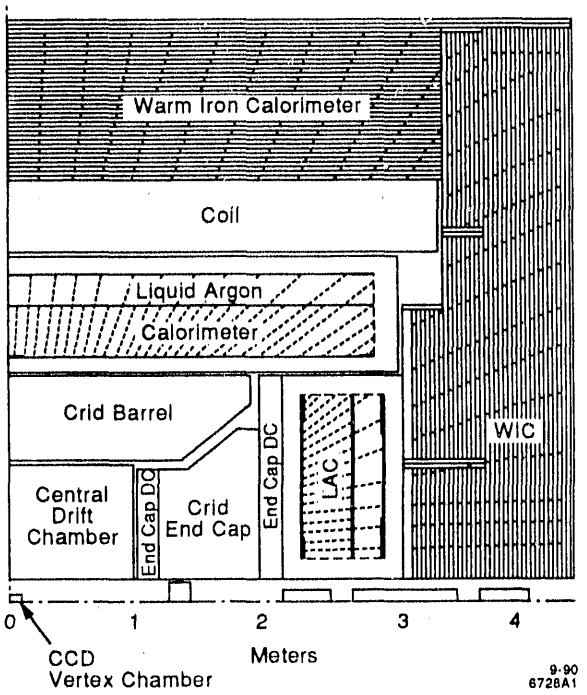

Fig. 1 Vertical section of one quadrant of the SLD. The beam axis is along the bottom. The beams collide at the interaction point located in the lower left corner.

64 channels of transimpedance amplification, 119 MHz analog sampling, and analog-to-digital conversion. Each end of the CDC contains 85 curved motherboards with approximately 43 cm × 7 cm surface area, arranged on 10 different radii or super-layers, as illustrated in fig. 3. The boards carry jacks which engage pins connected to the sense wires. Four boards with the greatest curvature cover the inner-most radius (layer 0). The outer-most radius (layer 9) contains 13 boards with the smallest curvature. Motherboards are mounted on both ends of the CDC sense wires in order to determine the position of the hit along the wire through charge division. The 85 boards on the other side of the CDC are identical except for a mirror-image readout order, which is accomplished by a modification in the programmable device on the motherboard [6]. This insures correlated readout of the data on both ends of the wire, as required by the external FASTBUS data processing system.

The motherboards for the endcap drift chamber systems are rectangular [6] and fabricated out of rigid-flex material, so that they can be bent around the chamber as shown in fig. 2.

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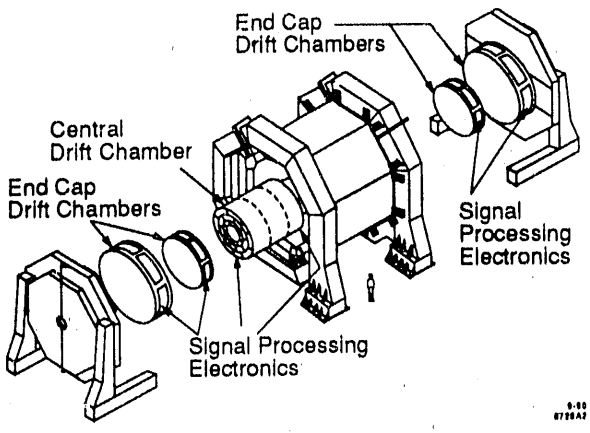

Fig. 2 Isometric view of the detector with the drift chamber barrel and endcaps. The barrel electronics are mounted on both ends of the central chamber. The endcap electronics are mounted around the circumference of the 4 endcap chambers. The dimensions of the chambers are shown in fig. 1.

II. Control Flow

Figure 4 illustrates the control flow from the FASTBUS racks to the motherboards. System timing and control is governed by a FASTBUS Timing and Control Module (TCM) [8]. This master timing source is used throughout the SLD detector and provides a means to synchronize detector elements to the SLD master clock. The CDC and EDC systems are controlled from a single TCM module. This module uses a three-signal serial protocol to transmit commands, data, and timing information to the controller logic resident in the detector. A 119 MHz sampling clock used by the front-end electronics is sent into the chamber on separate fibers. The SLD protocol provides a general purpose structure for all functions of the system, i.e., calibration, acquisition of analog information, digitization and transmission of information from the drift sense wires.

The difficulties of access to the drift signal processing electronics strongly influenced the architecture of the system. As most of the electronic components are physically inside the magnet and shielding structure of the detector, access for maintenance requires several days of downtime. The resulting need for reliability suggested a design approach which attempts redundancy in critical components and eliminates single point failures which could disable major portions of the detector. This redundancy begins with two independent fiber optic control paths that distribute the three TCM control and timing signals and the 119 MHz clock into the detector.

Since the organization of the CDC and EDC electronics is very similar, only the CDC control and data path is discussed here in detail. The optical signals from the TCM are converted to differential ECL levels for distribution inside the chamber. This is accomplished on a 19 cm × 13 cm Fiberoptics/ECL conversion board, containing optical receivers (HFBR2416), fast comparators

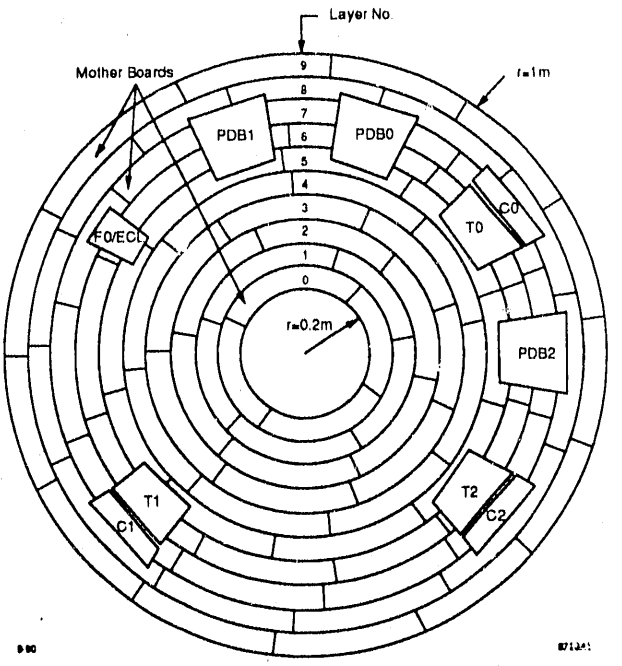

Fig. 3 View of one end of the central drift chamber. The curved motherboards are arranged in 10 radii or super layers. The boards are plugged onto pins connected to the sense wires, which go into the drawing plane. The auxiliary boards are mounted above the motherboards. (C=Controller, T=Transition, FO/ECL=Fiberoptics/ECL conversion, PDB=Power Distribution Board).

(AD96687), and ECL line drivers. The ECL signals are fanned-out and routed on shielded ribbon and TWINAX (for 119 MHz sampling clock) cables to three sets of controller and transition boards. The controllers generate analog and digital signals from the incoming protocol, which are then distributed via the transition boards to the three groups of motherboards (25 or 30 each) as illustrated in fig. 4.

A block diagram of the controller board is shown in fig. 5. The ECL signals from the conversion board are translated to TTL levels and routed to five 35 MHz programmable EPLD surface-mount devices (ALTERA EPM5128), each comprising more than 6,000 equivalent gates. The subdivision of the electronics into five sets was chosen in order to reduce the impact of a single-component failure. Each EPLD state machine controls three serial input 12-bit digital-to-analog converters, which provide analog bias, calibration, and hit-threshold voltages to the motherboards [6]. The digital circuitry on the controller supplies two fast digital strobes, required by the motherboards in calibration and leakage current mode [6].

During run time the motherboards are power-pulsed to reduce power consumption in the detector [6]. The power-on of a motherboard can be disabled by an inhibit line connected to each board. The pattern of boards to

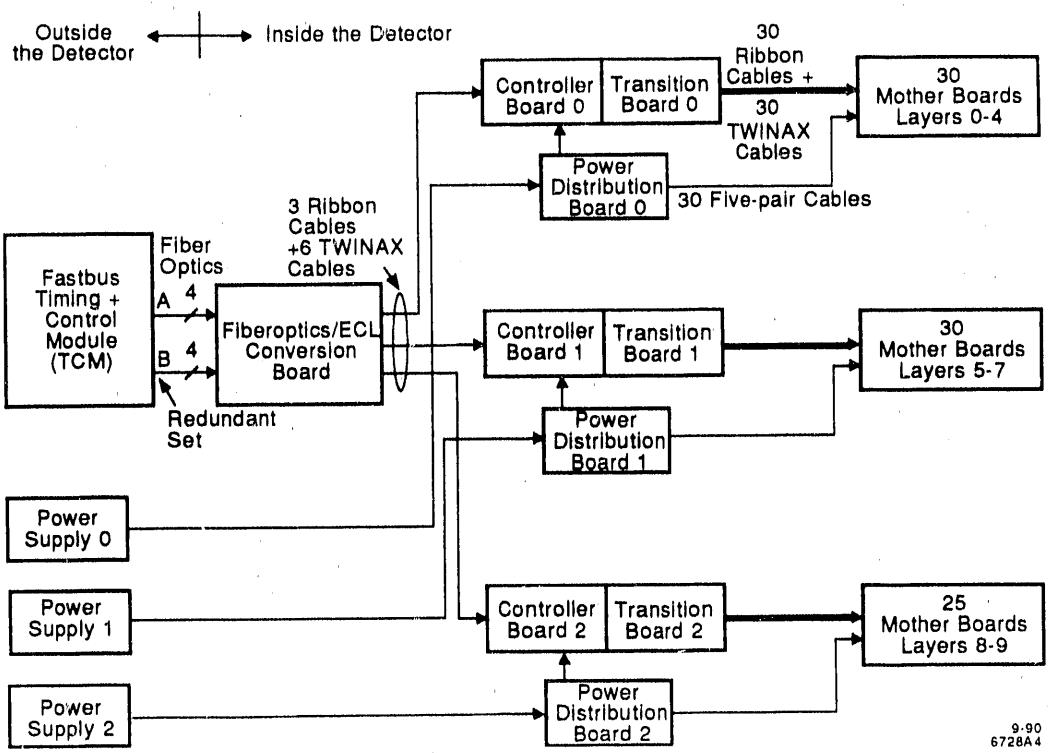

Fig. 4 Control and power flow of the central drift chamber electronics for one end of the chamber.

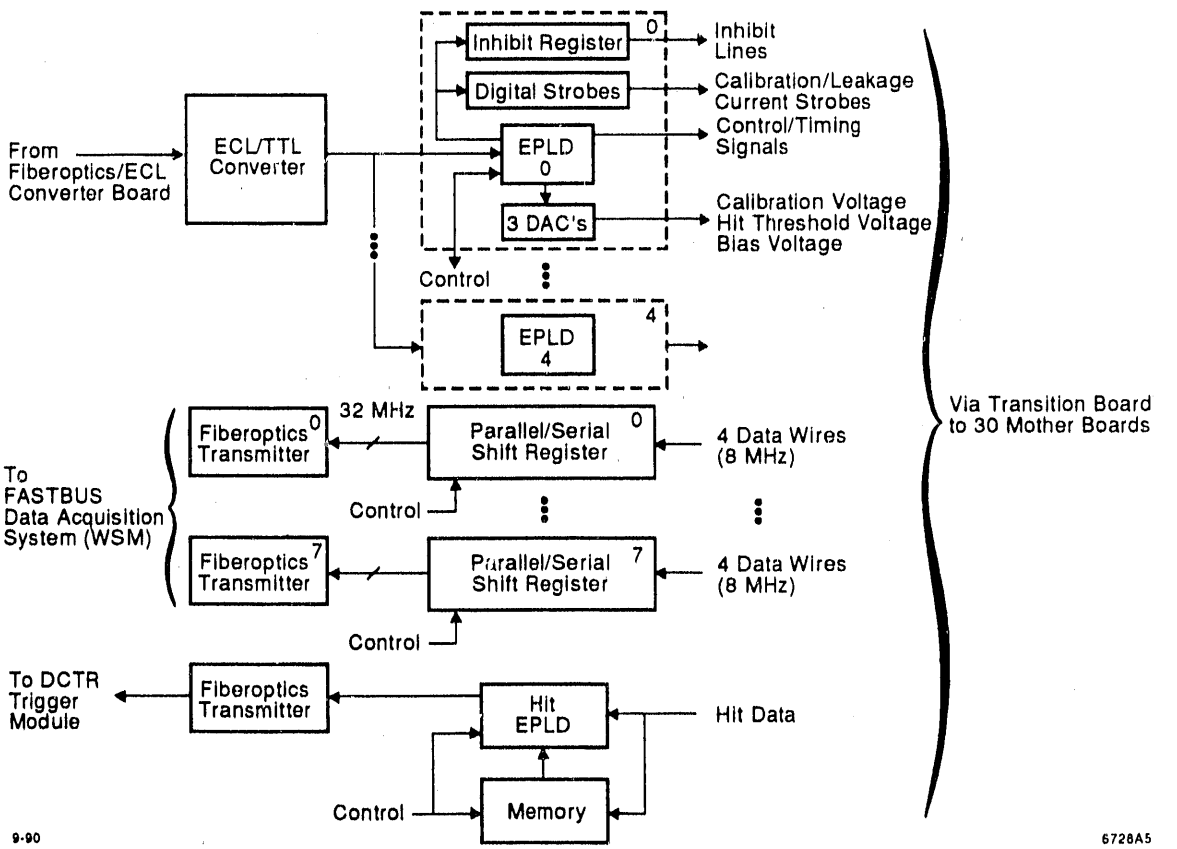

Fig. 5 Block diagram of the central drift chamber controller board.

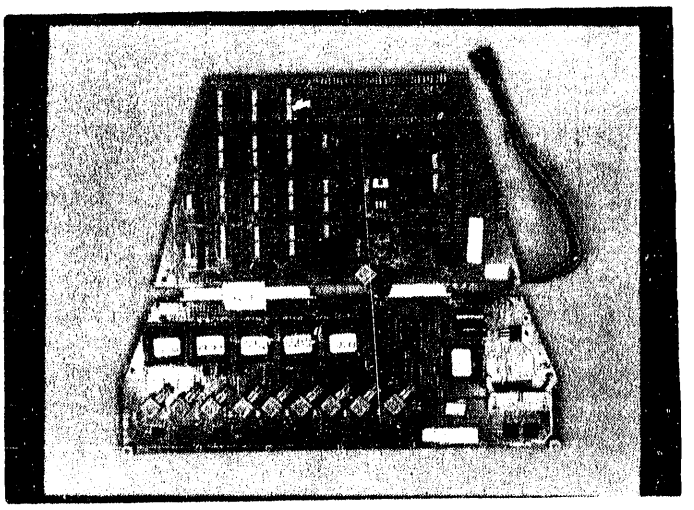

Fig. 6 Picture of the top side of the controller and transition boards. The boards are plugged together by a 96-pin and a 48-pin connector. Both boards also have surface-mount components mounted on the back-side.

be enabled during run-time is set by the EPLD and a serial bit-stream from the TCM, which is loaded into inhibit shift registers. Failing boards can therefore be turned off individually, while a time-out circuit on the controller interrupts continuous power to all boards in case of a failure of the FASTBUS control system.

The signals produced on the controller and the incoming TCM control signals are sent to the transition board (fig. 4). This board plugs into the controller board and buffers and distributes the signals to the motherboards. The three-wire protocol, the inhibit line, the analog voltages, and the two digital strobes are sent to the motherboards on shielded ribbon cables, which plug in 20-pin connectors on the transition board. The board also includes ECL circuitry to receive and distribute the incoming 119 MHz sampling clock to the motherboards. Figure 6 shows a picture of the two-sided controller (29 cm × 11 cm) and transition (26 cm × 15 cm) boards. The controller board holds the majority of active components and is easily disconnected from the transition board in case of a component failure.

III. Signal Flow

Figure 7 shows the data flow from the sense wires of the drift chamber to the FASTBUS WSM data processing modules [9,10]. The current signals collected on the sense wires are amplified and stored in analog form on the 64-channel motherboards. New data are stored in memory (discarding the old) at the beam-crossing rate of 120 Hz until a SLD read-out trigger decision (2 Hz average rate) occurs. The data is then digitized, serialized, and sent to the controller board via the ribbon-cable and the transition board at a rate of 8 MHz. On the controller, data from 30 motherboards is interleaved in sets of four (at 32 MHz), converted and optically transmitted to the outside of the detector by means of HFBR1414 optical drivers as shown in fig. 5. The data from 5,120 wires of the CDC is sent out of the SLD on 23 fifteen-meter long fibers on each end. The transmission requires 65 msec.

In the fastbus racks the data is processed in the WSM modules, where the data from the two ends of the CDC are corrected and correlated. Parameters for the correction are acquired in calibration runs taken several times a day. The corrected data is passed via the FASTBUS system to an AEB (ALEPH Event Builder) module [11] for first level online data processing.

The drift chamber data is also utilized in the readout trigger decision of the SLD. After each beam-crossing a serial bit-stream is generated by hit-circuitry [6] on the motherboard, in which a set bit indicates a wire on which the signal exceeded a pre-set threshold voltage. The hit pattern of all motherboards is sent in parallel to the transition/controller boards, where the data is temporarily stored and serialized by an EPLD (fig. 5). The information is then optically transmitted to a FASTBUS Drift Chamber Trigger Module (DCTR) outside of the detector. The hit data from up to 30 motherboards (1,920 channels) is transmitted on one fiber (fig. 7) at a rate of 8 MHz.

IV. Low Voltage Distribution

The low voltage for the drift chamber is supplied by power supply chassis located in racks on the detector. Each chassis serves one chamber power distribution board (fig. 4) and contains six switching power supplies and monitoring circuitry for current and voltage levels. Twenty meters of 24 twisted pairs of 16-gauge cable connect the supplies to the power distribution boards inside the SLD. The five voltages required by the motherboards are fanned out and protected by polymer fuses, which can be reset by turning the power off and on. Each of the three 30 cm × 26 cm power distribution boards on each chamber end serves up to 30 motherboards and holds up to 185 fuses. The power for the controller and transition boards is also fused on the distribution board.

The circuit density in the detector has required careful attention to thermal design and cooling. To reduce power consumption and heat most of the electronics is power pulsed with a duty factor of less than 5%. The RMS consumption of a motherboard is 3W in the write mode and 1W in the read mode [6]. This yields a maximum of 250W for each end of the chamber. The electrical energy is stored locally on the motherboards, which also reduces the required current capacity of the power supplies and cables. The fuses on the distribution board are sized to shut off the power to a board running in a continuous (failure) mode.

The heat generated by the electronics is removed by convection to the water-cooled drift chamber end plate. A micro-processor located on the transition board monitors temperature transducers on the motherboards and optically transmits the digitized thermal data of 32 motherboards on one fiber to a CAMAC module outside the

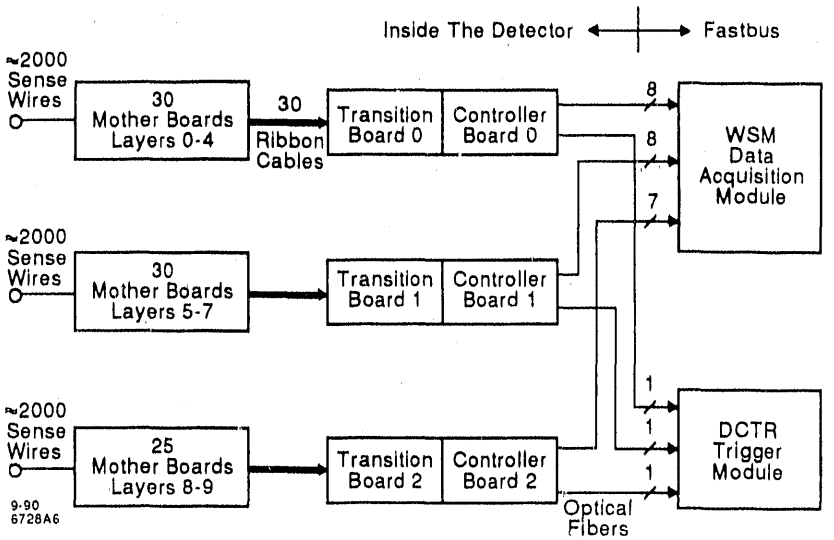

Fig. 7 Data flow of the central drift chamber electronics.

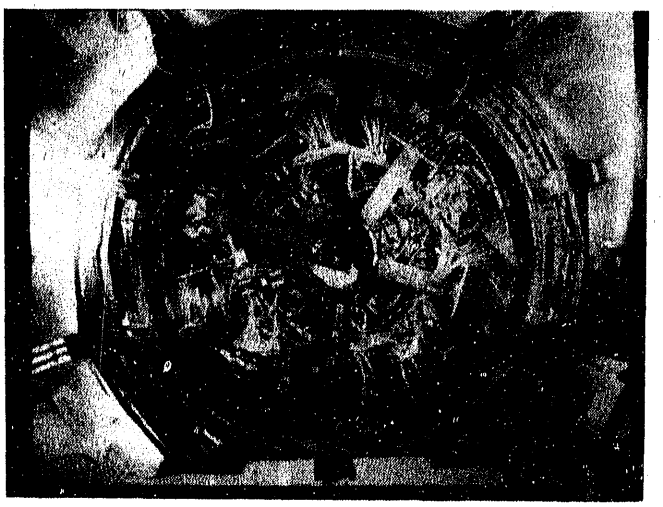

Fig. 8 Picture of one end of the central drift chamber with the motherboards, the auxiliary boards, and interconnections.

detector. The analog-to-digital converters are included in the MC68HC811 processor chip, which is disabled during data acquisition time.

V. Packaging

Figure 3 shows the location of the Fiberoptics/ECL conversion board, and the three sets of CDC controller, transition, and power distribution boards. The boards are mounted inside the chamber above the motherboards. A view of one end of the CDC with the boards and interconnections is shown in fig. 8.

The printed circuit boards for the EDC have a similar layout, but different space constraints from the CDC and are arranged on the circumference of the endcap chambers as indicated in fig. 2.

VI. Summary and Project Status

The organization and packaging of the electronic system for the drift chamber of the SLD is described. The location of the electronics inside the SLD magnet volume places a premium on compactness, reliability, and low power consumption. The cable plant is kept small through the use of a highly multiplexed control and readout scheme on optical fibers. Only 37 control and data fibers are necessary to service one end of the barrel.

As of October 1990, all 170 barrel motherboards and all support boards are installed and tested in the SLD at SLAC.

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