Physical Parameter-Based SPICE Models for InGaZnO Thin-Film Transistors Applicable to Process Optimization and Robust Circuit Design

Dae Hwan Kim, *Member, IEEE*, Yong Woo Jeon, Sungchul Kim, Yongsik Kim, Yun Seop Yu, *Member, IEEE*, Dong Myong Kim, *Member, IEEE*, and Hyuck-In Kwon

***Abstract*—In this letter, we show that the physics-based equation that was derived for amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) in our previous work can be successfully incorporated into the SPICE model via Verilog-A. The proposed model and extracted SPICE parameters successfully reproduce the measured current–voltage characteristics of amorphous indium–gallium–zinc-oxide (a-IGZO) TFTs and the load line diagram of a-IGZO TFT inverters. The main advantage of our model is that each parameter has its physical meaning and most of them can be related with the fabrication conditions of AOS TFTs. To show the advantage of the proposed models and extracted SPICE parameters more clearly, we investigate the effect of ionized donor concentration (N_{D}^{+}) on the inverter circuit operation and determine the optimum value of N_{D}^{+} and device dimensions considering the tradeoff between the power consumption and the output swing in a-IGZO inverters. The proposed physics-based SPICE model via Verilog-A is expected to play a significant role in the process optimization and circuit design with AOS TFTs.**

***Index Terms*—Amorphous indium–gallium–zinc-oxide (a-IGZO), amorphous oxide semiconductor (AOS), inverter, SPICE, thin-film transistor (TFT), Verilog-A.**

I. Introduction

DEMONSTRATION OF amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistor (TFT)-based analog and digital circuits has been extensively documented in recent years [1], [2]. This activity reflects the level of maturity achieved in the a-IGZO TFT fabrication technology. In most of previous works [1], [2], to simulate the circuit operation with a SPICE tool, the Rensselaer Polytechnic Institute (RPI) TFT model [3], [4] was used with the parameters extracted from the current–voltage (I–V) characteristics of a-IGZO TFTs. The RPI TFT model and extracted parameters have shown that they are useful in the prediction of a-IGZO TFT-based circuit behaviors. Although the RPI model is a powerful model based on the parameters with a physical meaning, it can be insufficient in simulating the unusual characteristics of amorphous oxide semiconductor (AOS) TFTs considering that it has been mainly derived from the amorphous silicon (a-Si) TFT. In this letter, we show that the physical parameter-based equation that was derived for AOS TFTs in our previous paper [5] can be successfully incorporated into the SPICE model via Verilog-A. We have shown that the proposed model can simulate the operational behavior of AOS TFTs in various bias conditions and reflect the peculiar electrical characteristics of AOS TFTs including the active layer thickness dependence of the electrical behaviors [5]. Based on the SPICE simulation with physics-based and process-controlled parameters, the ionized donor concentration dependence of the a-IGZO TFT inverter behavior is predicted for the first time.

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D. H. Kim, Y. W. Jeon, S. Kim, Y. Kim, and D. M. Kim are with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea.

Y. S. Yu is with the Department of Information and Control Engineering, Electronic Technology Institute, Hankyong National University, Anseong 456-749, Korea.

H.-I. Kwon is with the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 156-756, Korea (e-mail: hyuckin@cau.ac.kr).

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II. Physics-Based I–V Model for AOS TFTs

In our previous work [5], we proposed the physics-based I–V model for AOS TFTs with concrete techniques for parameter extraction as

$$I_{DS} = q\mu_{Band}\frac{W}{L} \times \int_{V_S}^{V_S+V_D}\int_{\phi_B}^{\phi_S} \frac{Q_{\mathrm{free}}(\phi, V_{CH}(y))}{Q_{\mathrm{free}}(\phi, V_{CH}(y)) + Q_{loc}(\phi, V_{CH}(y))} \times \frac{n_{\mathrm{free}}(\phi, V_{CH}(y))}{E_{AOS}(\phi, V_{CH}(y))} d\phi dV_{CH}(y) \quad (1)$$

where q is the electronic charge, μ_{Band} is the conduction band mobility, W is the channel width, L is the channel length, V_{S} is the source voltage, V_{D} is the drain voltage, ϕ_{S} is the surface potential, ϕ_{B} is the back potential, Q_{free} is the free charge density per unit area, Q_{loc} is the localized charge density per unit area which can be obtained from the extracted acceptorlike and donorlike density of states (DOS), n_{free} is the free electron density, and E_{AOS} is the surface electric field. Recently, Lee *et al.* [6] have reported the percolation conduction as a dominant conduction mechanism at high gate-to-source voltages (V_{GS}s) in AOS TFTs. However, the trap-limited

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TABLE I
SPICE MODEL PARAMETERS OF THE LOAD AND DRIVER TFTs

parameter	value		parameter	value		parameter	value	parameter	value
	Load	Driver		Load	Driver				
N_{TA} [$eV^{-1}cm^{-3}$]	8×10^{18}	7.5×10^{18}	N_D [cm^{-3}]	5×10^{16}	5×10^{16}	N_{TD} [$eV^{-1}cm^{-3}$]	1×10^{20}	N_C [cm^{-3}]	6×10^{18}
kT_{TA} [eV]	0.067	0.08	V_{FB} [V]	0.13	0.067	kT_{TD} [eV]	0.06	μ_{Band} [cm^2/Vs]	23.5
N_{DA} [$eV^{-1}cm^{-3}$]	5×10^{16}	3×10^{16}	W [μm]	50	175	N_{DD} [$eV^{-1}cm^{-3}$]	1×10^{18}	T_{OX} [nm]	100
kT_{DA} [eV]	0.8	0.8	L [μm]	30	30	kT_{DD} [eV]	0.55	T_{IGZO} [nm]	50

conduction was assumed because of the low V_{GS}'s in our model, and it showed good agreement with the measured results. Compared with the previously reported a-Si TFT models, the proposed model was proved to be more effective in reproducing the electrical characteristics of AOS TFTs where the free carrier charge can be comparable with or larger than the localized one out of the induced charge.

III. EXPERIMENTS, RESULTS, AND DISCUSSIONS

For this research, the enhancement load-type a-IGZO TFT-based inverter was integrated on a highly doped silicon substrate with a staggered bottom gate structure. The device structure and detailed process sequences are the same as that in [5]. The pads of all nodes in two TFTs were prepared in the inverter layout in order to separately extract the model parameters of the load and driver TFTs.

Table I summarizes the extracted parameters for the SPICE simulation in each TFT of the inverter based on the physical parameter-based equation for AOS TFTs. The parameters of T_{ox}, T_{IGZO}, N_{TA}, kT_{TA}, N_{DA}, kT_{DA}, N_{TD}, kT_{TD}, N_{DD}, kT_{DD}, V_{FB}, N_C, and N_D^+ in Table I represent the thickness of the gate oxide, thickness of a-IGZO active thin film, intercept density at the conduction band edge (E_C) of the acceptorlike exponential tail states, characteristic decay energy of the acceptorlike exponential tail states, intercept density at E_C of the acceptorlike exponential deep states, characteristic decay energy of the acceptorlike exponential deep states, intercept density at the valance band edge (E_V) of the donorlike exponential tail states, characteristic decay energy of the donorlike exponential tail states, intercept density at E_V of the donorlike exponential deep states, characteristic decay energy of the donorlike exponential deep states, flat-band voltage, conduction band effective DOS, and ionized donor concentration, respectively.

Fig. 1(a) and (b) depict the transfer curves and the load line diagram obtained from the measured and SPICE-simulated data in both TFTs. The results show that the SPICE-simulated transfer curves and the load line diagram are in good agreement with the measured ones, which verifies that the proposed physics-based model and the extracted model parameters are reasonable and very efficient in predicting the behavior of the a-IGZO TFT-based circuits.

To show the usefulness of the proposed models and extracted SPICE parameters more clearly, we investigate the effect of N_D^+ on the inverter operation and determine the optimum value of N_D^+ and W_{load}/W_{driver} considering the tradeoff between the

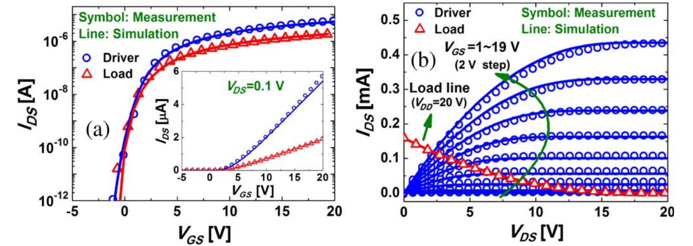

Fig. 1. (a) Transfer curves and (b) load line diagram obtained from the measured and SPICE-simulated data in both TFTs of the a-IGZO inverter. The inset of Fig. 1(a) shows the transfer characteristic in the linear scale.

power consumption and the output swing in a-IGZO inverters. The ionized donor concentration (N_D^+) is one of the most important physical parameter which can be managed by controlling the magnitude of oxygen vacancy (V_o) in amorphous oxide materials. Unlike the fitting parameter-based models, each parameter in our model has its physical meaning, which is the important advantage of our model. For example, the N_D^+ can be increased by reducing the partial pressure of oxygen during the deposition process of amorphous oxide thin films in AOS TFTs. Therefore, by using the proposed models and extracted SPICE parameters, we can easily predict the effect of TFT-fabrication conditions on the AOS TFT-based circuit behaviors.

Fig. 2(a) and (b) shows the voltage transfer curves (VTCs) and time transient characteristics of the a-IGZO inverter simulated using the extracted SPICE parameters with various values of N_D^+. The results show that the variation of N_D^+ much affects the inverter behaviors. As the value of N_D^+ increases, the output voltage (V_{OUT}) decreases at low input voltages (V_{IN}'s) in the VTC, and the output peak-to-peak voltage $(V_{OUT,P-P})$ increases in the transient characteristics. This phenomenon can be explained based on the modulation of channel resistance with a variation of N_D^+ in both TFTs. As well known, the increase of N_D^+ or V_o causes the negative shift of the threshold voltage in AOS TFTs, so the channel resistance decreases in both TFTs with an increase of N_D^+. In Fig. 2(a), the high V_{OUT} is close to the supply voltage (V_{DD}) in all circuits, which is due to the nonnegligible subthreshold current of the load TFT. Because ϕ_S is calculated by the numerical integration along the channel depth in our model, it can reflect the residual channel current due to the undepleted back surface in AOS TFTs [5].

Fig. 2(c) depicts the simulated channel resistance of both TFTs with various values of N_D^+. As expected, the channel resistance decreases with an increase of N_D^+ in both TFTs.

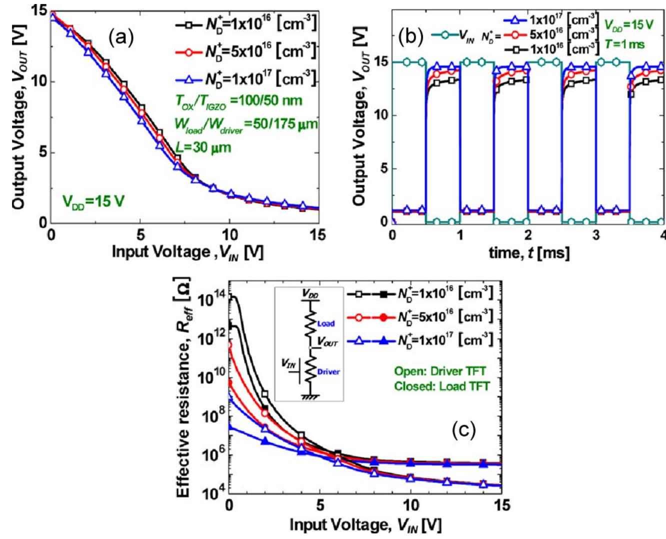

Fig. 2. Simulated N_{D}^{+}-dependences of (a) VTC, (b) transient characteristics, and (c) effective channel resistance of load and driver TFTs in inverters.

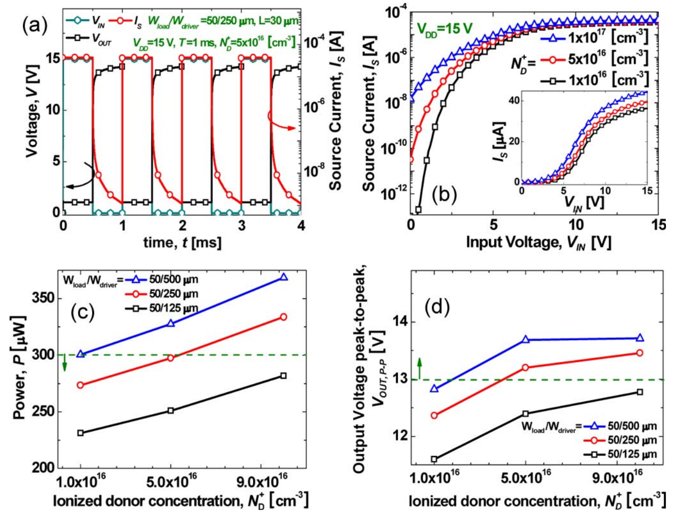

Fig. 3. (a) Simulated V_{IN}, V_{OUT}, and I_{S} of transient characteristics and (b) N_{D}^{+}-dependent short circuit current I_{S} as the function of V_{IN} in a-IGZO inverter. (c) Calculated P_{total} with the change of N_{D}^{+} and/or $W_{\mathrm{load}}/W_{\mathrm{driver}}$ and (d) simulated $V_{\mathrm{OUT,P-P}}$ with the change of N_{D}^{+} and/or $W_{\mathrm{load}}/W_{\mathrm{driver}}$ in the inverter.

Fig. 2(c) also shows that the degree of the channel resistance decrease is more prominent in the driver TFTs and at low V_{IN}'s. Considering that the decrease of the channel resistance in the driver TFT causes the improvement of the pull-down characteristics of the inverter and the reduction of resistance–capacitance delay in the pull-down path, the decrease of V_{OUT} at low V_{in}'s in the VTC and the increase of $V_{\mathrm{OUT,P-P}}$ in the transient characteristics with an increase of N_{D}^{+} can be considered as a reasonable result. During the transient simulation, we included a constant capacitance of 13.9 pF in the output node, which was calculated considering all the capacitances from the load TFT, driver TFT, and the external loads. The capacitance from the external load is included to imitate the real operation condition of the inverter circuits.

Although the result in Fig. 2 shows the effect of N_{D}^{+} on the inverter operation, we also have to consider the power consumption (P_{total}) for the circuit optimization. Fig. 3(a) shows the V_{IN}, V_{OUT}, and the short circuit current (I_{S}) in the transient characteristics of the a-IGZO TFT inverter, and Fig. 3(b) depicts the N_{D}^{+}-dependence of I_{S} as a function of V_{IN}. The result in Fig. 3(b) clearly shows that I_{S} increases with an increase of N_{D}^{+}, which represents that the higher power consumption is required in the inverter circuits with higher N_{D}^{+}-TFTs. If we compare this result with that of Fig. 2(b), we get to know that there is a tradeoff between the magnitude of $V_{\mathrm{OUT,P-P}}$ and the power consumption regarding the N_{D}^{+}, so it is necessary to find out the optimum value of N_{D}^{+}. Fig. 3(c) and (d) shows the simulated values of P_{total} and $V_{\mathrm{OUT,P-P}}$ in the a-IGZO inverters with various values of N_{D}^{+} and $W_{\mathrm{load}}/W_{\mathrm{driver}}$. If we assume the figure-of-merit (FOM) of the a-IGZO inverter as $P_{\mathrm{total}} < 300$ μW and $V_{\mathrm{OUT,P-P}} > 13$ V, the results in Fig. 3(c) and (d) show that the value of N_{D}^{+} and $W_{\mathrm{load}}/W_{\mathrm{driver}}$ should be decided to be $4.0 \times 10^{16} < N_{\mathrm{D}}^{+} < 5.5 \times 10^{16}$ cm^{-3} and 50/250 μm to fulfill the requirement. The procedures and results in Figs. 2 and 3 confirm the usefulness of our model and parameters in the process optimization as well as the circuit design with AOS TFTs.

IV. CONCLUSION

In this letter, we show that the physics-based equation that was derived for AOS TFTs in our previous paper [5] can be successfully incorporated into the SPICE model via Verilog-A. The derived equation shows good compatibility with the SPICE model. To confirm the usefulness of the model in a systematic optimization of the process/circuit design parameters in AOS TFTs more clearly, we simulate the effect of N_{D}^{+} on the inverter operation and determine the optimum value of N_{D}^{+} and $W_{\mathrm{load}}/W_{\mathrm{driver}}$ considering the tradeoff between the power consumption and the output swing in a-IGZO inverters. We expect that the proposed SPICE model will be very useful in the circuit design for innovative AOS TFT-based applications.

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