Physics-Based SPICE Model of a-InGaZnO Thin-Film Transistor Using Verilog-A

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***Abstract*—In this work, we report the physics-based SPICE model of amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) and demonstrate the SPICE simulation of amorphous InGaZnO (a-IGZO) TFT inverter by using Verilog-A. As key physical parameter, subgap density-of-states (DOS) is extracted and used for calculating the electric potential, carrier density, and mobility along the depth direction of active thin-film. It is confirmed that the proposed DOS-based SPICE model can successfully reproduce the voltage transfer characteristic of a-IGZO inverter as well as the measured *I-V* characteristics of a-IGZO TFTs within the average error of 6% at V_{DD}=20 V.**

***Index Terms*—Amorphous InGaZnO (a-IGZO), SPICE, Verilog-A, density-of-states (DOS), thin-film transistors (TFTs)**

I. INTRODUCTION

As a representative amorphous oxide semiconductor (AOS) material, amorphous InGaZnO (a-IGZO) has been studied and developed intensively as an active layer of thin-film transistors (TFTs) for switching/driving devices in flexible e-paper, transparent/lightweight display backplanes for active-matrix liquid crystal display (AMLCD) and/or active-matrix organic light-emitting diode display (AMOLED) [1, 2], stackable logic circuitry [3], and 3-D memories [4]. In order to design and integrate various innovative systems using AOS TFTs, the circuit simulation with physics-based and process-controlled parameters, not fitting parameters, is indispensible for process/structure optimization. However, physical parameter-based SPICE simulations of oxide TFTs have been rarely reported.

In this work, we report the physics-based SPICE model of AOS TFTs and demonstrate the SPICE simulation of a-IGZO TFT inverter by incorporating the proposed model into HSPICE via Verilog-A. As key physical parameter, subgap density-of-states (DOS) is experimentally extracted and used for calculating the electric potential, carrier density, and mobility along the depth direction of active thin-film. Then, the DC *I-V* characteristics is calculated by using the double integral with the surface potential (ϕ_S) and back potential (ϕ_B) as the function of V_{GS} (gate-to-source voltage) and V_{DS} (drain-to-source voltage). The simulated voltage transfer characteristic (VTC) of a-IGZO TFT inverter agrees well with the measured one, within the error ratio of 6%.

II. DOS-BASED MODEL

The acceptor-like subgap DOS ($g_A(E)$ [$eV^{-1}cm^{-3}$]) of AOS thin-films can be modeled as

$$g_A(E) = N_{TA} \times \exp\left(\frac{E-E_C}{kT_{TA}}\right) + N_{DA} \times \exp\left(\frac{E-E_C}{kT_{DA}}\right) \quad (1)$$

Here, the subscript of TA/DA means the acceptor-like tail/deep state, respectively.

In addition, the donor-like DOS ($g_D(E)$ [$eV^{-1}cm^{-3}$]) is

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presumably modeled as [5]

$$g_D(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{DD} \times \exp\left(\frac{E_V - E}{kT_{DD}}\right) \quad (2)$$

Here, the subscript of TD/DD means the donor-like tail/deep state, respectively. Then, the flat band voltage (V_{FB}) and E_{FB} (defined as the energy difference between Fermi-level E_F and conduction band minimum (E_C) at V_{GS}=V_{FB} condition) are calculated as following equations:

$$V_{FB} = \phi_{Gate} - \phi_{AOS} - \frac{Q_{ox}}{C_{ox}}$$
$$\phi_{Gate} - \phi_{AOS} = (\chi_{Gate} - \chi_{AOS}) - \frac{E_{FB}}{q} \quad (3)$$

$$q\left[n_{loc}(E_F) - n_{free}(E_F) + N_D^+\right] = 0 \quad (4)$$

Here, ϕ, χ, Q_{ox}, C_{ox}=ε_{ox}/T_{ox}, T_{ox}, q, n_{loc}, n_{free}, and N_D^+ are the work function, the electron affinity, the charge density per unit area in gate oxide, the gate oxide capacitance per unit area, the thickness of gate oxide, the charge of single electron, the localized charge density due to trapped charge in subgap DOS, the free electron density, and the donor doping concentration, respectively. In this work, Q_{ox} is postulated to be negligible and E_{FB} acts as a reference energy level in the calculation of V_{GS}-modulated electric potential $\phi(x, V_{CH}(y))$=$\phi(x, y)$ at a given location as shown in Fig. 1(a).

Then, n_{free} and n_{loc} can be calculated as follows:

$$n_{free}(x, V_{CH}(y)) = \frac{2}{\sqrt{\pi}} N_C F_{1/2}(\eta_F) \quad (5)$$

$$F_{1/2}(\eta_F) = \int_0^\infty \frac{\sqrt{\eta}}{1 + \exp(\eta - \eta_F)} d\eta \quad (6)$$

$$\eta_F(x, V_{CH}(y)) = \frac{q\phi(x, y) - qV_{CH}(y) - E_{FB}}{kT} \quad (7)$$

$$n_{loc}(x, V_{CH}(y)) = \int_{E_V}^{E_C} g_D(E)[1 - f(E)]dE - \int_{E_V}^{E_C} g_A(E) f(E) dE \quad (8)$$

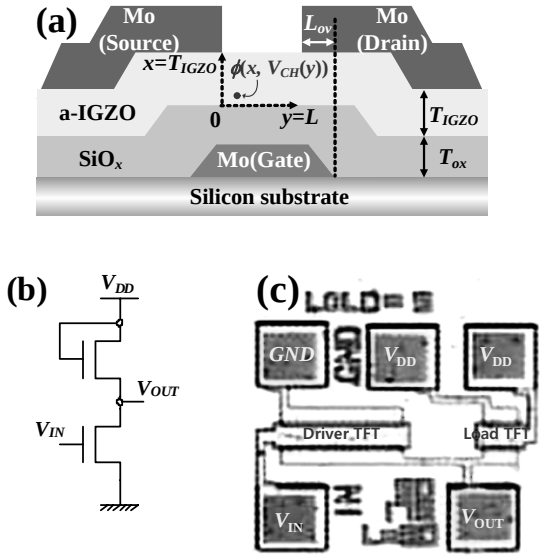

Fig. 1. (a) The cross-section of a-IGZO TFT with an inverted staggered bottom gate structure and the definition of local potential $\phi(x, V_{CH}(y))$, (b) The schematic circuit diagram and (c) The top view of integrated a-IGZO TFT-based inverter.

where N_C and $f(E)$ are the effective DOS in conduction band and the Fermi-Dirac distribution function, respectively. In addition, the potential difference along the channel length direction, as denoted by $V_{CH}(y)$, describes the electron quasi Fermi-level E_{Fn} lowering by $qV_{CH}(y)$ due to applied V_{DS}. Therefore, it is given that $V_{CH}(y=0)=V_S$ (near source region) and $V_{CH}(y=L)=V_D$ (near drain region). Here, if the surface potential ϕ_S is defined as $\phi(x=0, V_{CH}(y))=\phi(x=0, y)$, $V_{CH}(y)$ plays the role of increasing ϕ_S from y=0 to L. However, E_{Fn} is also lowered by $qV_{CH}(y)$, consequently, n_{free} decreases from y=0 to L, as shown in Eqs. (5-7). In addition, it is noticeable that even though $V_{CH}(y)$ is not given as the exact function of y, the double integrals in Eq. (13) can be calculated with a given V_{DS}. Meanwhile, the 2-D Poisson's equation can be solved, as denoted by Eq. (9), with the charge density ρ which is described with DOS parameters and ε_{AOS}=the dielectric constant of AOS thin-film as denoted by Eq. (9). Also, the free and localized charge density per unit area (Q_{free} and Q_{loc}) at a given y=y_0 can be calculated from Eqs. (10-11) with T_{AOS}=the thickness of AOS thin-film. Finally, the self-consistent pair of $\phi_B(\phi_S)$ and $V_{GS}(\phi_S)$ can be extracted with the surface electric field $E_{AOS}(x=0)$ by Eq. (12) and the current I_{DS} is given by using the double integrals as Eq. (13):

$$\frac{\partial^2\phi(x,y=y_0)}{\partial x^2}=\frac{-\rho}{\varepsilon_{AOS}}$$
$$=\frac{q}{\varepsilon_{AOS}}\left[n_{loc}(x,V_{CH}(y))+n_{free}(x,V_{CH}(y))-{N_D}^+\right] \quad (9)$$

$$Q_{free}(x,V_{CH}(y))=q\int_{x=x}^{x=T_{AOS}} n_{free}(x,V_{CH}(y))dx \quad (10)$$

$$Q_{loc}(x,V_{CH}(y))=q\int_{x=x}^{x=T_{AOS}} n_{loc}(x,V_{CH}(y))dx \quad (11)$$

$$V_{GS}=V_{FB}+\phi_s\big|_{y=y_0}+\left.\frac{Q_{loc}(x=0)+Q_{free}(x=0)+qN_D^+\times T_{AOS}}{C_{ox}}\right|_{y=y_0}$$
$$=V_{FB}+\phi_s\big|_{y=y_0}+\left.\frac{\varepsilon_{AOS}\times E_{AOS}(x=0)}{C_{ox}}\right|_{y=y_0} \quad (12)$$

$$I_{DS}=q\mu_{Band}\frac{W}{L}\int_{V_S}^{V_S+V_D}\int_{\phi_B}^{\phi_S}\frac{Q_{free}(\phi,V_{CH}(y))}{Q_{free}(\phi,V_{CH}(y))+Q_{loc}(\phi,V_{CH}(y))}$$
$$\times\frac{n_{free}(\phi,V_{CH}(y))}{E_{AOS}(\phi,V_{CH}(y))}d\phi\,dV_{CH}(y) \quad (13)$$

where ρ, μ_{Band}, W, and L are the charge density, the conduction band mobility, the channel width, and the channel length, respectively. The detailed process of the derivation of (13) was given in [5].

III. SPICE IMPLEMENTATION

In order to implement the DOS-based model into SPICE via Verilog-A, the core process is calculating $\phi(x, y=y_0)$ [at a given lateral location $y=y_0$] from $g_A(E)$ and $g_D(E)$ under a specific V_{GS} and V_{DS}, where $0\le x\le T_{AOS}$ and $0\le y_0\le L$. Once the *fundamental physical parameters* such as μ_{Band}, N_C, ${N_D}^+$, $g_A(E)$ and $g_D(E)$ are known, we can divide the AOS thin-film into infinitesimal sectors Δx along the vertical direction and assume the charge density ρ to be constant within a single sector. In this work, the AOS thin-film is divided into 100 sectors. Then, under specific V_{GS} and V_{DS}, the calculation of $\phi(x, y=y_0)$ can be conducted via 1-D field solver from $x=T_{AOS}$ [back interface] to $x=0$ [front interface] by assuming the back potential ϕ_B [defined as $\phi(x=T_{AOS}, V_{CH}(y))=\phi(x=T_{AOS}, y)$] as an appropriate value. The detailed procedure of 1-D field solver was given in Fig. 3 in [5] and the related description therein.

Under a specific V_{GS} and *fundamental physical parameters*, the ϕ_S is acquired with the assumed value of

Table 1. Module declaration and parameter definition

```
//** Module declaration and Input / Output terminals
1)  `include "discipline.h"
2)  module TFT(D, G, S);
3)  inout D, G, S;
4)  electrical D, G, S;

//** Parameters define
5)  parameter real PI= 3.14159;
6)  parameter integer depth_resolution= 100;
7)  parameter integer DOS_resolution= 100;

// Physical Parameters
8)  parameter real tox=100e-7;
9)  parameter real L=30*1e-4;
10) parameter real W=175*1e-4;
11) parameter real Tgizo = 50e-7;
12) parameter real epsilon_gizo=11.5;
13) parameter real epsilon=8.854e-14;
14) parameter real band_mobility=23.5;
15) parameter real delta_Vfb=0;
16) parameter real Ec = 3.2;
17) parameter real Nc = 6.00e18;
18) parameter real Nv = 1.00e16;
19) parameter real Nd = 5e16;
20) parameter real q=1.6e-19;
21) parameter real kT=0.0259;
22) parameter real Ioff=1e-18;

// Acceptor_like DOS parameters
23) parameter real NTA = 7.5e18;
24) parameter real kTta = 0.08;
25) parameter real NDA = 3e16;
26) parameter real kTda = 0.8;

// Donor_like DOS parameters
27) parameter real NTD = 1e20;
28) parameter real kTtd = 0.06;
29) parameter real NDD = 1e18;
30) parameter real kTdd = 0.55;

// Array and local variables
31) real potential_x[0:depth_resolution];
32) real Efield[0:depth_resolution];
33) real function_n[0:depth_resolution-1];
34) real function_p[0:depth_resolution-1];
35) real DOS[0:depth_resolution-1];
36) real Rho1[0:depth_resolution-1];
37) real Qfree[0:depth_resolution-1];
38) real Qloc[0:depth_resolution-1];
39) real VGS_compare[0:21];
40) real VDS_compare[0:100];
41) real pi_b_compare[0:2221];
42) real Cox;
43) real eta_f,mu,xi,FDIn,FDIp,Dop_effect,E_step;
44) real depth,lateral,Qfreei,pi_b_avg1,pi_b_avg2,Efbo,Efb,Vfb;
45) real t,A,DD ;
46) real Vgd,Vgs,Vds;
47) real itv,Vds_itv;
48) integer i,x,y;
```

Table 2. The initiation of $\phi_B(V_{GS})$

```
// Input of φB(VGS), pi_b_compare[N]=the array saving solutions
   of φB(VGS)
87)  pi_b_compare[0]= n0;
88)  …….
89)  pi_b_compare[2221]=nN;

// Mapping φB(VGS) corresponding to the simulated bias point
90)  pi_b_avg1=pi_b_compare[(x-1)*101+y-
     1]+(pi_b_compare[(x)*101+y-1]-pi_b_compare[(x-1)*101+y-
     1])*((Vgs-VGS_compare[x-1])/(VGS_compare[x]-
     VGS_compare[x-1]));
91)  pi_b_avg2=pi_b_compare[(x-
     1)*101+y]+(pi_b_compare[(x)*101+y]-pi_b_compare[(x-
     1)*101+y])*((Vgs-VGS_compare[x-1])/(VGS_compare[x]-
     VGS_compare[x-1]));
92)  potential_x[depth_resolution]=pi_b_avg1+(pi_b_avg2-
     pi_b_avg1)*((Vds_itv-VDS_compare[y-
     1])/(VDS_compare[y]-VDS_compare[y-1]));
```

Table 3. The calculation of n_{free} and n_{loc}

```
//** Declaration of EFB by using φB(VGS)
93)  analog begin
94)  Vgd=V(G, D);
95)  Vgs=V(G, S);
96)  Vds=V(D, S);
97)  Efbo=0.2475733;

// Calculating nfree
98)  if(Vds_itv<0)
99)  begin
100) lateral=Ioff;
101)       end
102) else
103) begin
104) Efb=Efbo+Vds_itv;
105) Vfb=0.3-Efb+delta_Vfb;
106) for(i=depth_resolution;i>0;i=i-1)
107) begin
108) eta_f=(potential_x[i]-Efb-Vds_itv)/(kT);
109) mu=pow(eta_f, 4)+50+33.6*eta_f*(1-0.68*exp(-
     0.17*pow(eta_f+ 1,2 ) ) );
110) xi=3*sqrt(PI)/(4*pow(mu,(3/8)));
111) FDIn=pow((exp(-eta_f)+xi),-1); /*Relative error +-0.4% */
112) FDIp=pow((exp(-(eta_f-(Ec/kT)))+xi),-1); /*Relative error +-
     0.4% */
113) function_n[i-1]=2*Nc*FDIn/pow(PI,0.5); /* [1/cm3] */
114) function_p[i-1]=2*Nv*FDIp/pow(PI,0.5); /* [1/cm3] */
115) Dop_effect=Nd;

// Calculating nloc
116) A=0;
117) DD=0;
118) for(t=0;t<=Ec;t=t+E_step)
119) begin
120) A=A+(NTA*exp((t-Ec)/kTta)+NDA*exp((t-
     Ec)/kTda))*(1/(1+exp((t-(Ec-Efb-
     (Vds_itv)+potential_x[i]))/kT)))*E_step;
121) end
122) for(t=0;t<=Ec;t=t+E_step)
123) begin
124) DD=DD+(NTD*exp((-1*t)/kTtd)+NDD*exp((-
     1*t)/kTdd))*(1-(1/(1+exp((t-(Ec-Efb-
     (Vds_itv)+potential_x[i]))/kT))))*E_step;
125) end
126) DOS[i-1]=A-DD;
```

ϕ_B. Then, whether the relation between V_{GS} and ϕ_S is satisfied consistently with Eq. (12) or not is checked with the present values of V_{GS} and ϕ_B. Unless it is satisfied,

Table 4. The calculation of $\phi(x)$, $E_{AOS}(x)$, $\rho(x)$, Q_{free} and Q_{loc}

```
// 1-D field solver calculation
49)  Rho1[i-1]=function_n[i-1]-function_p[i-1]+DOS[i-1]-
     Dop_effect;
50)  Efield[i-1]=Efield[i]+q*Rho1[i-1]*(Tgizo/depth_resolution)/
     (epsilon*epsilon_gizo);
51)  potential_x[i-1]=potential_x[i] + Efield[i-
     1]*(Tgizo/depth_resolution)
     +((Tgizo/depth_resolution)/2)*(Efield[i-1]-Efield[i]);

// Free charge(Qfree) and localized charge(Qloc) density calculation
52)  if(i>=depth_resolution)
53)  begin
54)  Qfree[i-1]=q*(function_n[i-1])*(Tgizo/depth_resolution);
55)  Qloc[i-1]=q*(DOS[i-1])*(Tgizo/depth_resolution); /* [C/cm2]
     */
56)  end
57)  else if(i>=1)
58)  begin
59)  Qfree[i-1]=Qfree[i]+q*(function_n[i-
     1])*(Tgizo/depth_resolution);
60)  Qloc[i-1]=Qloc[i]+q*(DOS[i-1])*(Tgizo/depth_resolution);
61)  end
62)  end

// Qfree(x) calculation
63)  for(i=depth_resolution;i>0;i=i-1)
64)  begin
65)  Qfreei=Qfreei+q*(potential_x[i-1]-
     potential_x[i])*(function_n[i-1]/Efield[i-1]);
66)  end
```

Table 5. The calculation of $I_{DS}(V_{GS}, V_{DS})$

```
// The current calculation
```

$$I_{DS}=q\mu_{Band}\frac{W}{L}\int_{V_S}^{V_S+V_D}\int_{\phi_B}^{\phi_S}\frac{Q_{free}(\phi,V_{CH}(y))}{Q_{free}(\phi,V_{CH}(y))+Q_{loc}(\phi,V_{CH}(y))}\times\frac{n_{free}(\phi,V_{CH}(y))}{E_{AOS}(\phi,V_{CH}(y))}d\phi dV_{CH}(y)$$

```
67)  for(i=depth_resolution;i>0;i=i-1)
68)  begin
69)  depth=depth+q*(W/L)*band_mobility*(Qfreei/(Qfree[0]+
     Qloc[0]+Qit))*(potential_x[i-1]-potential_x[i])*(function_n
     [i-1]/Efield[i-1]);
70)  end
71)  lateral=lateral+depth*itv;
72)  if(Vds-Vds_itv<0.1 && Vds-Vds_itv>0)/*************/
73)  begin
74)  itv=Vds-Vds_itv;
75)  end
76)  else
77)  begin
78)  itv=0.1;
79)  end
80)  end
81)  depth=0;
82)  Qfreei=0;
83)  end
84)  I(D,S) <+ lateral;
85)  end
86)  endmodule
```

then the assumed value of ϕ_B is adjusted until the relation between V_{GS} and ϕ_S agrees with Eq. (12). In this way, we can find the self-consistent solutions of $\phi_B(V_{GS})$ and $\phi_S(V_{GS})$. Once $\phi_B(V_{GS})$ and $\phi_S(V_{GS})$ are known, the output current $I_{DS}(V_{GS}, V_{DS})$ is able to be calculated by Eq. (13).

We have incorporated abovementioned procedures into HSPICE via Verilog-A. Although the source code of Verilog-A is too long to be shown here, we summarize it herein as denoted by following tables [Table 1~5] in which the key procedures implemented via Verilog-A are concisely described in a *high-level language* type.

IV. A-IGZO TFT INVERTER EXPERIMENTS AND RESULTS

A cross-sectional view of integrated a-IGZO TFTs with the staggered bottom gate structure is shown in Fig. 1(a). The detailed process sequence for a-IGZO TFTs is the same as in [5]. Structural parameters are as follows: the channel length (L)=30 μm, the gate-to-S/D overlap length (L_{ov})=5 μm, the thickness of the gate oxide (T_{ox})=100 nm, and the thickness of a-IGZO active thin-film (T_{IGZO})=50 nm, respectively. As shown in Fig. 1(b), the enhancement load-type a-IGZO TFT-based inverter was integrated. The channel width W_{load}/W_{driver} was 50/175 μm for the load/driver TFT, and the pads of all nodes in two TFTs were prepared in the inverter layout in order to separately extract subgap DOSs of the load and driver TFTs (five pads as seen in Fig. 1(c)).

The $g_A(E)$ was experimentally extracted from the multi-frequency response of C-V characteristics [6]. All a-IGZO DOS parameters are given in Table 6.

By using the 1-D field solver via Verilog-A [*i.e.*, Table 2 and 4] and Eqs. (9-12), $\phi_S(V_{GS})$ and $\phi_B(V_{GS})$ are acquired as seen in Fig. 2(a). Fig. 2(b) also shows the V_{GS}-modulated energy band around the source region (*i.e.*, y=0), which is calculated from the 1-D field solver. Especially, the floating body effect with ϕ_B is clearly reproduced.

The measured device parameters of the driver and load TFTs consisting of a-IGZO inverter are summarized in Table 7. The difference of field-effect mobility (μ_{FE}) is attributed to both the ratio of W_{load}/W_{driver} and the definition of μ_{FE}.

The SPICE simulated transfer and output characteristics based on the extracted ϕ_S and ϕ_B show a good agreement with the measured ones both in the linear and in the log scale, as seen in Fig. 3. It verifies that the proposed DOS-based SPICE model of a-IGZO TFTs is reasonable and very efficient. The used SPICE parameters are also summarized in Table 6.

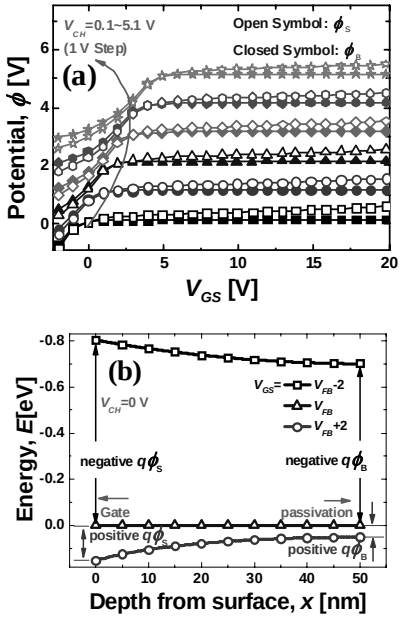

Fig. 2. (a) The self-consistent $\phi_S(V_{GS})$ and $\phi_B(V_{GS})$ solution pair of the driver TFT extracted from the 1-D field solver, (b) The V_{GS}-modulated energy band diagram of the driver TFT at $V_{CH}(y=0)$=0 V with definitions of ϕ_S and ϕ_B.

Table 6. Used SPICE parameters

parameter	value		parameter	value
	driver	load		
N_{TA} [eV^{-1}cm^{-3}]	7.5×10^{18}	8×10^{18}	N_{TD} [eV^{-1}cm^{-3}]	1×10^{20}
kT_{TA} [eV]	0.08	0.067	kT_{TD} [eV]	0.06
N_{DA} [eV^{-1}cm^{-3}]	3×10^{16}	5×10^{16}	N_{DD} [eV^{-1}cm^{-3}]	1×10^{18}
kT_{DA} [eV]	0.8	0.8	kT_{DD} [eV]	0.55
parameter	value		parameter	value
	driver	load		
N_D [cm^{-3}]	5×10^{16}	5×10^{16}	N_C [cm^{-3}]	6×10^{18}
V_{FB} [V]	0.067	0.13	μ_{Band} [cm^2/Vs]	23.5
W [μm]	175	50	T_{OX} [nm]	100
L [μm]	30	30	T_{AOS}=T_{IGZO} [nm]	50

Table 7. The measured performance parameters

TFT	V_T [V]	μ_{FE} [cm^2/Vs]	SS [V/dec]	I_{ON} [μA] (V_{GS}=20 V, V_{DS}=0.1 V)	I_{ON}/I_{OFF}
Driver	5.42	19.8	0.67	5.73	8.04×10^5
Load	5.04	6.39	0.66	1.91	6.36×10^6

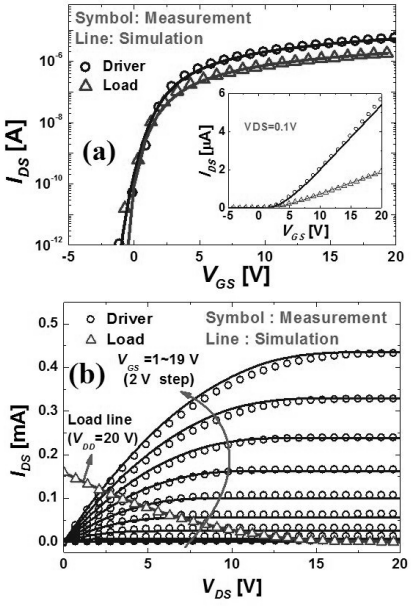

Fig. 3. (a) The transfer and (b) Output characteristics of a-IGZO TFTs calculated by using Eq. (13), The inset of (a) shows the transfer characteristic in the linear scale. The measured load line curve also agrees well with the simulated one.

The average/maximum error between the measured and simulated transfer characteristic is 3.06/10.1% and 5.73/20% (driver and load TFT, respectively) in Fig. 3(a). Also, the average/maximum error between the measured and simulated output characteristic is 0.33/6.4% and 2.29/3% (driver and load TFT, respectively) in Fig. 3(b). High error value of transfer characteristics is mainly attributed to the subthreshold current regime.

Finally, the VTC of a-IGZO inverter in Fig. 1(c) is measured at a room temperature without photo-illumination. The a-IGZO inverter is also simulated by

Table 8. The HSPICE input code for a-IGZO inverter simulation

```
//** The simulation of VTC in a-IGZO inverter

1)   Inverter simulation
2)   .hdl  'DeAOTS_DC_Model_inverter.va'
3)   .option post

4)   Vg G 0 dc
5)   Vd D 0 20
6)   Vs S 0 0

7)   Xtft1 Vout G S TFT_DRIVER
8)   Xtft2 D D Vout TFT_LOAD

9)   .dc Vg 0.0 20 0.5

10)  .print V(Vout)
11)  .end
```

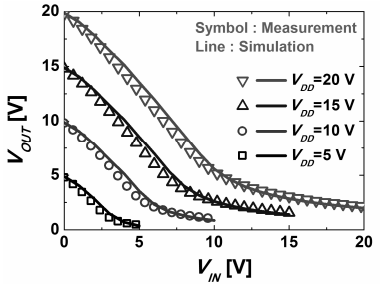

Fig. 4. The measured VTC for a-IGZO TFT inverter compared with SPICE simulation. The average error between the measured and simulated VTC is 6% at V_{DD}=20 V.

using the proposed DOS-based SPICE model. The input code used in HSPICE simulation is shown in Table 8.

Fig. 4 shows that the measured VTC agrees well with the simulated one at various supply voltages (V_{DD}). The average/maximum error between the measured and simulated VTC is 6/12.6% at V_{DD}=20 V. Consequently, the proposed DOS-based SPICE model is found to be efficiently applicable to AOS-based circuit simulation.

V. CONCLUSIONS

The physics-based SPICE model of AOS TFTs is proposed and demonstrated in a-IGZO TFT inverter by using Verilog-A. The DOS-based SPICE model can successfully reproduce the measured *I-V* characteristics of a-IGZO TFTs and the VTC of a-IGZO inverter very efficiently. Especially, it is noticeable that the proposed SPICE model and the simulation methodology are expected to be very useful in the process optimization as well as the circuit design of AOS TFTs because subgap DOS is the process-controlled parameter. As further study, the *C-V* model is underway. The physics-based SPICE model via Verilog-A is expected to play a significant role in process optimization and circuit design for innovative AOS TFT-based applications such as display backplane, wearable computers, e-paper, transparent SoC, solar cell, and 3-D stacked memories.

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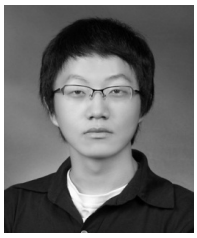

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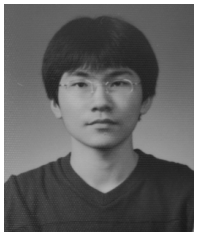

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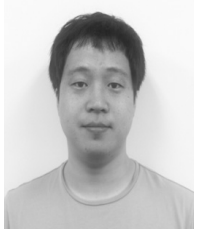

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