Pico-A/V range CMOS transconductors using series-parallel current division

A. Arnaud and C. Galup-Montoro

A simple design procedure for very small transconductors with extended linear range, using series-parallel division of current, is presented. It is based on a previously reported one-equation all-region transistor model. Using this technique, a 33 pico-A/V transconductor equivalent to a 30 GΩ resistor is demonstrated.

Introduction: In recent years there has been considerable research effort in the development of integrated transconductance amplifiers (OTAs) with very small transconductance and improved linear range due mainly to their application in biomedical circuits and in neural networks [1]. Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with linear range up to 1 V [1–4]. The use of complex OTA architectures also increases noise, mismatch offset and transistor area, and results in design trade-offs [1]. Simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area. However, the use of series–parallel division of current [4] in an OTA, as in Fig. 1, allows the implementation of an area efficient current divider. For the NMOS current mirrors in Fig. 1, N unity transistors M_2 are placed in series or in parallel to achieve an effective output transconductance G_m:

$$G_m = \frac{g_{m1}}{N^2} \tag{1}$$

g_{m1} is the tranconductance of the transistors M_1 in the differential input pair. In this Letter a simple and widely-general equation for the linear range of a CMOS differential pair, in terms of the transistor size and bias current, is developed. This expression is employed to set a design procedure for very small tranconductance OTAs by means of series–parallel current division. Using this technique, a 33 pico-A/V transconductor with a ±150 mV linear range has been designed, fabricated in a standard 0.8 μm CMOS technology, and tested. For the theoretical deductions and also for the simulations the all region MOSFET model of [5] is employed, since it allows an accurate representation of the series–parallel association in Fig. 1.

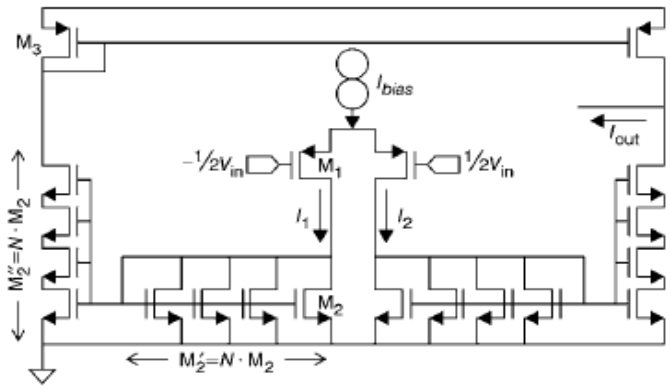

Fig. 1 *PMOS-input symmetrical OTA with series-parallel current division to reduce transconductance without loss in linear range*

Transconductance design methodology: For a given acceptable error α, the linear range V_{lin} of the differential pair in Fig. 1 is defined:

$$\text{if } |V_{in}| < V_{lin}, \quad \text{then} \quad \left|\frac{I_{diff} - g_{m1}\cdot V_{in}}{g_{m1}\cdot V_{in}}\right| \le \alpha \tag{2}$$

The differential current is $I_{diff} = I_1 - I_2$, and the bias current is $I_{bias} = I_1 + I_2$ (see Fig. 1). To calculate $I_{diff}(V_{in})$, the compact model of [5] is employed:

$$V_{in} = n\phi_t\left[\sqrt{1+\frac{i_b+i_d}{2}} - \sqrt{1+\frac{i_b-i_d}{2}} + \ln\left(\sqrt{1+\frac{i_b+i_d}{2}}-1\right) - \ln\left(\sqrt{1+\frac{i_b-i_d}{2}}-1\right)\right] \tag{3}$$

i_b, i_d are the normalised bias and differential current, respectively, $I_{diff} = I_S \cdot i_d$, $I_{bias} = I_S \cdot i_b$. The normalisation current is $I_S = (1/2) \times \mu C_{ox} n \phi_t^2 (W_1/L_1)$, where μ is the effective mobility, C_{ox} the oxide capacitance per unit area, W_1, L_1 the transistor's width and length, ϕ_t the thermal voltage, and n is the slope factor slightly dependent on the gate voltage. For fixed i_b, (3) defines $V_{in} = f(i_d)$; expanding the inverse function $i_d = f^{-1}(V_{in}) = g(V_{in})$ in series,

$$i_d = \sum_{j=1}^{\infty} k_j \cdot V_{in}^j, \quad k_j = \frac{1}{j!}\cdot\left.\frac{d^j i_d}{dV_{in}^j}\right|_{V_{in}=0} = \frac{1}{j!}\cdot\left.\frac{d^j g}{dV_{in}^j}\right|_{i_d=0} \tag{4}$$

The coefficients up to third order are calculated with the inverse function derivation rule:

$$g'(i_d=0) = \frac{2\cdot i_f}{n\phi_t\cdot(\sqrt{1+i_f}+1)} = \frac{g_{m1}}{I_S} \tag{5}$$

$$g''(i_d=0) = 0 \tag{6}$$

$$g'''(i_d=0) = \frac{1}{2n^3\phi_t^3}\cdot\frac{(\sqrt{1+i_f}-1)\cdot(3\sqrt{1+i_f}-1)}{(1+i_f)^{3/2}} \tag{7}$$

$i_f = i_b/2$ is the inversion level [5] of M_1. For $i_f \ll 1$, the transistor is in weak inversion, and for $i_f > 100$ the transistor is in strong inversion. Substituting (4) up to third order in (2), it is possible to estimate the linear range of the transconductor:

$$V_{lin} = 2n\phi_t\sqrt{\frac{6\alpha(1+i_f)^{3/2}}{3(1+i_f)^{1/2}-1}} \tag{8}$$

$$V_{lin} \simeq 3n\phi_t\sqrt{\alpha(1+i_f)} \tag{9}$$

The plot in Fig. 2 shows the linear range of a PMOS differential pair in terms of the inversion level as measured, simulated and predicted by (8) and (9). The measurements were performed by varying the bias current of a standard symmetrical OTA. Equations (8) and (9) are very convenient for design. Suppose that an analogue circuit requires a transconductor of an extremely low value G_{mX}, and an input linear range V_{lin_X}. The inversion level i_{f1} of the input pair is determined by (8) or (9) and, for a given bias current, the normalisation current is $I_S = 2I_{bias}/i_{f1}$. Then, g_{m1} from (5), (W_1/L_1) from I_S definition and $N = \sqrt{(g_{m1}/G_{mX})}$ from (1) can be determined. The design space has been reduced to a single dimension, the bias current of the input pair, that can be determined from the power consumption and area budgets. The size of M_2 and M_3 only influence leakage currents, matching and noise. By using a high division factor N^2, it is possible to obtain transconductances in the order of pico-A/V, limited only by leakage current [6]. Although biasing the input differential pair deep in strong inversion allows a wide linear range to be achieved, it may not be suitable for a low voltage power supply. In this case the series–parallel current division technique is still valuable but a different topology for the input pair is required, e.g. those proposed in [2, 3].

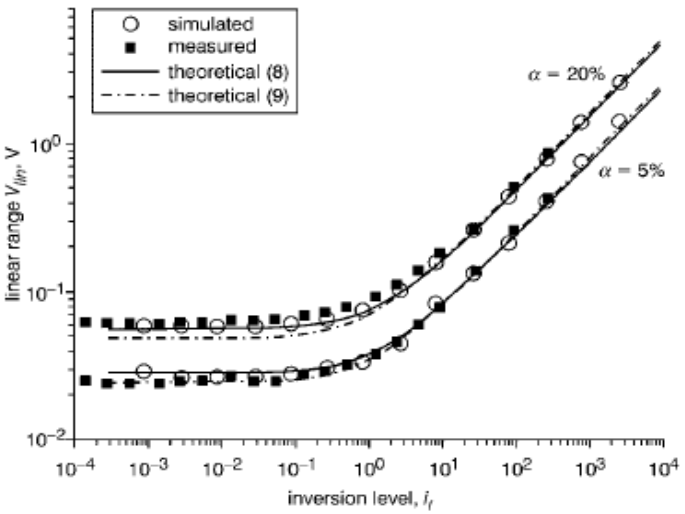

Fig. 2 *Measured, simulated and theoretical linear range in terms of i_f of input pair for symmetrical OTA*

Transconductor design example: Using this technique a $G_m =$ 35 pico-A/V CMOS-OTA intended to be employed in the signal conditioning circuit of a biomedical sensor has been designed. The specifications require 150 mV linearity for $\alpha = 5\%$. Using (9), the inversion level of the input pair resulted in $i_{f1} = 35$. $W_1 = 4\ \mu m$, $L_1 = 100\ \mu m$, $I_{bias} = 40$ nA, values were selected according to the area and current budgets, and a factor $N = 70$ allows the desired transconductance to be achieved. The measured G_m was 33 pico-A/V, the circuit operates up to 2 V power supply, with a total area of only 0.08 mm^2. Fig. 3 shows the output current of the OTA, and the linear range. The measurement procedure for current output is that proposed in [6].

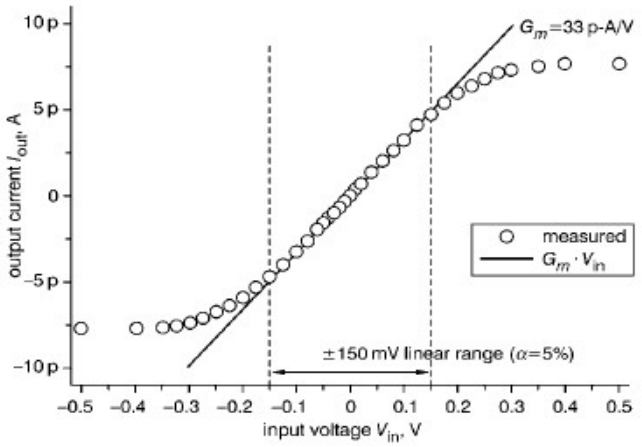

Fig. 3 *Output current and linear range of 33 pico-A/V transconductor*

Conclusion: A simple expression for the linear range of a differential pair valid in all transistor operation regions has been deduced. Using this expression, a design methodology for extremely low transconductances, with extended linear range, using series-parallel current division, has been presented. A 33 p-A/V transconductor fabricated in a 0.8 μm CMOS technology has been demonstrated using this technique.

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