Picosecond large-signal switching characteristics of a pseudomorphic AlGaAs/InGaAs modulated doped field effect transistor

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We present the first comprehensive study of the large-signal switching characteristics of an AlGaAs/InGaAs modulation-doped field-effect transistor on a picosecond time scale. Electro-optic sampling is used to measure drain voltage response to a steplike gate input with a 2.8 ps rise time, at various dc biases. A large-signal switching time of 6.2 ps is obtained. Features deleterious to high-frequency device operation are observed, related to equivalent circuit parameters, and reduced by appropriate choice of operating point.

Since its demonstration,[1] the modulation-doped field-effect transistor (MODFET) has been of great interest for high-speed digital and analog applications. Originally fabricated with a GaAs channel, performance has been improved using an InGaAs channel to improve electron confinement and mobility, and reduce AlGaAs-layer DX-center effects. Pseudomorphic AlGaAs/InGaAs MODFETs have been demonstrated with a current-gain cutoff frequency, f_t, exceeding 150 GHz,[2] and AlInAs/GaInAs MODFETs with f_t up to 250 GHz have been fabricated.[3] An essential part of the development of such high-speed devices is measurement of their large-signal performance. These measurements are necessary to test our understanding of the physics of MODFET operation, and to allow design of high-speed MODFET circuits.

Attempts to characterize devices with response times of a few picoseconds have made apparent the difficulty of using all-electronic test methods. The cutoff frequency must be estimated by extrapolating small-signal network-analyzer measurements made at frequencies significantly below f_t, because broadband network analyzers are presently limited to a maximum frequency of approximately 70 GHz. Similar bandwidth limitations are encountered with time-domain measurements using sampling oscilloscopes, which currently have a resolution of 5 ps at best. The recent measurement of a 1.4 ps fall time using nonlinear transmission lines[4,5] shows promise for progress in all-electronic measurement. However, generation of both positive- and negative-going signals with fast rise times has

not been demonstrated, and will be needed for large-signal measurements of active devices. The above difficulties with all-electronic measurements are not encountered using very high bandwidth optoelectronic techniques based on ultrafast lasers: optoelectronic excitation[6,7] and electro-optic detection,[8] allow generation and detection of electrical signals with subpicosecond rise and fall times. These optoelectronic techniques have been applied to small-signal characterization of passive coplanar striplines to 1 THz[9,10] and MODFET devices to 100 GHz.[11] In addition to the very high bandwidth of optoelectronic methods, the ability to generate large electrical signal amplitudes has been employed in the study of switching of active devices.[12-14] Large-signal characterization of active devices is important because of the wide range of high-speed large-signal device applications, including analog sampling circuits, oscillators, and all digital circuits. It is also important in understanding device operation since large-signal operation on very short time scales involves rapid changes of carrier distributions throughout the device. As the time scale of the signals at the device input and output approaches that required for reequilibration of carrier distributions, it will become necessary to include these non-quasi-static effects in nonlinear device models. Large-signal measurements on a very short time scale will allow the development and verification of nonlinear circuit models, and their comparison with existing models based on bias-dependent small-signal measurements.[15] In this letter, we report the first comprehensive study of the large-signal switching characteristics of a pseudomorphic AlGaAs/InGaAs MODFET on a picosecond time scale.

The AlGaAs/InGaAs MODFET is fabricated on a wafer grown by molecular beam epitaxy. The 13 nm

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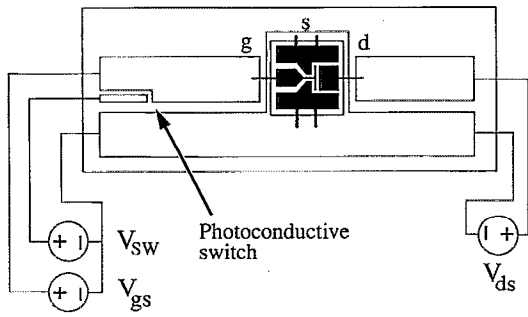
FIG. 1. Test fixture for electro-optic measurement, with metallic coplanar striplines fabricated on semiinsulating GaAs. The transistor is mounted in the center, with independent gate and drain bias. The photoconductive switch, activated by an optical pulse, sends a steplike signal to the gate input. The voltage on the coplanar lines is measured using an external electro-optic probe (not shown). Note that the drawing is not to scale.
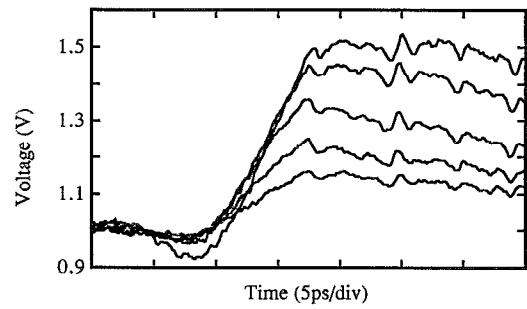

FIG. 2. Drain output signal for negative-going gate transient, corresponding to transistor switch-off. Response is shown for increasing gate step amplitudes of ΔV_g, $1.9\Delta V_g$, $2.7\Delta V_g$, $3.6\Delta V_g$, and $4.4\Delta V_g$, where ΔV_g is approximately -0.17 V. The switching time is 6.5 ps for a 0.42 V drain voltage swing. The dc operating point is $V_{ds}=1$ V and $V_{gs}=0.5$ V.

$In_{0.20}Ga_{0.80}As$ channel is grown on an undoped GaAs buffer layer, followed by 5 nm of undoped $Al_{0.25}Ga_{0.75}As$. This is delta doped at 5×10^{12} cm^{-2}, followed by growth of 30 nm of $Al_{0.25}Ga_{0.75}As$ doped 5×10^{17} cm^{-3} and 40 nm of GaAs doped at 5×10^{18} cm^{-3}; the dopant is Si. Mesa device isolation is used, and ohmic contacts are made with AuGe/Ni. The gate is defined using electron-beam lithography, and a gate recess is made using wet etching. The two-finger gate is 0.35 μm long, with a total width of 0.1 mm. Additional fabrication details are described in Ref. 16.

For characterization the wafer is lapped to 100 μm, and a single device is diced out and wire bonded in the common-source configuration in a coplanar stripline test fixture, as shown in Fig. 1. One bond is used for each of the gate and the drain, and two bonds are used for each of the two source pads; all are approximately 250 μm long. The test fixture is fabricated on semiinsulating GaAs to have an impedance of approximately 50 Ω. The coplanar stripline conductors are 50 μm wide, separated by a 5 μm gap. External power supplies allow independent control of the gate-source and drain-source bias.

The source of 100 fs optical pulses is a colliding-pulse mode-locked (CPM) dye laser.[17] One of the CPM output beams illuminates a photoconductive switch located 3 mm from the gate. By varying the switch voltage V_{sw}, the amplitude and sign of the gate transient can be controlled. The generated transient can be sampled at any point on the coplanar stripline using the second, delayed, CPM beam and an external electro-optic probe.[8,18,19]

The measured rise time of the input signal at the gate is 2.8 ps, which is due mainly to dispersion on the coplanar stripline between the photoconductive switch and the gate input. The subsequent decay of the gate input is much slower, because of the long lifetime of the semi-insulating GaAs used in the photoconductive switch. This time constant is 40 ps.

In Fig. 2 we show the drain output voltage, measured about 50 μm from the drain wire bond. The dc operating point of $V_{ds}=1$ V and $V_{gs}=0.5$ V is chosen to make the transistor conducting. The gate transient for the curves

shown in Fig. 2 was *negative*, which reduces the drain current and leads to a positive-going drain signal. The drain output is shown for a series of gate transients with increasing amplitude, obtained by varying the switch bias V_{sw}. The amplitude of the step at the gate input is ΔV_g, $1.9\Delta V_g$, $2.7\Delta V_g$, $3.6\Delta V_g$, and $4.4\Delta V_g$, where ΔV_g is approximately -0.17 V. From Fig. 2 we see three main features in the drain response. The first is a small negative-going transient, occurring just before switching occurs. This precursor is followed by switching of the transistor; a drain output transient of 0.5 V is created for the largest gate input amplitude. Finally, after switching, the drain voltage decreases slowly, due to the slow decrease of the gate input signal.

The 10%–90% switching time in Fig. 2 is $\tau_s=6.5$ ps. To compare the large-signal switching time to the value expected from small-signal characterization, we used a network analyzer to measure another transistor on the same wafer, before thinning, and found $f_t=71$ GHz. From this, the rise time can be estimated using $\tau_s=2.2/2\pi f_t$ to be $\tau_s=5$ ps, which compares very well with the measured large-signal value. However, the measured dc transconductance g_m of the device in the test fixture is 175 mS/mm. The ratio of drain and gate step amplitudes in the time-resolved data confirms this value of g_m. This transconductance value is significantly lower than the 680 mS/mm for the device measured by network analyzer, and would be expected to increase the switching time; the reason it does not is not understood.

In addition to the rapidity of the drain voltage switching, another interesting feature seen in Fig. 2 is the negative-going precursor to the switching signal. Such a precursor is generally undesirable in digital circuit applications because it increases the gate delay, and causes increased crosstalk between adjacent circuits. From Fig. 2 we see that the magnitude of the precursor varies nonlinearly with the magnitude of the gate transient, increasing for the largest gate input amplitude in Fig. 2. We have also observed that the magnitude of the precursor depends strongly on the operating point. To illustrate this, we present in Fig. 3 the drain output signal for drain-source biases of 0.4, 1.0, and 1.5 V. The gate input signal ampli-
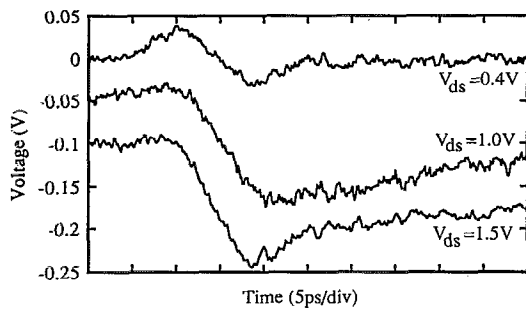
FIG. 3. Drain output signal as a function of drain-source bias, for a positive-going gate step corresponding to transistor switch-on. The dc drain bias has been subtracted from each curve, and then the curves are offset by 50 mV. The curves correspond to drain-source biases of 0.4, 1.0, and 1.5 V, as labeled; for all curves $V_{gs}=0.5$ V. The gate step amplitude is 0.16 V.

tude is constant, and the dc gate bias V_{gs} is 0.5 V. For Fig. 3, the gate transient is *positive*, which turns the transistor on, and creates a negative-going drain signal. To allow comparison between the transient parts of the signals, the dc drain bias has been subtracted from each curve; the curves are then offset by 50 mV. From Fig. 3 we see that the drain transient is qualitatively different for different operating points and is accompanied in this case by a positive-going precursor. For a drain-source bias of 1.0 V, we see a clean drain transient with a very small precursor, no overshoot, and a switching time of 6.9 ps. In contrast, for $V_{ds}=0.4$ V, the precursor is much larger. For $V_{ds}=1.5$ V, a significant overshoot is observed. It is interesting to note that in this case the switching time is reduced to 6.2 ps.

The precursor signal seen in Figs. 2 and 3 is due to the feedthrough of the gate input signal, which is coupled directly from the gate to the drain by the capacitance C_{gd}. For constant C_{gd}, the precursor is proportional to $C_{gd}[dV_g(t)/dt]$. We can understand the variation of the precursor seen in Fig. 3 in terms of the variation of C_{gd} with operating point. It is well known that as the gate-drain bias changes, the width of the depletion region between the gate and the drain is modified, also changing C_{gd}. For the gate-source bias used in Fig. 3, C_{gd} decreases for increasing drain-source bias. Therefore, by choosing the operating point $V_{ds}=1.0$ V, C_{gd} is greatly reduced, and the precursor is nearly eliminated, as seen in Fig. 3. The variation of the precursor seen in Fig. 2 for varying gate step amplitude cannot be interpreted with such a simple picture, because the capacitance C_{gd} changes significantly during the switching. This nonlinear capacitance can be modeled using nonlinear time-domain models of switching.[15] Such modeling is in progress.

In conclusion, we have presented a study of the large-signal switching response of an AlGaAs/InGaAs MODFET. The large-signal switching time was measured for both switch-on and switch-off, for various dc bias conditions. The fastest switching time measured was 6.2 ps. A transient on the leading edge of the drain output was observed, due to capacitive coupling of the gate signal to the drain, which can be eliminated by appropriate choice of

operating point. These results illustrate the capability of electro-optic sampling for study of very high speed active electronic devices. These techniques can easily be used for other high speed electronic devices such as heterojunction bipolar transistors. In addition, the high bandwidth of this technique means that as transistor performance continues to increase, this approach will remain applicable, even on a subpicosecond time scale.

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