Piece-wise Linear Model for Transmission Line with Capacitive Loading and Ramp Input

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***Abstract*— Transmission line effects become increasingly significant for on-chip high-speed interconnects. Efficient and accurate transmission line models are required for analysis and synthesis of such interconnects. In this paper we first present an efficient model for the far-end response of a single transmission line considering ramp input and capacitive loading. Our model divides the time axis into a number of regions according to the time of flight and the input rising time, and then approximates the far-end response by piece-wise linear waveform in each region. We name the resulting model as the PWL model. Experiments show that the waveform from the PWL model differs from the SPICE simulation result with the average voltage difference less than 0.9%Vdd, and the PWL model is at least 1000× faster than SPICE simulation. We further apply the PWL model to calculate the delay, rising time and oscillation amplitude of the coplanar waveguide (CPW) structure, and achieve less than 10% average error compared to SPICE simulation. Combining the PWL model and decoupling technique, we analyze the far-end response of bus structures and obtain waveform almost perfectly matching the SPICE simulation result.**

***Index Terms*— Transmission line, inductance, VLSI interconnect, interconnect modeling, signal integrity**

I. INTRODUCTION

Inductance effects in on-chip interconnects becomes increasingly important with smaller transition time and lower wire resistance (as a result of copper interconnect), especially in global interconnects such as clock tree, power/ground network, and parallel buses [1], [2], [3]. Significant inductance causes prominent transmission line effects such as overshoot and undershoot. To accurately analyze these phenomena, we need to model the high-speed interconnects by transmission line models. Because of the high integration level, these models need to be highly efficient for interconnect modeling and synthesis in VLSI designs.

Existing work on transmission line modeling can be divided into two types. The first type is numerical simulation, such as the convolution simulation [4], [5], state-based approach [6] and waveform relaxation techniques [7], [8]. Although these methods can provide accurate solutions, generally they are too time consuming for large-scale analysis. To improve the efficiency, reduced-order modeling techniques, such as asymptotic waveform approximation (AWE) [9], [10], Pade approximation [11] and Krylov subspace methods [12], have been proposed to model transmission lines with a finite number of poles of the transfer function. Although these methods can provide solutions more efficient than SPICE simulation, it is still time-consuming, if not impossible, to apply them in VLSI interconnect synthesis.

The second type of transmission line models is closed-form solutions. This type of solutions is usually much more efficient than numerical approaches and can be used for iterative VLSI interconnect synthesis. Based on two-pole approximation, [13] proposed a closed-form solution to the far-end delay and noise of a single transmission line with loading, but the model is unable to consider the distributed nature of transmission lines with limited poles and therefore is not accurate. Based on a series of modified Bessel functions, [14] and [15] provided an accurate closed-form solution for the far-end response of a single transmission line, but they only consider step inputs. Based on the reflection characteristics of the traveling wave in transmission lines, [16] proposed a traveling wave analysis (TWA) model for the far-end response of a single transmission line, but the model computes the waveform based on a three-pole model and an equivalent RC model, which may lead to significant errors as will be shown in section II of this paper. Based on the solution from [14], a recent work [17] provided a closed-form solution to the delay of the ramp response of an open-ended transmission line by linear approximation, but the model only works when the far-end rising time is less than twice of the time of flight. In summary, none of the existing efficient models [13]-[17] consider both ramp input and loading capacitance with high accuracy.

To meet the demand of a fast and accurate transmission line model for large-scale on-chip interconnect synthesis, in this paper we provide an efficient model for the far-end response of a transmission line considering both capacitive loading and ramp inputs. This model divides the time axis into a series of regions according to the time of flight and input rising time, and then approximates the responses by piece-wise linear (PWL) waveform. We name this model as the PWL model. Experiments show that the waveform computed by the PWL model matches the SPICE simulation result with an average voltage difference less than 0.9% and the model is at least 1000× faster than SPICE simulation. We further apply the PWL model to compute the delay, rising time and oscillation at the far end of coplanar waveguide (CPW) structures and achieve less than 10% average error compared to SPICE simulation. Compared to the existing methods [14] and [16], it reduces errors by 80% on average with similar or shorter runtime. Then, with the decoupling model proposed in [18], we apply the PWL model to analyze the far-end response of bus structures. The waveform derived from the

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TABLE I
NOTATIONS

R	total wire resistance
L	total wire inductance
C	total wire capacitance
R_d	driver resistance
C_L	loading capacitance
t_{ri}	input rising time
t_f	flight time of the original transmission line
t'_f	flight time of the transformed transmission line
t_{do}	delay at far-end
t_{ro}	rising time at far-end
V_i	input waveform
V_{o1}	voltage response at far-end with step input
V_{o2}	voltage response at far-end with ramp input

Fig. 1. A single open-ended transmission line.

PWL model almost perfectly matches those obtained from SPICE simulations.

The rest of the paper is organized as follows: In section II we present and verify the PWL model; In section III we apply the PWL model to analyze CPW structures and bus structures. We conclude the paper in section IV with discussion of future work.

II. Piece-wise Linear Model for Transmission Line

In this section, we present the piece-wise linear (PWL) model for a single transmission line. The PWL model includes three steps: 1. Transform the transmission line to a new transmission line without loading capacitance based on moment matching; 2. Construct the step response based on the piece-wise linear assumption and the solution to an open-ended transmission line from [14]; 3. Derive the ramp response based on the step response from step 2.

We first briefly review the solution for an open-ended transmission line presented in [14], and then discuss the PWL model step by step in following subsections II-B to II-D. For clear explanation, in table I we summarize the notations used in this paper. Generally, we use subscript "i" for the notations related to the input, subscript "o1" for those related to the far-end step response, and subscript "o2" for those related to the far-end ramp response.

A. Accurate Solution for Open-ended Transmission Line

[14] proposed an accurate transient solution for a single open-ended transmission line with a linear driver as shown in Figure 1. The driver is modeled as a voltage source with a driver resistance, and input is assumed to be a step input. Using the inverse Laplace transformation, [14] first rigorously derived the accurate solution for an infinite long transmission line, and the transient voltage at the position x along the transmission line is

$$V_{inf}(x,t) = V_{dd}\frac{Z_0}{Z_0+R_d}e^{(-R/2L)t}u_0(t-x\sqrt{LC}) \times \left\{ \begin{array}{l} I_0\left(\sigma\sqrt{t^2-(x\sqrt{LC})^2}\right) \\ +\frac{1}{1-\Gamma}\sum_{k=1}^{k=\infty}\left(\frac{t-x\sqrt{LC}}{t+x\sqrt{LC}}\right)^{k/2} I_k\left(\sigma\sqrt{t^2-(x\sqrt{LC})^2}\right) \\ \cdot(4-(1+\Gamma)^2\Gamma^{k-1}) \end{array} \right\} \quad (1)$$

where the characteristic impedance of the transmission line $Z_0 = \sqrt{L/C}$, the reflection coefficient at the near end $\Gamma = (R_d - Z_0)/(R_d + Z_0)$, $\sigma = R/(2L)$, and I_k ($k = 0, 1, 2, \ldots$) is the kth order modified Bessel function.

Based on this solution and the reflection theory, the transient solution for an open-ended transmission line with a finite length ℓ is derived as,

$$V_{fin}(t) = 2V_{inf}(t) + 2V_{dd}\frac{Z_0}{Z_0+R_d}e^{-(R/2L)t}\sum_{n=1}^{q}\sum_{i=0}^{n}\sum_{j=0}^{\infty} \frac{n(n-i+j)!}{i!j!(n-i)!}(-1)^i\Gamma^(n-i+j)u_0(t-(2n+1)\ell\sqrt{LC}) \times \left\{ \begin{array}{l} \left(\frac{t-(2n+1)\ell\sqrt{LC}}{t+(2n+1)\ell\sqrt{LC}}\right) I_{i+j}\left(\sigma\sqrt{t^2-\left((2n+1)\ell\sqrt{LC}\right)}\right) \\ +\frac{1}{1-\Gamma}\sum_{k=1}^{k=\infty}\left(\frac{t-(2n+1)\ell\sqrt{LC}}{t+(2n+1)\ell\sqrt{LC}}\right)^{(i+j+k)/2} \\ \cdot I_{i+j+k}\left(\sigma\sqrt{t^2-\left((2n+1)\ell\sqrt{LC}\right)^2}\right)(4-(1+\Gamma)^2\Gamma^{k-1}) \end{array} \right\} \quad (2)$$

The solution in (2) is accurate, but it does not consider loading or input rising time.

B. Consideration of Capacitive Loading

In this section, we consider the capacitive loading at the far end of the transmission line. As shown in Figure 2 we model the driver by a voltage source and a driver resistor, and the loading by a loading capacitor. The input can be either step input or ramp input.

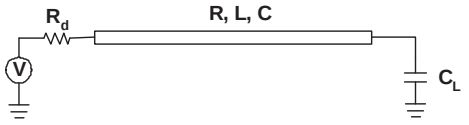

Fig. 2. Circuit model of a single transmission line.

Assuming the total resistance, capacitance and inductance for the transmission line are R, C and L as in Figure 2, the transfer function according to [19] is,

$$\begin{array}{rcl} H(s) & = & \frac{V_o(s)}{V_i(s)} \\ & = & \frac{1}{(1+sR_sC_L)\cosh(\theta)+(\frac{R_s}{Z_0}+sC_LZ_0)\sinh(\theta)} \\ & = & \frac{1}{1+\sum_{i=1}^{\infty}b_is^i}, \end{array} \quad (3)$$

where,

$$\begin{array}{rcl} \theta & = & (R+sL)sC \\ Z_0 & = & \sqrt{(R+sL)/sC} \\ b_1 & = & R_dC_L + \frac{RC}{2} + R_dC + C_LR \\ b_2 & = & \frac{LC}{2} + \frac{R^2C^2}{24} + \frac{R_dRC_LC}{2} + \frac{(R_dC+C_LR)RC}{6} + C_LL \end{array} \quad (4)$$

The time of flight of the transmission line is $t_f = \sqrt{LC}$. It is difficult to obtain the time-domain response by directly

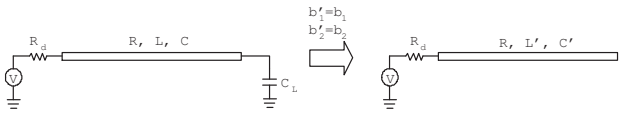

Fig. 3. Transformation to an open-ended line. (a) Original transmission line with loading. (b) Transformed transmission line without loading.

integrating the function (3) with the loading capacitance. However, (2) provides an accurate closed-form solution to a single open-ended transmission line. Therefore, we propose to transform the original transmission line with C_L (Figure 3(a)) to a new open-ended transmission line without C_L (Figure 3(b)). We match the transfer functions of the two transmission lines. More precisely we match the first two moments of the two transfer functions as shown in Figure 3. Assuming the C' and L' are the total capacitance and inductance of the open-ended transmission line after transforming, the transfer function of the transformed transmission line is,

$$\begin{aligned} H'(s) &= \frac{1}{\cosh(\theta')+\frac{R_s}{Z'_0}\sinh(\theta')} \\ &= \frac{1}{1+\sum_i b'_i s}, \end{aligned} \tag{5}$$

where,

$$\begin{aligned} \theta' &= (R+sL')sC' \\ Z'_0 &= \sqrt{(R+sL')/sC'} \\ b'_1 &= \frac{RC'}{2}+R_dC' \\ b'_2 &= \frac{L'C'}{2}+\frac{R'^2C'^2}{24}+\frac{R_dRC'^2}{6} \end{aligned} \tag{6}$$

To obtain C' and L', we match the first two moments of (3) and (5) by setting

$$\begin{aligned} b'_1 &= b_1 \\ b'_2 &= b_2 \end{aligned} \tag{7}$$

Therefore, we have

$$\begin{aligned} C' &= \frac{b_1}{R_d+\frac{R}{2}} \\ L' &= \frac{2\left(b_2-\frac{R^2C'^2}{24}-\frac{R_dRC'^2}{6}\right)}{C'} \end{aligned} \tag{8}$$

The time of flight of the transformed transmission line is,

$$\begin{aligned} t'_f &= \sqrt{L'C'} \\ &= \sqrt{(LC+\frac{R^2C^2}{12}+R_dRC_LC+\frac{(R_dC+C_LR)RC}{3} \\ &\quad +2C_LL-\frac{R^2C'^2}{12}-\frac{R_dRC'^2}{3})} \end{aligned} \tag{9}$$

By matching the first two moments, we map the effect of C_L into C' and L'. t'_f can be viewed as the effective time of flight considering the loading capacitance. Normally $t'_f > t_f$, but when C_L and in turn C' is sufficiently large, t'_f calculated by (9) may be smaller than t_f. In this case, t'_f is not physically meaningful. Because of the large capacitive loading, the circuit is capacitively dominant. Naturally, when $t'_f > t_f$ we can just match the first moment and obtain,

$$\begin{aligned} & b'_1 = b_1 \\ \Rightarrow\ & C' = \frac{b_1}{R_d+\frac{R}{2}} \\ \Rightarrow\ & t'_f = \sqrt{C'L} \end{aligned} \tag{10}$$

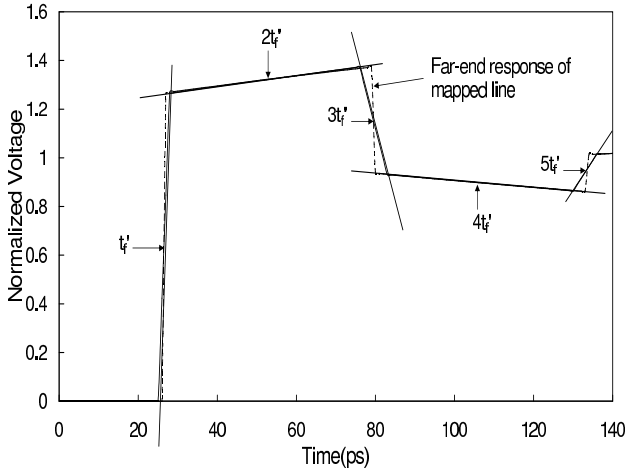

Fig. 4. Illustration of the PWL model.

L does not change in this special case, and because $C' > C$, $t'_f > t_f$ holds.

C. PWL Model for Step Response

The open-ended transmission line after transformation can be solved accurately by (2) originally developed in [14]. However, without the loading, the resulting waveform has steep risings at $t = (2n-1)t'_f$ $(n = 1, 2, 3, \ldots)$, which is not true with the loading capacitance present. Furthermore, it is not efficient to compute the entire waveform simply by time stepping as in [14]. Therefore, we develop a PWL model to approximate the waveform.

In the open-ended transmission line after transforming, the signal initiated at $t = 0$ from the driver is reflected at $t = (2n-1)t'_f$ $(n = 1, 2, 3, \ldots)$ at the far end. Correspondingly, the far-end response changes rapidly around these time points, but changes slowly between these points. Therefore, the time axis can be divided into a series of regions, $(0, t'_f)$, $(t'_f, 3t'_f)$, $(3t'_f, 5t'_f)$, $\cdots$ according to the time of flight. Two straight lines are used to approximate the response in each region: one line with a steep slope for the first rising/falling edge around $(2n-1)t'_f$ $(n = 1, 2, 3, \ldots)$, and the other line with a relative flat slope for the plateau waveform between $((2n-1)t'_f, (2n+1)t'_f)$ $(n = 1, 2, 3, \ldots)$. The lines for the rising/falling edges are determined by the voltages and slopes at $(2n-1)t'_f$, and the lines for the plateau waveforms are determined by the voltages and slopes at $2nt'_f$.

Our algorithm works as follows: We first compute the waveform voltages and slopes at nt'_f, $(n = 1, 2, 3, \cdots)$. Then we draw straight lines passing through these points with the calculated slopes. Finally, we obtain the crossing points of adjacent lines, and approximate the waveform by connecting these crossing points. Figure 4 illustrates the process.

In the following, we explain how to compute the voltages and slopes at nt'_f $(n = 1, 2, \ldots)$ for the PWL model. Without losing generality, we assume input signal rises from 0 to Vdd. In Figure 5, we illustrate the computation of the slope at t'_f. At this time point, the voltage rises from 0 to $V_{o1}(t'_f + \delta)$, where δ is a small quantity of time and chosen to be $0.001t_f$ in our model. Because of the loading capacitance, the rising of the

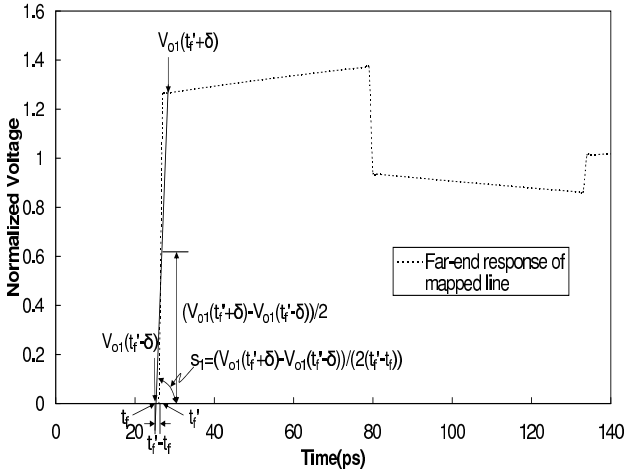

Fig. 5. Computation of the slope and voltage at t'_f.

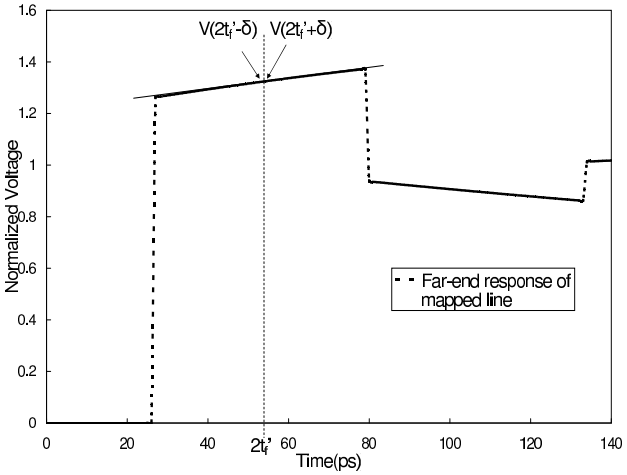

Fig. 6. Computation of the slope and voltage at $2t'_f$.

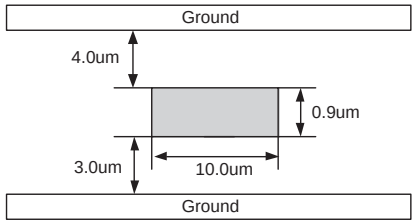

Fig. 7. Transmission line structure used in experiments

voltage is not steep but slower with a finite slope. To determine the slope, we approximate the time when the voltage reaches the 50% of the amplitude of the voltage rise by t'_f, which is the effective time of flight with the loading. Physically the signal reaches the far end at time t_f, which is the real time of flight of the transmission line and the starting point of the voltage rise. Therefore, we obtain the slope at t'_f as

$$s_1 = \frac{\frac{V_{o1}(t'_f+\delta)}{2}}{t'_f - t_f} = \frac{V_{o1}(t'_f+\delta)}{2(t'_f - t_f)}. \tag{11}$$

where the voltage $V_{o1}(t'_f+\delta)$ is computed by the formula from [14]. The voltage at t'_f is approximated by half of the rise as

$$v_1 = \frac{V_{o1}(t'_f+\delta)}{2} \tag{12}$$

To solve the slope and voltage at $2t'_f$, we approximate the waveform in region $(t'_f, 3t'_f)$ by the response of the transformed open-ended line directly. As shown in Figure 6, by the finite difference method we solve the slope at $2t'_f$ as

$$s_2 = \frac{dV_{o1}(2t'_f)}{dt} = \frac{V_{o1}(2t'_f+\delta) - V_{o1}(2t'_f-\delta)}{2\delta}. \tag{13}$$

and the voltage at $2t'_f$ as

$$v_2 = \frac{V_{o1}(2t'_f+\delta) + V_{o1}(2t'_f-\delta)}{2} \tag{14}$$

In this case, the approximating line is the tangent line at $2t'_f$.

The slope at $3t'_f$ is computed in the similar way as that at t'_f. However, because the rapid voltage change at $3t'_f$ in the far-end response comes from the reflected wave which has traveled a round trip along the line, we approximate the time to reach 50% of the falling by $2(t'_f - t_f)$ instead of $(t'_f - t_f)$. Therefore, the slope at $3t'_f$ is

$$s_3 = \frac{\frac{V_{o1}(3t'_f+\delta)-V_{o1}(3t'_f-\delta)}{2}}{2(t'_f - t_f)} = \frac{V_{o1}(3t'_f+\delta) - V_{o1}(3t'_f-\delta)}{4(t'_f - t_f)} \tag{15}$$

and the voltage at $3t'_f$ is approximated by

$$v_3 = \frac{V_{o1}(3t'_f+\delta) + V_{o1}(3t'_f-\delta)}{2} \tag{16}$$

The rest of the regions are calculated in the similar fashion: Regions $((2n-1)t'_f - \delta, (2n-1)t'_f + \delta)$ are similar to the region $(3t'_f - \delta, 3t'_f + \delta)$, where the slope and voltage are

$$\begin{aligned} s_{2n-1} &= \frac{V_{o1}((2n-1)t+\delta)-V_{o1}((2n-1)t-\delta)}{4(t'_f - t_f)} \\ v_{2n-1} &= \frac{V_{o1}((2n-1)t+\delta)-V_{o1}((2n-1)t-\delta)}{2} \end{aligned} \tag{17}$$

Regions $((2n-1)t'_f, (2n+1)t'_f)$ are similar to the region $(t'_f, 3t'_f)$, where the slope and voltage are

$$\begin{aligned} s_{2n} &= \frac{V_{o1}((2n)t'_f+\delta)-V_{o1}((2n)t'_f-\delta)}{2\delta} \\ v_{2n} &= \frac{V_{o1}((2n)t'_f+\delta)+V_{o1}((2n)t'_f-\delta)}{2} \end{aligned} \tag{18}$$

After obtaining the slopes and voltages for all the regions, the PWL waveform is readily constructed from all the straight lines determined by these slopes and voltages.

To verify the PWL model, we compare the far-end responses from the PWL model with the results of SPICE simulation, [14] and [16]. The experiments are carried out on a transmission line with $R = 1.92m\Omega/\mu m$, $C = 0.302fF/\mu m$ and $L = 0.155pH/\mu m$. We obtain these parameters by assuming that the transmission line has the structure shown in Figure 7. The wire dimensions are the same as those in the redistribution layer (RDL) in TSMC $0.13\mu m$ technology [20], and R, L and C are extracted by FastHenry [21] and FastCap [22]. In SPICE simulations, the transmission line is modeled by uniform distributed RLC segments. Each segment is $5\mu m$ long. We experiment with different wire lengths, driver sizes and loading capacitances. We show an underdamped waveform in Figure 8 and an overdamped waveform in Figure 9 respectively. From the figures, the PWL model produces the best results that are very close to SPICE waveforms in

both underdamped and overdamped cases. The waveforms from PWL model deviate slightly from SPICE simulation results around the knee points because of the piece-wise linear property of the model. The waveforms from [16] deviate from the SPICE simulation results greatly. This is because the waveform construction in [16] is based on a three-pole model which is not a good approximation when the transmission line effects are significant. [14] gives better results than [16], but it still has large errors due to the lack of considering capacitive loading. To quantitatively compare the waveforms, we also compute the average voltage difference compared to SPICE simulation for the waveforms in figures 8 and 9 between $t = t_f$ and $t = 300ps$ (the voltage is 0V before $t = t_f$ and stable at Vdd after $t = 300ps$) and show the results in Table II. From the table the voltage difference of the PWL model is less than 0.9%Vdd which is at least $3\times$ smaller than those of [16] and [14].

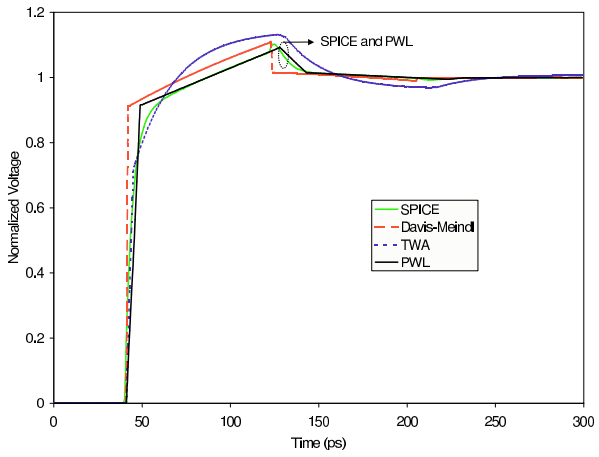

Fig. 8. Underdamped far-end waveform of a step input. $l = 6000\mu m$, $R_d = 16\Omega$, $C_L = 0.2pf$.

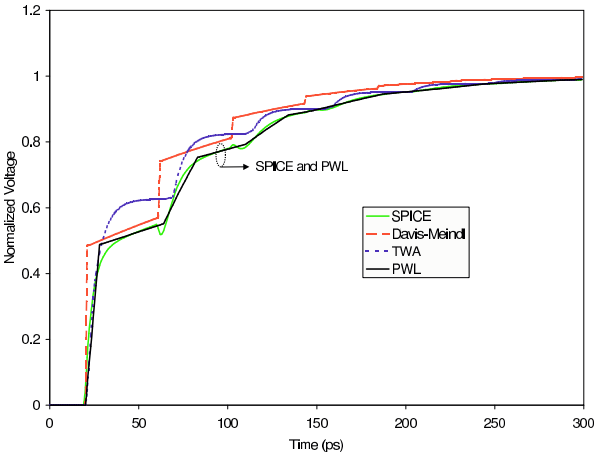

Fig. 9. Overdamped far-end waveforms of a step input. $l = 3000\mu m$, R_d=60Ω, $C_L = 0.2pf$.

D. PWL Model for Ramp Response

Based on the step response, we can further compute the ramp response with a finite rising time t_{ri}. As shown in Figure 10, the input waveform has two knee points at $t = 0$ and $t = t_{ri}$. Correspondingly, the far-end response waveform has knee points at $(2n-1)t_f$ and $(2n-1)t_f + t_{ri}$ $(n = 1, 2, 3, \ldots)$ as shown in figure 10. Therefore, according to the time of flight and input rising time, we divide the time domain into a series of regions with the boundary points of $(2n-1)t_f$ and $(2n-1)t_f + t_{ri}$, $(n = 1, 2, 3, \ldots)$ (The order of these time points depends on the detailed values of t_f and t_{ri}). Similar to the step response in section II-C, we approximate the waveform in each region with a straight line. Based on this observation, we construct the PWL waveform for a ramp input as follows: we first find the voltage and slope at the middle point of each region, and then approximate the waveform by a straight line passing through the point with the computed slope and voltage. The entire waveform is then approximated by connecting the crossing points of adjacent lines.

TABLE II

AVERAGE VOLTAGE DIFFERENCE IN %VDD.

Model	Fig.8	Fig.9
Davis-Meindl	0.025	0.013
TWA	0.030	0.027
PWL	0.009	0.004

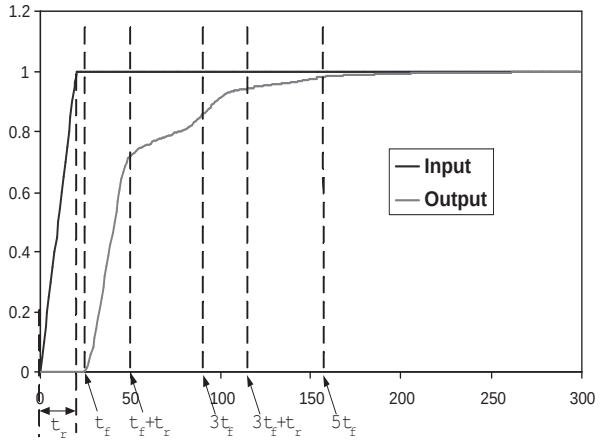

Fig. 10. Regions of ramp response

Following we explain how to compute the slopes and voltages for the ramp response. From the linear circuit theory [17], the ramp response can be computed from the step response by the following formula

$$\begin{aligned} V_{o2}(t) &= \int_{-\infty}^{\infty} V_{o1}(t)\frac{dV_i(t-\tau)}{dt}dt \\ &= \frac{1}{t_{ri}}\int_{t-t_{ri}}^{t} V_{o1}(t)dt \end{aligned} \tag{19}$$

where V_{o1} is the step response. Because we have already obtained the PWL waveform of the step response V_{o1} in section II-C, we can compute the slope and voltage efficiently without resorting to the Bessel function based formula (2). Taking the derivative of (19) on both sides, we obtain the slope of the ramp response at time t as

$$\frac{dV_{o2}(t)}{dt} = \frac{V_{o1}(t) - V_{o1}(t-t_{ri})}{t_{ri}} \tag{20}$$

Because $V_{o1}(t)$ is a PWL waveform, the integration in (19) can be computed easily as a sum and the voltage of the ramp

TABLE III
AVERAGE VOLTAGE DIFFERENCE IN %VDD.

Model	Fig.11	Fig.12
Davis-Meindl	0.064	0.059
TWA	0.059	0.072
PWL	0.005	0.002

response at time t is

$$V_{o2}(t) = \frac{1}{t_{ri}} \sum_{(t_i,t_{i+1})\subseteq(t-t_{ri},t)} \frac{V_{o1}(t_i)+V_{o1}(t_{i+1})}{2}(t_{i+1}-t_i) \quad (21)$$

where (t_i, t_{i+1}) is a linear piece in the PWL expression of $V_{o1}(t)$ in $(t - t_{ri}, t)$. Because of the simplicity of (20) and (21), the computation of ramp response from step response is extremely efficient. We compute the slope and voltage at the middle point of each region defined above, and then construct the ramp response with the straight lines determined by the slopes and voltages.

To verify the PWL model for ramp response, we compare the waveform from the PWL model with the results of SPICE, [14] and [16]. We carry out experiments on the same structure shown in Figure 7 in section II-C. We show an underdamped waveform in Figure 11 and an overdamped waveform in Figure 12. From the figures, the PWL model again produces the waveforms closest to the results of SPICE simulation in both cases. The waveforms from both [14] and [16] deviate from the results of SPICE simulation greatly due to both the lack of consideration of ramp input and the inaccuracy of the models discussed in section II-C. Table III shows the average voltage difference for different models. From the table the voltage difference of the PWL model is less than 0.5% Vdd which is much smaller than those of [16] and [14].

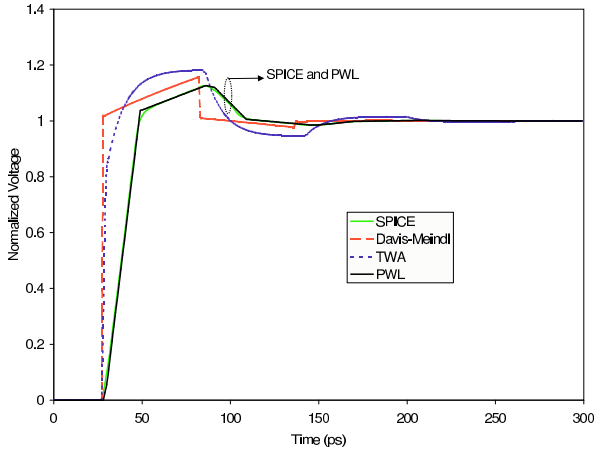

Fig. 11. Underdamped ramp response. $l = 4000\mu m$, $R_d = 15\Omega$, $C_L = 0.1pf$. Input rising time is $20ps$.

We further study the error margin introduced by the transformation from the original loaded transmission line to an open-ended line In figures 13, 14 and 15, we show the far-end rising time, 50% delay and oscillation amplitude computed from both SPICE and the PWL model with different loadings and wire lengths. The geometry of the wire is the same as in Figure 7. The unit of loading is the minimum inverter size. From

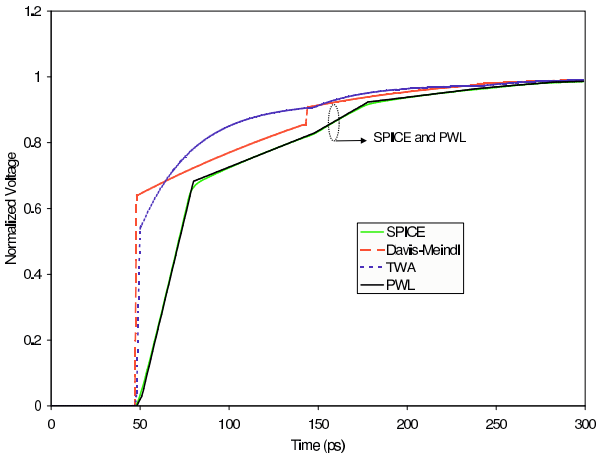

Fig. 12. Overdamped ramp response. $l = 7000\mu m$, R_d=30Ω, $C_L = 0.3pf$, Input rising time is $30ps$.

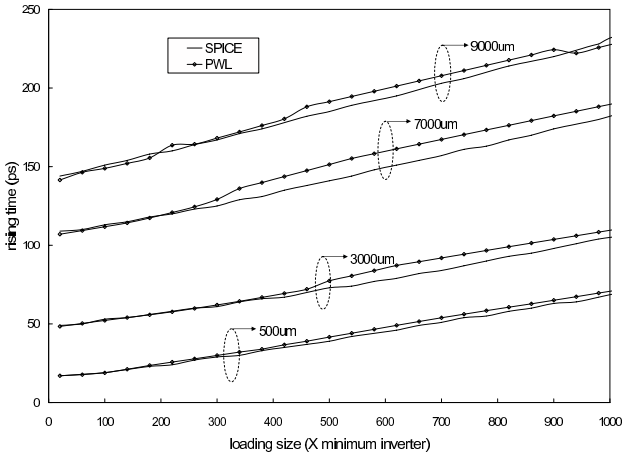

Fig. 13. Rising time for different loadings. $R_d = 30\Omega$. Input rising time is $20ps$.

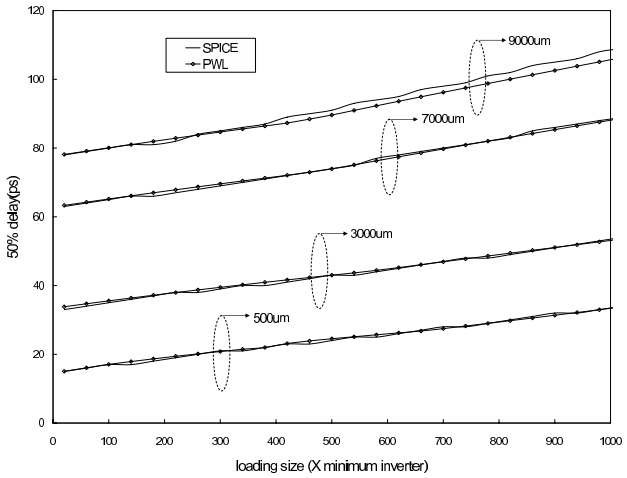

Fig. 14. Delay for different loadings. $R_d = 30\Omega$. Input rising time is $20ps$.

figures 13 and 14, it is clear that the model is highly accurate compared to SPICE in terms of rising time and 50% delay. The model has relatively larger error when the loading becomes larger. However, the maximum relative error is only 6.5%.

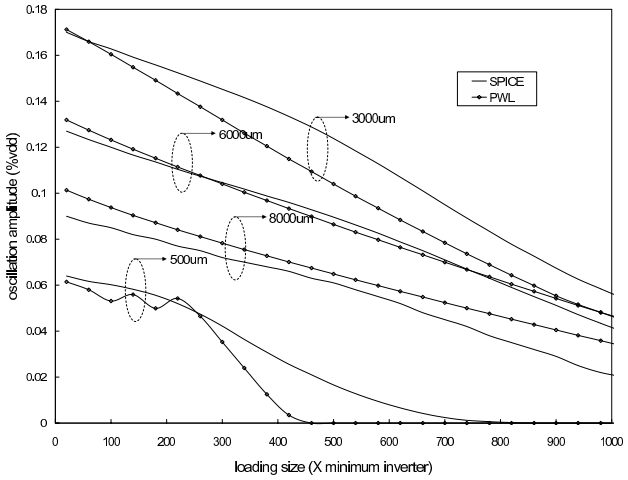

Fig. 15. Noise for different loadings. $R_d = 15\Omega$. Input rising time is $20ps$.

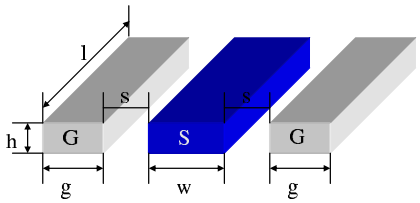

Fig. 16. Coplanar waveguide structure

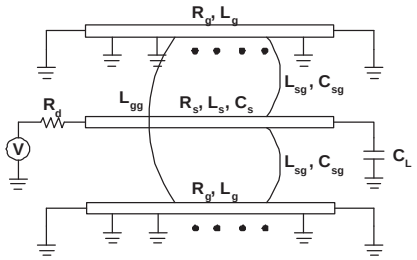

Fig. 17. Circuit model of coplanar waveguide

With regard to oscillation amplitude, the PWL model is highly accurate compared to SPICE when the loading is less than $300\times$, and the error is less than 10% according to Figure 14. When the loading becomes larger and the oscillation amplitude becomes smaller, the relative error increases. However, the maximum absolute error is less than 2% Vdd. Since the loading of an on-chip interconnect is normally smaller than $1000\times$ of the minimum inverter, the PWL model can be safely applied to model on-chip transmission lines with small errors.

III. Applications of PWL Model

In this section, we first apply the PWL model to analyze the coplanar waveguide (CPW) and then multiple coupled RLC lines sandwiched between two ground planes. We model the two interconnect structures by transmission lines and use the PWL model to solve the transmission lines. We compare the results with SPICE simulation under the distributed RLC circuit models for the two interconnect structures. Clearly the errors in the experiments include those from circuit modeling and the PWL model. This is different from the comparison in section II where an transmission line is assumed and no error of circuit modeling is considered.

A. Analysis of Coplanar Waveguide

1) Circuit Model: With increasing clock frequency, coplanar waveguide clock tree becomes common practice to overcome the issues of signal integrity. As shown in Figure 16, a coplanar waveguide (CPW) consists of a central signal wire (S) sandwiched between two grounded shielding wires (G), where l is the length of the wires, h is the thickness of the wires, s is the spacing between the signal wire and the shielding wires, and w and g are the widths of the signal wire and the shielding wire respectively. The CPW structure can be modeled by self and coupling parasitics as shown in Figure 17. R_s, C_s and L_s are the self resistance, ground capacitance and self inductance of the signal wire. R_g and L_g are the self resistance and inductance of the shielding wires. C_{sg} and L_{sg} are the coupling capacitance and coupling inductance between the signal wire and a shielding wire. L_{ss} is the coupling inductance between the two shielding wires. Such a model is complicated to analyze. Noticing that in a CPW structure most current on the signal wire returns from the shielding wires, we can assume all the current returns from the shielding wires and thus model the CPW as a single transmission line as shown in Figure 2 but with the parameters defined by the following effective loop parasitics [23], [17],

$$\begin{array}{rcl} R & = & R_s + R_g/2 \\ L & = & L_s - 2L_{sg} + \frac{L_{gg}}{2} + \frac{L_g}{2} \\ C & = & 2C_{sg} + C_s \end{array} \quad (22)$$

2) Calculation of Delay, Rising Time and Oscillation Amplitude: With the single transmission line model (22)-(22), we compute the far-end response of CPW structures with the PWL model. After obtaining the waveform, the delay, rising time and oscillation amplitude can be easily computed by linear interpolation. To achieve high efficiency, we do not need to compute the whole waveform. Instead, we take a need-based approach based on the PWL model. In this approach, a knee point is calculated only when it is needed by the computation. For example, the maximum overshoot will happen around $3t'_f$, so calculating the knee points up to $4t'_f$ is needed. Similarly, maximum undershoot will happen around $5t'_f$, thus we only need to calculate the regions up to $6t'_f$. To compute the delay t_{do} and the rising time t_{ro}, we just need to calculate the knee points till the voltage meet the corresponding bound, for example 90% for t_{ro}.

3) Runtime: The runtime of the PWL model is proportional to the number of linear segments computed. The most time consuming computation in the model is the calculation of the modified Bessel functions when construct the step response. Four points need to be computed based on the modified Bessel function for each region defined in section II. However, with the need-based procedure discussed in section III-A.2, we only need to calculate a few regions to obtain the delay, rising time and noise, thus the algorithm is very efficient as will be shown in the next section.

TABLE V

RUNTIME AND RESULTS FROM DIFFERENT MODELS. SPICE AND [14] CALCULATE UP TO $300ps$ BY TIME STEPPING ($1ps$/STEP).

Model		runtime (s)				50% delay (ps)				rising time (ps)				amplitude of oscillation (%Vdd)			
setting	type	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]
1	underdamped	88.10	0.01	0.01	0.18	24	25	25	24	10	8	9	6	4.6	4.5	9.2	5.1
2	overdamped	148.10	0.01	0.01	0.18	42	42	42	41	83	83	46	80	0	0	0	0
3	underdamped	368.23	0.01	0.01	0.12	83	84	83	80	58	56	48	48	8.6	8.9	10.3	8.8
4	overdamped	23.23	0.01	0.01	0.73	33	33	12	9	47	47	26	26	0	0	0	0
5	underdamped	121.39	0.01	0.01	0.20	55	55	39	38	26	26	10	1	4.6	5.2	11.3	8.0
6	underdamped	344.70	0.01	0.01	0.02	112	113	96	93	28	25	26	1	13.5	14.2	16.7	15.7

TABLE IV

SAMPLE EXPERIMENT SETTINGS (ALL GEOMETRIES ARE IN μm)

setting	l	w	s	g	$R_d(\Omega)$	$C_L(fF)$	$t_{ri}(ps)$
1	3000	6	1	4	30	45	0
2	5000	10	2	5	40	45	0
3	10000	8	2	8	24	90	0
4	1000	8	1	4	60	90	30
5	5000	10	2	10	24	45	30
6	10000	10	1	10	24	90	30

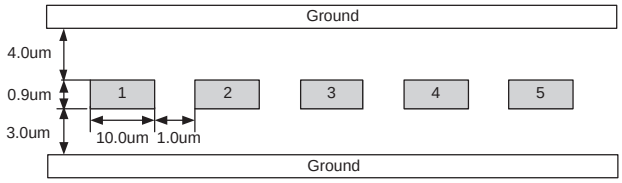

Fig. 18. Five coupled parallel transmission lines.

4) Experiments: We carry out a set of experiments to compare the runtime and accuracy of the PWL model to SPICE simulation and the efficient models [16] and [14]. In SPICE simulation, both the signal wire and the ground wires are modeled by uniformly distributed RLC segments. Each segment is $5\mu m$ long. The coupling between wires is model by mutual inductance and capacitance as shown in Figure 17. The wire thickness is $1\mu m$ in our experiments. We present some sample CPW structures in table IV and summarize the experiment results in table V. According to table V, both our model and [16] are at least $1000\times$ faster than SPICE, and [14] is about $100\times$ faster than SPICE. The error of the PWL model is less than 10% for delay and noise, and is less than 20% for rising time in the worst case. The PWL model sometimes obtains smaller rising time compared to SPICE simulation. This is because the time point of 90% Vdd happens to be around the knees. The error is normally less than 20% however. In contrast, both [16] and [14] can introduce significantly large errors in delay, rising time and oscillation amplitude. The PWL model reduces errors by 80% on average compared to [16] and [14].

B. Analysis of Multiple Coupled Lines

On-chip global buses are normally long and wide. Because strong inductive coupling exists between these wires, the signal integrity of such structures is a great concern in modern VLSI designs. Because a parallel bus can not be modeled as individual transmission lines due to the coupling between wires, we can not directly apply the PWL model to analyze the bus structure. However, with the decoupling technique in [18] we can transform multiple aligned lines to independent transmission lines, on which we can apply the PWL model. In this section, we combine this decoupling technique and the PWL model to analyze multiple coupled transmission lines. According to the transformation in [18], we first transform the coupled lines to the same number of decoupled lines with independent drivers and loadings, and then we analyze each decoupled transmission line with the PWL model, and finally obtain the response of the original coupled lines by linear combination of the responses of the decoupled lines.

We carry out experiments on a five-net structure shown in Figure 18. All the lines are aligned and identical with the same drivers and loadings. The length of the lines is $5000\mu m$ and the spacings between the lines are $1.0\mu m$. The driver resistance is 30Ω and the loading capacitance is $0.2pF$. The rising time of inputs is $30ps$. As an example, we show the result of one experiment in figures 19 and 20. In this example, line 2 switches from ground to Vdd, line 3 switches from Vdd to ground and all other lines are held to the ground at the near end. We compare the results from the PWL model with those obtained from SPICE simulations. In SPICE simulation, we model each transmission line with uniformly distributed RLC segments. Each segment is $5\mu m$ long. The coupling between wires is model by mutual inductance and capacitance. Figure 19 shows the responses of the two aggressor nets 2 and 3. The waveforms from the PWL model and SPICE simulation match so well that it is hard to distinguish them in the figures. Figure 20 shows the responses of victim nets 1, 4 and 5. The PWL model still well matches the overall waveform shape with small discrepancy. The model deviates a little from the SPICE simulation around the first knee due to the piece-wise linear nature of the model, but it captures the rising edges, oscillation amplitude and failing tails of the waveform almost perfectly.

IV. CONCLUSION

We have developed an efficient model for the far-end transient response of a single transmission line with capacitive loading and ramp inputs for high-speed on-chip interconnect analysis. The model divides the time axis into a number of regions according to the time of flight and input rising time, and approximates the response by piece-wise linear waveform. We call this model the PWL model. The waveform derived from the PWL model matches SPICE simulation result with the average voltage difference less than 0.9%Vdd. The PWL

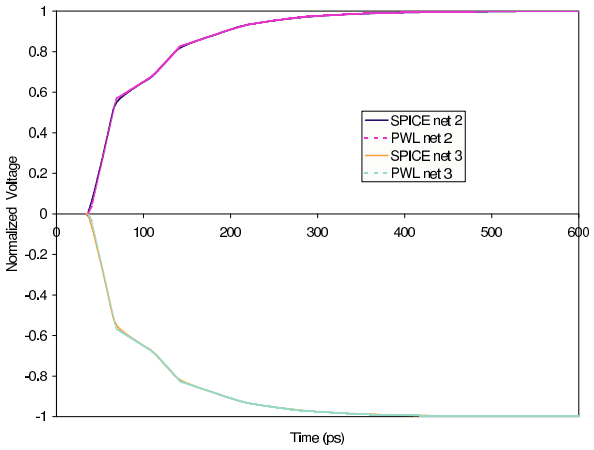

Fig. 19. Far-end response of aggressor nets 2 and 3.

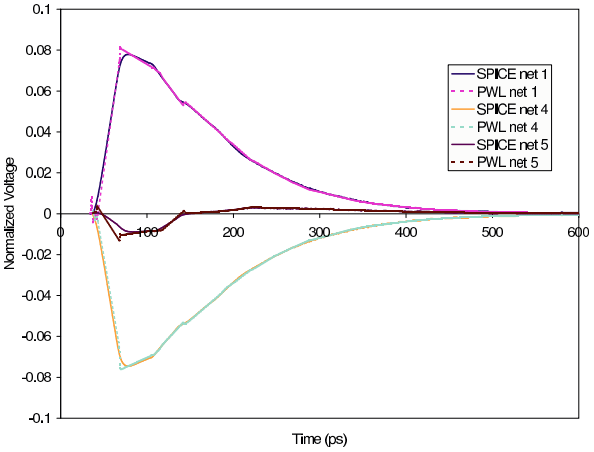

Fig. 20. Far-end response of victim nets 1, 4 and 5

model is at least 1000× faster than SPICE simulation. To the best of our knowledge, the PWL model is the first efficient transmission line model considering both loading capacitance and ramp inputs. We have further applied the PWL model to compute the delay, rising time and oscillation amplitude of the coplanar waveguide (CPW) structure. Experiments show the PWL model achieves less than 10% average error compared to SPICE simulation. Combining the PWL model and the decoupling technique, we also have computed the far-end responses of bus structures, and the resulting waveform almost perfectly matches the SPICE simulation result.

In this work we only considered capacitive loading. We will extend our model to consider more general terminations such as RC and RLC loading. Furthermore, we only considered linear drivers and receivers, but for on-chip applications the drivers and receivers are normally active devices. The nonlinearity of the devices will impact the accuracy of the model, and we plan to extend our model to consider the nonlinearity of drivers and loadings in our future work.

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