Alexandre Herculano Mendes Silva

Pipelined Analog-To-Digital Conversion Using Current-Mode Reference Shifting

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Orientador: Prof. Doutor João Carlos da Palma Goes

Júri:

Presidente:	Prof. Doutor Luís Augusto Bica Gomes de Oliveira
Arguente:	Doutor Michael Figueiredo
Vogais:	Prof. Doutor João Carlos da Palma Goes

FACULDADE DE
CIÊNCIAS E TECNOLOGIA
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Sumário

A arquitectura concorrencial é a mais popular em conversores analógico-digital (ADC *analog-to-digital converter*) que operam a elevada velocidade e média-alta resolução. Nesta arquitectura os circuitos de geração das tensões de referência são fundamentais. Estes são necessários para manter uma referência estável com uma baixa impedância para garantir que a carga dos condensadores em vários blocos do ADC evolua de forma rápida para o seu estado final. Normalmente, para se alcançar isto são necessárias soluções que consomem uma grande parte da energia e área. Na literatura as opções existentes para gerar uma referência estável dividem-se em ter *buffers* internamente e em ter condensadores externos ao chip com elevada capacidade. A utilização de *buffers* internos é a solução ideal para a integração do sistema mas requer um circuito com uma grande largura de banda e consequentemente uma elevada dissipação de potência. O uso de condensadores externos com elevada capacidade permite uma poupança energética significativa mas aumenta o número de componentes externos e o custo global do sistema. Para além disso, as oscilações causadas pelas ligações ao exterior do chip tornam esta solução pouco viável para conversores de alta velocidade.

Esta dissertação apresenta um ADC que utiliza um conversor digital-analógico multiplicativo realizado em condensadores comutados e modo de funcionamento em corrente. O circuito efectua a soma ou subtracção das referências com corrente evitando desta forma o uso de *buffers* de tensão. As correntes necessárias ao funcionamento deste bloco são geradas internamente com um circuito de geração de correntes que apresenta um baixo consumo energético.

O conversor proposto foi projectado numa tecnologia CMOS 65 nm e opera a frequências de amostragem entre 10 e 80 MS/s. Este funciona com uma tensão de alimentação de 1.2 V e dissipa um total de 10.8 mW a 40 MS/s.

Termos Chave

Conversor Analógico-Digital (ADC), Modo de conversão em corrente, condensadores comutados, corrente de referência, conversão A/D concorrencial.

Abstract

Pipeline Analog-to-digital converters (ADCs) are the most popular architecture for high-speed medium-to-high resolution applications. A fundamental, but often unreferenced building block of pipeline ADCs are the reference voltage circuits. They are required to maintain a stable reference with low output impedance to drive large internal switched capacitor loads quickly. Achieving this usually leads to a scheme that consumes a large portion of the overall power and area. A review of the literature shows that the required stable reference can be achieved with either on-chip buffering or with large off-chip decoupling capacitors. On-chip buffering is ideal for system integration but requires a high speed buffer with high power dissipation. The use of a reference with off-chip decoupling results in significant power savings but increases the pads of chip, the count of external components and the overall system cost. Moreover the amount of ringing on the internal reference voltage caused by the series inductance of the package makes this solution not viable for high speed ADCs.

To address this challenge, a pipeline ADC employing a multiplying digital-to-analog converter (MDAC) with current-mode reference shifting is presented. Consequently, no reference voltages and, therefore, no voltage buffers are necessary. The bias currents are generated on-chip by a reference current generator that dissipates low power.

The proposed ADC is designed in a 65 nm CMOS technology and operates at sampling rates ranging from 10 to 80 MS/s. At 40 MS/s the ADC dissipates 10.8 mW from a 1.2 V power supply and achieves an SNDR of 57.2 dB and a THD of -68 dB, corresponding to an ENOB of 9.2 bit. The corresponding figure of merit is 460 fJ/step.

Keywords

Analog-to-Digital Converter (ADC), current-mode reference shifting, switched-capacitor, CMOS current reference, pipelined A/D conversion.

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Chapter 1

Introduction

An increasing amount of analog and mixed signal circuits is found in mobile devices. They are an integral part of wireless communication systems, touchscreens, sensors, power management units and other analog/digital mixed signal applications needed to provide an enhanced user experience. As we are moving towards system-on-a-chip (SoC) solution, these circuits have to be integrated on a single chip with digital circuits in deep sub-micron CMOS technology. Low-voltage operation, low power dissipation and minimum silicon area are of great importance in the design of the system. Low power permits longer lasting battery operated devices, while small area directly relates to lower fabrication costs. The analog-to-digital converter (ADC) is of paramount importance in these analog/digital mixed signal applications. This block is used as an interface between analog circuits and digital sub-systems. The continuous scaling of CMOS technology allows smaller parasitic capacitance and consequently more power efficient and faster digital circuits. Typically, the performance and energy efficiency of the overall system are limited by the ADC.

1.1 Motivation

Among the different ADC architectures, pipeline ADCs are the most attractive solution for high-speed medium-to-high resolution applications. In a pipeline ADC the conversion is distributed through several stages. Each stage resolves n bits and produces a residual voltage to the next stage. By employing redundancy the accuracy requirements for the sub-ADCs are relaxed allowing low power comparators. The overall accuracy of the ADC is mainly limited by the errors of the multiplying digital-to-analog converter (MDAC) (i.e., the DAC inaccuracy and finite DC gain and bandwidth of the residues amplifiers). Due to the high accuracy requirements for the residue amplifiers they tend to dominate the power consumption. To address the issue of the power and complexity of residue amplifiers several techniques have been developed. Digital calibration techniques have been used to relax analog circuit requirements such as high gain, high bandwidth and linearity. This technique measures the errors introduced and compensates them in digital domain. The comparator-based design achieves low power by replacing the op-amps by a combination of a comparator and a current source. For low precision applications, parametric amplifiers are another alternative. These advances mean that designers must focus their attention to the reference voltage circuitry. This circuit is required to provide stable reference voltages for the ADC and comprises 20-30% of the overall power and area of the ADC. Actually the non-linearity and noise of these circuits appears as an error in the stages residues, degrading the overall ADC performance. A review of the literature shows that the required stable reference can be achieved with either on-chip buffers or with large off-chip decoupling capacitors. On-chip buffering requires power hungry buffers operating at high speed. The use of off-chip reference decoupling results in significant power savings but is not viable for high speed ADCs due to the ringing caused by the inductance of the package.

To address these challenges, a pipeline ADC employing a multiplying digital-to-analog converter (MDAC) with current-mode reference shifting is presented. The currents are generated on-chip by a switched-capacitor current reference circuit that dissipates minimal power. Moreover, this solution does not require extra pins and external components.

1.2 Thesis organization

Chapter 2 provides a background on ADCs. Some A/D converter architectures are reviewed with a special emphasis on pipeline ADC. Chapter 3 introduces the multiplying digital-to-analog converter with current-mode reference shifting and their design issues. Chapter 4 presents the circuit design of the Pipeline ADC. Chapter 5 presents the performance results of the proposed ADC. Finally, Chapter 6 summarizes the main conclusions.

1.3 Contributions

The main objective of this work is to demonstrate the use of the current-mode reference shifting MDAC circuit as an alternative to the traditional MDAC circuit. For this purpose, a 10-bit pipeline ADC using the proposed MDAC circuit is designed. The designed ADC precludes reference voltage buffers that dissipate a considerable amount of power, and off-chip decoupling capacitors.

The delay line with self-biased inverters described in this work has been used in the design of a ring oscillator with an accurate oscillation frequency. The circuit was published in an article submitted to the MIXDES, 18th International Conference, 2011, entitled *A Self-Biased Ring Oscillator with Quadrature Outputs Operating at 600 MHz in a 130 nm CMOS Technology* [1].

Chapter 2

Analog-to-Digital Converters

Analog-to-digital converters are used as an interface between analog and digital sub-systems, performing the transformation from continuous time and amplitude to discrete time and quantized amplitude. This chapter begins with an overview of some of the important performance parameters used for characterizing data converters. Next some A/D converters architectures are presented with a special emphasis in the pipeline architecture.

2.1 Ideal A/D Converter

An analog-to-digital converter (ADC) performs the quantization of analog signals into a number of discrete amplitude levels at discrete time points [2] . A basic block diagram of an A/D interface is shown in Figure 2.1.

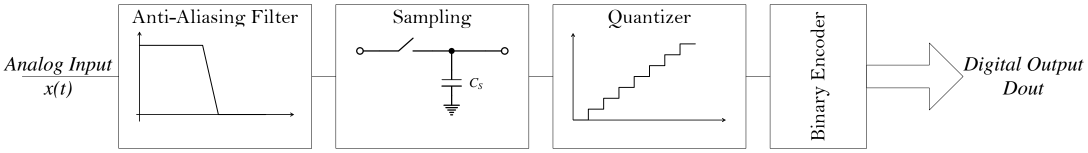


Figure 2.1: Block diagram of an A/D interface.

The analog input signal is band-limited to avoid ambiguity resulting from the sampling process. Signals sampled at a frequency outside one half of the sample rate are aliased so that they are indistinguishable from the signal itself. The sampler succeeding the anti-aliasing filter transforms a continuous time signal into its discrete time equivalent. The sampled signal is quantized in amplitude and encoded as a sequence of N bits. An ideal N-bit quantizer divides the full-scale (FS) into 2^N uniform quantization levels. The ideal quantization step corresponding to the least significant bit (LSB) of a converter is 1 LSB and is given by $1\,\mathrm{LSB} = \mathrm{FS}/2^N$. The full-scale range defines the maximum analog input range that can be quantized.

2.2 A/D Converter Specifications

An ADC is characterized through its static (DC) performance and its dynamic (AC) performance. High accuracy measurement ADC applications require very good static performance, whereas communications applications place much more emphasis on dynamic performance [3].

2.2.1 Static Specifications

The most important measures of static or DC-linearity of A/D converters are offset, gain errors, integral nonlinearity errors (INL) and differential nonlinearity errors (DNL). These properties actually indicate the accuracy of a converter and include the errors of quantization, nonlinearities and noise.

2.2.1.1 Offset and Gain Errors

An offset error changes the transfer characteristic so that all the quantization steps are shifted by the ADC offset. It may be measured in LSBs or as a percentage of full-scale. The gain error defines the deviation of the slope of a data converter from the expected value.

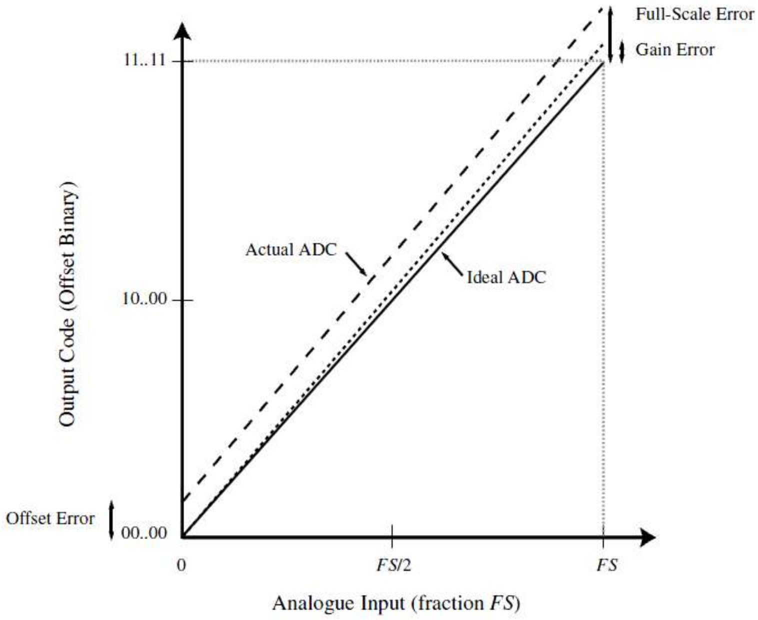


Figure 2.2: ADC gain and offset error characteristics [3].

2.2.1.2 Differential Non-linearity (DNL)

It is defined as the deviation of the step size of a non-ideal data converter from the ideal value of 1 LSB.

$$DNL_k = \frac{x_{k+1} - x_k}{\Delta} - 1, \quad i = 0, \dots, 2^N - 2 \tag{2.1}$$

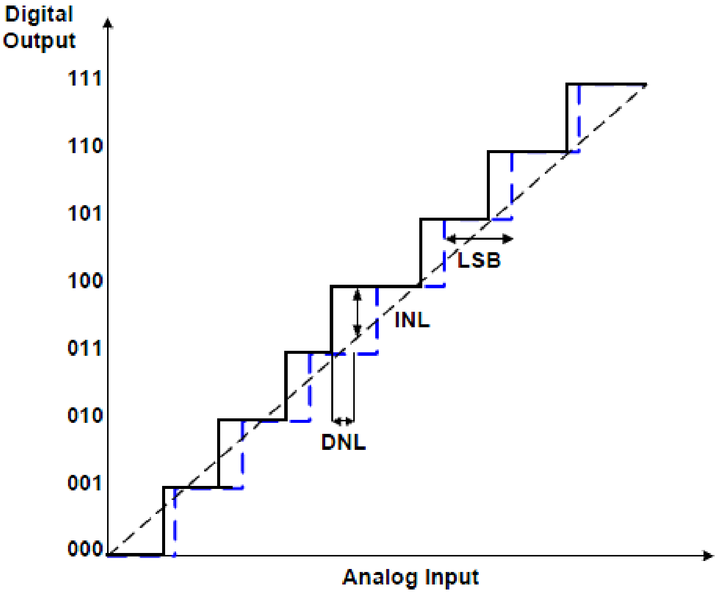

Digital
Output
111
110
101
100
011
010
001
000
LSB
INL
DNL
Analog Input

Figure 2.3: Transfer function for a 3-bit ADC.

2.2.1.3 Integral Non-linearity (INL)

The INL error refers to the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transitions after correction for offset and gain errors.

$$INL = \sum_{0}^{N-1} DNL_i \tag{2.2}$$

2.2.2 Dynamic Specifications

*2.2.2.1 Signal-to-Noise Ratio (*SNR*)*

Is the ratio between the power of the signal an the total noise produced by quantization and the noise of the circuit.

$$\mathrm{SNR}_{dB} = 10 \times \log\left(\frac{P_{signal}}{P_{noise}}\right) \tag{2.3}$$

The SNR is dominated by quantization noise and circuit thermal noise but also includes other noise sources.

*2.2.2.2 Total Harmonic Distortion (*THD*)*

The total harmonic distortion (THD) is the ratio between the harmonics of the input signal (only the significant harmonics) and the signal power.

$$\mathrm{THD}_{k} = 10 \times \log\left(\sum_{i=2}^{k} \frac{{A_i}^2}{{A_1}^2}\right) \tag{2.4}$$

*2.2.2.3 Spurious Free Dynamic Range (*SFDR*)*

Is the ratio of the root-mean square signal amplitude to the root-mean-square value of the highest spurious spectral component (ignoring the DC component). SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal (blocker).

$$\mathrm{SFDR} = 10 \times \log\left(\frac{A_1^2}{A_{spur}^2}\right) \tag{2.5}$$

2.2.2.4 Signal-to-Noise and Distortion Ratio

The definition is similar to that of the SNR, except that nonlinear distortion terms are also accounted for. The SNDR is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise (excluding dc).

$$\mathrm{SNDR}_{dB} = 10 \times \log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right) \tag{2.6}$$

As a function of SNR and THD, SNDR can be found by

$$\mathrm{SNDR}_{dB} = -10 \times \log\left(10^{-\mathrm{SNR}/10} + 10^{-\mathrm{THD}/10}\right) \tag{2.7}$$

SNDR is dependent on both the amplitude and the frequency of the signal. At low input levels, SNDR is limited by noise, while distortion dominates for higher signal levels.

*2.2.2.5 Effective Number of Bits (*ENOB*)*

Is a measure for quantifying the ADC performance like SNR and SNDR, but gives a better indication of ADC accuracy.

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}_{dB} - 1.76}{6.02} \tag{2.8}$$

2.2.3 ADC Figures of Merit

A figure of merit is a useful measure to compare the efficiency of different design solutions [4]. A commonly used FOM_{power} represents the used energy per conversion

$$\mathrm{FOM}_{power} = \frac{P}{2^{\mathrm{ENOB}} \cdot min\{f_s, 2 \times ERBW\}} \quad [pJ] \tag{2.9}$$

Where f_s is the sampling rate, ERBW is the effective resolution bandwidth and P is the total power dissipation.

2.3 Data Converters for Communications Applications

The ADC is a key component in digital communications systems. The resolution and sample rate of the A/D converter of a receiver depends on the target system and the topology and performance of the RF and baseband blocks. In applications like mobile TV and LTE the bandwidth is of the order of 4 MHz to 10 MHz and the ENOB required is in the range from 8-10 bits of resolution. In this case ADCs operating from 8 to 80 MS/s with 10-bit of resolution are often employed [5]. Other applications require an ADC width lower sample rate but higher resolutions (11-12 ENOB). The receiver architecture is usually Direct Conversion or Low-IF, with significant support of digital functionality to reduce the effect of circuit imperfections in the Analog/RF domain. A typical receive path used in these applications is shown in Figure 2.4 [6]. The RF modulated signal is converted directly to baseband where it is applied to the ADC and converted into a digital signal. The digitized signal is processed in the digital signal processing (DSP) block. A variable gain amplifier (VGA) preceding the ADC adjusts the signal power to optimize the dynamic range of the receiver and the ADC.

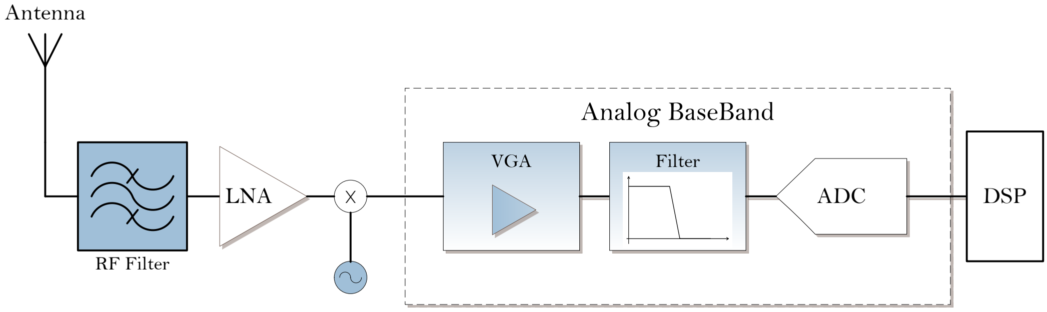


Figure 2.4: General block diagram for a wireless radio receiver.

The quantization and sampling process are performed at baseband by the ADC. According to the sampling theorem, the sample rate must be at least twice the signal bandwidth. However in some applications only a small part of the RF-band is of interest and the sampling is done at a fraction of the input frequency (sub-sampling). This can be done without corrupting the signal information because the Nyquist criterion has to be fulfilled only for the channel bandwidth rather than for the entire spectrum [7].

2.4 ADC architectures

There are several ADC architectures which are suitable for at least one or more performance specifications. For very low resolution, flash architecture is the best choice. The pipeline ADC is most suitable for low-power high-speed medium-to-high resolution applications.

2.4.1 Flash ADC architecture

The Flash ADC achieves a high conversion rate due its simple architecture. In an N bit flash ADC there are $2^N - 1$ comparators, each one detecting a single transition voltage. The reference voltages for the comparators are generated using a resistor ladder as shown in Figure 2.5.

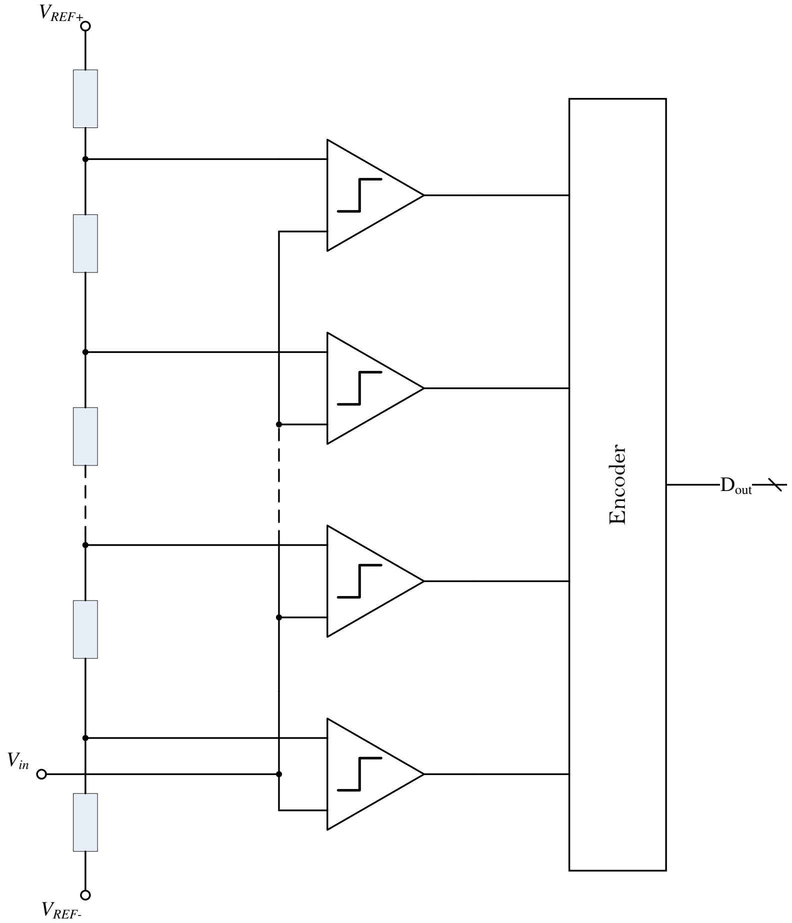


Figure 2.5: Flash ADC.

One drawback of flash ADCs is the fact that the number of comparators grows exponentially with the number of bits, which increases power dissipation and die area. That is why this architecture is typically employed in low resolution systems.

2.4.2 Pipeline A/D architecture

For medium-to-high resolution applications with input signal bandwidths larger than a few MHz, pipeline ADCs show speed and power advantages when compared to other architectures.

2.4.2.1 Architecture description

A general block diagram of a pipeline ADC is shown in Figure 2.6. It consists of an input sample-and-hold (S/H) followed by k low-resolution stages, delay elements for output synchronization, and a digital correction logic. The quantization process is distributed over several stages so that each stage converts only a subset of the total number of bits. The resolution-per-stage is a designer choice and has been subject of research. In most of the implementations available in literature a multi-bit pipelined stage is used in front-end and the back-end is designed with minimum resolution stages to reduce power dissipation.

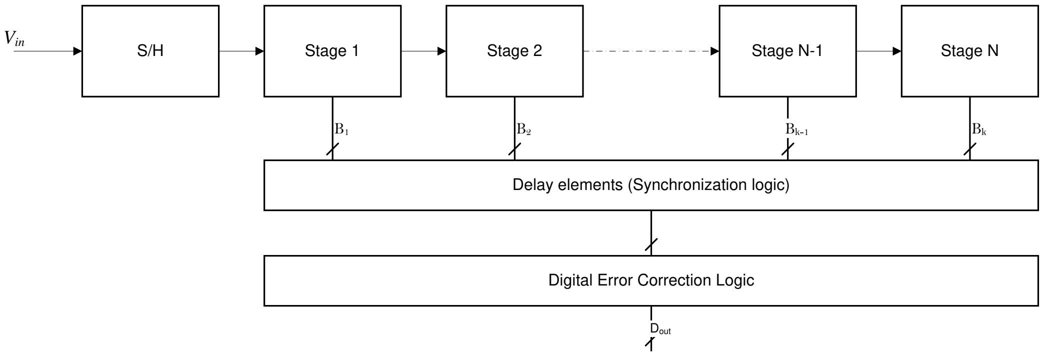


Figure 2.6: Block diagram of a generic pipeline A/D converter.

The generalized stage of a pipeline ADC is depicted in Figure 2.7. The analog input voltage is quantized by an *N*-bit low-resolution sub-analog-to-digital converter (sub-ADC) and converted back to analog by the sub-DAC. The analog voltage resulted from this operation is subtracted from the analog input signal and the resulting residue voltage is amplified by a gain stage with a gain nominally equal to 2^N. The S/H operation, the D/A conversion and the amplification are all performed by a single stage called multiplying digital-to-analog converter (MDAC).

The front-end S/H is an optional block used to ensure that the first-stage multiplying DAC and the first-stage sub-ADC sample the same input signal voltage. This is particularly important for very high frequency signals because the aperture error defined as $V_e = 2\pi f_{in} V_{ref}(\Delta\tau)$ is dependent of the input signal frequency.

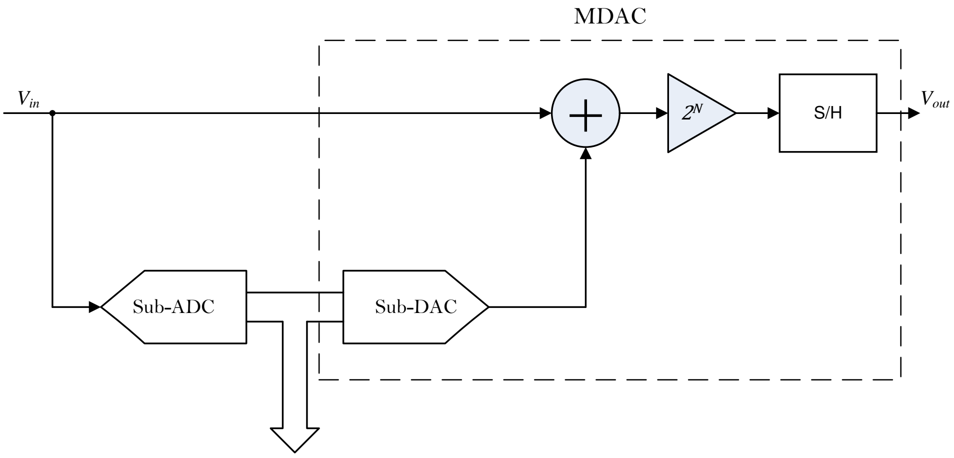


Figure 2.7: Block diagram of a generic stage in a pipeline ADC.

The most important non-idealities that deteriorate the performance of a pipeline ADC are noise, offset error, gain errors and settling errors. Gain errors in the MDAC are caused by the finite amplifier gain and capacitor mismatches. Thermal noise is mainly due to sampling switches and the sample-and-hold-amplifier. The main error source in the sub-ADC is the offset voltage of the comparators. A digital error correction algorithm known as redundant sign digit (RSD) coding is commonly employed to relax the accuracy requirements for the comparators of the sub-ADCs.

The pipeline ADC can achieve speed similar to that of the Flash ADC, but its latency is high. The number of components is approximately linear with the resolution. Table 2.1 summarizes the key tradeoffs of the flash and pipeline ADC architectures.

Notice that there are many other A/D architectures that rely on the MDAC building block. These are the two-step flash with residue amplification and multi-step algorithmic. Since they are out of the scope of this thesis, they will not be described here.

Table 2.1 Comparison of ADC architectures.

Architecture	Latency	Speed	Accuracy	Area
Flash	Low	High	Low	High
Pipeline	High	Medium-high	Medium-high	Medium

2.4.2.2 Time Alignment and Digital Error Correction

The digital outputs from each stage, generated at different time, are aligned by the time alignment circuit, and then move on to the digital correction stage. Figure 2.8 shows the synchronization logic for an *N*-bit pipeline ADC of 2-bit per stage. The logic is mainly composed of memory and shift circuits, such as flip-flops (FF). The digital outputs of the synchronization logic are time-aligned and they are ready for digital correction.

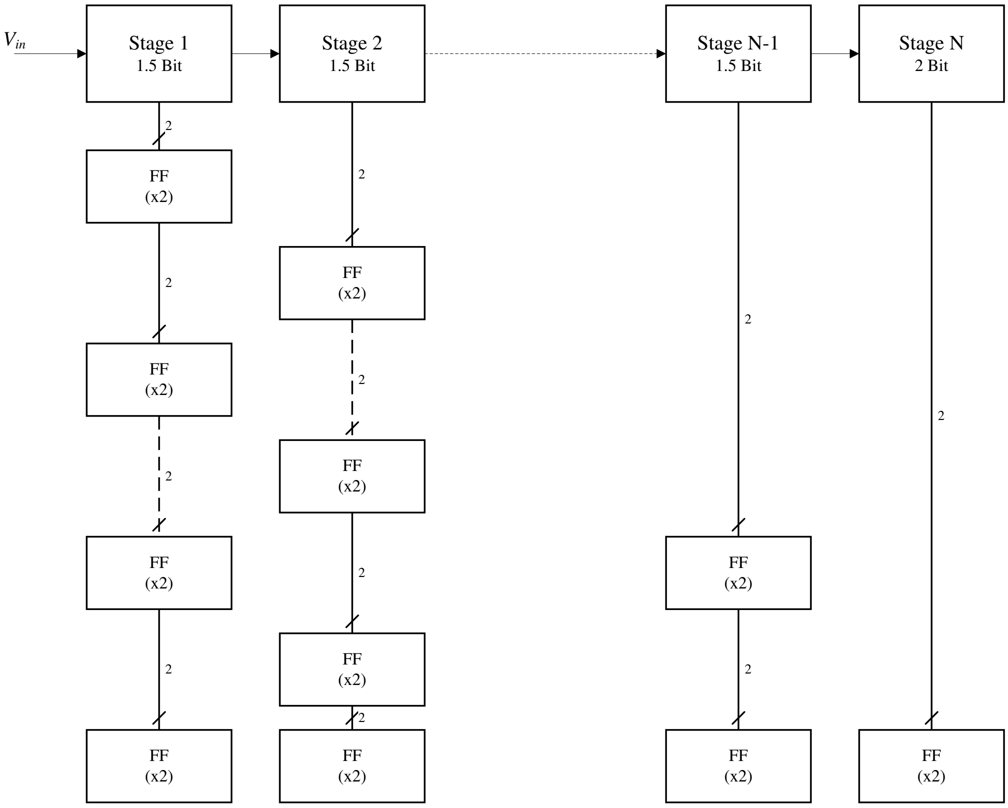


Figure 2.8: Pipeline ADC, synchronization and time-alignment logic.

Digital correction techniques are used to significantly reduce the accuracy specifications in the comparators used in sub-ADCs. For example, in 1.5-bit stage architecture the quantization errors can be large as $\pm V_{REF}/4$. Figure 2.9 shows the transfer function of a 1-bit stage. This architecture uses only a single comparator. The analog input has a maximum range defined from $-V_{REF}$ to V_{REF}. For an input that is less than zero the output bit is set to logic zero and for inputs greater than zero the output bit is set to logic one. The comparator offset results in the residue voltage exceeding the full-scale range. This means that the part of the transfer function that goes above V_{REF}, is either code saturated or it is flattened by the output stage of the OTA. The maximum offset of the comparator that can be tolerated has to be within the magnitude of a LSB.

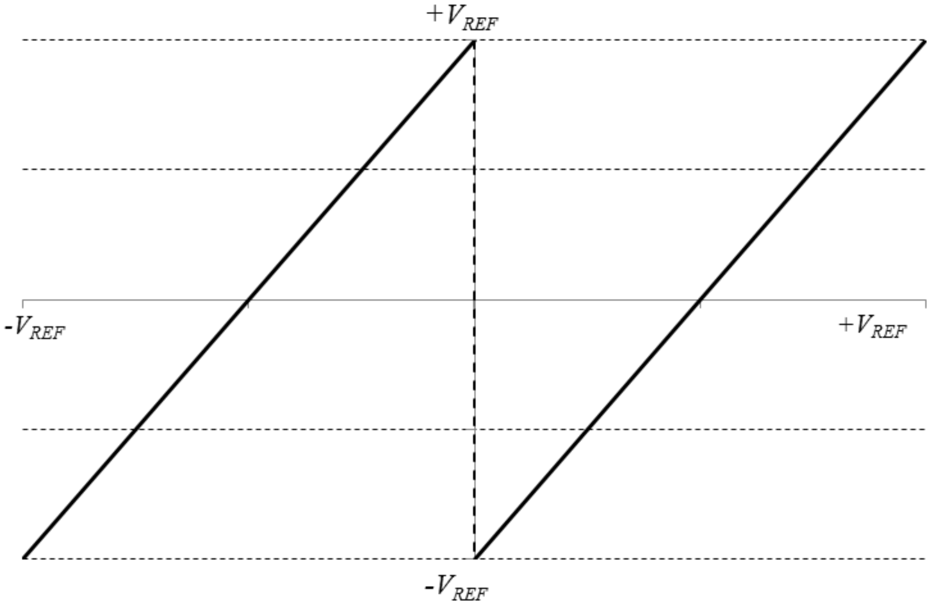


Figure 2.9: Transfer function of a 1-bit MDAC.

The non-idealities in the comparators can be corrected by adding a redundant bit. For example, a 1.5-bit stage has a true resolution of 1-bit and 0.5-bit redundancy. The new transfer characteristic has three segments that have to be coded by two digital outputs. The comparator decision levels are set to $-V_{REF}/4$ and $+V_{REF}/4$ as shown in Figure 2.10. The residue voltage stays in the input range of next stage provided the offset is within $\pm V_{REF}/4$. Note that the correction logic only corrects indecisions in the comparators. The errors caused by sub-DAC and amplifier are not compensated, and require more complicated digital calibration techniques.

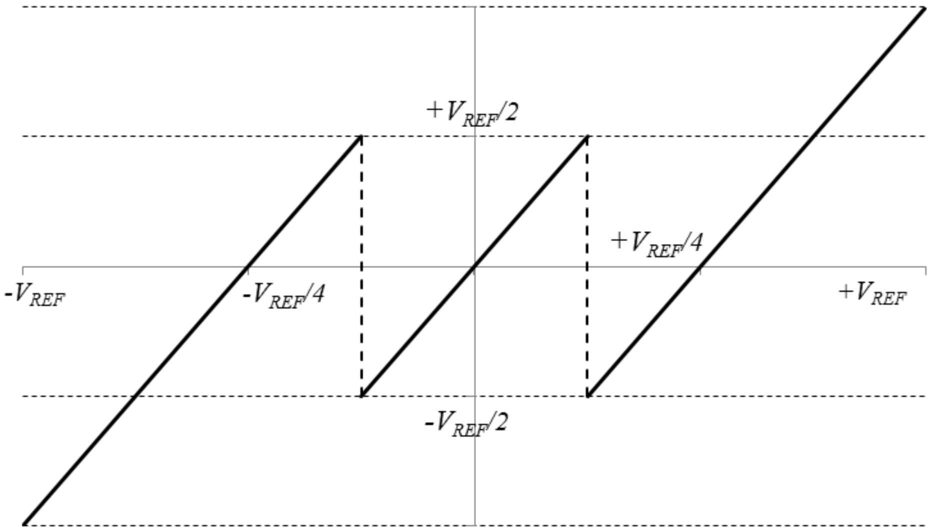


Figure 2.10: Transfer function of a 1.5-bit MDAC.

2.5 Building blocks of Pipeline Analog-to-Digital Converters

2.5.1 Opamp (OTA) circuits

2.5.1.1 Brief Review of Opamp topologies

Due to the complexity in the design, the OTA is the most important building block in the MDAC implementation. The finite DC gain and the bandwidth determine the settling accuracy of the closed–loop system.

The telescopic OTA is one of the most popular and fastest architectures offering a large bandwidth and good phase margin. However, due to the high number of stacked transistors the maximum output voltage swing is limited, making this architecture not suitable for low voltage applications. The output swing and common-mode range of the amplifier can be extended using either folding or mirroring techniques. In the current mirror architecture shown in Figure 2.11, the signal current is mirrored to an output stage through a cascode current mirror.

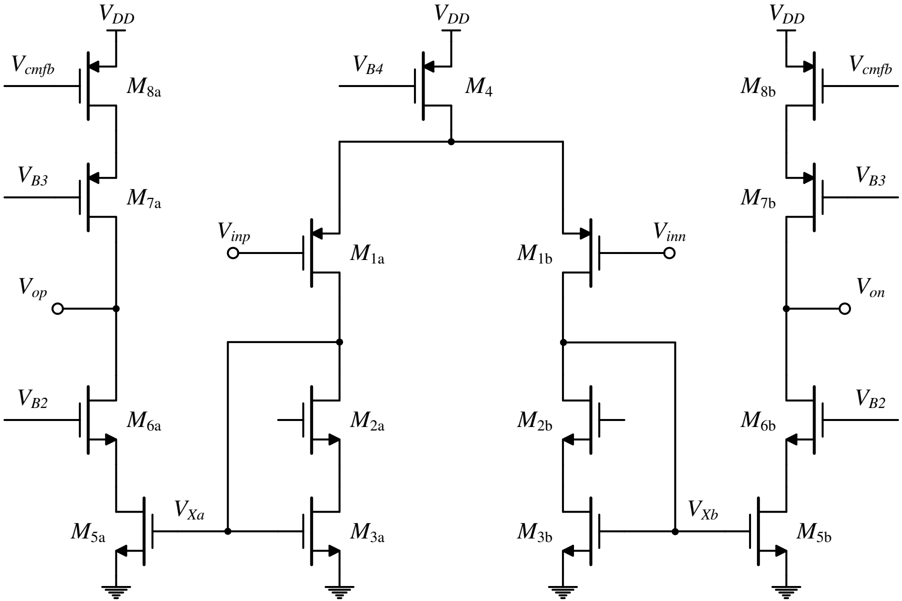


Figure 2.11: Class A Current Mirror OTA.

The DC gain, bandwidth and noise depend on the current-mirror ratio *K*, which is typically between one and four. A higher current-mirror ratio increases the efficiency but it also increases the parasitic capacitances, reducing the phase margin.

$$A = Kgm_1\{(gm_6ro_6ro_5) \parallel (gm_7ro_7ro_8)\} \tag{2.10}$$

The input referred noise is given by

$$v_{n,in}^2 = \frac{8kT\gamma}{gm_1}\left\{1 + \frac{gm_3}{gm_1} + \frac{gm_5}{K^2 gm_1}\right\} \tag{2.11}$$

The maximum output current available to charge or discharge the output load is limited to KI_B. Therefore the settling response is limited by slew rate, which is given by

$$\mathrm{SR} = \frac{KI_B}{C_L} \tag{2.12}$$

The large signal behavior of the class A current mirror OTA can be improved using an adaptive biasing technique. This can be achieved employing two flipped voltage followers (FVFs) connected at the source of M_{1a} and M_{1b} as depicted in Figure 2.12 [8].

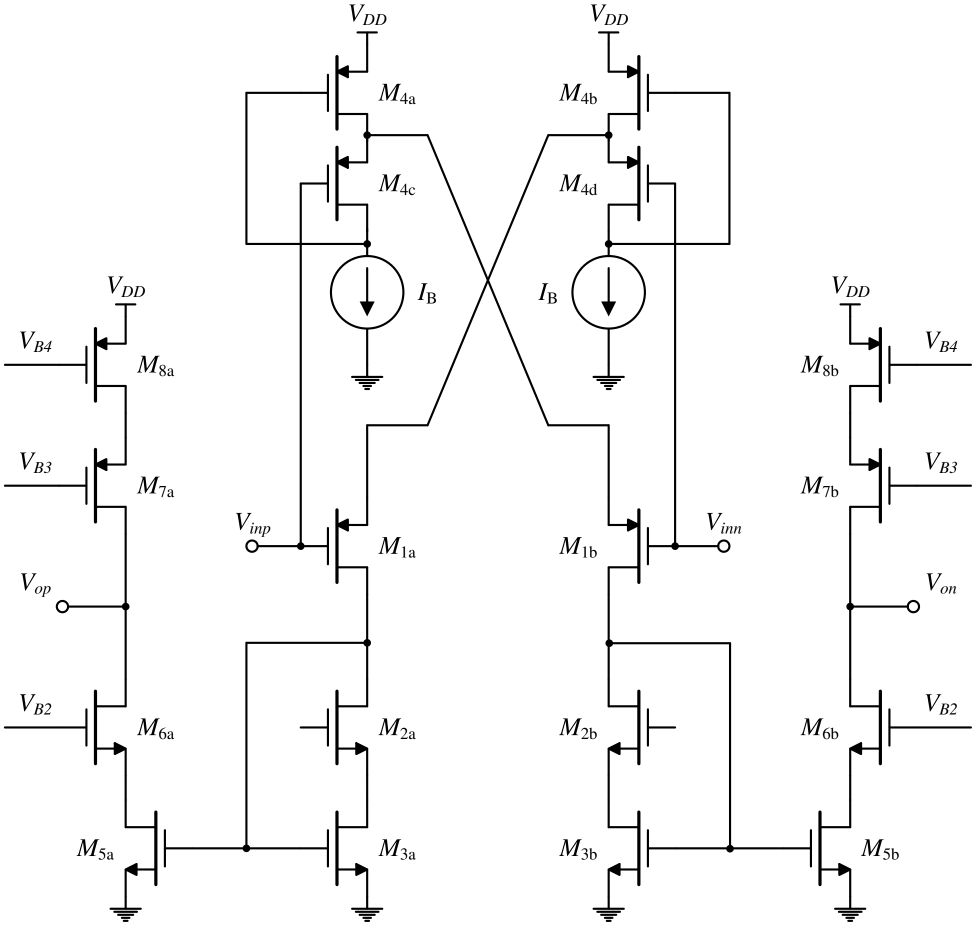

V_{DD}
V_{DD}
M_{4a}
M_{4b}
M_{4c}
M_{4d}
V_{DD}
I_B
I_B
V_{DD}
V_{B4}
M_{8a}
M_{8b}
V_{B4}
V_{B3}
M_{7a}
M_{7b}
V_{B3}
V_{inp}
M_{1a}
M_{1b}
V_{inn}
V_{op}
V_{on}
V_{B2}
M_{6a}
M_{2a}
M_{2b}
M_{6b}
V_{B2}
M_{5a}
M_{3a}
M_{3b}
M_{5b}

Figure 2.12: Class AB Current Mirror OTA.

The circuit provides low and well-controlled quiescent currents and boosts the current when a large voltage is applied. The small signal behavior is also improved being that the circuit presents a bandwidth twice higher of a class A stage.

2.5.1.2 DC Gain and Bandwidth requirements

The finite opamp gain causes discontinuities in the residue transfer function resulting in missing codes. The DC gain required to meet the desired resolution is given by

$$A > \frac{2^N}{\beta} \tag{2.13}$$

Bandwidth determines the settling accuracy of the MDAC for small-signal input signals. If the opamp is modeled as a single pole system, its step response can be expressed as

$$h(t) = h_0\left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.14}$$

The bandwidth required can be determined using the following equation

$$e^{-\frac{t}{\tau}} < \frac{1}{2^N} \tag{2.15}$$

Substituting $\tau = \frac{1}{\beta \mathrm{GBW}}$ and $t = \frac{1}{2fs}$ yields

$$\mathrm{GBW} > \frac{N \ln 2}{\beta\pi} f_s \tag{2.16}$$

The slope of the step response is proportional to the final value. Thus, for a large input step this means that the opamp should supply a larger current to the load [9] . However the opamp can supply only a finite current to the load capacitor. Consequently the output cannot change faster than the slew rate, which is given by

$$\frac{dV_{out}}{dt} = \frac{I_{SR}}{C_L} \tag{2.17}$$

Where C_L is the load capacitance and I_{SR} is the total available slewing current.

The minimum OTA slew rate to ensure no slewing occurs, is given by the initial slope of the linear settling response for the maximum expected step change.

$$\mathrm{SR} > V_{REF} \times \beta \times \mathrm{GBW} \tag{2.18}$$

2.5.2 Sampling switch

A simple sampling circuit consists of a switch and a capacitor as shown in Figure 2.13. To implement the switch a MOS transistor is operated in the triode region. When the MOS switch is closed the value of the on-resistance is in a range from a few tens of Ohms to a few kilo-Ohms. When the switch is turned off, it exhibits a resistance so high that is considered an open switch.

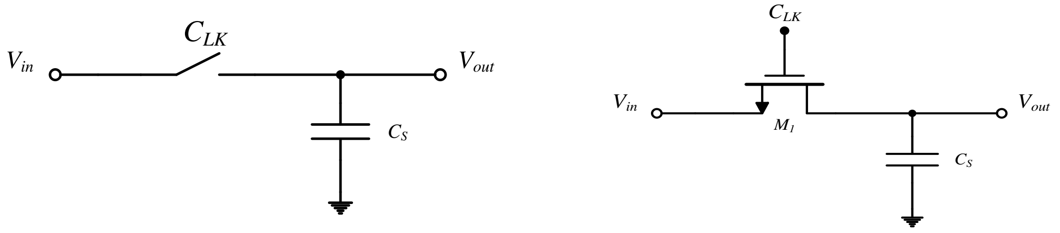


Figure 2.13: Simple sampling circuit. Implementation of the switch by a MOS device.

Neglecting second order effects the on-conductance is given by (approximation to the linear region:

$$G_{on} = \frac{I_D}{V_{ds}} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{tn}\right) \tag{2.19}$$

where μ_n is the mobility, W and L are width and length of the MOS transistor, respectively, C_{ox} is the gate oxide capacitance, and V_{tn} is the threshold voltage. Equation (2.19) shows that the MOS on-conductance is dependent on the input signal level which limits the allowable input signal swing. When the input voltage varies over a large range, a transmission gate consisting of a PMOS and NMOS transistor in parallel can be employed. However their on-resistance is still too high when track high speed signals. In these cases, switch bootstrapping techniques can be employed. In addition to the finite on-resistance, there are also parasitic capacitances associated with the MOS switch. This is illustrated in Figure 2.14. These non-linear junction capacitances can limit the sampling linearity, especially in high frequency applications.

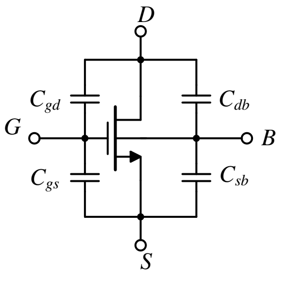


Figure 2.14: Capacitances associated with a MOS transistor.

2.5.2.1 Charge injection and clock feed-through

When a MOS device is on, a channel must exist and has a finite amount of mobile charge in its channel. When the transistor turns off, charge injection occurs and channel charge is dispersed into the source, drain and bulk terminals of device. The total charge in the inversion layer can be expressed by:

$$Q_{ch} = WLC_{ox}(V_{GS} - V_t) = C_G(V_{GS} - V_t) \tag{2.20}$$

where C_G is the total gate channel capacitance, V_{GS} the gate-source voltage and V_t the threshold voltage of the device. The charge injected on the source side is absorbed by the input source, while the charge distributed by the drain is deposited on the sampling capacitor C_S, introducing an error in the charge stored on the sampling capacitor.

In addition to channel charge injection, clock feed-through also occurs. When the gate swings from high to low, the MOS switch couples the clock transition to the sampling capacitor through its gate-drain overlap capacitance. This error can be expressed as

$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_S} \tag{2.21}$$

2.5.2.2 The bottom-plate sampling technique

A simple way to reduce signal dependent charge injection is the use of the bottom-plate sampling [10], illustrated in Figure 2.15. In sampling mode both MOS switches are conducting. At the sampling instant the $\emptyset_1$ goes down and switch M_2 turn off, which leaves node V_{out} floating. When M_1 turns off, the charge injection due to M_1 only distort the voltage on node V_{out}. Since this node floats after M_2 turns off, the total charge stored on C_S is not changed.

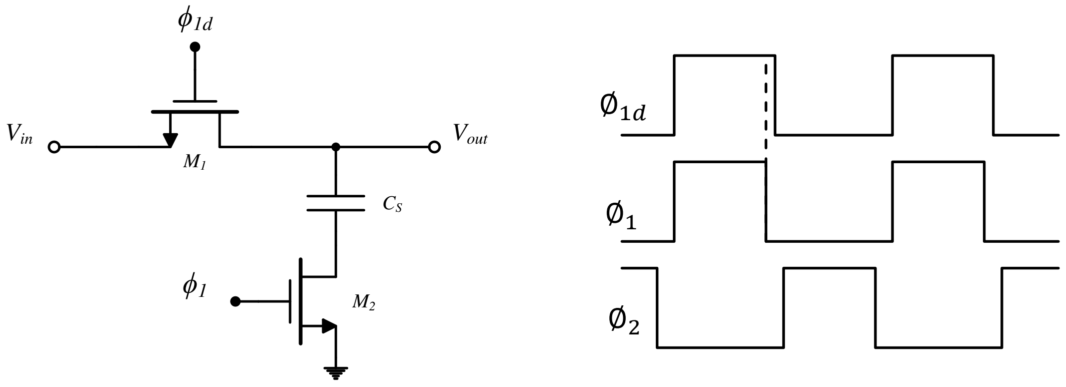


Figure 2.15: Bottom plate sampling.

2.5.2.3 Bootstrapped Switches

In high-speed low-voltage designs, the non-ideal behavior of the switches is a significant limitation. The non-linear voltage dependence of the switches on-resistance produces distortion [10]. One solution offered by some technologies to extend the signal range and reduce distortion is the low-threshold devices. However these devices suffer from leakage, which results in loss of the stored charge. Another way to reduce switch on-resistance and to extend the linear range is to employ a voltage higher than the supply to control the switches. This solution results in high stress voltages causing reliability problems. Switch boosting can still realized by making the gate voltage track the source voltage with an offset. With this approach, the circuit's long-term reliability is improved since the terminal-to-terminal voltages of the switch transistor never exceeds V_{DD} [11]. The method is conceptually illustrated in Figure 2.16.

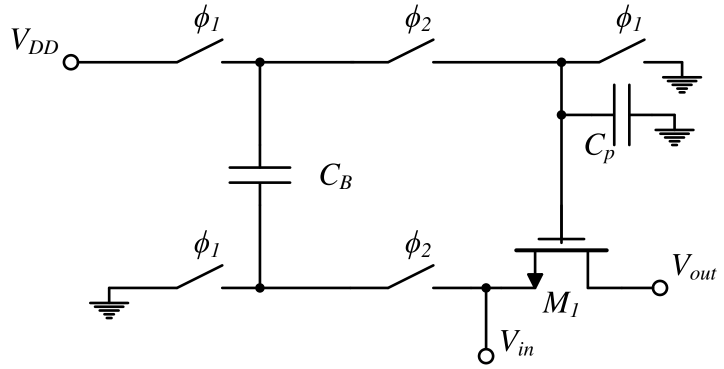


Figure 2.16: Conceptual scheme of switch bootstapping.

During the nonuse phase the gate of the switch is grounded and the capacitor C_1 is pre-charged to V_{DD}. In the ON state, this capacitor will act as a floating voltage source in series with the input signal making the gate voltage of the switch equal to V_{GS}=(V_{DD}+V_{in}). Actually the voltage at the gate of M_1 is lower than this ideal value due to charge sharing and is given by

$$V_{GS} = \frac{C_B}{C_B + C_p}(V_{DD} + V_{in}) \tag{2.22}$$

Figure 2.17 shows the conceptual output waveforms of the bootstrap circuit. A practical implementation of the bootstrapped switch is shown in Figure 2.18 [12].

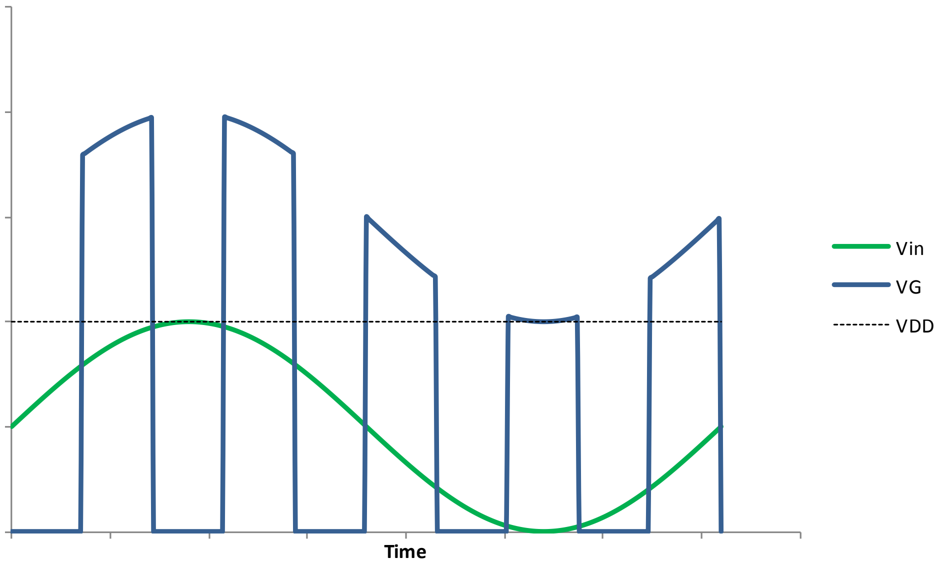


Figure 2.17: Conceptual bootstrap circuit output.

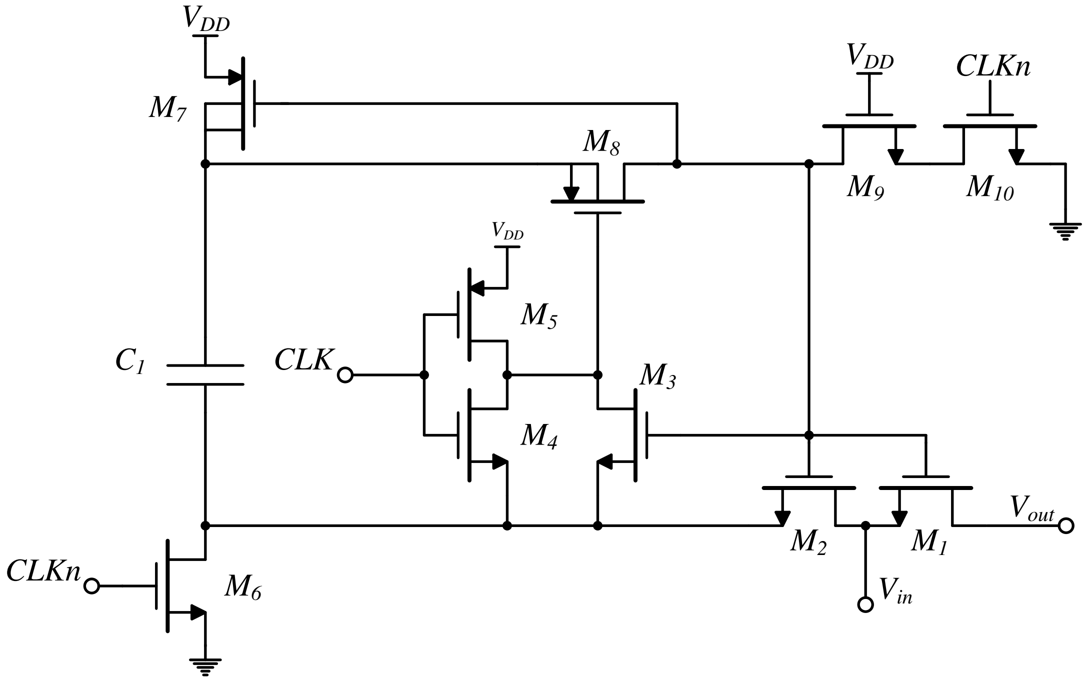
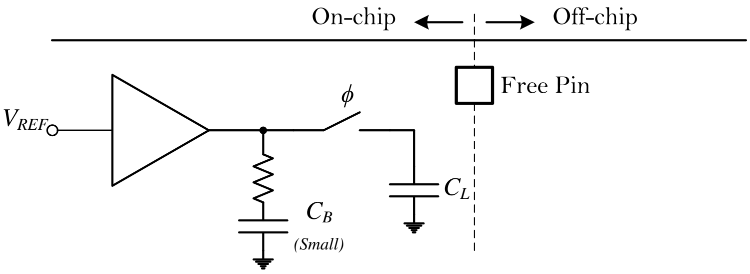

V_{DD}
M_7
M_8
V_{DD}
$CLKn$
M_9
M_{10}
V_{DD}
M_5
C_1
CLK
M_3
M_4
M_2
M_1
V_{out}
V_{in}
$CLKn$
M_6

Figure 2.18: Schematic of the clock boosting circuit [9].

2.5.3 Reference buffers

Reference buffers are essential building blocks in data converter systems. In a pipeline ADC these circuits generates the DAC reference voltages $\pm V_{REF}$ and define the input and output full-scale ranges. As with respect to other blocks like S/H and MDAC, this block determines the resolution achievable. Therefore, it is necessary to guarantee that these buffers settle to the same value every cycle to avoid distortion and inter-stage gain errors. There are in general two options to generate an accurate reference voltage. The first option is to have a high speed on-chip buffer. A second one is to have an on-chip weak reference buffer with external decoupling [13] . Table 2.2 describes and analyses the advantages and drawbacks of both approaches.

Table 2.2: Description of the advantages and drawbacks of commonly reference voltage circuits.

<table>
<tr><th>On-chip buffer with wide bandwidth</th><th>On-chip buffer with external decoupling</th></tr>
<tr><td>High speed buffer with high power consumption. On-chip low pass filter added at the output reference node to get low-noise reference [14]. The buffer requires dedicated supply pins.</td><td>Low bandwidth buffer with low power consumption. The external capacitor appears in series with the package inductance which causes ringing on the internal reference voltage.</td></tr>
<tr><td colspan="2">
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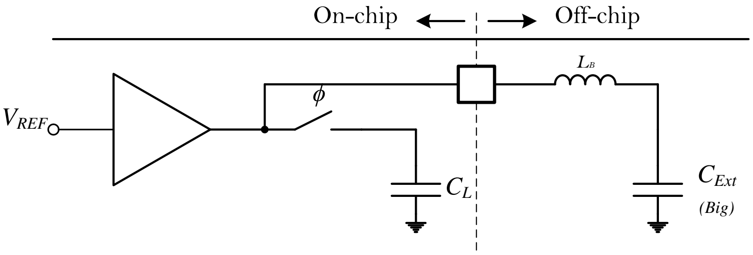
<tr><td colspan="2">
</td></tr>
</table>

Generally, commercial available ADCs use high speed buffers on-chip, since an internal reference with external decoupling capacitors increases the pad/pin count of the chip, the required number of external components and, consequently, the overall system cost.

2.6 Time-Interleaving ADCs

Time-interleaving ADCs provides an effective solution to increase the sampling rate of A/D interfaces [15]. By using parallel A/D converters, operating at a fraction of the full sample rate of the ADC, the overall sampling rate is increased to a value proportional to the number of ADC channels. Figure 2.19 shows the block diagram of an architecture in which four ADCs are used in parallel. The ADC in each time-interleaved path operates at a sample frequency of f_s/M as illustrated in the timing diagram shown in Figure 2.20.

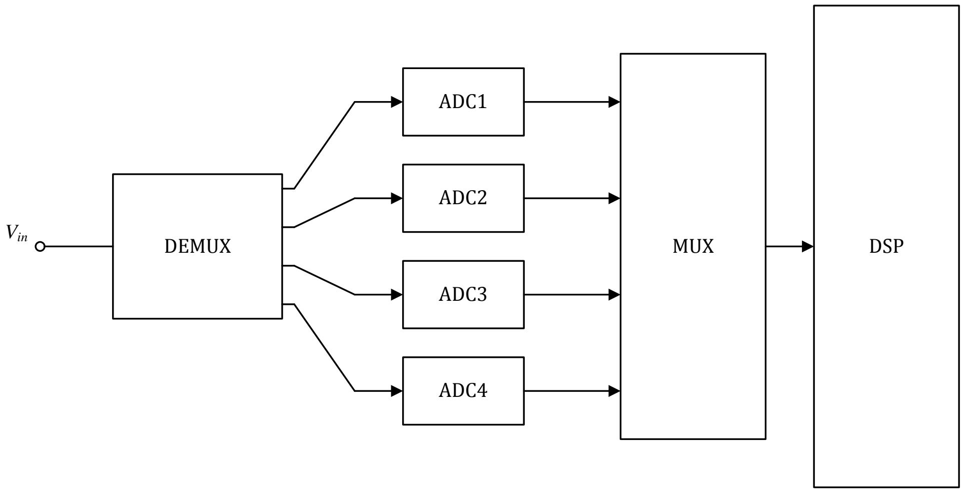


Figure 2.19: Four-channel time-interleaving ADC.

The performance of time-interleaving ADCs is seriously degraded by mismatch between ADC channels [16]. Offset, gain, timing and bandwidth mismatches of the ADC channels effectively modulate the input signal and introduce unwanted spectral tones. Those mismatch effects has been subject of intensive research and they have been fully characterized [17].

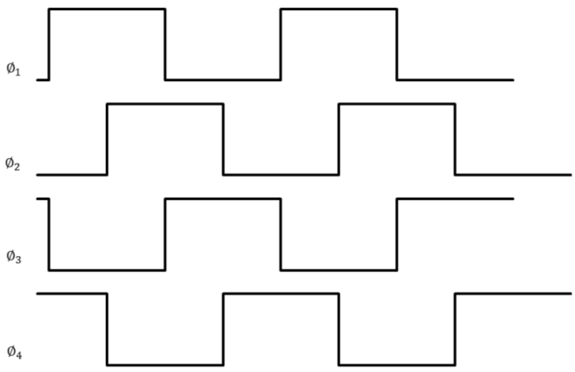


Figure 2.20: Timing diagram for a time-interleaved 4-Channel ADC system.

2.7 Summary

In this chapter some important metrics used for characterizing an ADC were presented. A brief review of the flash and pipeline ADC architectures were given. The architecture that achieves the largest conversion rate is the flash ADC. The pipeline ADC is most suitable for low-power high-speed medium-to-high resolution applications. Design techniques to generate reference voltages needed in any data converter system have been addressed.

Chapter 3

Multiplying Digital-to-Analog Converter with current mode reference shifting

The multiplying D/A converter (MDAC) is the main building block within a pipelined stage. It performs the D/A conversion, subtraction and amplification of the residue [17]. The non-linearity errors in the MDACs can produce a large number of missing codes in the overall conversion characteristic of the ADC [4]. Usually, these errors are minimized employing high gain and high unity gain bandwidth operational transconductance amplifiers (OTA) resulting in high power dissipation. As the OTA is one of the most critical parts in the design of a pipelined stage, several architectural advances have been done to relax their requirements and reduce power dissipation. These advances are leading the designers to focus their attention to the ADCs auxiliary circuitry such as the reference circuitry. These circuits are required to provide stable reference voltages that need to settle to the linearity of the ADC, in order to avoid distortion and inter-stage gain errors. In a traditional implementation of a pipeline ADC the reference circuitry comprises 20-30% of the overall power and area of the ADC as illustrated in Figure 3.1 [18] .

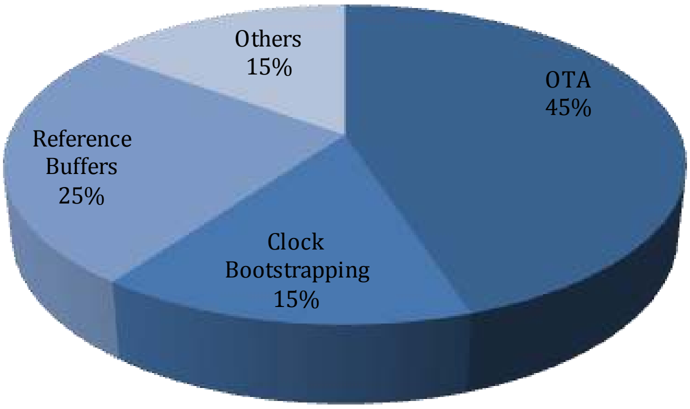


Figure 3.1: Power distribution in a typical pipeline ADC.

To reduce the power associated with reference circuitry, a mismatch insensitive MDAC (MI-MDAC) with current mode level shifting is proposed in [19]. The circuit does not require either positive or negative reference voltages, as the required level shifting (DAC function) is performed in current mode.

This chapter starts with a review of the conventional 1.5-bit pipelined stage. Next the MI-MDAC is introduced and an analysis of the circuit is presented.

3.1 Review of the Conventional 1.5 Bit MDAC

The simplest pipeline stage is a 1-bit stage with one redundant quantization level, often referred as a 1.5-bit stage. The ideal transfer function is depicted in Figure 3.2, which may be described by

$$V_{out} = \begin{cases} 2V_{id} + V_{REF} \quad , & -V_{REF} < V_{id} < -\dfrac{V_{REF}}{4} \\ 2V_{id} \quad , & -\dfrac{V_{REF}}{4} < V_{id} < +\dfrac{V_{REF}}{4} \\ 2V_{id} - V_{REF} \quad , & +\dfrac{V_{REF}}{4} < V_{id} < +V_{REF} \end{cases} \tag{3.1}$$

The comparator decision levels are set to $-V_{REF}/4$ and $+V_{REF}/4$ and the MDAC characteristic is divided in three segments. Each segment is obtained either by adding or subtracting a reference. The slope of each one of the 3 segments corresponds to the gain stage of two.

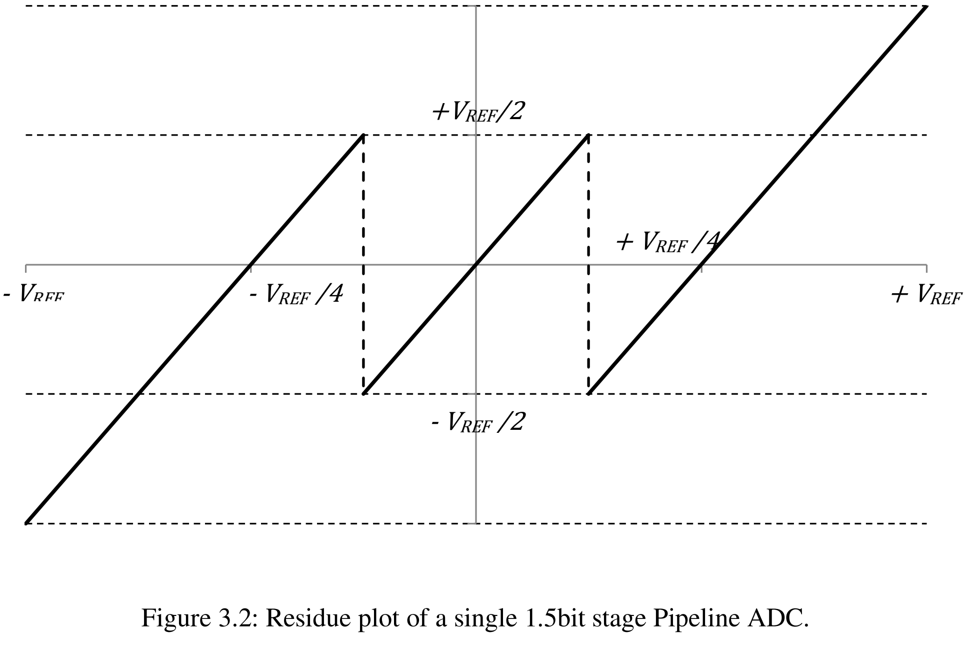


Figure 3.2: Residue plot of a single 1.5bit stage Pipeline ADC.

A commonly used 1.5-bit per stage MDAC is shown in Figure 3.3 [20]. The operation is as follows: during phase $\emptyset_1$ the input signal is sampled in two capacitors C_1 and C_2. At the beginning of $\emptyset_2$, the output code of the sub-ADC (local flash quantizer) is available, and appropriate reference levels are connected to the bottom plate of C_1. Capacitor C_2 is connected in a feedback loop around the amplifier and the charge stored on C_1 is transferred to C_2. The resulting output voltage is given by:

$$V_{out} = \frac{C_1 + C_2}{C_2} V_{in} + \frac{C_1}{C_2} \cdot B \cdot V_{REF} \tag{3.2}$$

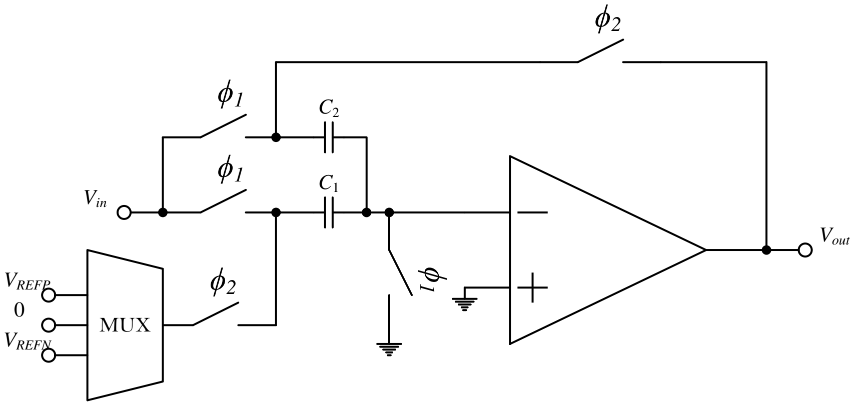


Figure 3.3: Switched capacitor MDAC for a 1.5-bit pipeline stage. Single-ended version shown for simplicity.

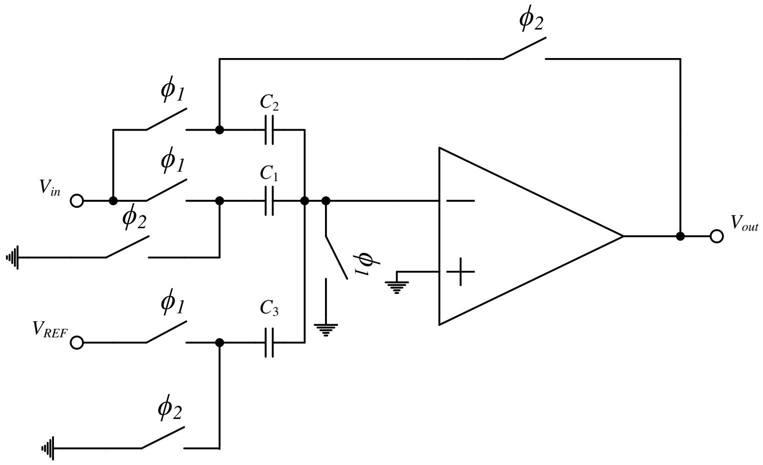
For equally sized capacitors, the resulting output voltage, at the end of $\emptyset_2$, will be two times the sampled input voltage. The accuracy of the residue generated by the conventional switched capacitor MDAC is determined by the gain and bandwidth of the amplifier, capacitor matching and the settling accuracy of the reference buffers.

The feedback factor β is expressed as

$$\beta = \frac{C_2}{C_1 + C_2 + C_p} \tag{3.3}$$

Neglecting parasitics, the feedback factor approaches the ideal value of 0.5.

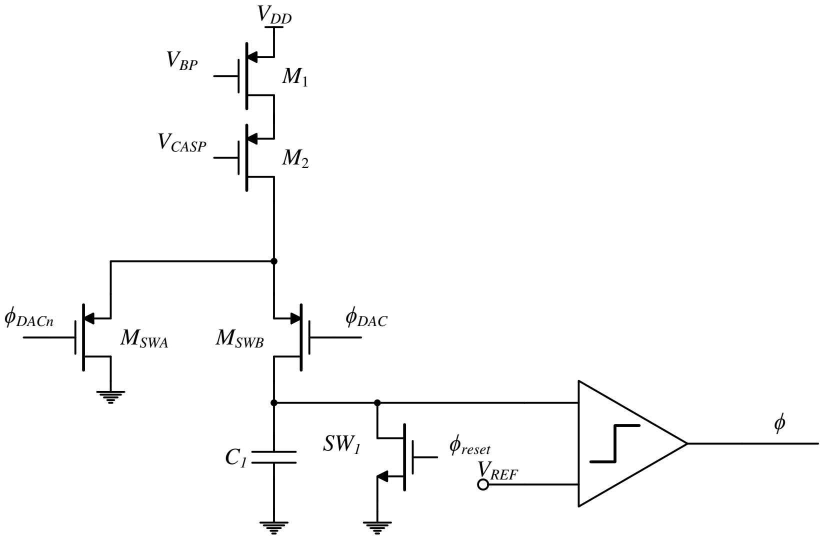
A modified version of the conventional 1.5-bit MDAC is shown in Figure 3.4, where the reference voltage is sampled in a separate capacitor during the sampling phase [21]. This prevents signal-dependent loading and ensures that the load seen by the reference buffer is the same every cycle. In this case a weak reference buffer only causes a fixed settling error and a high speed buffer is avoided.



ϕ_2
ϕ_1
C_2
ϕ_1
C_1
V_{in}
ϕ_2
V_{out}
ϕ_1
ϕ_1
C_3
V_{REF}
ϕ_2

Figure 3.4: Modified MDAC in which a separate capacitor is used to sample reference voltages.

To further lower the power consumption of the reference circuitry, the reference buffers can be replaced by a current source and a comparator as shown in Figure 3.5. The idea is to integrate a current on a capacitor and detecting the reference crossing via a comparator [22].



V_{DD}
V_{BP}
M_1
V_{CASP}
M_2
ϕ_{DACn}
M_{SWA}
M_{SWB}
ϕ_{DAC}
ϕ
SW_1
C_I
ϕ_{reset}
V_{REF}

Figure 3.5: A fixed current is integrated on a capacitor and a comparator detects the reference crossing.

The drawback of this solution is the reduced feedback factor and the corresponding increase of noise.

3.2 Mismatch insensitive MDAC with current mode level shifting

The mismatch insensitive MDAC (MI-MDAC) with current mode level shifting was proposed in [19] as a low power alternative for the conventional MDAC. The reference buffer used to generate the DAC reference levels is replaced with two current sources connected to the OTA input terminals. Moreover, the circuit has an enhanced feedback factor allowing a faster settling speed.

3.2.1 Circuit description

The schematic of the MI-MDAC is shown in Figure 3.6. The gain of two is obtained by voltage sum, instead of charge distribution, as occur in the conventional implementation. The level shifting occurs when current sources I_P and I_N are turned on. These current sources sink/source current through the feedback capacitors changing the output voltage by an amount proportional to the respective current, feedback capacitance and duration of the integration phase.

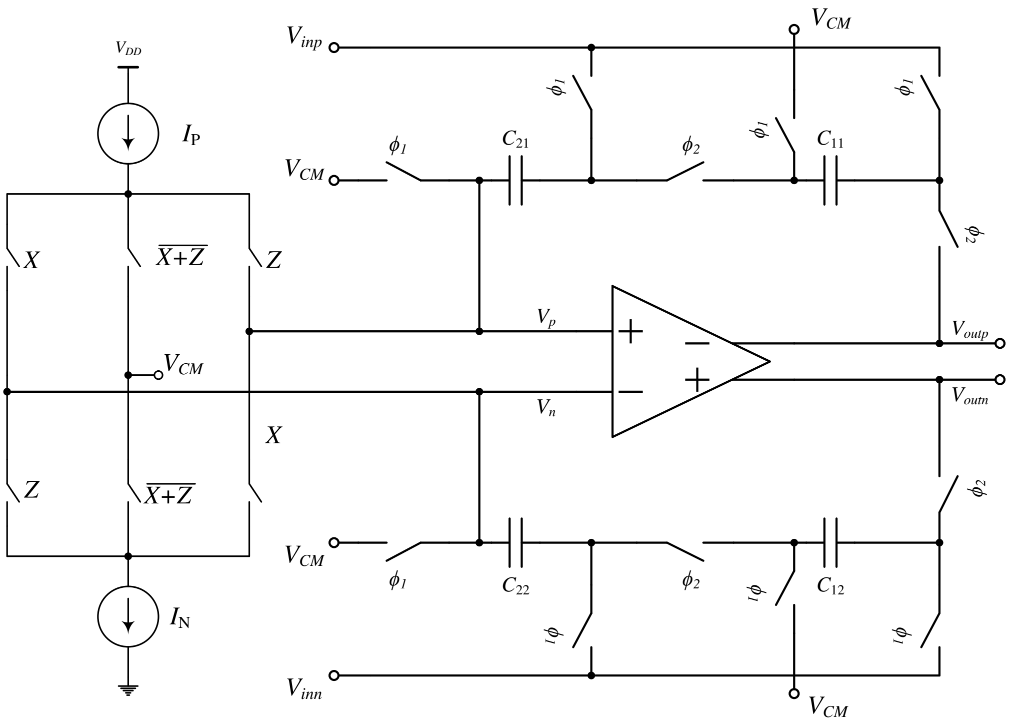
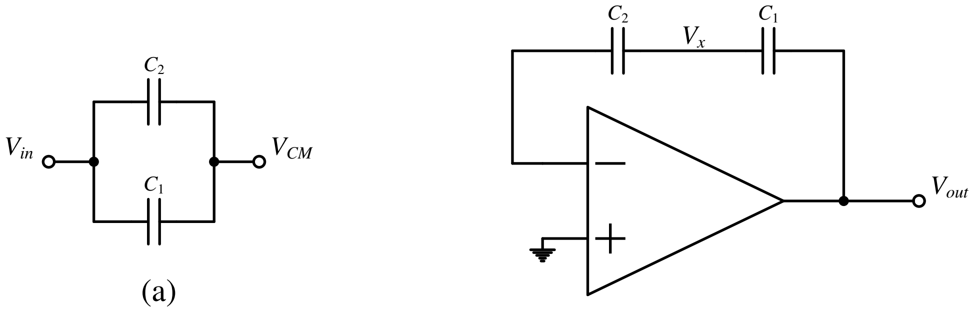

V_{DD}
I_P
X
$\overline{X+Z}$
Z
V_{CM}
Z
$\overline{X+Z}$
X
I_N
V_{inp}
V_{CM}
ϕ_1
C_{21}
ϕ_1
ϕ_2
ϕ_1
C_{11}
ϕ_1
V_{CM}
ϕ_2
V_p
V_n
V_{outp}
V_{outn}
ϕ_2
V_{CM}
ϕ_1
C_{22}
ϕ_2
ϕ_1
C_{12}
ϕ_1
ϕ_1
V_{inn}
V_{CM}

Figure 3.6: Fully differential schematic of the 1.5-bit MI-MDAC with current-mode reference shifting.

3.2.2 Circuit analysis

The single-ended version of the MI-MDAC shown in Figure 3.7 is used to derive the MDAC transfer function.



(a)

(b)

Figure 3.7: Single-ended 1.5 bit MI-MDAC configuration during (a) sampling and (b) amplification phase.

During the sampling phase, the input voltage V_{in} is sampled on two capacitors C_1 and C_2. The charge on the two capacitors is given by

$$Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$$

In the amplification phase the charge is given by

$$Q_{C1} = C_1(V_x - V_{out}),Q_{C2} = C_2 V_x$$

The MDAC transfer function can be found by deriving the charge conservation equations at node V_x and at the inverting input of the opamp.

$$C_2 V_{in} = C_2 V_x \tag{3.4}$$

$$(-C_1 + C_2) V_{in} = C_1(V_x - V_{out}) + C_2 V_x \tag{3.5}$$

By solving these two equations for the output voltage V_{out}, results in

$$V_{out} = \frac{2C_1}{C_1} V_{in} = 2V_{in} \tag{3.6}$$

The complete expression for the MDAC transfer function can be found in [23]. This expression includes the influence of parasitic capacitors associated with the bottom plate of the main capacitors and the nonlinear intrinsic capacitors of the switches. In [23] it is also demonstrated that the MDAC is insensitive to mismatch of the main capacitors, but is sensitive to parasitic capacitors, so one additional short-capacitor is used to compensate for this effect. Compared with the conventional MDAC, this circuit shows a 2-bit accuracy improvement in respect to the gain accuracy.

The circuit configuration during X operation mode of the MDAC is shown in Figure 3.8. The current source I_N is connected to the non-inverting input of the opamp, while I_P is connected to the inverting input.

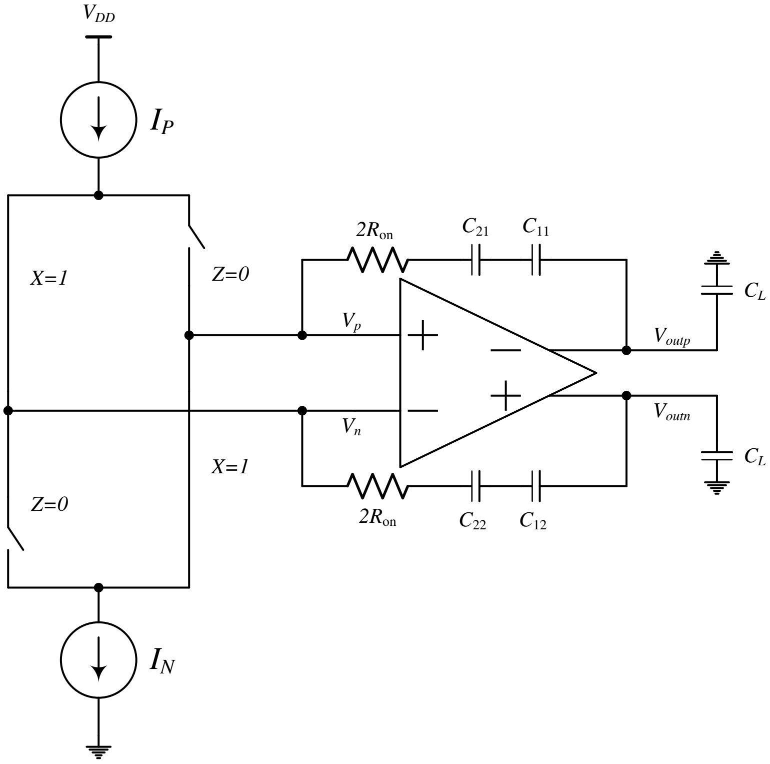


Figure 3.8: MDAC configuration during amplifying phase (Current level shifting active X=1).

Defining $I_P = I_N = I_{REF}/2$, $R_1 = R_2 = 2R_{on}$, $C_1 = C_{11}C_{21}/(C_{11} + C_{21})$, $C_1 = C_{12}C_{22}/(C_{12} + C_{22})$, the opamp (OTA) input voltage can be defined as,

$$I_P = I_N = \frac{I_{REF}}{2} \tag{3.7}$$

$$\begin{aligned} V_p &= V_{op} - \left(R_1 + \frac{1}{sC_1}\right)\frac{I_{REF}}{2} \\ V_n &= V_{on} + \left(R_1 + \frac{1}{sC_2}\right)\frac{I_{REF}}{2} \end{aligned} \tag{3.8}$$

$$\frac{V_{od}}{I_{REF}} \cong \frac{1}{2\left(1 + \frac{s}{A_0 p_1}\right)}\left(R_1 + R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}\right) \tag{3.9}$$

Considering a step function $I_{REF}(s) = I_{REF}/s$, $V_{od}(t)$ is obtained applying the inverse Laplace transform:

$$\begin{aligned} V_{od}(t) = \frac{I_{REF}}{2C_1}\left(t + \frac{(e^{-\mathrm{GBW}t} - 1)(1 - \mathrm{GBW}R_1C_1)}{\mathrm{GBW}}\right) + \\ \frac{I_{REF}}{2C_2}\left(t + \frac{(e^{-\mathrm{GBW}t} - 1)(1 - \mathrm{GBW}R_2C_2)}{\mathrm{GBW}}\right) \end{aligned} \tag{3.10}$$

Assuming GBW<<1/(R_iC_i), the output voltage is given by

$$V_{od}(t) = \frac{I_{REF}}{C}\left(t + \frac{e^{-\mathrm{GBW}t} - 1}{\mathrm{GBW}}\right) \tag{3.11}$$

The final expression can be found by considering a rectangular pulse as the input signal. This signal can be decomposed in a sum of a positive step function starting at t = 0 and a negative step function starting at t = T_i. The output response can be expressed as

$$V_{out}(t) = \begin{cases} V_{od}(t), & t < T_i \\ V_{od}(t) - V_{od}(t - T_i), & t \geq T_i \end{cases} \tag{3.12}$$

$$\begin{aligned} & V_{od}(t) - V_{od}(t - T_i) \\ & = \frac{I_{REF}}{C}\left(T_i + \frac{e^{-\mathrm{GBW}t} - 1}{\mathrm{GBW}}\right) - \frac{I_{REF}}{C}\left((t - T_i) + \frac{e^{-\mathrm{GBW}(t - T_i)} - 1}{\mathrm{GBW}}\right) \end{aligned} \tag{3.13}$$

Summing the two expression equation simplifies to

$$\frac{I_{REF}T_i}{C} + \frac{I_{REF}}{\mathrm{GBW} \times C}\left(\frac{1}{e^{\mathrm{GBW}t}} - \frac{e^{\mathrm{GBW}T_i}}{e^{\mathrm{GBW}t}}\right) \quad t \geq T_i \tag{3.14}$$

The output voltage of the fully-differential MDAC is given by

$$\begin{aligned} V_{od} = 2V_{id}\left(1 - e^{-\frac{t}{\beta GBW}}\right) + B \cdot \frac{I_{REF}T_i}{C} \\ + \frac{I_{REF}}{\mathrm{GBW} \times C}\left(\frac{1}{e^{\mathrm{GBW}t}} - \frac{e^{\mathrm{GBW}T_i}}{e^{\mathrm{GBW}t}}\right) \end{aligned} \tag{3.15}$$

In order to graphically analyze the transient output response of the circuit, a behavioral MATLAB simulation was carried out using the derived equations. The opamp is represented by a single pole model with 80 dB DC gain and 320 MHz GBW. A feedback factor β = 0.8 and an integration time T_i = 4 ns were considered. The step response and the response to the level shifting performed by the current sources are shown in Figure 3.9.

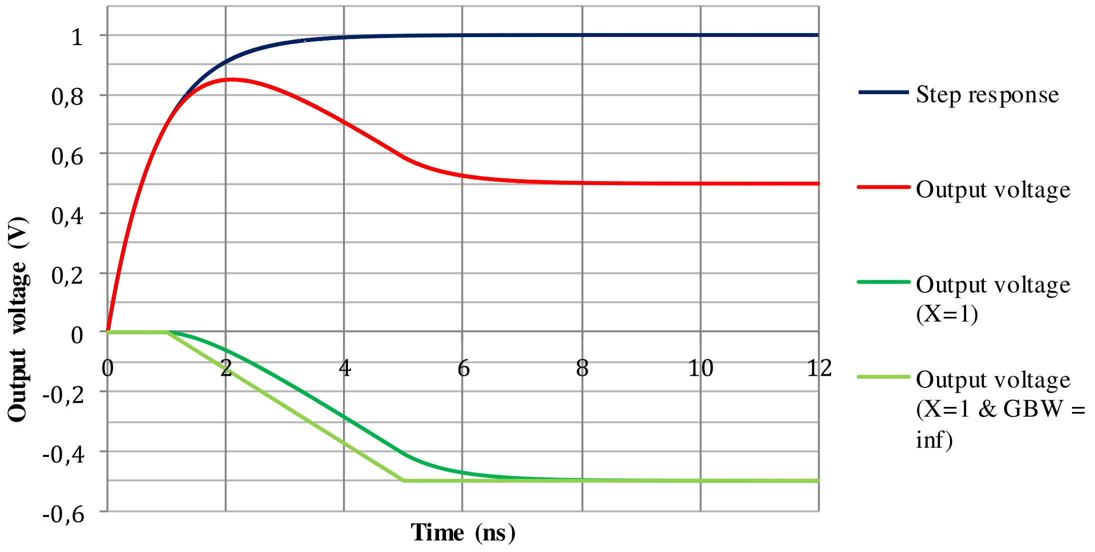


Figure 3.9: Transient waveforms at the output of the MDAC.

The output starts to settle exponentially to the value corresponding to the term $2\,V_{id}$. The level shifting starts at $t = 1$ns and the response have a ramped characteristic until the end of the integration phase. After that the output voltage settles to the final value.

3.2.3 Dynamic limitation of the operational amplifier

The dynamic limitation of the amplifier introduces an error in the desired output level shifting. Assuming all capacitors equal and a fixed T_i, the error magnitude is given by

$$\varepsilon_{\text{GBW}} = \frac{V_{od} - V_{od\_ideal}}{V_{od\_ideal}} = \frac{\frac{1}{e^{\text{GBW}t}} - \frac{e^{\text{GBW}T_i}}{e^{\text{GBW}t}}}{\text{GBW}T_i} \qquad (3.16)$$

Where V_{od_ideal} is given by (3.14) with GBW=∞. The error is dependent on the closed loop bandwidth, the integration time, and the time of the amplification phase. Assuming that the output response of the amplifier used in the MDAC is not limited by slew rate, this error is not signal dependent.

3.2.4 Integration Time Variations

Assuming $\text{GBW} = \infty$, all capacitors equal, and an integration time given by $T_i(1 + \varepsilon_{Ti})$, where ε_{Ti}, represents the deviation from the ideal integration time, the error in the output level shifting is given by

$$\varepsilon_T = \frac{V_{od} - V_{od\_ideal}}{V_{od\_ideal}} = \frac{T_i(1 + \varepsilon_{Ti}) - T_i}{T_i} = \varepsilon_{Ti} \qquad (3.17)$$

This means that this error is dependent on the jitter noise of the system. The average power in the reference error amplitude spectrum is given by [24]

$$P_{Jitter} = \sigma^2 \times \left(\frac{V_{REF}}{T_i}\right)^2 \qquad (3.18)$$

where σ is the rms value of the jitter.

3.2.5 Current Sources

One typical implementation of the current sources is shown in Figure 3.10. Current sources are implemented with single cascode devices and a differential pair used as current switch. This circuit routes the tail reference current I_{REF} to the output or towards a dummy connection.

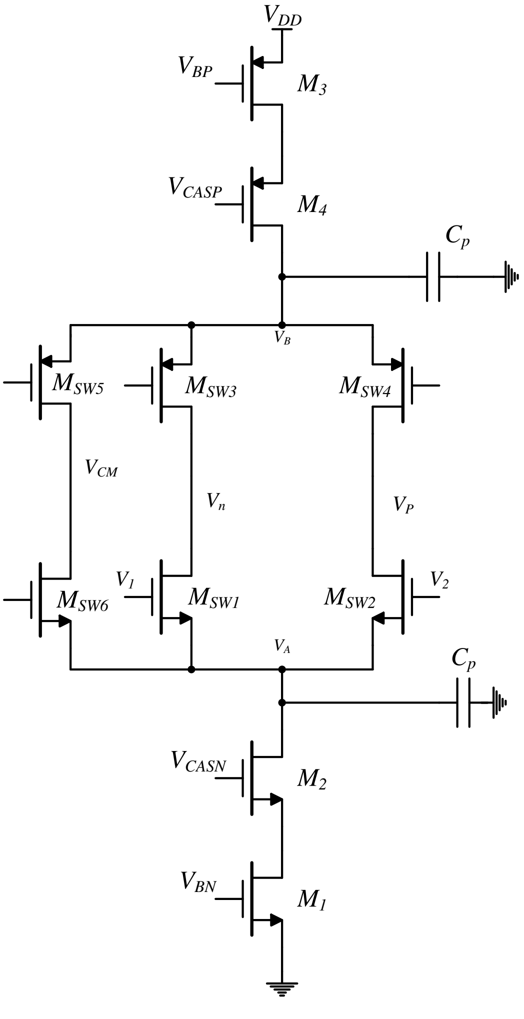

V_{DD}
V_{BP}
M_3
V_{CASP}
M_4
C_p
V_B
M_{SW5}
M_{SW3}
M_{SW4}
V_{CM}
V_n
V_P
V_1
V_2
M_{SW6}
M_{SW1}
M_{SW2}
V_A
C_p
V_{CASN}
M_2
V_{BN}
M_1

Figure 3.10: Schematic view of NMOS and PMOS single Cascode current sources.

Cascode transistors are used to increase the output resistance. Hence the effects of channel length modulation are significantly reduced. The value of parasitic capacitances associated with current sources is also reduced since the cascode source is designed with a lower area than the bias transistor.

3.2.5.1 Causes of nonlinearity

Since the operation performed by the current sources is done at the input, any error or nonlinearity in this operation is undistinguishable from the input signal and hence it will appear at the output without suppression and degrade the MDAC conversion accuracy. The nonlinearity is mainly caused due to the following effects:

- Finite Output resistance. Since the output of current switches is connected to the opamp input and the voltage V_n is signal dependent the current is modulated by voltage at node n.
- Charge and discharge of parasitic capacitances associated with current sources;
- Imperfect synchronization of the control signals of currents switches;

Output resistance is improved by using cascode current sources with large channel length. It is also important to design the Output switch $M_{SW1,2,3,4}$ and their gate voltage so as to keep the output switch in saturation. This minimizes the excursion of the voltage at common source node A. The linearized model shown in Figure 3.11 can be used to analyze the non-ideal behavior of the current sources.

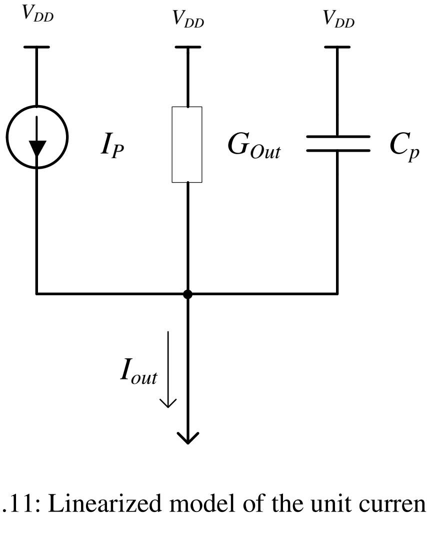


Figure 3.11: Linearized model of the unit current source.

The reference voltage mismatches between stages is another source of noise and distortion. In a traditional pipeline ADC, the reference voltage provided to each stage is generated by the same analog buffer. Thus, any deviation from the nominal value will be seen as an absolute gain error. In the proposed scheme, the reference voltage is generated when a current flows through the feedback capacitors converting this way a current into a voltage in each stage. So, due to mismatches (transistor, capacitor, and integration time mismatch), charge injection and the presence of parasitic capacitors, the reference voltages may differ from each other.

$$V_{REF} = \frac{I_{REF}(1+\Delta I_{REF})T_i(1+\Delta T_i)+Q_{inj}}{C(1+\Delta C)+C_p} \tag{3.19}$$

3.2.5.2 Switching noise

The reference current can also be disturbed by switching noise. During the switching voltage at node A drops. This voltage change is coupled to node BN through the gate-drain overlap capacitance of M_1, disturbing I_{REF} and hence I_{OUT}.

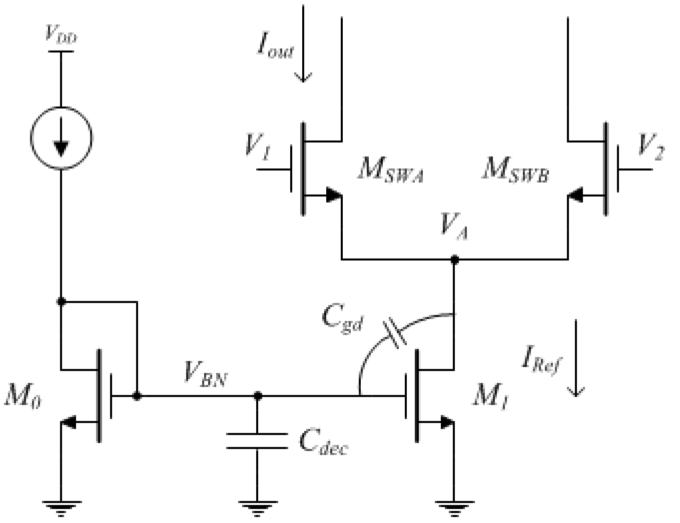


Figure 3.12: Differential pair operating as a current switch

To minimize any disturbance on V_{BN}, a decoupling capacitor should be connected from node BN to ground as shown in Figure 3.12. This capacitor also filters out the noise injected on the current sources from other blocks. To save area this capacitor could be implemented using a MOSCAP device in the accumulation region.

3.3 Current Shifting Period Controller

To operate the proposed MDAC circuit as intended, three different clock phases are needed: two non-overlapping clock phases, used in most of the switched-capacitor circuits, and a clock phase used to control the integration time. The timing diagram of the clock signals is shown in Figure 3.13. An example of a non-overlapping clock generator, widely found in the literature, is shown in Figure 3.14.

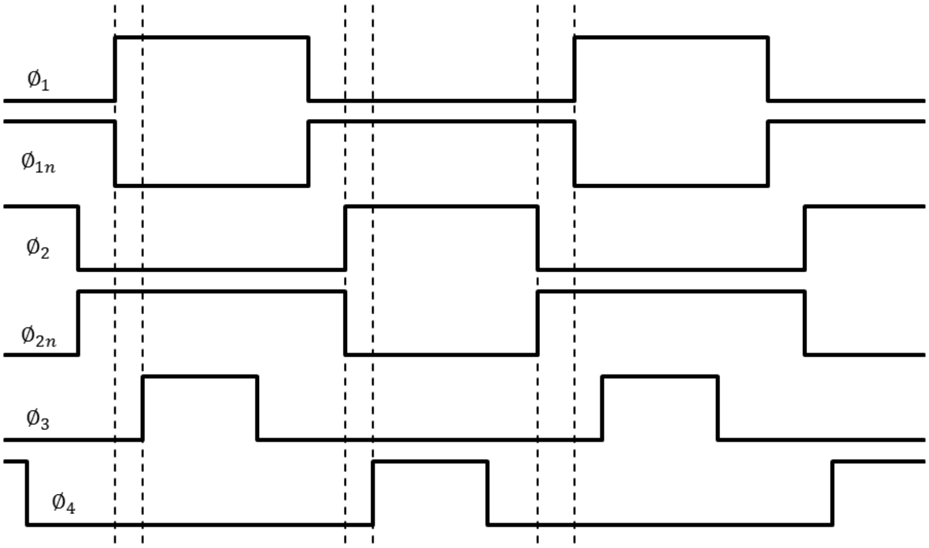


Figure 3.13: Clock phases timing diagram.

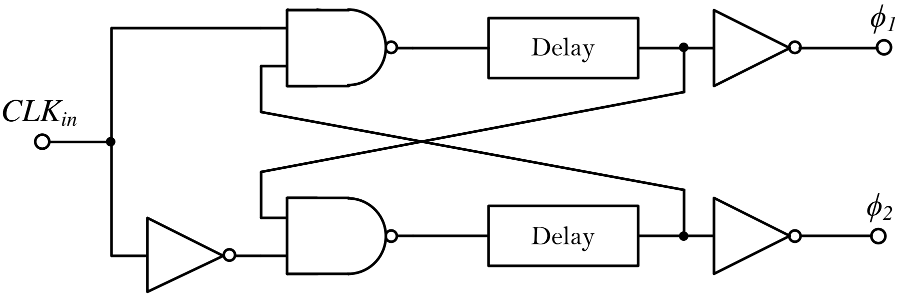


Figure 3.14: Standard non-overlapping Clock Generator.

The integration time of the MDAC is controlled by the clock phases $\emptyset_3$ and $\emptyset_4$. This phases can be obtained with a SC replica and a comparator [22] as shown in Figure 3.15.

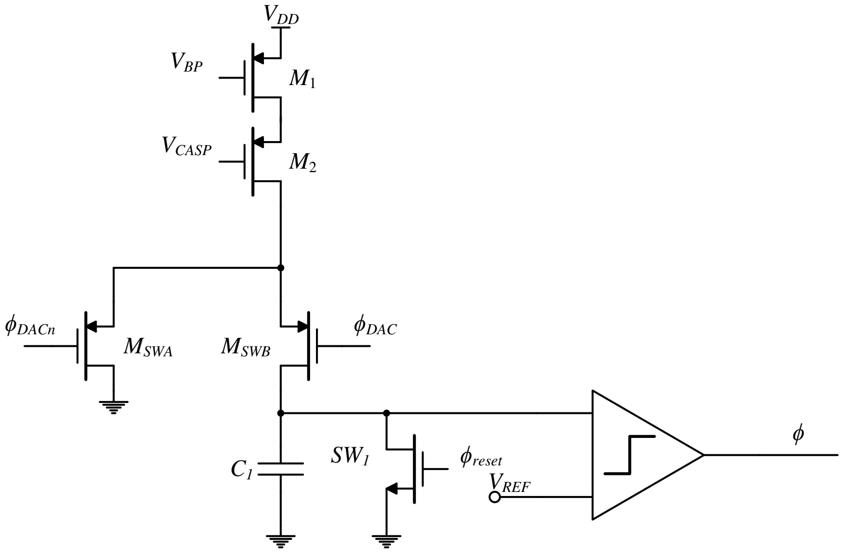

V_{DD}
V_{BP}
M_1
V_{CASP}
M_2
ϕ_{DACn}
M_{SWA}
M_{SWB}
ϕ_{DAC}
ϕ
C_I
SW_I
ϕ_{reset}
V_{REF}

Figure 3.15: Current shifting period controller.

The required phase can also be obtained with a delay locked loop (DLL). Figure 3.16 depicts a block diagram of a DLL. The circuit employs negative feedback to produce clock phases with a precision spacing. The delay elements can be realized using a current-starved inverter or a self-biased inverter as proposed in [1]. Self-biasing circuits have various performance advantages, such as: a) less sensitivity against PVT variations; b) capability of supplying switching currents greater than the quiescent bias current; c) external biasing voltages (and the corresponding biasing circuitry) become unnecessary.

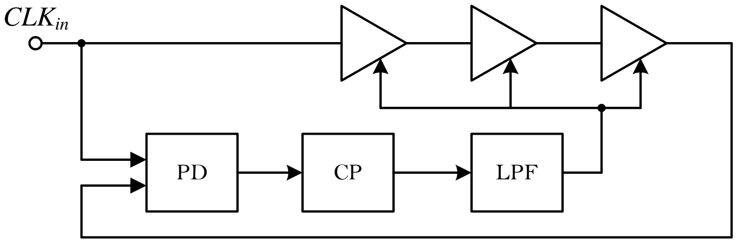

CLK_{in}
PD
CP
LPF

Figure 3.16: Delay locked loop (DLL).

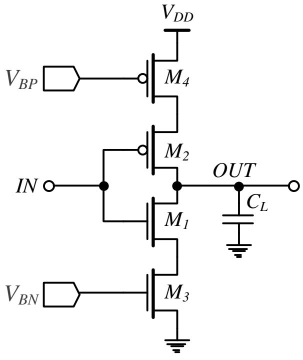

V_{DD}
V_{BP}
M_4
M_2
IN
OUT
C_L
M_1
V_{BN}
M_3

Figure 3.17: Current-starved delay element.

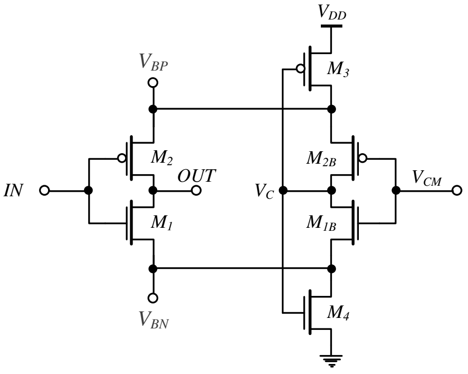

V_{DD}
V_{BP}
M_3
M_2
OUT
M_{2B}
V_{CM}
IN
V_C
M_1
M_{1B}
V_{BN}
M_4

Figure 3.18: Self-biased inverter.

3.4 Noise analyses

Thermal noise is an important limiting factor in medium/high resolution ADCs. In a pipeline ADC, noise sources are mainly contributed by the MDAC, of the front-end stage, from the references and from the sampling clock jitter. In the particular case of the MDAC block thermal noise is dominated by the switches noise, and by opamp thermal noise. The noise contribution from the current sources should be considered if the proposed new MDAC circuit is employed.

3.4.1 Switches noise

During the sampling phase thermal noise generated by switches is sampled on the sampling capacitor. This noise is referred as KT/Cnoise. The output referred noise due to switches noise is given by [25]

$$\overline{v_{sw}^2} = 2 \cdot \frac{KT}{\beta} \cdot \left(\frac{1}{C_F}\right) \tag{3.20}$$

where $K$is Boltzmann's constant, $T$is the absolute temperature, β is the feedback factor and C_F is the value of the equivalent feedback capacitor. Regarding the noise produced by feedback switches, their contribution is made small and can be neglected if their time constant is made larger than the opamp bandwidth [26].

3.4.2 Opamp Noise contribution

During the amplification phase the amplifier contributes with additional noise [25]. The noise power at the output of the MDAC can be found from

$$\overline{v_{opamp}^2} = 2 \cdot \frac{KT}{\beta} \cdot \left(\frac{2}{3} \cdot \frac{\gamma}{C_c}\right) \tag{3.21}$$

where β is the feedback factor, C_c is the compensation capacitor (assuming that a two-stage OTA topology is used) and γ represents the excess noise factor of the opamp.

3.4.3 Current Source Noise contribution

The contribution to the output noise from the current source is given by:

$$\overline{v_{ncs}^2} = \frac{2\gamma KT g_m T_i}{C^2} \tag{3.22}$$

where γ is the transistor excess noise factor and T_{i} is the integration time. Considering $g_m = \frac{2I_D}{V_{ov}}$ and $I_D = \frac{V_{REF} \times C}{T_i}$ the noise contribution from the charging current can be rewritten as

$$\overline{v_{nocs}^2} = \frac{4\gamma KTV_{REF}}{V_{ov}C} \tag{3.23}$$

where V_{ov} is the overdrive voltage of the bias transistor and C represents the total equivalent feedback capacitor.

The output voltage noise at the output of MDAC is the sum of the all contributions.

$$\overline{v_{no}^2} = \overline{v_{sw}^2} + \overline{v_{opamp}^2} + \overline{v_{ncs}^2}$$

Thermal noise of ADC can be found by summing the squares of the input referred voltages

$$V_{n,tot}^2 = V_{n,1}^2 + \left(\frac{1}{G_1} V_{n,2}\right)^2 + \cdots + \left(\frac{1}{G_1 G_2 \ldots G_{N-1}} V_{n,N}\right)^2 \tag{3.24}$$

where $V_{n,i}$ is the noise power at stage input, and G_i the interstage gain of the i^{th} stage.

3.4.4 Quantization noise

An ideal quantizer produces an error e_q that ranges from -LSB/*2* to +LSB/*2*. This error is known as quantization error. Assuming that quantization error is random, this can be treated as white noise. The quantization noise power is given by

$$V_{NQ}^2 = \frac{V_{LSB}}{\sqrt{12}} \tag{3.25}$$

The RMS noise voltage is the sum of quantization noise, thermal noise and jitter noise.

$$V_n^2 = V_{NQ}^2 + V_{n,tot}^2 + V_{njitter}^2 \tag{3.26}$$

The resulting SNR for the ADC is given by

$$\mathrm{SNR} = 20 \log \frac{V_p/\sqrt{2}}{V_n} \tag{3.27}$$

The signal-to-noise plus distortion ratio is given by

$$\mathrm{SNDR} = 20 \log \frac{V_p/\sqrt{2}}{V_n + V_D} \tag{3.28}$$

3.5 Switched-Capacitor Current Reference Generator

The reference currents for the MDAC should be generated on-chip and present a low temperature dependence and good supply rejection. Furthermore, these currents should scale with the conversion rate. Precise crystal based clocks and temperature independent voltages references are commonly available on-chip. Therefore, using an external clock derived from a crystal-controlled oscillator, an on-chip precise voltage reference and a simple SC structure, is possible to implement a current reference with low temperature dependence.

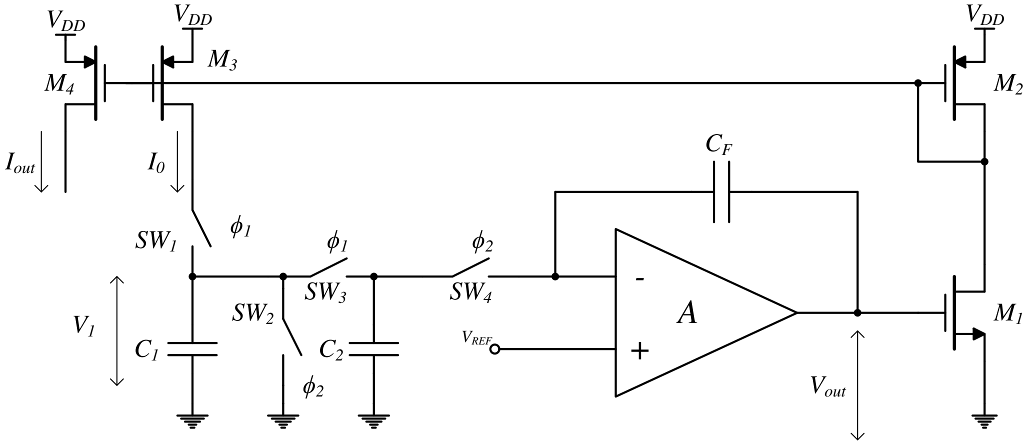


Figure 3.19: Basic scheme of the SC current reference.

A possible implementation of such SC structure is shown in Figure 3.19 [27]. The circuit operates in two non-overlapping clocks. During $\emptyset_1$, C_1 is charged with current I_0. The voltage across C_1 ramps with a slope given by

$$\frac{dV_1}{dt} = \frac{I_0}{C_1 + C_2} \tag{3.29}$$

At the end of this phase the voltage across C_1 reaches its maximum. This voltage V_{1max} is sampled on C_2 and the difference between V_{1max} and V_{REF} is integrated by an SC integrator. In the steady state the value of current I_0 is given by

$$I_0 = \frac{V_{REF} C_1}{T_{\emptyset 1}} \tag{3.30}$$

The value of I_0 depends on a constant voltage reference, a time interval derived from a crystal-controlled oscillator and an on-chip capacitor. The reference current tracks this process dependent capacitance, which shows typical dispersion in the range of ±10-20%, and it is possible to achieve a more predictable behavior of any SC structure.

3.6 Summary

In this chapter, the conventional 1.5-bit MDAC was briefly reviewed and a new architecture for realizing the 1.5 stage was presented. Several design issues of this new architecture were discussed and an analysis of the thermal noise of the MDAC was conducted. The design challenges of the switches in a low voltage technology have been addressed. The chapter concludes with a description of a switched-capacitor current reference with low temperature dependence.

Chapter 4

Design of the 10-bit Pipeline ADC

This chapter describes the design of the major building blocks of the proposed ADC. The techniques described in previous chapter are used to design a 10-bit pipeline ADC without the need of a power hungry buffer to define the reference voltages for the MDAC. The ADC is designed in a 65 nm one-poly-eight-metal (1P8M) CMOS technology and is operated from a 1.2 V power supply.

4.1 ADC architecture

The architecture of the proposed pipeline ADC, shown in Figure 4.1, is composed of a front end S/H circuit, followed by eight 1.5-bit pipelined stages, and a final 2-bit flash quantizer stage. The ADC also has on-chip current generation, a clock generator and a digital error correction circuit. To reduce the power consumption of the pipeline ADC the capacitors and the bias currents of each stage are scaled down along the pipeline chain. For further power and area reduction, the opamps are shared between successive stages.

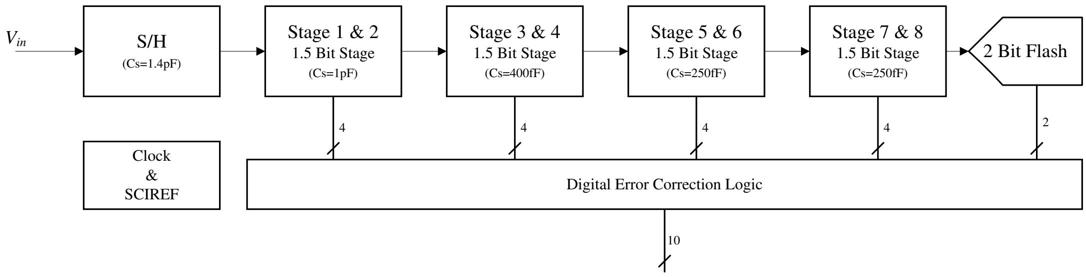

V_{in}
S/H
(Cs=1.4pF)
Stage 1 & 2
1.5 Bit Stage
(Cs=1pF)
Stage 3 & 4
1.5 Bit Stage
(Cs=400fF)
Stage 5 & 6
1.5 Bit Stage
(Cs=250fF)
Stage 7 & 8
1.5 Bit Stage
(Cs=250fF)
2 Bit Flash
4
4
4
4
2
Clock
&
SCIREF
Digital Error Correction Logic
10

Figure 4.1: Top level architecture of the 10-bit pipeline ADC.

The estimated input referred noise due to thermal noise is 220 μVrms. Additional noise components, such as quantization noise, rms jitter noise and reference circuits noise increases the total input referred noise of the ADC to 356 μVrms. Considering a full-scale range input signal the expected SNR is about 57.4 dB. The target specifications for this work are to achieve 9.2 bits of ENOB with a power dissipation of 8 mW at 40 MS/s corresponding to a FOM of 340 fJ/Conversion. The power dissipation should scale according to sampling rate. Table 4.1 shows the target specifications and Table 4.2 presents the estimate of the different noise sources.

Table 4.1: Target specifications for the designed ADC.

Technology	65nm TSMC Logic LP Process
Supply Voltage	1.2 V ±8%
Sampling rate	20-80 MS/s
Reference	0.5 V (differential)
Resolution	10-bit
Power Dissipation	8 mW @40MS/s
SNDR	57.2 dB
ENOB	9.2 bits
FOM	340 fJ/step

Table 4.2: Noise components of the pipeline ADC.

	Vrms	dBV	dB
Quant. Noise	2,8E-04	-71,0	61,5
DNL Noise	1,4E-04	-77,0	67,5
Thermal Noise	2,2E-04	-73,3	63,8
References noise	1,1E-04	-78,9	69,4
Jitter Noise	2,1E-04	-73,4	63,9
SNR	4,5E-04	-66,9	57,4

4.2 Analog Building blocks

4.2.1 Front-end S/H circuit

A front-end S/H is required to ensure the sub-ADC and MDAC of the first stage sample the same input for high input frequencies. The performance of the ADC at high signal frequencies is predominantly set by the front-end S/H circuit. Since it is in front of the signal chain, its thermal noise and distortion are not attenuated by any preceding gain stages and thus it has to fulfill the full resolution requirement [17]. The conventional flip-around front-end sample-and-hold [20] shown in Figure 4.2 was used in front-end of the pipeline. This topology has the advantage of a feedback factor near unity.

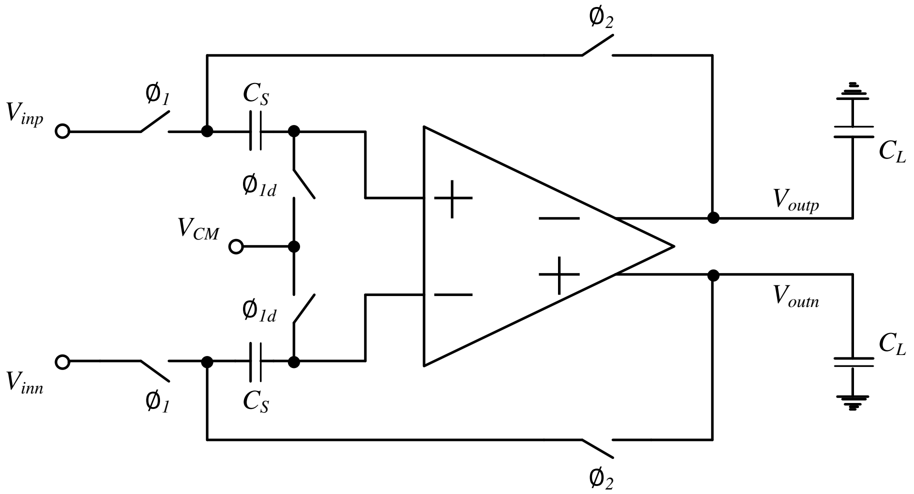
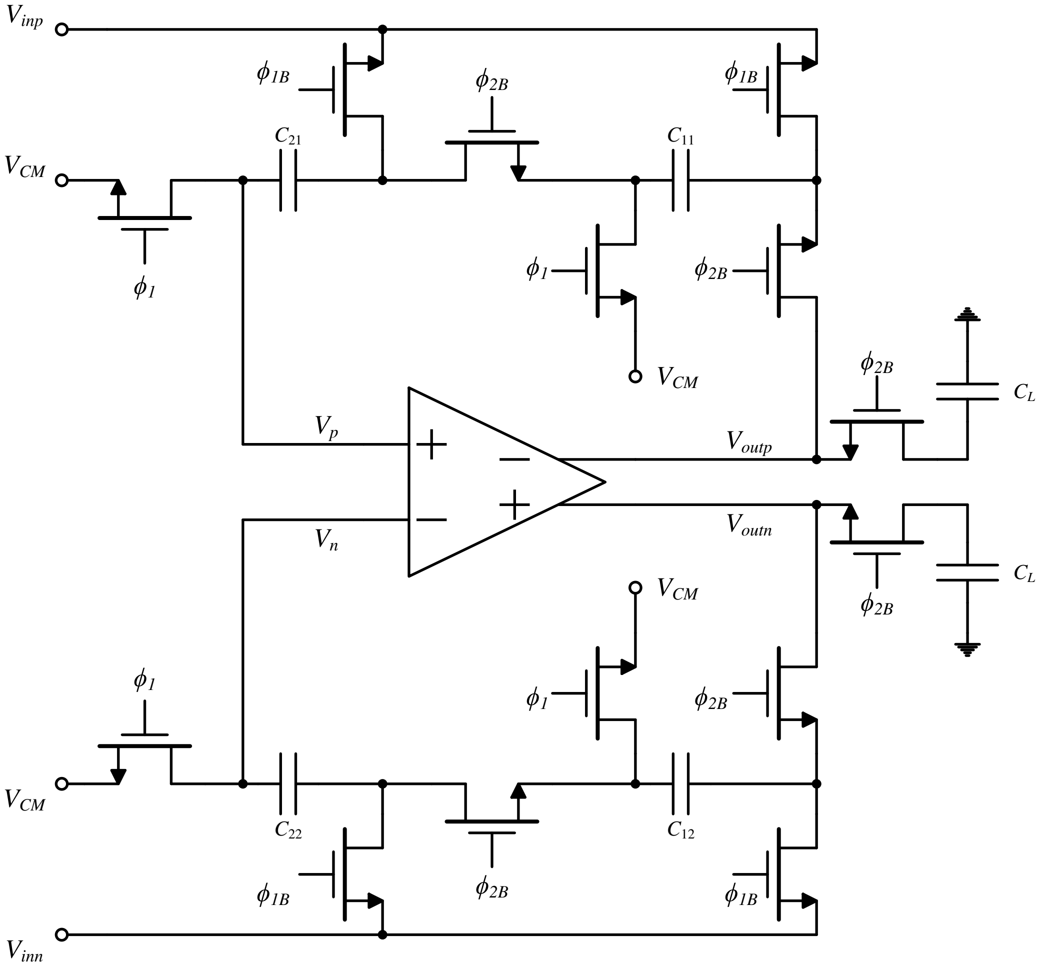


Figure 4.2: Front-end S/H circuit.

As the feedback factor of the S/H stage is ideally the same as the first stage of the pipeline, the amplifier used in first stage is reused in S/H. Input switches are realized using bootstrapped switches and input common mode sampling transistors are implemented with simple NMOS switches. A Capacitor with a nominal capacitance value of 1.4 pF is used. Output referred noise of S/H was estimated to be below 120 μVrms for a full-scale input signal of 1Vpp.

4.2.2 MDAC for the 1.5-bit pipelined stage

The MI-MDAC architecture presented in the last chapter was used to implement the 1.5-bit stage of the pipeline. The circuit schematic of the MDAC is shown in Figure 4.3.



V_{inp}
ϕ_{1B}
ϕ_{2B}
ϕ_{1B}
C_{21}
C_{11}
V_{CM}
ϕ_1
ϕ_1
ϕ_{2B}
V_{CM}
ϕ_{2B}
C_L
V_p
V_{outp}
V_n
V_{outn}
V_{CM}
C_L
ϕ_{2B}
ϕ_1
ϕ_1
ϕ_{2B}
V_{CM}
C_{22}
C_{12}
ϕ_{1B}
ϕ_{2B}
ϕ_{1B}
V_{inn}

Figure 4.3: Fully differential circuit implementation of the MDAC. Parasitic compensation circuit and current source reference shifting circuit implementation not shown (for simplicity).

Input switches are realized using bootstrapped switches, which help to reduce the time constant and improve linearity. Bootstrapping is also employed in the feedback switches. Bottom-plate sampling switches are implemented with simple NMOS transistors and are controlled by an earlier phase which helps reduce the signal-dependent charge injection. Capacitors are implemented with MOM capacitors and have a nominal unit capacitance value of 1 pF.

4.2.2.1 Implementation of the current sources

Current sources are implemented with single cascode and a differential pair is used as a current switch as shown in Figure 4.4. This circuit routes the tail current I_{REF} to the output or towards a dummy connection.

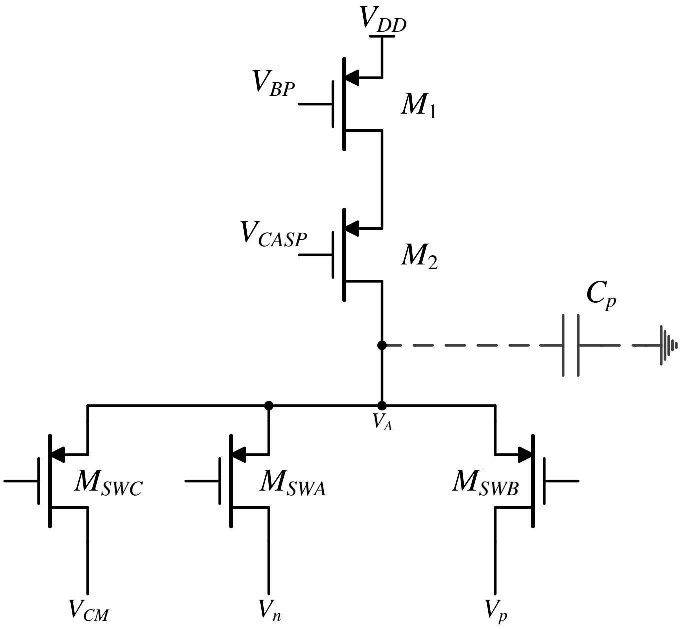


Figure 4.4: Schematic view of PMOS single Cascode current sources.

Transistor M_1 was designed with a large channel length and consequently a large area to improve matching and enhance output impedance. The size of M_2 is large enough to enhance output impedance, but not too high to maintain the parasitic capacitance C_p at its drain at a reasonable value. Current switches are implemented with simple PMOS transistors and are biased in saturation region. This increases the output impedance of the current source and minimizes the variations at the common source node of the switches. To minimize any disturbance on V_{BP} and V_{CASP} a decoupling capacitor is connected from these nodes to analog supply voltage V_{DD}. These capacitors are implemented with MOSCAPs.

4.2.3 Opamp

The architecture of the amplifier utilized in the MDAC is shown in Figure 4.5. It uses a current mirror configuration with a PMOS input pair, which permits the use of a low input common mode voltage and simple NMOS switches can be used to sample this voltage. The non-dominant pole is larger than in a NMOS input pair because the current mirror is implemented with NMOS devices.

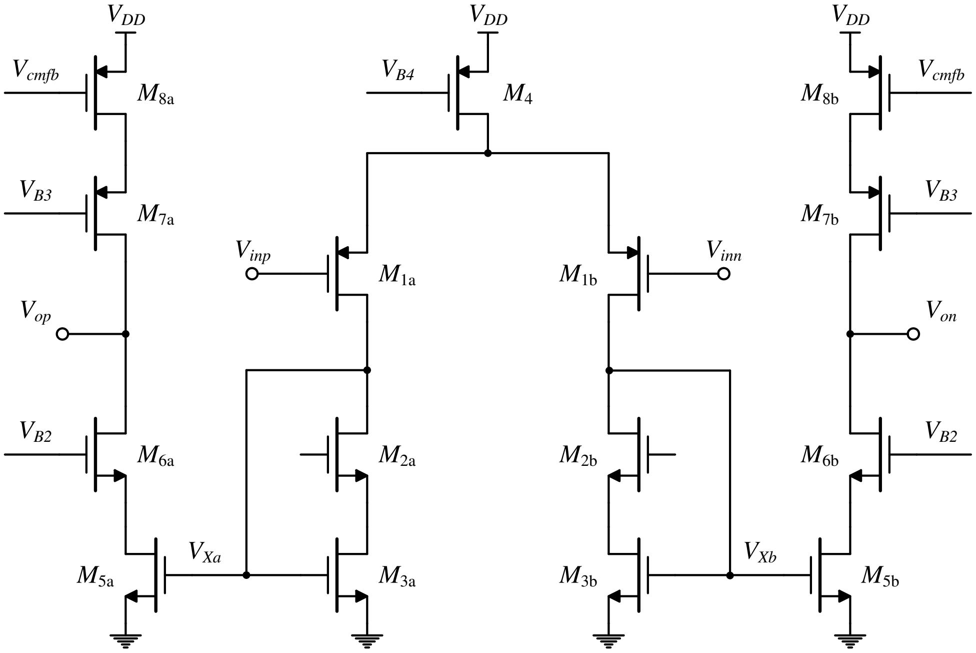

V_{DD}
V_{DD}
V_{DD}
V_{cmfb}
M_{8a}
V_{B4}
M_4
M_{8b}
V_{cmfb}
V_{B3}
M_{7a}
M_{7b}
V_{B3}
V_{inp}
M_{1a}
M_{1b}
V_{inn}
V_{op}
V_{on}
V_{B2}
M_{6a}
M_{2a}
M_{2b}
M_{6b}
V_{B2}
V_{Xa}
V_{Xb}
M_{5a}
M_{3a}
M_{3b}
M_{5b}

Figure 4.5: Schematic of the Current mirror amplifier.

The common mode of amplifier is controlled by two passive switched capacitor commom-mode feedback (CMFB) circuits that are operated in opposite clock phases in parallel. The circuit is shown in Figure 4.6.

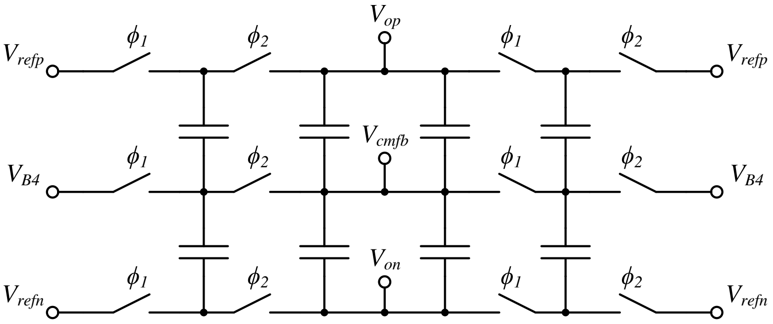

V_{op}
V_{refp}
ϕ_1
ϕ_2
ϕ_1
ϕ_2
V_{refp}
V_{cmfb}
V_{B4}
ϕ_1
ϕ_2
ϕ_1
ϕ_2
V_{B4}
V_{on}
V_{refn}
ϕ_1
ϕ_2
ϕ_1
ϕ_2
V_{refn}

Figure 4.6: Passive switched capacitor CMFB circuit.

The open loop DC-gain of the amplifier is enhanced to 75 dB by introducing the regulation amplifiers shown in Figure 4.7 and Figure 4.8. These circuits are biased with very low bias currents and use the same bias circuit of the core amplifier.

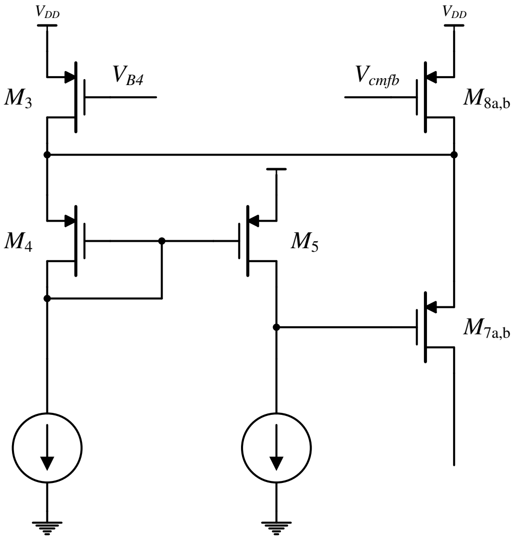


Figure 4.7: High-swing low-voltage regulation PMOS amplifier.

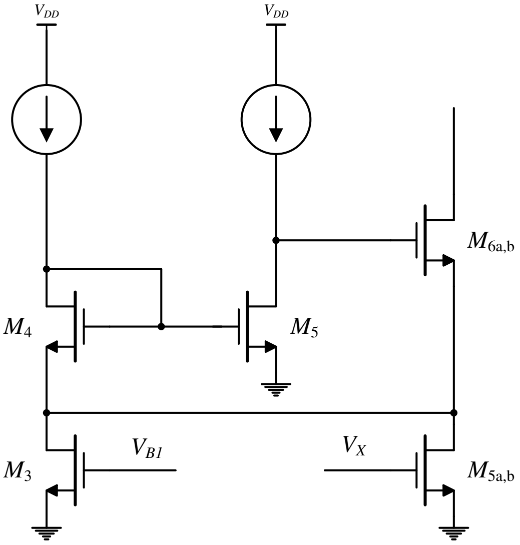


Figure 4.8: High-swing low-voltage regulation NMOS amplifier.

The amplifier was simulated over PVT corners using the BSIM4 model in CADENCE Spectre simulation. The simulated frequency response at typical conditions shows a 320 MHz GBW and 72° phase margin at the frequency of closed loop gain in the target feedback configuration. The DC gain simulated is 75 dB and the typical settling time to 10-bit accuracy is 7.2 ns. Table 4.3 summarizes the results.

Table 4.3: Opamp simulation results.

	Typical	Minimum	Maximum
Supply Voltage (V)	1.2	1.3	1.1
Temperature (°C)	27	125	−40
DC Gain(dB)	75	68	78
GBW (MHz)	320	240	360
PM (°)	72	64	75
Ts$^+$/Ts$^-$(ns) (0.1%)	7.2/7.24	9.2/9.28	6/6.04
Power Consumption (mW)	2.4	3	1.8
C_L(pF)		4	

4.2.4 Sub-Analog-to-Digital Converter (sub-ADC)

As stated before, the quantization in each pipeline stage is performed with a local low-resolution flash quantizer (sub-ADCs). To maximize the available settling time of the MDAC output, the sub-ADCs should provide their output to the MDAC as soon as possible. Therefore the sub-ADC of pipeline A/D converters are of flash type. Each flash sub-ADC comprises a comparator bank, a thermometer to binary encoder and a small decoding logic to generate the control signals of the MDAC.

As previously mentioned, each stage comprises a 1.5-bit sub-ADC with exception of last stage that quantizes two bits. The 1.5-bit flash quantizer circuit shown in Figure 4.9 employs two comparators, two gated SR latches, an X, Y, Z encoder and a thermometer-to-binary digital encoder.

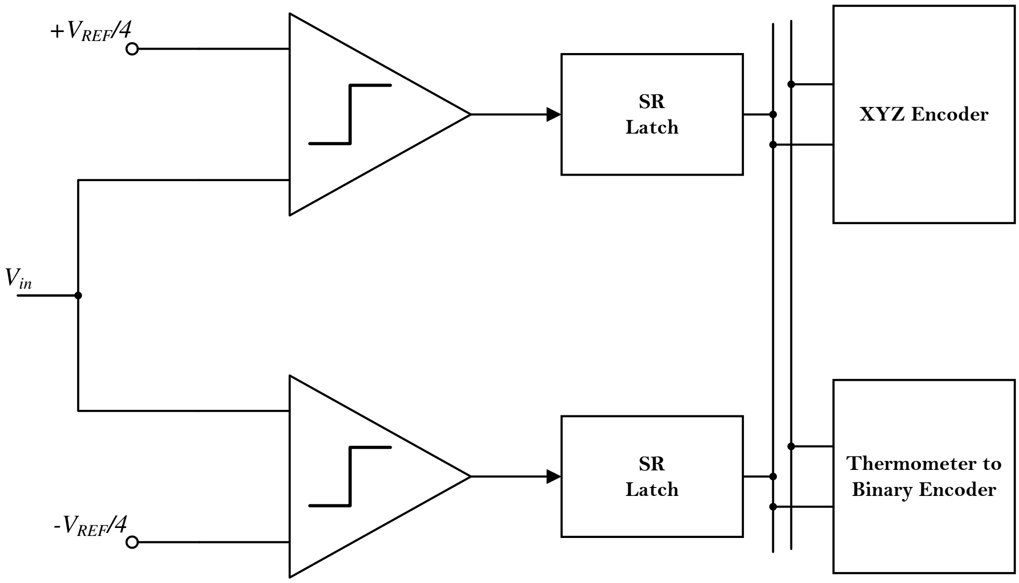


Figure 4.9: Block diagram of a 1.5-bit flash quantizer.

The 2-bit FQ used at the end of the pipeline has an identical structure as that the 1.5-bit version but has one more comparator and the threshold comparator levels are $-V_{REF}/2$, 0 and $+V_{REF}/2$.

4.2.4.1 Sub-ADC Comparator

Since redundancy is applied to relax the comparator offset requirements, dynamic comparators are often used in sub-ADC, because of their potential for low power and small area. A fully differential comparator can be realized employing a charge distribution comparator. The charge sharing dynamic comparator [28] used in this work is shown in Figure 4.10. The offset of this comparator depends mainly on the mismatch between the capacitors and the offset of the differential pair amplifier.

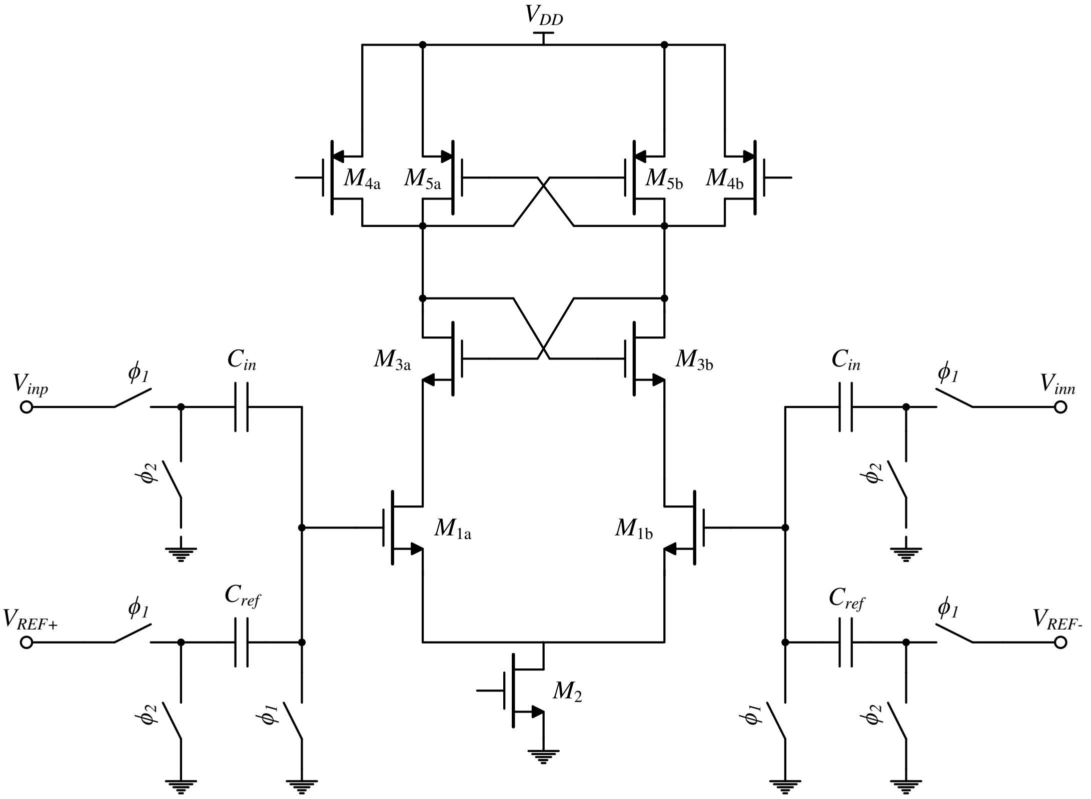

V_{DD}
M_{4a}
M_{5a}
M_{5b}
M_{4b}
M_{3a}
M_{3b}
V_{inp}
ϕ_1
C_{in}
C_{in}
ϕ_1
V_{inn}
ϕ_2
ϕ_2
M_{1a}
M_{1b}
V_{REF+}
ϕ_1
C_{ref}
C_{ref}
ϕ_1
V_{REF-}
M_2
ϕ_2
ϕ_1
ϕ_1
ϕ_2

Figure 4.10: Charge distribution comparator.

The threshold of the comparator can be found applying charge conservation and is given by

$$V_{inp} - V_{inn} = \frac{C_{ref}}{C_{in}}(V_{REF+} - V_{REF-})$$

This means that the threshold voltage of the comparator can be adjusted linearly with the capacitance ratio.

4.2.5 Clock Generation

The timing diagram of the clock signals is shown in Figure 4.11. The clock signals $\emptyset_1$ and $\emptyset_2$ are generated using the standard circuit shown in Figure 4.12. The delay of the NAND gate and the delay element controls the non-overlapping time. The delay element is realized with an even-numbered chain of inverters. The clock signals are re-buffered locally, in each pipelined stage.

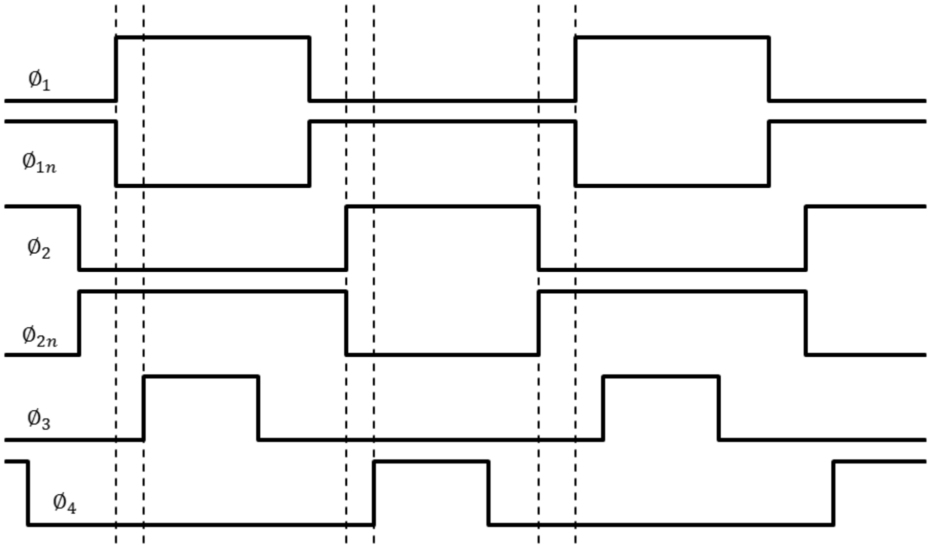


Figure 4.11: Clock phases timing diagram.

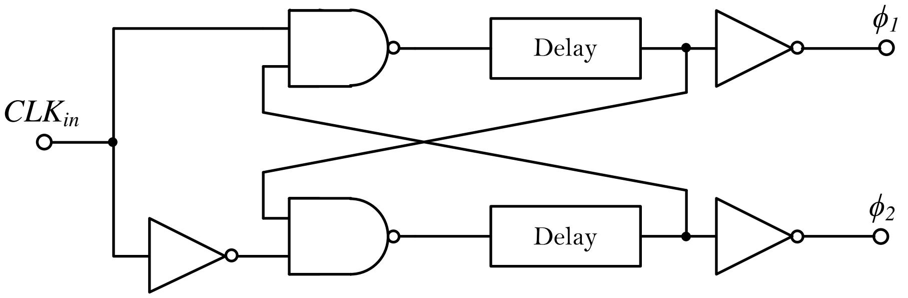


Figure 4.12: Standard Non-overlapping Clock Generator.

Phases $\emptyset_3$ and $\emptyset_4$ that define the integration time of MDAC are generated by the circuit shown in Figure 4.13. The circuit consists of a current source that charges a capacitor during a specified amount of time. At the beginning of $\emptyset_{1\mathrm{d}}$ the output goes high and capacitor C_1 begins to charge up. When the capacitor has been charged to approximately $\mathrm{V_{DD}}/2$ an inverter triggers and $\emptyset_3$ goes low. The time interval is defined by $T_I = \frac{V_{DD/2} \times C_1}{I_P}$. This means that the integration time can be adjusted by changing the size of the capacitor and the value of current I_P. A large grounding transistor SW_1 discharges the capacitor during $\emptyset_2$. The current source is connected to ground during $\emptyset_{3n}$ to discharge the parasitic capacitor and prevent long turn-on times.

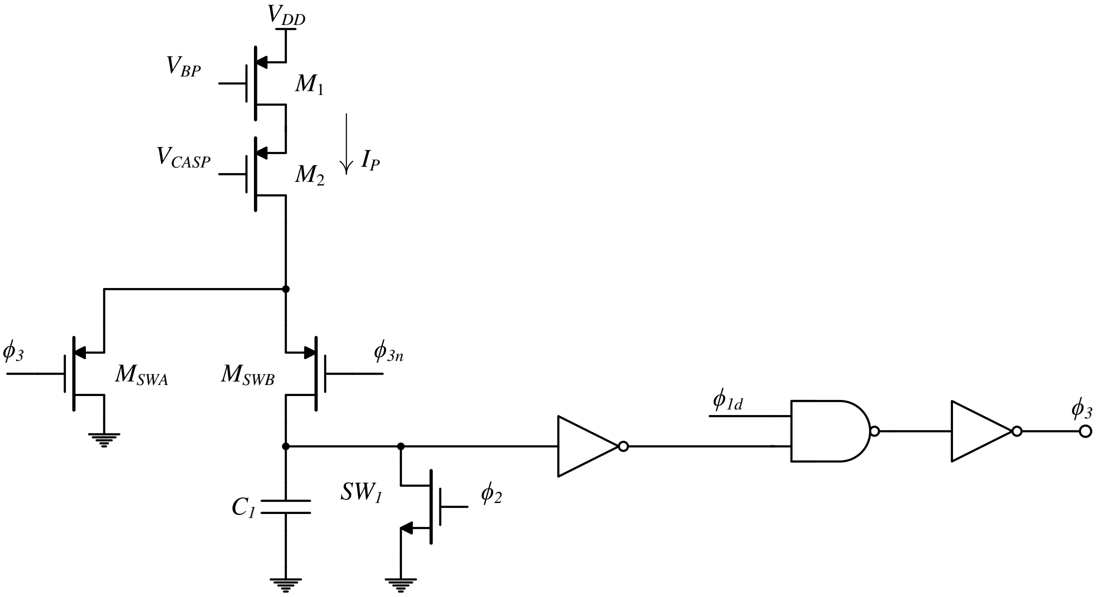


Figure 4.13: Schematic of the timing control circuit.

The noise from the charging current I_P will translate into jitter noise when the voltage across the capacitor C_1 crosses the threshold voltage V_M of the inverter. The rms jitter can be expressed as

$$\sigma_t^2 = \overline{v_n^2}\left|\frac{V_M}{T_i}\right|^{-2} \tag{4.1}$$

The expression for the noise voltage $\overline{v_n^2}$ was found in chapter 3 and is given by $\frac{4\gamma KTV_M}{V_{ov}C}$. The final expression for timing jitter is

$$\sigma_t^2 = \frac{4\gamma KT{T_i}^2}{V_{ov}C_1\,V_M} \tag{4.2}$$

Considering a capacitor size of 1 pF, an integration time of 3 ns and a threshold voltage $V_M = 600$ mV leads to an rms jitter of 1.6 ps.

4.2.6 Current generation and distribution

Figure 4.14 shows the circuit schematic of a complete current reference generator. Capacitors C_1, C_2 and C_F were set to 1 pF, 0.4 pF and 1 pF, respectively. The bottom plate of C_1 and C_2 was connected to ground to reduce parasitic effects. Simulations showed that the reference current generated varies less than ±5% considering PVT variations and ±3% variation in voltage reference V_{REF}. This voltage is generated by a band-gap circuit which is available in most ADCs.

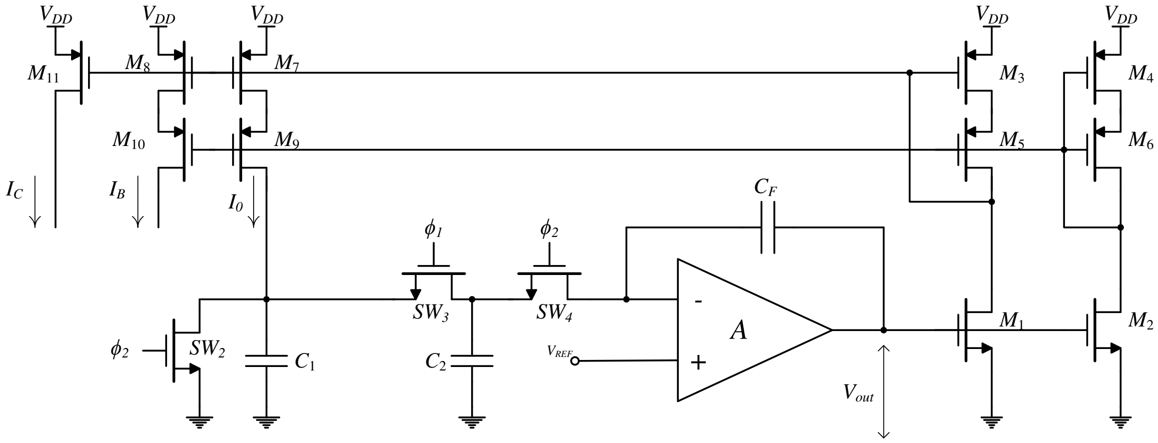

V_{DD}
V_{DD}
V_{DD}
V_{DD}
V_{DD}
M_{11}
M_8
M_7
M_3
M_4
M_{10}
M_9
M_5
M_6
I_C
I_B
I_0
C_F
ϕ_1
ϕ_2
SW_3
SW_4
-
A
+
M_1
M_2
ϕ_2
SW_2
C_1
C_2
V_{REF}
V_{out}

Figure 4.14: Circuit diagram of the implemented current reference.

The reference current is mirrored and a current is generated for each stage as shown in Figure 4.15. The mirrored currents are routed to each stage and then a local biasing circuit generates biasing voltages V_B and V_{CAS}. Routing a current is preferred to routing a voltage to each stage because the matching depends only on local transistor matching rather than matching across the chip.

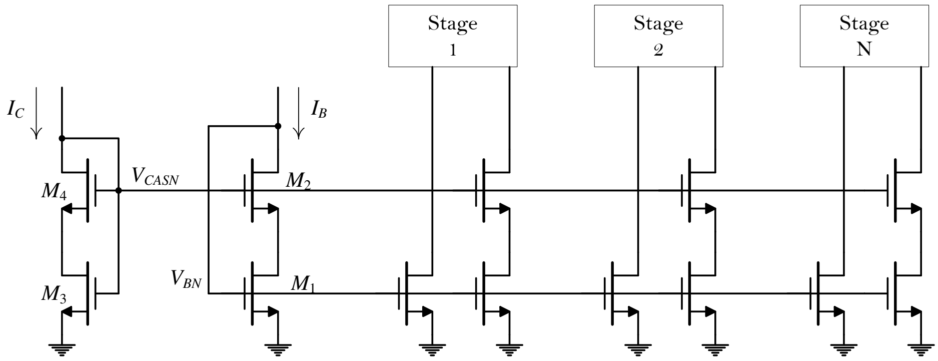

Stage 1
Stage 2
Stage N
I_C
I_B
M_4
V_{CASN}
M_2
M_3
V_{BN}
M_1

Figure 4.15: Current distribution for the stages.

4.3 Summary

The adopted architecture and the circuits used in the implementation of the 10-bit pipeline ADC were described. The MDAC has been implemented with a new structure that does not require a reference buffer to define the reference levels for the MDAC. Instead, this block has been replaced by a current source and the biasing reference currents were generated by a switched capacitor current reference. The current mirror architecture was chosen to implement the amplifier of the pipelined stages. Details of the implementation and simulations results for the opamp used in the first stage were presented. The design details for comparators used in sub-ADC and the back-end flash were also presented.

Chapter 5

Simulation Results

In this chapter the dynamic performance of the proposed ADC is validated through electrical simulation and exhaustive FFT analysis over process, supply and temperature (PVT) corners.

The block diagram of the proposed ADC is depicted in Figure 5.1. As already mentioned in Chapter 4 the ADC consists of a front-end S/H followed by 8 pipelined stages, and a final 2-bit flash quantizer. The bias voltages and currents are generated on-chip by a reference buffer and a switched-capacitor current reference generator. The reference buffers are only used to define the reference levels for the sub-ADCs. The power supply is divided in two domains (analog and digital). The analog supply (AVDD) powers the opamps, the bias circuitry and the comparators. The digital supply (DVDD) powers the clock circuitry and the digital logic. The external clock signal controls the sampling rate and the bias currents.

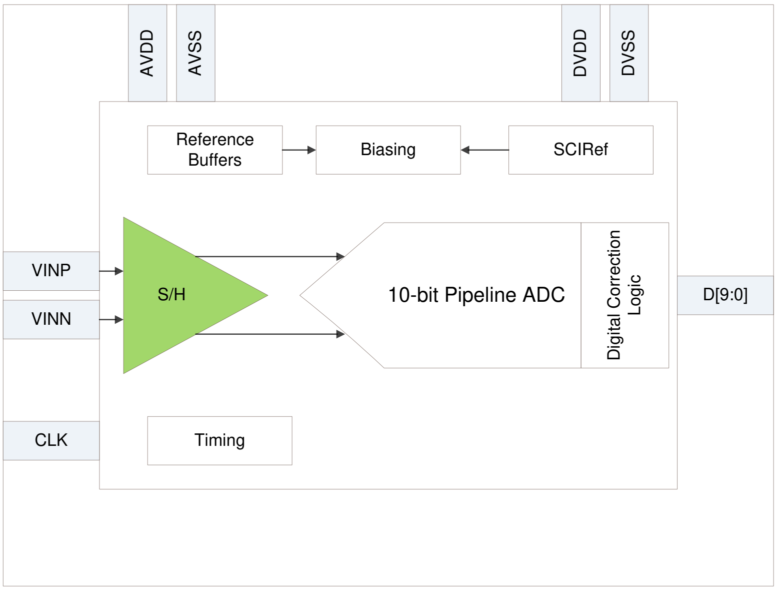

AVDD
AVSS
DVDD
DVSS
Reference Buffers
Biasing
SCIRef
VINP
VINN
S/H
10-bit Pipeline ADC
Digital Correction Logic
D[9:0]
CLK
Timing

Figure 5.1: Block diagram of the implemented ADC.

Figure 5.2 shows the frequency response to a near 10MS/s input signal frequency (F_{in}) and 40MS/s sampling frequency. The ADC achieves a SNDR of 59.8 dB and a THD of -68 dB.

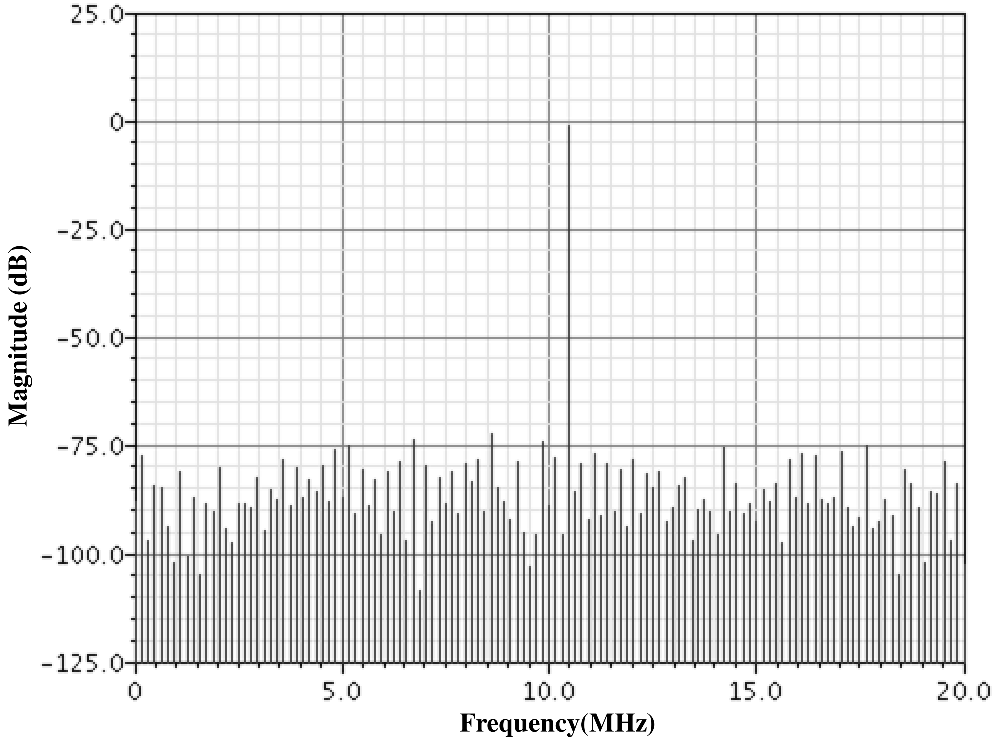


Figure 5.2: 256-point FFT for F_s = 40MS/s and A_{in} = -0.5 dBFS.

The dynamic performance of the ADC was evaluated by sweeping the sampling frequency (F_s) at F_{in} = 10MHz. The ENOB is plotted as function of sampling frequency in Figure 5.3. The SNDR and SNR are shown in Figure 5.4. Figure 5.5 depicts the SFDR and THD.

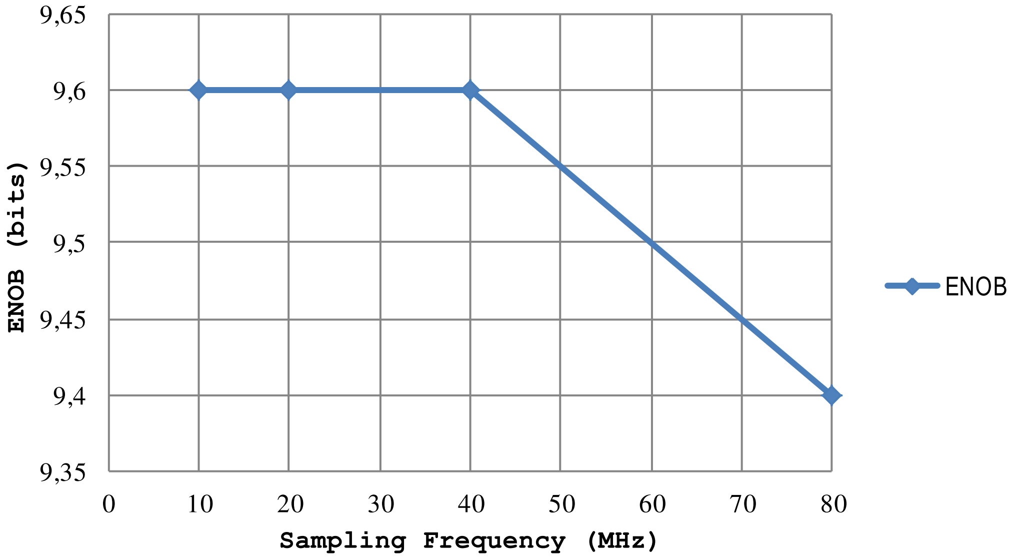


Figure 5.3: Simulated ENOB *versus* *F*s (-0.5 dBFS and *F*in = 10 MHz).

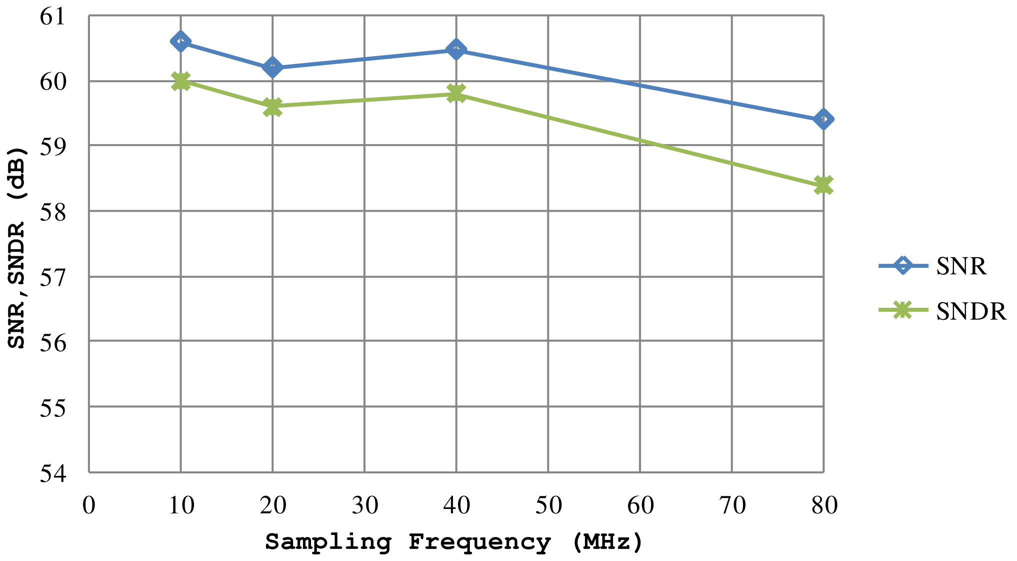


Figure 5.4: Simulated SNR and SNDR *versus* *F*s (-0.5 dBFS and *F*in = 10 MHz).

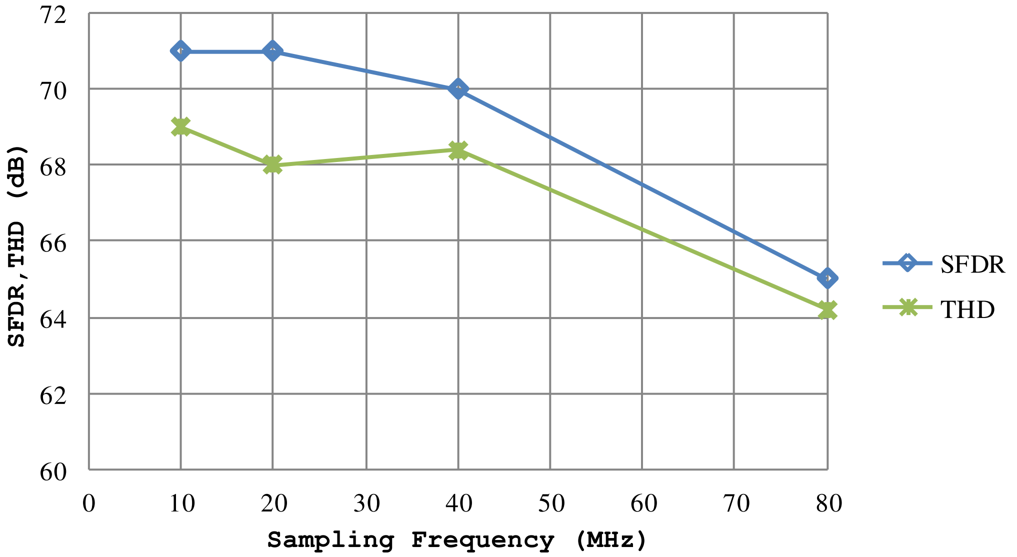


Figure 5.5: Simulated SFDR and THD *versus* *F*s (-0.5 dBFS and *F*in = 10 MHz).

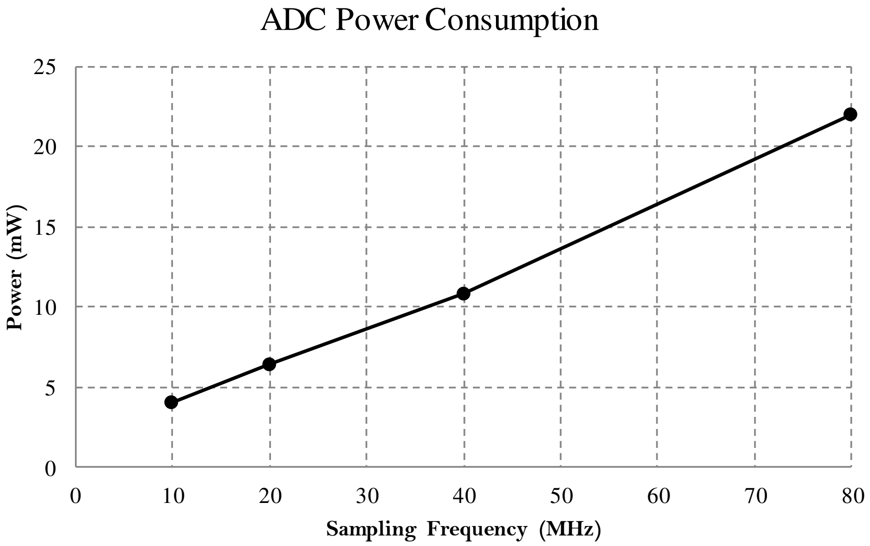


Figure 5.6: Power consumption vs. Sampling Frequency.

The power consumption is plotted as a function of sampling frequency in Figure 5.6. At 40 MS/s the ADC dissipates 10.8 mW (7.2 mW/3.6 mW analog/digital) from a 1.2 V power supply. The Power consumption scales almost linearly with sampling rate. The total power of Pipeline (ADC excluding the auxiliary circuitry) is distributed through the amplifiers (66%), the clock bootstrapping circuitry (23%) and the sub-ADCs (11%). The power of auxiliary circuitry corresponds to 20% of total power of ADC. This power is distributed through the reference buffer (6%), current reference generator (9%), biasing circuit (2%) and clocking phase buffers (2%). Compared to a conventional design the power of reference circuitry (reference buffer + current reference generator) is reduced from 25% to 15% of the total power consumption.

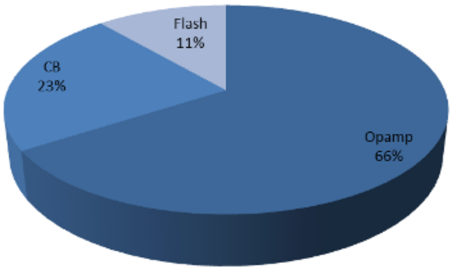


Figure 5.7: ADC Power distribution (excluding auxiliary circuitry).

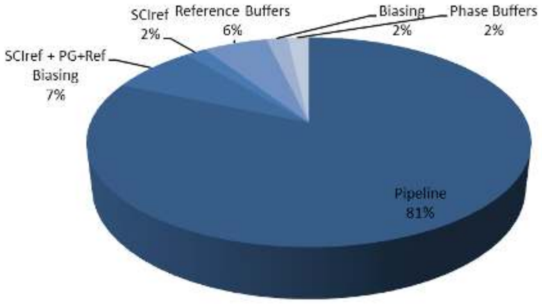


Figure 5.8: ADC Power distribution.

The dynamic performance was also evaluated over PVT corners. It was considered an 8% variation on power supply, a minimum temperature of -40 ° C and a maximum of +125 ° C. Table 5.1 summarizes the results.

Table 5.1: Performance results.

Sampling Frequency 10MS/s Input signal frequency 2 MHz					
	MIN	TYP	MAX	UNIT	Power (mW)
SNR	58	60.6	60.6	dB	4
SFDR	61	71	71	dBc	
THD	60	69	69	dB	
SNDR	56	60	60	dB	
ENOB	9	9.6	9.6	bit	

Sampling Frequency 20MS/s Input signal frequency 4 MHz					
	MIN	TYP	MAX	UNIT	Power (mW)
SNR	58	60.2	60.8	dB	6.4
SFDR	61	71	72	dBc	
THD	60	68	71.2	dB	
SNDR	56	59.6	60.4	dB	
ENOB	9	9.6	9.74	bit	

Sampling Frequency 40MS/s Input signal frequency 8 MHz					
	MIN	TYP	MAX	UNIT	Power (mW)
SNR	58.4	60.48	60.48	dB	10.8
SFDR	61	70	70	dBc	
THD	60	68.4	68.4	dB	
SNDR	56	59.8	59.8	dB	
ENOB	9	9.6	9.6	bit	

Sampling Frequency 80MS/s Input signal frequency 10 MHz					
	MIN	TYP	MAX	UNIT	Power (mW)
SNR	58.2	59.4	59.6	dB	22
SFDR	56	65	68	dBc	
THD	56	64.2	67.6	dB	
SNDR	54	58.4	59	dB	
ENOB	8.6	9.4	9.5	bit	

The results presented above only include quantization noise. In order to analyze the circuit performance in the presence of the different noise components, the 10-bit ADC is simulated using a transient noise analysis. The performance results simulated at 40 MS/s with 10 MHz input signal are summarized in Table 5.2. At this sampling frequency the ADC achieves a FOM of 460 fJ/step.

Table 5.2: Summary of the simulated ADC key performance parameters.

Parameter	Simulation results
Technology	65nm TSMC Logic LP Process
Supply Voltage	1.2 V ±8%
Sampling rate	20-80 MS/s
Input Range	1.0Vpp Diff.
Resolution	10-bit
Power Dissipation	10.8 mW @40MS/s
SNDR	57.2 dB
ENOB	9.2 bits
FOM	460 fJ/step

Summary

In this chapter, the full ADC was characterized by way of its dynamic performance. The simulations results show that the ADC can achieve an ENOB of 9.2 bits and a THD of -68 dB when operates at $F_s = 40$ MS/s. The key simulated results were summarized in Table 5.2. The power simulations for each building block of the ADC were presented in Figure 5.8.

Chapter 6

Conclusions

This chapter summarizes the main conclusions and discusses the areas for future work.

6.1 Conclusions

Pipeline ADCs are the most attractive solution in high-speed medium-to-high resolution applications. Within this architecture, the residue amplifiers, the front-end S/H and the reference circuitry dominate the power dissipation. However, most of the reported pipeline ADCs in the literature only addresses the power of the amplifiers and the S/H ignoring the reference circuitry. The solutions to reduce power of the S/H are to remove the S/H or embed the S/H within the first stage. Digitally assisted analog design and comparator-based switched-capacitor circuit are published as alternatives to high gain amplifiers.

This work presents the design of a pipeline ADC that does not require big reference buffers to generate stable reference levels for the MDAC. This is achieved replacing the conventional MDAC by a closed-loop MDAC circuit that realizes the DAC function in current mode. The technique has been demonstrated in the design of a 10 bit, 40 MS/s pipeline ADC in a 65 nm CMOS technology. The reference currents were generated on-chip by a switched-capacitor current reference generator that shows low power dissipation and does not require extra pins. The performance of the overall A/D conversion system was verified by electrical simulations and FFT analysis. The simulations results show that the ADC dissipates 10.8 mW and achieves an ENOB of 9.2 bit and a THD of -68 dB when operates at a sampling frequency of 40MS/s. This translates in a FOM of 460 fJ/step.

The ADC shows power savings of 40% in the reference circuitry and 30% in the residue amplifiers. The proposed architecture enables a 25% reduction on the power dissipation when comparing to a traditional pipeline ADC where power hungry voltage buffers are employed to generate the DAC reference levels for the MDAC.

6.2 Future Work

Some suggestions for future work:

- Implement the physical layout of the ADC and execute post-layout simulations to examine the performance degradation in the presence of parasitic capacitance.

- Extend the architecture used in this work to higher resolution and/or speed. Due to the simple structure of the pipeline ADC this can be done easily. To reach higher resolutions, only the front-end stages such as the S/H and the first-stage need to be designed. The rest of the stages can be re-used from this work.

- Characterize the non-linearity errors from the current sources and develop methods to minimize these errors.

- Implement the residues amplifiers with a class AB two-stage amplifier. A two-stage amplifier reduces the input capacitance and maximizes the feedback factor, while a class AB operation reduces the static power dissipation.

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