Plasma Enhanced Atomic Layer Deposition of Al_2O_3/SiO_2 MIM Capacitors

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***Abstract*— Metal–insulator–insulator–metal (MIIM) capacitors with bilayers of Al_2O_3 and SiO_2 are deposited at 200 °C via plasma enhanced atomic layer deposition. Employing the cancelling effect between the positive quadratic voltage coefficient of capacitance (αVCC) of Al_2O_3 and the negative αVCC of SiO_2, devices are made that simultaneously meet the International Technology Roadmap for Semiconductors 2020 projections for capacitance density, leakage current density, and voltage nonlinearity. Optimized bilayer Al_2O_3/SiO_2 MIIM capacitors exhibit a capacitance density of 10.1 fF/μm^2, a leakage current density of 6.8 nA/cm^2 at 1 V, and a minimized αVCC of -20 ppm/V^2.**

***Index Terms*— Al_2O_3/SiO_2, metal-insulator-metal capacitors, MIMCAPs, MIIM, plasma enhanced atomic layer deposition, PEALD, quadratic voltage coefficient of capacitance, αVCC.**

I. INTRODUCTION

BACK end of line (BEOL) metal-insulator-metal capacitors (MIMCAPs) reduce the need for discrete off-board components and have become core passive devices in integrated circuits (IC). Applications of MIMCAPs include analog-to-digital converters, analog noise filters, DC voltage decoupling, and electrostatic discharge protection. According to the 2020 node of the International Technology Roadmap for Semiconductors (ITRS), scaling the area of these devices for analog/mixed-signal ICs will require increasing capacitance density (to greater than 10 fF/μm^2) while simultaneously maintaining low voltage nonlinearity (less than 100 ppm/V^2, characterized by the quadratic voltage coefficient of capacitance, αVCC) and low leakage current density (less than 10 nA/cm^2 at 1V) [1]. In addition to these conflicting performance requirements, BEOL processing allows for temperatures of no more than 400 °C [2].

Increasing capacitance density may be achieved either by decreasing the insulator film thickness or by introducing high dielectric constant (κ) materials. Simply decreasing the insulator film thickness leads to increased tunneling leakage as well as increased voltage nonlinearity [3], [4]. On the other hand, most high-κ insulators also have drawbacks such as large positive αVCCs, small metal-insulator barrier heights, and increased conduction through defect levels [5]. Thus, single insulator devices have been unable to simultaneously meet all three performance projections of future ITRS nodes. A promising approach to meeting all of these competing performance needs is to use multi-layer insulator stacks to combine materials with complementary properties (e.g. a high-κ, positive αVCC insulator with a low leakage, negative αVCC insulator) [6]–[12]. Previous reports of multi-insulator structures that meet or come close to meeting upcoming ITRS projections are listed in Table II. Note however that these previous studies employ either complex or uncommon materials, break vacuum between insulating layers, or are processed outside the specified BEOL temperature limit.

In the present work, Al_2O_3/SiO_2 bilayers are investigated for potential use in BEOL RF MIMCAPs. Al_2O_3 and SiO_2 are attractive due to their large metal-insulator barrier heights, high dielectric breakdown strength, and common usage in IC fabrication. In addition, SiO_2 is one of the few materials to exhibit a negative αVCC and thus can be used in combination with the positive αVCC of Al_2O_3 to target ultra-low device voltage nonlinearity through αVCC canceling [7]. Plasma enhanced atomic layer deposition (PEALD) is used to deposit high quality pin-hole free nanolaminate Al_2O_3/SiO_2 stacks at low temperature without breaking vacuum. The self-limiting reactions of PEALD enable precise control over film thickness, which is critical for optimizing the αVCC cancelling effect for ultra-thin films. The capacitance density, leakage current density, and αVCC of Al_2O_3/SiO_2 MIIMCAPs are benchmarked against future ITRS projections.

II. EXPERIMENTAL

$Si/SiO_2/Ta/TaN$ substrates with the SiO_2 layer planarized via chemical mechanical polishing were used as the bottom electrodes. PEALD of Al_2O_3 and SiO_2 was performed at 200 °C in a Picosun SUNALE R-200 reactor using alternating N_2-purge-separated pulses of O_2 and either trimethylaluminum (TMA) or bis(diethylamino)silane (BDEAS), respectively. TMA was held at 17 °C and BDEAS held at 55 °C. The deposition rates of Al_2O_3 and SiO_2 were approximately 0.10 nm/cycle and 0.11 nm/cycle, respectively. The Al_2O_3 layer was always deposited first. 250 μm diameter evaporated Al dot top contacts with areas of $\sim$0.05 mm^2

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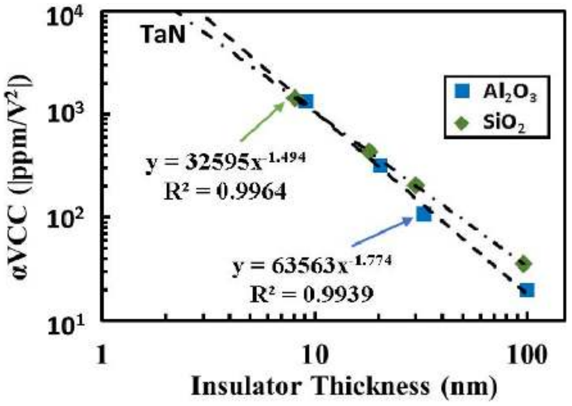

Fig. 1. Plot of αVCC for Al_2O_3 (blue squares) and $|\alpha VCC|$ for SiO_2 (green diamonds) vs. film thickness (d_{ox}). Dashed lines indicate power law fits.

were defined via shadow mask. The area of each device was measured and used for area normalizations. The average error in the area measurement is found to be +/−1.8%. Film thickness of select samples was measured using either an FEI Tecnai F20 high-resolution transmission electron microscope (TEM) or a J. A. Woollam M2000 spectroscopic ellipsometer. 100 kHz capacitance vs. voltage (CV) measurements were conducted using an Agilent E4980. Current vs. voltage (IV) measurements were taken using an Agilent B1500A. All electrical tests were conducted with the bottom electrode held at ground and performed in the dark at a controlled 25 °C. CV measurements were swept to approximately one-half breakdown voltage in order to avoid excessive stress during testing. To reduce displacement current, CV and IV measurements were performed at sweep rates of 0.2 V/s.

III. RESULTS AND DISCUSSION

The voltage nonlinearity of MIMCAPs can be described by the quadratic equation, $\Delta C/C_0 = \alpha V^2 + \beta V$. Shown in Fig. 1, the αVCC for Al_2O_3 and $|\alpha VCC|$ for SiO_2 are plotted together as a function of single layer insulator thickness. A simple power law was found to fit well the thickness dependence of αVCC. Combining the power law fits with the capacitive voltage divider equation, approximate layer thicknesses were estimated for Al_2O_3/SiO_2 bilayers that simultaneously meet ITRS projections for capacitance density and αVCC.

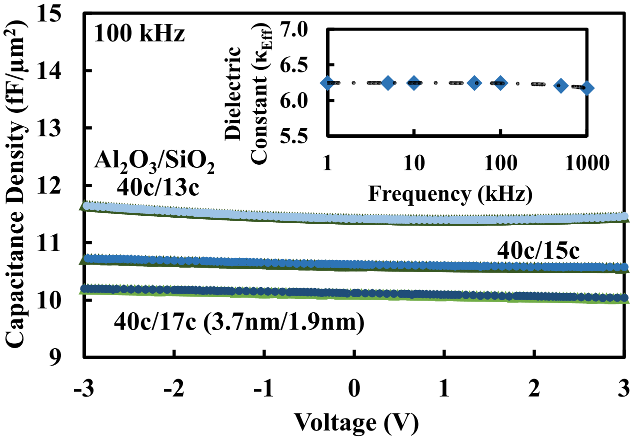

Fig. 2. Forward (blue) and reverse (green) sweeps of capacitance density vs. voltage for $TaN/Al_2O_3/SiO_2/Al$ stacks targeting ITRS 2020. Inset: the effective dielectric constant vs. frequency for the 3.7nm/1.9nm device.

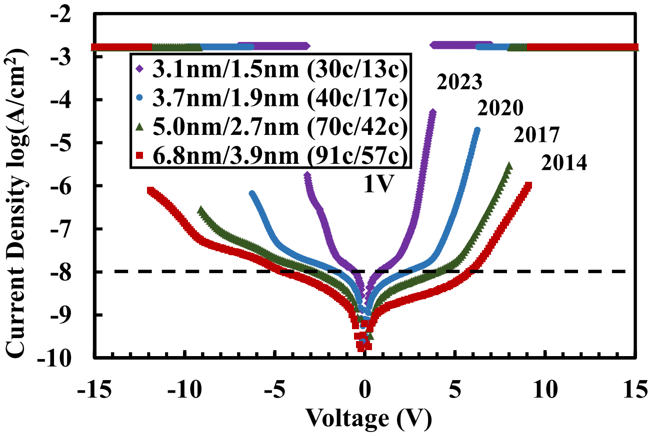

Fig. 3. Current density vs. voltage sweeps for $TaN/Al_2O_3/SiO_2/Al$ stacks targeting various ITRS nodes. The estimated thickness and number of PEALD cycles for each insulator pair are included in the legend.

Shown in Fig. 2 are forward/reverse capacitance density vs. voltage sweeps for MIIM devices with 40c of Al_2O_3 and either 13c, 15c, or 17c of SiO_2, where "c" represents the number of PEALD cycles. As the difference in thickness between these ultra-thin film stacks is difficult to measure accurately, the number of PEALD cycles is used for identification. The 40c/17c Al_2O_3/SiO_2 MIIM devices (measured via TEM to be approximately 3.7 nm/1.9 nm) were found to meet the ITRS 2020 projection for capacitance density with 10.1 fF/μm^2 and a minimized αVCC of −20 ppm/V^2. Note that optimized αVCC values are not exactly as predicted by simple theory which considers only "bulk" αVCC mechanisms [7]. αVCC mechanisms are not well understood [4] and the discrepancy is likely due to contributions of secondary nonlinearity mechanisms [12] such as electrode effects [13], [14]. As shown in the inset, the effective dielectric constant of these devices shows little frequency dependence up to 1 MHz. A slight negative β can be observed for all of these devices, which might be attributed to the electrode work function difference. The thickness control of PEALD is a clear advantage for minimizing αVCC. As seen in Fig. 2, the difference between the device with 300 ppm/V^2 (40c/15c) and the device with −20 ppm/V^2 (40c/17c), was only 2 PEALD cycles of SiO_2.

Current density vs. voltage sweeps for Al_2O_3/SiO_2 stacks targeting future ITRS nodes are shown Fig. 3. The small asymmetry seen between positive and negative polarity likely arises from (i) the work function difference of Al (4.2 eV) vs. TaN (4.6 eV) electrodes and (ii) the presence of deep level defects in the SiO_2 which may enable trap-assisted-tunneling at low bias [5]. The intersection between the vertical and horizontal dashed lines indicates the ITRS maximum leakage limit of 10 nA/cm^2 at 1V. Results are summarized in Table I. The 3.7 nm/1.9 nm (40c/17c) Al_2O_3/SiO_2 device meets all ITRS 2020 projections with a low $\alpha VCC/C_{ox}^2$ of

TABLE I

COMPARISON OF Al_2O_3/SiO_2 STACKS MEETING INCREMENTAL ITRS NODES

ITRS Node	Al_2O_3/SiO_2 (nm)	C/A (fF/μm^2)	αVCC (ppm/V^2)	J at 1V (A/cm^2)	J at -1V (|A|/cm^2)
2023	3.1 / 1.5	12.8	- - -	1.22×10^{-8}	1.43×10^{-8}
2020	3.7 / 1.9	10.1	-20	6.79×10^{-9}	8.65×10^{-9}
2017	5.0 / 2.7	7.9	20	2.75×10^{-9}	5.24×10^{-9}
2014	6.8 / 3.9	5.6	14	1.34×10^{-9}	2.83×10^{-9}

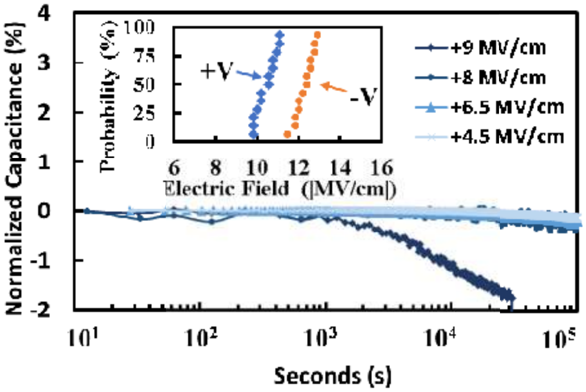

Fig. 4. Capacitance variation vs. positive constant voltage stress time. Inset shows plot of voltage ramped breakdown for positive and negative polarity.

TABLE II

COMPARISON OF LOW VOLTAGE NONLINEARITY MIIM CAPACITORS

Dielectric Stack	Film Thickness (nm)	C_{ox} (fF/μm^2)	αVCC (ppm/V^2)	J at 1V (A/cm^2)	Deposition Method	Dep/Anneal Temperature (°C)
HfO_2/SiO_2 [7]	12/4	6	14	2.0×10^{-9}	ALD/ PECVD	420
Sm_2O_3/SiO_2 [8]	7.5/4	7.3	-46	1.8×10^{-8}	Sputter/ PECVD	420
Er_2O_3/SiO_2 [9]	8.8/3.0	7	-73	4.2×10^{-9}	Sputter/ PEALD	400
STO/ZrO_2 [6]	20/20	11.5	-60	3.5×10^{-8} (at 2V)	Sputter/ MOCVD	550
$STO/Al_2O_3/STO$ [10]	25.5/1.0/25.5	19.1	610	1.0×10^{-9}	ALD	600
ZTO/BZTO [11]	17/7	13.4	14	7.5×10^{-9}	E-Beam	400
$SiO_2/HfO_2/SiO_2$ [12]	3/4/3	12.4	32	1.0×10^{-9}	ALD	300
Al_2O_3/SiO_2 This Work	3.7/1.9	10.1	-20	6.8×10^{-9}	PEALD	200
ITRS 2020	- - -	10	< 100	$< 1.0 \times 10^{-8}$	- - -	400 [2]

0.2 $\mu m^4/V^2 fF^2$ (a figure of merit proposed in [6]). Targeting film thicknesses to meet the ITRS 2023 capacitance density requirement resulted in leakage current density exceeding the 10 nA/cm^2 limit at 1V. Reduced leakage, which would possibly allow further scaling of this stack, could likely be achieved either by either the use of larger work function electrodes to increase the metal-insulator barrier heights or annealing to reduce defect density. The use of low oxygen affinity ($-\Delta H_{OX}$) metals may also reduce αVCC.

In Fig. 4 the 3.7 nm/1.9 nm (40c/17c) Al_2O_3/SiO_2 device shows little variation with positive constant voltage stress time at fields below 9 MV/cm which, as seen in the inset with voltage ramped breakdown, is close to the breakdown strength of this stack. The difference in breakdown between positive and negative polarities is due to the built-in field of the electrodes. The negative polarity requires higher field to overcome the built-in field.

IV. CONCLUSION

Al_2O_3/SiO_2 bilayers deposited via PEALD at 200 °C are investigated for applications in MIIM capacitors. An insulator stack consisting of 3.7 nm of Al_2O_3 and 1.9 nm of SiO_2 demonstrates a capacitance density of 10.1 fF/μm^2, a leakage current density of 6.8 nA/cm^2 at 1V, and an αVCC of -20 ppm/V^2. Benchmarking our results against the ITRS roadmap, it is seen that the Al_2O_3/SiO_2 stack simultaneously meets the 2020 node for capacitance density, leakage current density, and voltage nonlinearity projections with mainstream materials and low temperature processing.

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