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Plasma-etched pattern transfer of sub-10 nm structures using a metal–organic resist and helium ion beam lithography

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ABSTRACT

Field emission devices are promising candidates to replace silicon FinFETs as next-generation nanoelectronic components. For these devices to be adopted, nanoscale field emitters with nanoscale gaps between them need to be fabricated, requiring the transfer of e.g. sub-10 nm patterns with sub-20 nm pitch into substrates like silicon and tungsten. New resist materials must therefore be developed that exhibit the properties of sub-10 nm resolution and high dry etch resistance. A negative tone, metal–organic resist is presented here. It can be patterned to produce sub-10 nm features when exposed with helium ion beam lithography at line doses on the order of 10s of pC/cm. The resist was used to create 5 nm wide, continuous, discrete lines spaced on a 16 nm pitch in silicon, and 6 nm wide lines on 18 nm pitch in tungsten, with line edge roughness of 3 nm. After the lithographic exposure, the resist demonstrates high resistance to silicon and tungsten dry etch conditions (SF_6 and C_4F_8 plasma), allowing the pattern to be transferred into the underlying substrates. The resist's etch selectivity for silicon and tungsten was measured to be 6.2:1 and 5.6:1, respectively; this allowed 3-4 nm thick resist films to yield structures that were 21 and 19 nm tall, respectively, while both maintained sub-10 nm width on sub-20 nm pitch.

Keywords: metal–organic resist, ion beam resist, helium ion beam lithography, high resolution pattern, high dry etch resistance

The ability of integrated circuit technology to follow Moore's law has depended on the continuous reduction in the size of field-effect transistors (FETs), first in the planar MOSFET architecture and now more recently in the 3D FinFET architecture. This has been accomplished by reducing the FET's channel length, width and gate oxide thickness, and by changing the gate dielectric material, according to Dennard scaling rules.[1] Unfortunately, these scaling rules have begun to break down because as the gate length is reduced to dimensions of 32 nm and smaller, the supply voltages need to be scaled down as well, but doing so does not provide enough voltage to turn on the p–n junction. Further, power density in the newest microprocessors has become so large that powering all transistors simultaneously would rapidly exceed the thermal power budget for the chip, resulting in diminished performance, decreased lifetime and, eventually, permanent device failure.

Overheating can be addressed by powering 50% of transistors on a single chip on a single clock cycle,[2] but this presents a significant technical design challenge. Considering these problems together, it has been predicted by the International Technology Roadmap for Semiconductors (ITRS) that it will no longer be economically feasible to decrease FET device dimensions past the "7 nm node,"[3] thus imbuing a sense of uncertainty on the future direction of the semiconductor industry.

Field emission devices are promising candidates to succeed silicon FinFETs because they can operate in high power density regimes where chip temperatures can reach 300 °C and above. Solid-state transistors fail in this regime because the p–n junction's functionality is lost when electrons in the p-doped regions are thermally excited to the same conduction electron concentration as in the n-doped regions.[4] Conversely, field emission devices remain operational because as the temperature is elevated, the current remains exponentially dependent on the field until the temperature is sufficient to initiate thermionic emission, which usually occurs hundreds of degrees above 300 °C.[5] These devices are also attractive because they are capable of operating at frequencies of hundreds of GHz; this has been achieved by fabricating 150 nm vacuum gaps using optical lithography and resist trimming.[6] Other researchers recently demonstrated that when sub-50 nm emitter–collector gaps were fabricated, electric fields high enough for field emission could be achieved at less than 10 V; the devices were CMOS-compatible, functional at atmospheric pressure, and able to be independently gated on a single integrated chip.[4] Turn-on voltages can be further reduced by fabricating sharper emitters with smaller emitter–collector gaps, incentivizing creation of new fabrication techniques that yield tightly-spaced, sub-10 nm structures.

While electron beam lithography (EBL) offers high resolution patterning to create sub-10 nm structures in resist,[7] it is difficult to pattern these with high density, e.g. with sub-10 nm wide lines spaced less than 20 nm apart. This is because secondary, Auger and backscattered electrons (SEs, AEs and BSEs) scatter in between the nanostructures during patterning, which exposes the resist in that space, resulting in bridges between lines following the development process.[8] This "proximity effect" limits the resolution of the pattern that can be produced. To alleviate this issue, a technique that uses a focused helium ion beam instead of an electron beam has been explored over the past decade. Previous helium ion beam lithography (HIBL) studies have demonstrated a reduced proximity effect[9] – owing to less backscattering, a smaller interaction volume with the substrate, and sub-nm beam diameter[10] – resulting in sub-10 nm resolution.[11] This is accompanied by orders of magnitude higher resist sensitivity than can be achieved with EBL,[12] due to a higher SE yield per incident helium ion compared to each incident electron.[13]

Once the pattern has been defined in resist by lithography, it must be transferred into the underlying material, which is often done using inductively-coupled plasma reactive-ion etching (ICP–RIE). The most common metal used to produce field emission devices is tungsten, which exhibits a low work function and has a high thermal conductivity, preventing the device from being destroyed via Joule heating.[4] Transferring the desired nanoscale pattern (e.g. sub-10 nm structures with sub-10 nm gaps in between) into tungsten is a challenge because the probability of landing ions in ever smaller gaps becomes ever lower. This leads to a decrease in etch efficiency, which inherently decreases the etch rate and selectivity. To increase etching efficiency, ICP forward power must be increased, but this also increases the etch rate of the resist. The thickness of the resist would then need to be increased in order to achieve the desired etch depth, which would require a higher dose, which in turn would reduce the resolution of the pattern. To avoid this problem, one may use a hard mask to withstand the aggressive nature of the plasma etch,[4] but doing this introduces more

processing steps and leads to higher production costs. Another route is to enhance the etch selectivity of the resist by introducing into the molecular chemistry a metal species that effectively oxidizes upon lithographic exposure to become the hard mask. This has previously been demonstrated by our group using supramolecular, Ni- & Cr-containing assemblies while maintaining sub-10 nm patterning capability,[14] albeit at relatively low pattern density compared to what is needed for modern nanoelectronics.

In this Letter, a metal–organic, negative tone resist candidate, $Cr_8F_8(O_2C^tBu)_{16}$ (Figure 1), first introduced by our group in reference 15 and henceforth denoted as Cr_8F_8(Pivalate)$_{16}$, is presented. It is formed by the binding of eight chromium atoms (in green in Figure 1) in a ring-like structure, with an exterior composed entirely of *tert*-butyl groups (pivalates).[15] The pivalates provide a high solubility in non-polar solvents, which allows the resist molecule to be dissolved in hexane and spun onto substrates (e.g. Si and W). The molecule achieves high-resolution patterning because it is simultaneously low density (ρ = 1.212 g cm^{-3}), meaning it does not have many lateral-scattering centers for the lithography beam to interact with as it travels through, and has a high molecular weight (2192 g mol^{-1}), meaning that the number of resist molecules that are required to produce a thin film is significantly reduced, leading to a high-resolution pattern. Upon exposure, SEs and AEs break carbon bonds in the resist, liberating some C and O while permitting other O and Cr to react to form a chromium–oxide hard mask that is particularly resistant to the ICP–RIE chemistry used to etch both silicon and tungsten.[14]

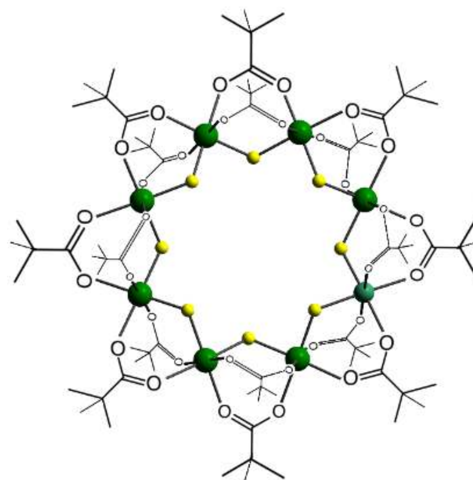

Figure 1 The structure of the Cr_8F_8(Pivalate)$_{16}$ molecule in a ball-and-stick representation. Chromium atoms are green and fluorine atoms are yellow. Hydrogen atoms are omitted for clarity.

Prior to the spin-on application of Cr_8F_8(Pivalate)$_{16}$ resist, atomic force microscopy (AFM) was used to evaluate the surface morphology of silicon and tungsten substrates (Figure 2a-b). The root mean square (RMS) roughness was measured to be 0.29 nm for silicon. For tungsten, which was sputter-deposited onto silicon as a 100 nm thick film on top of a 5 nm sputter-deposited titanium adhesion layer, the RMS roughness was 0.42 nm. The tungsten was 45% rougher than silicon; topographical contrast revealed that the film was comprised of nanograins that individually were ~5 nm wide and as long as 50 nm. For all sputter processes, wafers were first cleaned inside the chamber with argon plasma and targets were pre-sputtered for 60 seconds to remove surface oxides.

The exact nature of the resist film at this stage is uncertain. Previous studies of similar compounds sublimed onto gold show that an ordered monolayer forms,[17] but subsequent layers are not ordered as there are only weak Van der Waals interactions between the molecules of metal rings. The films formed here, shown here by AFM (Figure 2c-d) to be approximately 3.5 nm thick (approximately two layers), are therefore amorphous. The resist is monodispersed, and in some ways resembles the molecules studied by Ober and co-workers[18] that form molecular glasses rather than conventional polymeric resists. We have not observed a glass transition temperature as Cr_8F_8(Pivalate)$_{16}$ sublimes before such a transition is observed. This low sublimation temperature is again due to the very weak intermolecular forces within the resist films.

Samples were created by dicing wafers into 20 mm x 20 mm pieces. Both substrate types, bare silicon and tungsten-coated silicon, provided a smooth enough surface upon which sub-10 nm features could be clearly resolved. This is evident in Figure 3, which shows plan view helium ion microscope (HIM) images of $Cr_8F_8(Pivalate)_{16}$ resist nanostructures following HIBL and subsequent development in hexane. The $Cr_8F_8(Pivalate)_{16}$ resist (30 mg) was dissolved in hexane (3 g) and then the solution was filtered using a 0.2 μm polytetrafluoroethylene syringe filter before being spun onto substrates with a spin rate of 6000 rpm for 40 seconds, followed by a 100 ˚C soft bake for two minutes to evaporate the solvent. The spacing of adjacent lines (i.e. the pitch) was set to be 16-22 nm using a Raith ELPHY MultiBeam pattern generator, which controlled the helium focused ion beam (35 keV, 0.50 pA) on a Zeiss ORION NanoFab. The exposure clearing dose of the resist on each substrate was determined using a one-dimensional matrix of single-pixel-wide lines that were 5 μm long. The width of the line was therefore the width of the ion beam, which is estimated at 0.5 nm;[10] the beam step size was 1 nm. At any pitch, patterns were exposed in sets of 20 lines with one pass of the beam per line, and the line dose of each set ranged from 10 to 100 pC/cm with incremental steps of 1 pC/cm. Following lithography, the resist was developed in hexane for 10 seconds to dissolve away the unexposed resist, then blown dry with nitrogen.

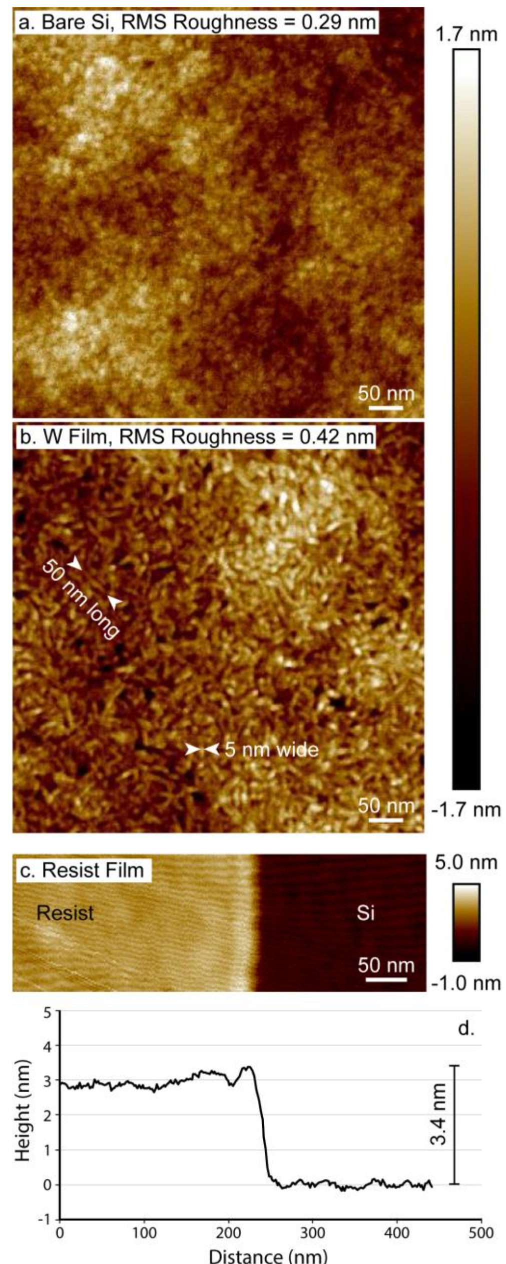

Figure 2 AFM images of substrates prior to spin-on application of resist: (a) silicon and (b) 100 nm tungsten film (on silicon). The (c) roughness and (d) thickness of patterned resist is also demonstrated by AFM.

It can be seen in Figure 3 that discrete, continuous lines were successfully patterned at all pitches on silicon, with no bridging between any adjacent lines. On tungsten, patterning was likewise successful at 18, 20 and 22 nm pitch; at 16 nm pitch (Figure 3h), the line uniformity was poor and bridging had occurred, a hallmark of being just beyond the lithographic resolving limit. The line width, on average, was measured to be 5.5 nm (standard deviation, σ = 0.9 nm) on silicon at 16 nm pitch and 5.6 nm (σ = 0.9 nm) on tungsten at 18 nm pitch. The line edge roughness (LER), defined as 3σ, was approximately 3 nm for both sets of Si and W lines. Tungsten performed slightly worse than silicon in both the minimum achievable pitch and minimum line width because tungsten has a significantly larger atomic number (Z = 74 for W, Z = 14 for Si) and therefore leads to a larger number of SEs and AEs generated by the primary ion beam; this effect is triggered by both incident electrons in EBL[16] and incident He ions in

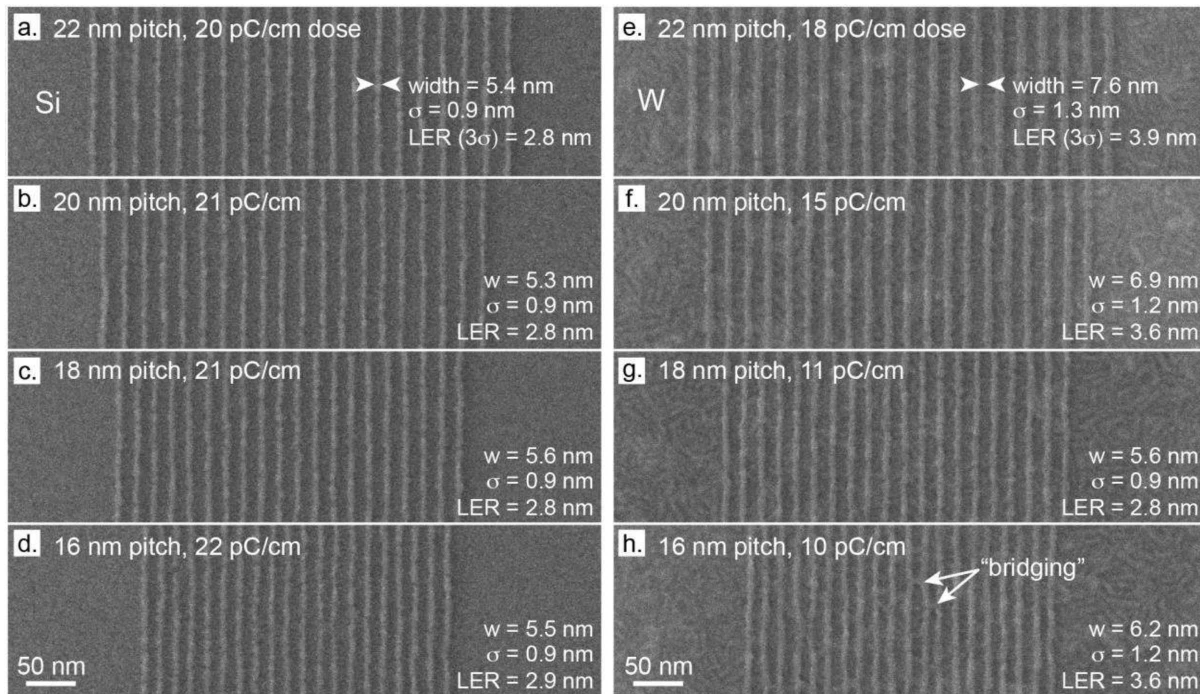

Figure 3 Plan view HIM images of lines spaced with pitches of 22, 20, 18 and 16 nm on silicon substrate (parts a-d, respectively) and on a 100 nm thick tungsten film that was sputter-deposited onto a silicon substrate (parts e-h, respectively). Average width (w), standard deviation (σ) and line edge roughness, LER (3σ), to the nearest 0.1 nm were determined using GenISys ProSEM software.

HIBL.[13] The ejected SEs can be calculated using the Joy model[19] to have a scattering angle of 80° relative to the incident beam vector,[20] which leads to the exposure of resist material adjacent to the beam's entry point. A similar mechanism is at play with low energy ion recoil events initiated by incident ions, which scatter SEs at the same high angle in addition to physically displacing atoms.[21] The more SEs and AEs that are generated, the wider the exposure radius is that surrounds the beam entry point, leading to wider lines and, when the pitch is too small, bridging between them. While this proximity effect diminishes the smallest achievable line width and pitch, the generation of more SEs and AEs also has the benefit of decreasing the necessary exposure dose, which was as much as 1.9 times lower at 18 nm pitch for tungsten (11 pC/cm) compared to silicon (21 pC/cm). The necessary exposure dose also decreased on tungsten as a function of decreasing pitch – whereas it did not for silicon – due to the intensity of the proximity effect when lines are written ever closer to each other on a high Z material. Based on these results, the outlook for patterning sub-10 nm wide lines on tungsten is that the achievable pitch may be slightly higher compared to silicon (18 versus 17 nm), in exchange for nearly half of the exposure dose. It must also be noted that these HIBL doses are an order of magnitude below the threshold dose at which He implantation has been shown to induce dislocation damage in Si.[22]

In Figure 4, the resist is shown at its smallest successfully-etched pitch for silicon (17 nm) and tungsten (18 nm), both in plan view (Figure 4a and d) and when tilted to 87° to better show its thickness (Figure 4b and e). The same spin settings were used to apply the resist to both silicon and tungsten. Resist thickness was measured at the front edge of the titled lines (the higher tungsten roughness perhaps accounts for the thinner measurement) and confirmed by AFM (Figure 2c and d). It should be noted that the resist had been changed to a

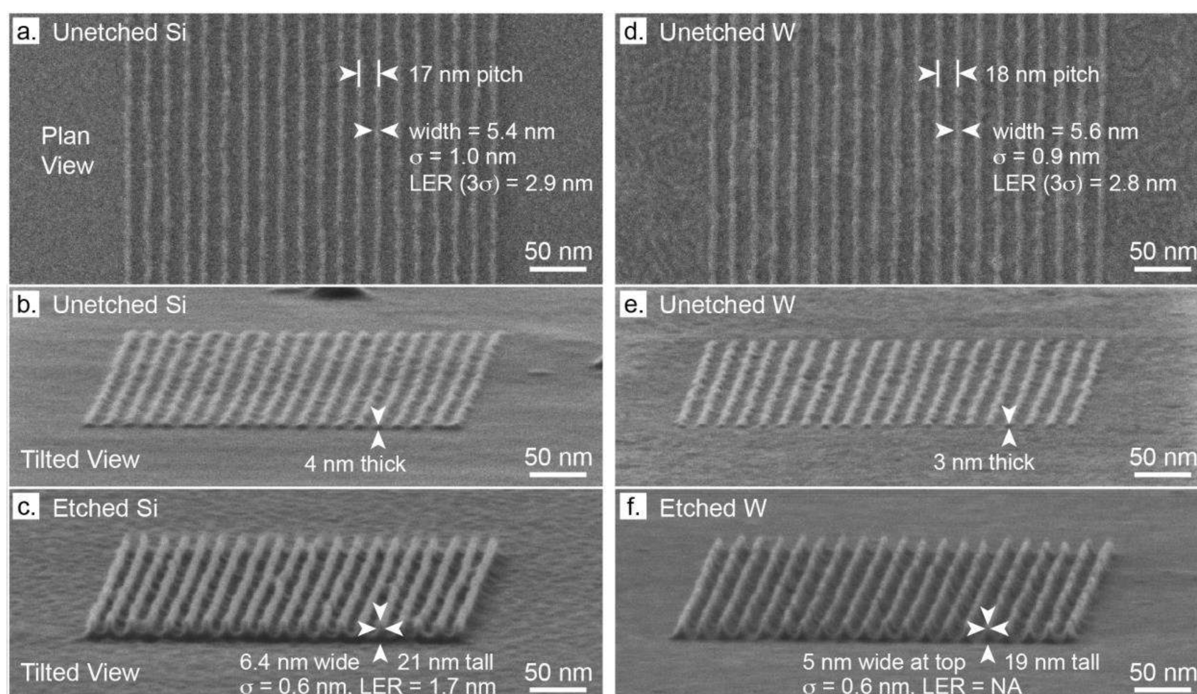

Figure 4 HIM images of lines spaced with pitches of 17 and 18 nm on silicon substrate (parts a-c) and on a 100 nm thick tungsten film that was sputter-deposited onto a silicon substrate (parts d-f), respectively. In the top row of images (parts a and d), developed resist structures are shown in plan view prior to an ICP–RIE etch. In the middle row (parts b and e), developed resist structures are shown when tilted to 87° prior to the etch. In the bottom row (parts c and f), fin-like structures are shown following the etch. Measurements to the nearest 0.1 nm were made using GenISys ProSEM software. The LER of etched Si lines was determined via plan view image (not shown); the LER of etched W lines was not determined because the triangular shape of the cross-section does not lend itself to LER calculation.

chromium–oxide material by the time the lines were imaged, as a result of the lithographic exposure. It has been observed that this resist can shrink under exposure of an electron or helium ion beam; as bonds are broken and carbon and oxygen are volatilized, the resist film volume consolidates slightly into the oxide material. The initial resist thickness, which was not measured, is therefore necessarily larger than depicted here. Regardless, the tilted view images in Figure 4 show more clearly than the plan view images that the resist structures are resolvable against the roughness of the substrates beneath them. The ability to spin the resist into a sub-5 nm thick film also helps to reduce the smallest feature size and dose; a thinner resist yields fewer lateral-scattering sites for the traversing beam and also means that fewer ions are needed to generate enough SEs and AEs to change the small volume of resist material into the chromium–oxide material.

It is important to note that when characterizing these nanostructures, each HIM image was captured via a single scan of a 600 nm x 600 nm area, meaning that sputtering of nanostructure material by the low-current He ion beam (1.0 pA, 30 keV) was negligible; tests were done to show that even multiple scans of the same area at these settings did not alter the size of structures. This ensured that HIM imaging could be used as a non-destructive technique while offering higher resolution (and higher depth of field, important for imaging tilted structures) than, for example, a scanning electron microscope operated with an immersion lens. Further, measurements made on AFM and HIM micrographs were calibrated

against images taken of a NIST-traceable standard (50 nm wide gold lines spaced on 100 nm pitch); the same microscope settings were used on both the experimental samples and the standard to ensure measurement accuracy.

After characterizing the resist on substrate, samples for both silicon and tungsten were subjected to the same 30 sec, ICP–RIE process (forward power: 20 W RIE, 1200 W ICP) using SF_6 and C_4F_8 gases flowing at 22 and 35 sccm, respectively. Figure 4c shows that the average width of the resultant silicon fins was 6.4 nm, with an average height of 21 nm; the resist has been completely etched away. The effective etch rates, based on a 3.4 nm resist thickness (Figure 2d) were therefore determined to be 0.11 and 0.70 nm/sec for the resist and silicon, respectively. This indicates that silicon etches approximately 6.2 times faster than the resist when subjected to these etch conditions (i.e. the selectivity is 6.2:1). For tungsten (Fig 5f), the structures etched with less of a straight-sidewall fin shape and more of an angled-sidewall triangular shape, suitable for a sharp-tipped field emitter. The average width at the top and bottom of the triangle was 5 and 16 nm, respectively, with an average height of 19 nm. The resist has been completely etched away from the top of these W structures in 30 sec, resulting in etch rates of 0.11 and 0.63 nm/sec for the resist and tungsten, respectively (i.e. the selectivity is 5.6:1). It is impossible to compare these results directly with other common resists since the etch selectivities of those resists have not been reported for sub-20 nm pitches. At 100 nm pitch, the etch selectivities of common resists on silicon are 2.0:1 for PMMA, 2.9:1 for ZEP520A and 4.2:1 for HSQ.[23] Etch selectivity is expected to decrease at smaller pitch due to the decreasing probability of landing ions between the features, so the 6.2:1 selectivity for Si reported here at 17 nm pitch is especially notable, by comparison. The improvement in etch performance demonstrated here by Cr_8F_8(Pivalate)$_{16}$ on silicon has also been demonstrated previously for related metal–organic resists, where selectivities greater than 100:1 could be achieved at larger pitches.[14] It is also notable that while lines narrower than those shown in Figures 3 and 4 have been patterned by other groups in resist (e.g. 4 nm lines on 8 nm pitch by a combination of HIBL and nanoimprint lithography[24]), the etched structures reported here are both the narrowest and tallest to be transferred to substrate on a sub-20 nm pitch. The next smallest transferred patterns found in the literature are on 22 nm pitch via thermal scanning probe lithography.[25]

In comparison to a previous study of Cr_8F_8(Pivalate)$_{16}$ with EBL (100 keV, 300 pA),[15] HIBL required a dose three orders of magnitude smaller to achieve its smallest-pitched lines (EBL achieved 40 nm pitch lines at a 30,500 pC/cm line dose, compared to 16 nm pitch at 22 pC/cm here). It must be mentioned that orders-of-magnitude smaller dose with HIBL is accompanied by orders-of-magnitude smaller current, as well (e.g. 0.5 pA He ions versus 300 pA electrons). While at first glance that might indicate that HIBL writing speeds are approximately equivalent to EBL writing speeds, it is important to also consider how the resist thickness impacts doses. In the EBL study, the resist was ten times thicker (30 nm) than in this HIBL study. If the resist thickness were to increase here, we might expect the HIBL dose to actually decrease because we would be taking advantage of a cascade of scattering events that cannot similarly take place when the thickness is confined to something as small as 3 nm (that decrease in dose with increasing thickness, it must be noted, would come at the expense of resolution). Additionally, it is well known that the clearing dose increases as a function of decreasing pitch, as was the case in the comparative EBL study, where the smallest pitch was 40 nm. If we were able to compare 17 nm pitch EBL lines with the 17 nm pitch HIBL lines shown here, we would expect the HIBL dose to be even more favorable than the three orders of magnitude difference noted above.

For mass manufacturing, the high exposure doses inherent to EBL, which translate into long writing times, have always outweighed the allure of EBL's small-probe, high-resolution capability. Much work has been put into developing EBL tools that split one primary beam into many beamlets in order to decrease writing times by exposing many patterns in parallel.[26] Here we see a demonstration of HIBL yielding both better resolution and orders-of-magnitude smaller dose than EBL. While single-beam HIBL, with the same pixel-by-pixel exposure mechanism as EBL, may still not offer the lithographic speed desired by industry, perhaps this study indicates that if any beam is to be split and operated in parallel, it is a beam of helium ions and not electrons.

In conclusion, it has been demonstrated that the molecule $Cr_8F_8(Pivalate)_{16}$, when used as a resist, is capable of producing sub-10 nm structures in silicon and tungsten, spaced on sub-20 nm pitch, following pattern transfer with an ICP–RIE. This result is due to several interrelated factors associated with the resist material and method of lithography, HIBL. First, the ability to spin the resist into sub-5 nm thick films reduces lateral scattering as the beam travels through the resist, resulting in high resolution. Second, the material's high molecular weight and low density limits the number of scattering sites that the beam encounters, which also improves resolution. Third, the nature of helium ion beam interactions yields more SEs and AEs per incident beam species than is achievable by the more traditional EBL; the HIBL dose can therefore be orders of magnitude lower, which allows for a low current to be selected, which results in a sub-nm probe diameter that further improves patterning resolution. Finally, because exposing the resist changes it from a metal–organic compound to a chromium–oxide material, the material exhibits extremely high etch selectivity to both silicon and tungsten in the presence of an SF_6/C_4F_8 etch, allowing for the transfer of 6 nm wide lines into the substrates, even when etch efficiency is reduced by tightly spacing the lines on sub-20 nm pitch. It is therefore possible to fabricate sub-10 nm wide, 19 nm tall silicon and tungsten structures in a single lithography-and-etch step, opening new possibilities for future nanoelectronics. The role of HIBL in that future should also not be discounted.

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