Plasma Planarization for Sensor Applications

Yuan Xiong Li, *Student Member, IEEE,* Patrick J. French, and Reinoud F. Wolffenbuttel, *Member, IEEE*

Abstract—**Filling trenches in silicon using phosphosilicate glass (PSG) provides many possibilities for novel device structures for sensors and actuators. This paper describes a plasma planarization technique that provides fully planarized PSG filled silicon trenches for sensor applications. The technique consists of planarizing the substrate using two photoresist layers and plasma etching-back. The lower resist layer is the AZ5214 image reversal resist, which is patterned and then thermally cured. The upper resist layer is a global HPR204 coating. The plasma etching-back is carried out using CHF_3/C_2F_6 gas mixture with an O_2 addition. It is shown that by using the image reversal photoresist approach, fully planarized surface coating can be obtained without resorting to an additional mask. By adding 25 sccm (14%) O_2 into the 137 sccm CHF_3 +18 sccm C_2F_6 gas mixture, the etch rates for the photoresist and PSG can be matched. Process optimization for the two layer resist coating and plasma etching is discussed. [140]**

I. Introduction

DURING the fabrication of micromechanical structures for sensors and actuators by silicon micromachining, the topography of the substrate is increasingly modified. In conventional surface micromachining, phosphosilicate glass (PSG) of 0.5–2 μm is often used as the sacrificial layer. The patterning of the PSG layer creates surface nonplanarity. This surface nonplanarity will result in elevated (step-up) beams, as shown in Fig. 1(a). Local stress concentration may take place at the corners of the step-up support, which degrades the mechanical performance of the beam. Due to the finite stiffness of the step-up support, significant error may result if the double-clamped beam theory ("fixed" boundary conditions) is used in modelling the mechanical behavior of the beam [1]. If the PSG layer can be placed in a recess in the silicon substrate by etching a trench in the bulk silicon followed by a PSG filling, the beam will become genuinely double-clamped, as shown in Fig. 1(b). Furthermore, if two sacrificial PSG layers are required for a given device application, the total nonplanarity of the substrate is further increased. The nonplanarity results in complications in subsequent processing associated with lithography and step coverage, as in the case of multilayer interconnection of modern integrated circuit fabrication [2]. These difficulties include variations in resolution and linewidth in the vicinity of high steps due to the limited depth of focus of wafer steppers and discontinuous metal or dielectric coverage of features with vertical walls [3]. Therefore, planarization technique is important in sensor fabrication and provides many possibilities for sensor and actuator structures.

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The authors are with the Laboratory for Electronic Instrumentation, Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands.

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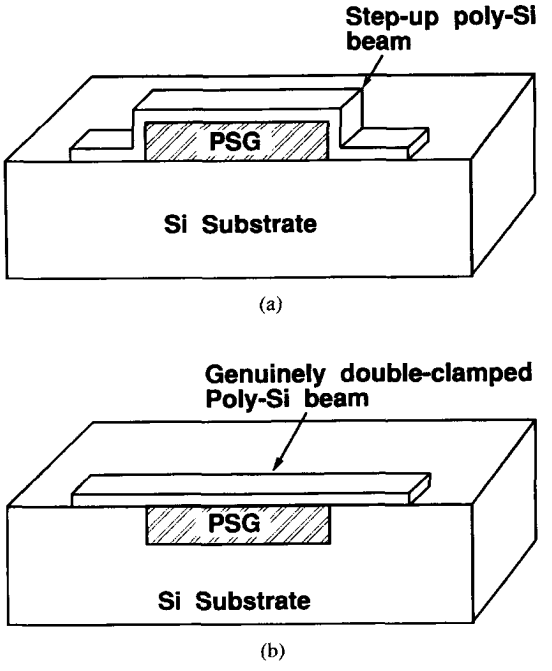

Fig. 1. (a) Step-up polysilicon beam fabricated using conventional surface micromachining process. (b) Genuinely double-clamped polysilicon beam achieved using PSG filled trenches.

Many techniques for planarizing of the substrate surface for IC fabrication have been developed. Basically, the techniques can be classified into two groups: local and global planarization. The local planarization includes reflow of PSG or BPSG (Borophosphosilicate glass) [4], [5]; Spin-on glass [6]–[8]; laser melting of PSG [9]; plasma etch-back of thick PSG [10], as well as oxide spacer approach [11]. However, with the local planarization techniques only the sharp corners are smoothened while the surface level across the wafer due to the substrate topography remains essentially unchanged. Therefore, they are not applicable to such micromachining applications as filling silicon trenches by PSG. The global planarization, including chemical mechanical polishing (CMP) and plasma planarization, provides possibilities of a completely planarized surface across the wafer. CMP has emerged recently as a new method of achieving complete planarization for submicron VLSI applications [12], [13]. However, this method suffers from difficulties in planarity control (feature size dependency, hollow formation in wide features, over-polishing of large array areas and residual contaminations). In plasma planarization [14], a low viscosity sacrificial layer (usually photoresist or polyimide) is used to coat the uneven substrate surface to obtain a practically flat surface. Subsequently, plasma etching is used to etch-back the sacrificial

TABLE I
STEP HEIGHT (μm) OF ORIGINAL APPROXIMATELY 2-μm-DEEP TRENCHES WITH SINGLE HPR204 RESIST COATING

	After 2 μm resist coating	After 250 °C, 15 min. thermal cure	A second 2 μm resist coating
150 μm isolated line	2.10	2.06	2.10
50 μm periodic line and space	1.22	1.51	0.65
20 μm periodic line and space	0.74	1.06	0.35

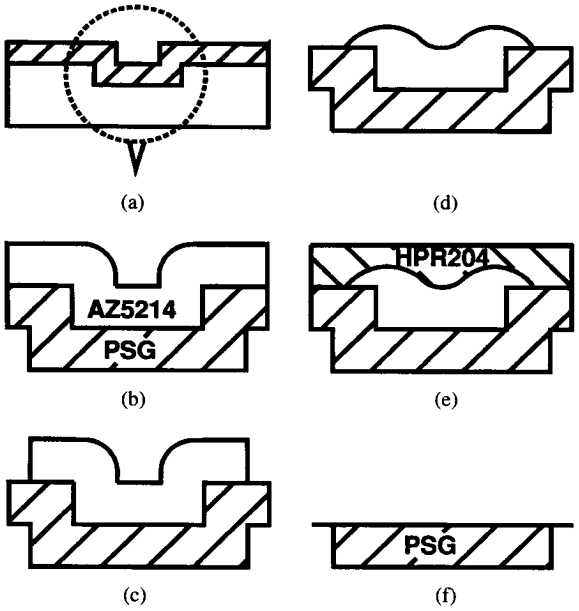

Fig. 2. Processing steps of the planarization technique. (a) PSG deposition, (b) AZ5214 image reversal resist coating, (c) resist patterning (d) thermal cure, (e) HPR204 resist coating, and (f) plasma etching back.

coating layer, during which the etch rate of substrate and sacrificial layer should be equal, to form a planar surface after the etching. It is expected that filling silicon trenches by PSG can be achieved using this approach for sensor applications. However, this application has, to date, received little attention in the literature.

In this paper, a plasma planarization technique providing fully planarized PSG filling in silicon trenches for sensor applications is described. The planarization technique involves two-layer-resist coating and plasma etching-back. Process optimization for the two-layer-resist coating and plasma etching-back will be discussed.

II. PLANARIZATION TECHNIQUE

A. Single-Layer Photoresist Coating Using HPR204 Resist

It has been reported that the effectiveness of a single photoresist coating using, e.g. HPR204 resist [15], [16], in

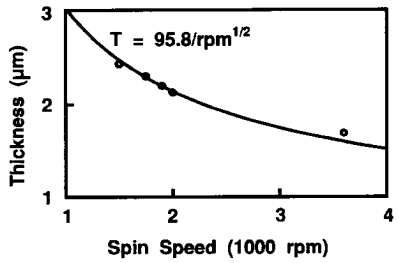

Fig. 3. Dependence of AZ5214 thickness on the spin-on speed.

planarization is feature-size dependent. Table I shows the measured step height of a wide (150 μm) isolated trench and those of 50 and 20 μm periodic line-and-space pattern with 2 μm HPR204 coating on 2 μm deep trenches. The step height after the resist has been subjected to a 250°C, 30 minutes thermal cure is also shown. It can be seen that the resulting step height of the isolated trench remains the same as the original trench depth while that of the periodic line-and-space trenches is reduced, depending on the feature size. After the thermal cure, the step height of the isolated line remains basically unchanged, while that of the periodic patterns is increased. This is probably due to more shrinkage of the thicker resist (on the space area) than the thinner resist (on the line area). Increasing the thickness of the resist to 4 μm by spinning-on an additional 2 μm HPR204 does not change the step height of the isolated line, although that of the periodic line-and-space is significantly reduced. These results are in agreement with previously reported observations [14], [15], [17], [18]. Usually the second coating tends to mix or dissolve a portion of the initial coating. This phenomena increases the viscosity and the relative solid component of the polymer solution at the interface between the coatings. This change in solution properties could adversely affect the spin-on planarization properties of the subsequent coating. Since in sensor applications the pattern is often large (tens of microns or greater) and usually with large separation, single-layer HPR204 resist coating up to 4 μm together with thermal cure is insufficient to provide a completely planarized surface. Therefore, an alternative approach must be used.

B. Two-Layer Resist Coating Technique

To obtain a near flat surface coating, it is desirable to fill the trenches first. This has been achieved by a two-resist-layer planarization scheme proposed by Schiltz *et al.* [19] and applied for VLSI fabrication [20], [21]. However, these studies used the same photoresist for the first coating as the second one. An additional mask—the negative of the mask used to realize the original pattern—had to be used to expose the first resist layer.

The drawback of using an additional mask in the above scheme can be overcome by the following planarization process shown in Fig. 2: First, a PSG layer is deposited with a thickness equal to the depth of the trenches [Fig. 2(a)]. An AZ5214 image reversal photoresist layer is then spun-on [Fig. 2(b)] and patterned through image-reversal using the same mask as that for the trench etching of the silicon

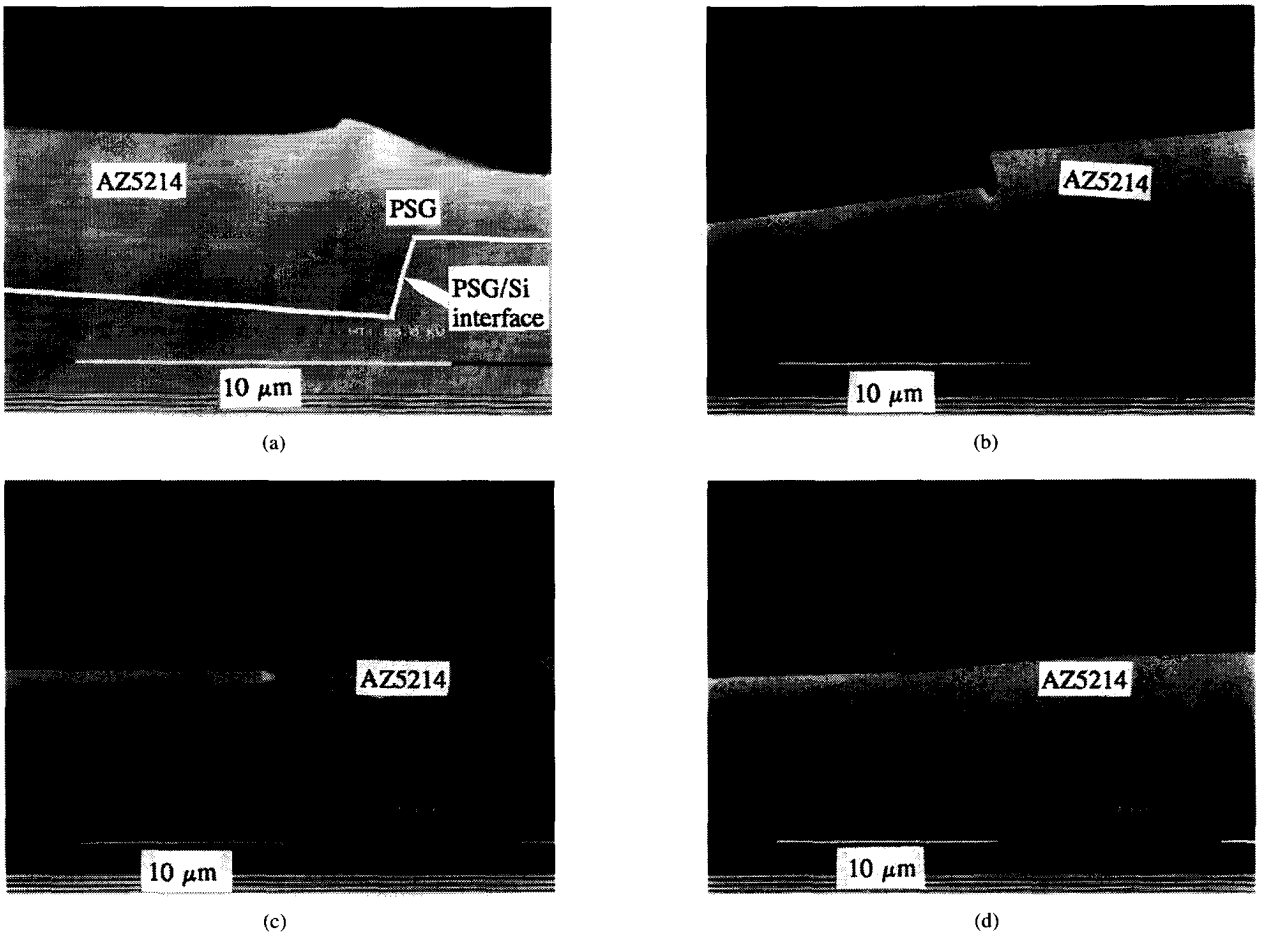

Fig. 4. (a) Filling of 2-μm deep PSG recess by 2-μm AZ5214 image reversal resist using the optimized coating process: spinning speed 2220 rpm, exposure energy of the stepper 80 mJ/cm^2, flood exposure time 10 seconds. The protruding of the resist at the edge is due to the abrupt change inthe substrate topography. Resist filling in trenches subjected to thermal cure at different temperatures for 15 minutes: (b) 100°C, without reflow, (c) 150°C, insufficient reflow, and (d) 200°C, sufficient reflow.

substrate [Fig. 2(c)]. Then the photoresist is thermally cured [Fig. 2(d)]. Subsequently, a 1.3-μm HPR204 photoresist layer is applied [Fig. 2(e)]. After baking to remove the solvent in the upper photoresist, the surface of the wafer is etched-back using a $CHF_3/C_2F_6/O_2$ chemistry to leave a PSG filled trench [Fig. 2(f)].

The application of image reversal resist in the proposed process eliminates the requirement for the extra mask. If the AZ5214 resist is processed in a normal processing sequence, i.e. coat, soft bake, expose, develop, and hard bake, a normal positive image is obtained. If, on the other hand, a post-exposure bake sequence is added, the tonal quality of this resist reverses from a positive to a negative one at a post exposure bake temperature of 90°C. The inversion process seems to be best explained by a cross-linking mechanism [22]. Upon exposure, the photoactive compound generates an acidic compound. Following the relatively high temperature post exposure bake, this acid diffuses through the resin system of the film and causes acid catalyzed cross-linking. Therefore, the exposed area becomes insoluble in the developer. A flood exposure is used to make the unexposed area soluble in the developer. When image reversal resist is exposed through the same mask as used for the silicon trench followed by the post exposure bake and flood exposure, the final resist pattern after the development is complementary of the silicon trench, i.e. photoresist is left at the trench areas, resulting in filling of the trench.

Coating and Patterning of AZ5214 Resist: The thickness of the image reversal resist must be the same as the depth of the silicon trench to obtain optimum trench filling, and the linewidth control of the resist is also important. Those two properties are determined by the spin-on speed, exposure energy of the stepper, and duration of flood exposure. The spin-on speed is the most important factor to determine the resist thickness, while exposure energy of the stepper and the time needed for the flood exposure are essential for the feature size control. Fig. 3 shows the measured thickness of AZ5214 resist versus spin-on speed, which is in good agreement with the theoretical model of the inversely proportional relation between the thickness and the square root of the spinning speed [23]. The exposure energy of the stepper and flood exposure time are determined according to the requirement of feature size. High exposure energy of the stepper and short flood exposure time tend to increase the feature size. To compensate for the misalignment of the stepper, a slightly larger resist feature size than the trench is desirable. This

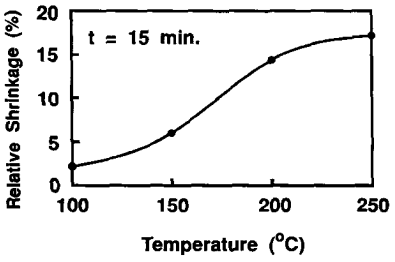

Fig. 5. Relative shrinkage of the AZ5214 resist after thermal cure versus temperature for 15-minute cure time.

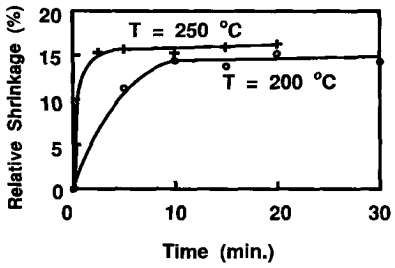

Fig. 6. Relative shrinkage of the AZ5214 resist versus the cure time at 200 and 250°C.

is achieved by using the optimized exposure energy of the stepper and flood exposure time of 80 mJ/cm^2 and 10 seconds, respectively. Fig. 4(a) shows the SEM photograph of 2-μm AZ5214 resist filling on 2-μm trench. It can be seen that at the edge of the trench, the resist is about half micron thicker than in the center of the trench due to an abrupt change of the surface topography in the substrate.

Thermal Curing of AZ5214 Resist: After developing, the AZ5214 image reversal resist is thermally cured. Such a thermal cure is necessary for three main reasons: 1) to improve planarization by increased thermal flow, so that the resist profile at the edge of the trench (shown in Fig. 4) is smoothened; 2) to compensate for misalignment of the resist block with respect to corresponding trench due to limited alignment accuracy of the stepper; and 3) to enhance the cross-linking of the resist to prevent any interface problem that might occur with the second coating [24]. During the thermal cure, shrinkage of the AZ5214 resist takes place due to the evaporation of the solvent. This effect must be taken into account in the determination of the original thickness of the resist coating. The degree of shrinkage has been examined at a temperature range of 100–250°C (Fig. 5) for a cure time from 2.5–30 minutes (Fig. 6). The relative shrinkage in Figs. 5 and 6 is defined as the ratio of the thickness reduction to the original thickness. It can be seen from Fig. 5 that the shrinkage is strongly dependent on the temperature and from Fig. 6 that at 200 and 250°C the shrinkage saturates after 10 and 2.5 minutes, respectively. The optimized curing temperature is experimentally determined by evaluating the reflow of the resist at different temperature. Fig. 4(b)–(d) shows the cross- sectional view of the resist filling at three curing temperatures. It can be seen that basically no reflow has taken place at 100°C and that the reflow at 150°C is not sufficient to smoothen the interface between the resist and the trench. A smooth interface is obtained at 200°C due to the reflow. It is obvious that the protruding part of the resist at the edge of the trench is completely flattened after the cure. Similar reflow effects are found at 250°C. Therefore, the cure temperature is chosen to be 250°C to ensure a wide process window and sufficient cross-linking [25]. A cure time of 15 minutes is used for stable resist thickness. The shrinkage of the resist at this cure condition is about 16%.

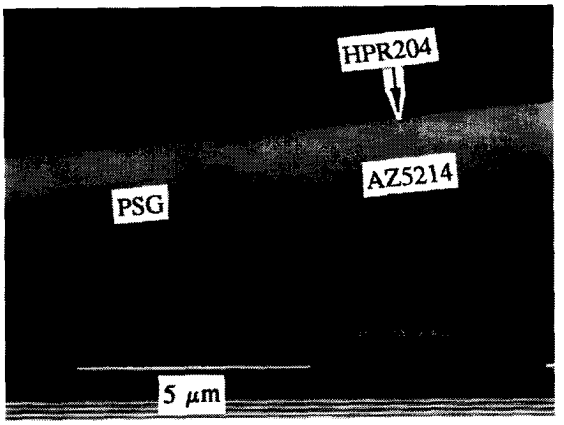

Fig. 7. Cross-sectional view of the final planarized surface using the two-layer resist technique.

A 1.3-μm HPR204 resist coating is applied after the thermal cure for the AZ5214 image reversal resist. This finally leads to an almost completely planar surface, as shown in Fig. 7.

C. Plasma Etch-Back

The planarized surface profile is transferred to the substrate using plasma etch-back. There are several required properties of etch-back. First, the etch rates for the resist and PSG layer must be equal. Secondly, the etching selectivity over the underlying layer (usually silicon or silicon nitride in most sensor applications) must be high enough to ensure the integrity of the substrate. Third, good uniformity must be achieved during the etching-back, and finally, the surface roughness introduced by the etching-back must be minimized. In other words, any form of redeposition from the plasma to the substrate must be eliminated. Generally, CF_4-based chemistries can be used for PSG etching and oxygen can be added to the chemistry to adjust the etch rate ratio between the PSG and photoresist [14]. However, the dominant reactive species in these chemistries are F atoms, which also have a high etch rate for silicon and silicon nitride, leading to a low selectivity over the underlying layers. A CHF_3-based chemistry, on the other hand, in which unsaturated fluorocarbon species (such as CF_2) are dominant, can also be used to etch the PSG. This type of chemistry usually etches silicon or silicon nitride with a lower etch rate than PSG, thus selective etching can be achieved [26]. Therefore, a gas mixture of CHF_3 with C_2F_6 addition was chosen for PSG etching.

Initial plasma etching experiments for PSG were performed to optimize the etching chemistry, so that the above mentioned requirements are met. The PSG layer containing 4% phosphorus was deposited in a LPCVD reactor. The etching was carried out in a commercial triode Reactive Ion Etching (RIE) machine

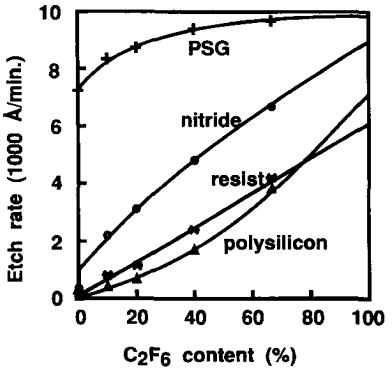

Fig. 8. Etch rate versus C_2F_6 content. RF power =300 W, pressure=180 mTorr (total flow rate of CHF_3 + C_2F_6 =180 sccm.)

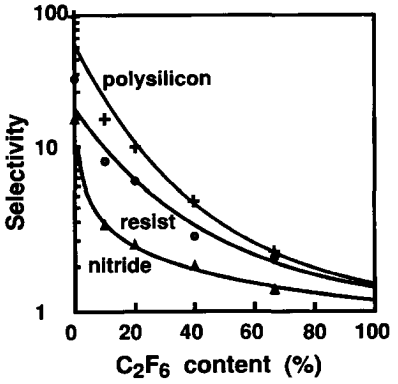

Fig. 9. Selectivity of PSG over the other films versus C_2F_6 content. RF power = 300 W, pressure = 180 mtorr, (total flow rate of CHF_3 + C_2F_6 = 180 sccm).

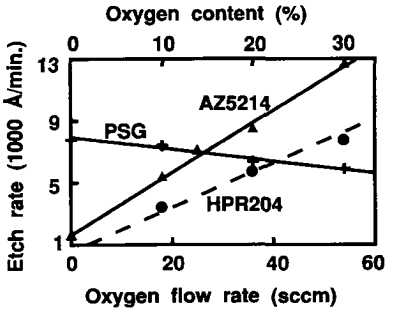

Fig. 10. Etch rate of PSG and resist versus O_2 content in the C_2F_6/CHF_3 chemistry. RF power = 300 W, pressure = 180 mtorr. C_2F_6 = 18 sccm, (total flow rate of CHF_3 + C_2F_6 +O_2 = 180 sccm.

(Drytek 384T). A 2 μm AZ5214 resist subjected to 250°C, 15 minutes thermal cure was used as the mask to simulate the real resist conditions described above. HPR204 resist was also used for comparison. The RF power (13.56 MHz), the chamber pressure, the total gas flow rate, the electrode temperature, and He pressure for backside cooling were fixed to 300 W, 180 mTorr, 180 sccm, 25°C, and 12 torr, respectively. For the etching selectivity experiments, either silicon nitride or polysilicon film was used since these two types of layers are often present under PSG layer. Etch rate of the film was determined by measuring the change in the film thickness due to the etching using a Leitz MVP-SP optical measurement system.

Dependence of Etch Rate and Selectivity on C_2F_6 Content: Fig. 8 shows the etch rates of the various films when the C_2F_6 content is varied and Fig. 9 shows the selectivity of PSG over the other films. All the etch rates increase approximately linearly, with all selectivities being reduced, with increasing C_2F_6 content. Those variations result from the increased ratio of F atom concentration to fluorocarbon concentration in the plasma at increasing C_2F_6 content. During the plasma etching, the substrate surface is subjected to fluxes of several different reactive species, such as F, $CF_y(y = 0 \sim 3)$ and energetic $CF_x^+(x = 0 \sim 3)$, which are generated by ionizing process. The F atoms are inherently reactive with any of the films investigated, including the photoresist, and the etching takes place spontaneously [27]. Both CF_2 and CF_3 radicals react with either oxide or nitride when the surface is under simultaneous ion bombardment [28]. However, a C-F film is formed on the silicon surface when the substrate is exposed to CF_2, which retards the etching [29], [30]. C-F film deposition also takes place on the photoresist surface, reducing the etch rate for the resist. As a result, selective etching of oxide and nitride over silicon and photoresist is achieved if CF_2 radicals are dominant over F atoms. In addition to enhancing the reaction of CF_y radicals, energetic molecular ions (CF_x^+) can remove a larger number of oxide molecules than noble gas ions such as Ar^+ [31]. Therefore, the relative concentration of the three F-containing species in the plasma determines the etching characteristics.

In the plasma containing only CHF_3 used in our experiments, CF_2 and CF_x^+ radicals are dominant [32]. Therefore, the etch rate for polysilicon is very low compared to that of PSG, resulting in a selectivity of about 100. Compared to nitrogen, oxygen is more reactive to the fluorocarbons, resulting in a higher etch rate for the PSG than that for the nitride, and an etching selectivity of about 20. When C_2F_6 is added to CHF_3, more F atoms are generated, and consequently the etch rates for all materials under investigation increase as indicated in Fig. 8. Due to the recombination of F atoms with the fluorocarbon radicals, the relative concentration of the CF_2 radicals is reduced, making the C-F layer on both the polysilicon and photoresist thinner, and thus leading to a rapid increase in their etch rate and a corresponding decrease in the etching selectivities. Since F atoms react with nitride more easily than with oxide (the activation energy is 4.0 Kcal/mol and 4.2 Kcal/mol, respectively), etch rate for the nitride increases rapidly at increasing C_2F_6, resulting in a rapid decrease in the etching selectivity. Although high selectivity can be achieved with a pure CHF_3 chemistry, it turns out that significant polymer deposition takes place at the sidewall of the etched features during the etching, causing problems related to feature size control, surface roughness, and reactor contamination.

The above experimental results clearly indicated that a compromise must be made for the C_2F_6 content for high etch rate and high selectivity and minimum polymer formation. A 10% C_2F_6 content (18 sccm) was chosen for PSG etching, yielding an etch rate of 7800 Å/min. with selectivities of 19.7, 3.8, and 4.8 over polysilicon, nitride, and photoresist,

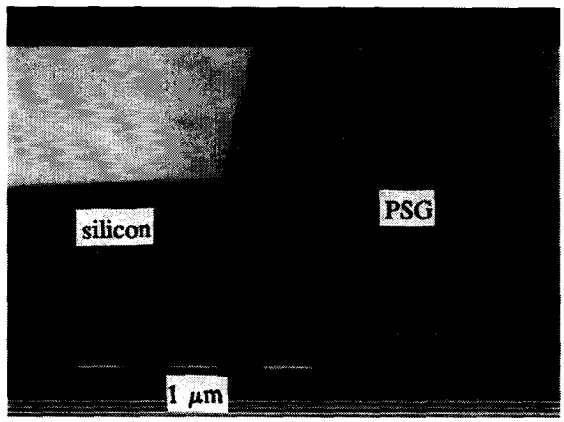

Fig. 11. SEM photograph of 1.85 μm silicon trench filled with PSG using the optimized two-layer resist coating and plasma etching-back. The interface between the PSG and silicon substrate is very smooth. The recess on the PSG surface near the trench edge is caused by enhanced etching of the resist.

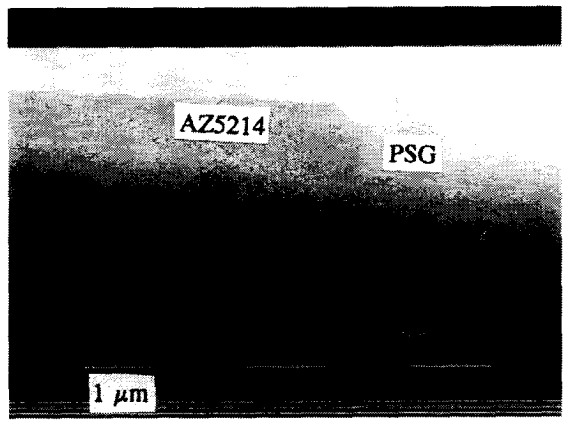

Fig. 12. SEM photograph indicating the enhancement of resist etching (hollow formation) at the interface of the resist and PSG.

respectively. This chemistry results in a nonuniformity in PSG etching of about 3%, which is found to be quite satisfactory for the intended application.

Effects of the Oxygen Addition: With the above optimized chemistry for selective and uniform PSG etching, the etch rate for PSG is much higher than that for the resist. However, a selectivity of 1 was required in the etching-back for planarization, as described above. For this reason, oxygen was introduced to the gas mixture. Fig. 10 shows the dependence of the etch rates of PSG and two types of resist on O_2 addition in the gas mixture. The etch rate for the resists increases linearly, and that of PSG decreases linearly with increasing O_2 ratio. Note also that the etch rate for AZ5214 is higher than that for HPR204. With 14% O_2 content (25 sccm), the etch rate for the PSG becomes almost the same as that for the AZ5214 resist (about 7300 Å/min.). Therefore, this O_2 content was used for the etching-back of the planarized surface. This chemistry results in a selectivity over polysilicon and silicon nitride of about 20 and 4, respectively.

D. Planarization Results and Feature Size Limitation

Fig. 11 shows the cross-sectional view of PSG filling in the silicon trench after the plasma etching-back. It is clear that the planarization technique results in good PSG filling of the silicon trenches. The PSG outside the trenches was removed completely and the boundary between the PSG and the trench edge was reasonably smooth. A concavity in the PSG filling near the trench edge can be seen. This was most probably due to the extra etching of the resist at the interface between the resist and the PSG. During the plasma etching, oxygen was released as a result of reaction of reactive radicals with silicon atoms in PSG subjected to energetic ion bombardment. Therefore, the local concentration of oxygen at the interface between the PSG and resist was enhanced, which increased the etch rate of the resist. This argument is supported by the observation that a concavity of the resist appears at the interface during the etching-back, as shown in Fig. 12. This concavity leads to a local surface unevenness of about 0.2 μm for a 2 μm deep silicon trench after the planarization. This technique, therefore, represents a considerable improvement in planarity. The global nonuniformity of the planarization is found to be about 6%, i.e. the maximal difference in nonplanarity across the substrate surface is about 250 Å.

If the width of the trench in the substrate is less than two times of the trench depth, the PSG at the two opposite trench sidewalls will merge together during the deposition due to the conformal nature of PSG deposition [see Fig. 2(a)]. Therefore, the approach of using image reversal resist coating and patterning is applicable only when the width of the substrate trench is much greater than the depth of the trench, which is the case in most micromachining applications.

III. Conclusion

A planarization technique for filling PSG in silicon trenches for sensor applications has been developed and tested for 2 μm deep silicon trenches. The technique involves depositing 2 μm PSG layer on the silicon substrate with trenches, planarizing the surface topography using two-layer resist coating, and finally, plasma etching-back to transfer the flat surface to the silicon substrate. This results in a planarized substrate surface with PSG filled trenches.

It has been shown that a single 2-μm HPR204 resist layer, together with thermal cure at 250°C for 30 minutes, was not sufficient to completely planarize the substrate with 2-μm-deep trenches. Furthermore, the degree of the planarization depends on the feature size of substrate topography. Even a 4-μm HPR204 coating by applying two 2-μm resist did not provide the desired complete planarization. By using AZ5214 image reversal resist patterned with the same mask as that used for definition of the silicon trench, together with 250°C, 15 minutes thermal cure, the recess can be effectively filled, resulting in a smooth surface. By subsequent 1.3-μm HPR204 resist coating, sufficient surface planarization was achieved.

Plasma etch-back was carried out in a C_2F_6/CHF_3 gas mixture with O_2 addition. By using 25 sccm O_2 addition in 18 sccm C_2F_6 and 137 sccm CHF_3, almost equal etch rates (~7300 Å/min.) for PSG and the resist was achieved with a selectivity of about 20 and 4 over polysilicon and silicon nitride, respectively. This ensured that the flat surface of the resist coating was transferred to the substrate, leaving PSG

filling only in the trench area. Local enhancement of resist etching at the interface between the resist and PSG resulted in a concavity of about 2000 Å in the PSG surface near the edge of the trench. However, this still represents a considerable improvement in planarity. This technique is therefore very suitable for sensor applications where the wide trenches in the substrate must be planarized.

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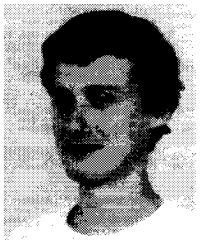
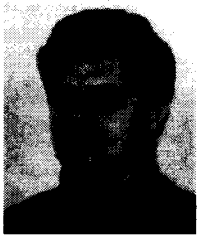
Yuan Xiong Li (S'91) received the B.Sc. degree in semiconductor physics and device physics from Hefei University of Technology, P. R. China, in 1982, and the M.Sc. degree in integrated circuit design and processing from Shanghai Institute of Metallurgy, Academia Sinica, P. R. China, in 1986, with his thesis work concerning the design and processing technology of high-frequency dual gate MOSFET's.

From 1986 to 1991, he was a Research Associate in the same institute, where he was engaged in research on high speed CMOS technology and ASIC design. Since September 1991 he has been at the Laboratory for Electronic Instrumentation, Department of Electrical Engineering, Delft University of Technology, working towards the Ph.D. on the subject of micromachining technology for sensor applications.



Patrick J. French received the B.Sc. degree in mathematics and M.Sc. degree in electronics from Southampton University, U.K., in 1981 and 1982, respectively. In 1986 he received the Ph.D. degree, also from Southampton University, based on a study of the piezoresistive effect in polysilicon.

After 18 months as a Post-Doctoral Researcher at Delft University, The Netherlands, he moved to Japan in 1988. For three years he worked on sensors for automotive applications at the Central Engineering Laboratories of Nissan Motor Company. He returned to Delft University in May 1991 and is now a Staff Member of the Laboratory for Electronic Instrumentation with interests in micromachining and process optimization related to sensors.



Reinoud F. Wolffenbuttel (S'86–M'88) received the M.Sc. degree in 1984 and the Ph.D. degree in 1988, both from the Delft University of Technology. His thesis work dealt with the application of silicon to color sensing.

Between 1986 and 1993 he was an Assistant Professor, and since 1993 he has been an Associate Professor, at the Laboratory of Electronic Instrumentation of the Delft University of Technology, where he is involved in instrumentation and measurement in general, and on-chip functional integration of microelectronic circuits and silicon sensor, fabrication compatibility issues, and micromachining in silicon in particular. In 1992 he was a Visiting Scientist at the University of Michigan, Ann Arbor, MI, and was involved in the research on low-temperature wafer-to-wafer bonding.