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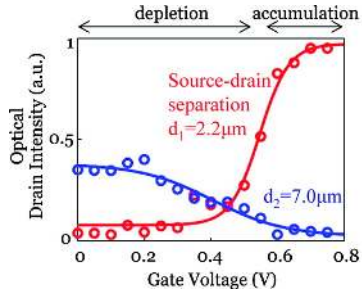

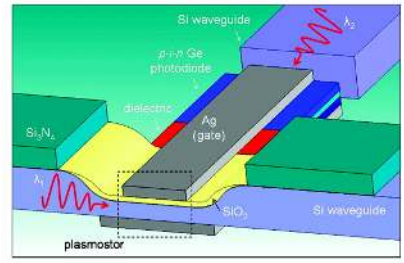

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PlasMOStor: A Metal−Oxide−Si Field Effect Plasmonic Modulator

Jennifer A. Dionne,[†,‡] Kenneth Diest,[†] Luke A. Sweatlock,[§] and Harry A. Atwater*

Thomas J. Watson Laboratories of Applied Physics, California Institute of Technology, Mail Code 128-95, Pasadena, California 91125

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ABSTRACT

Realization of chip-based all-optical and optoelectronic computational networks will require ultracompact Si-compatible modulators, ideally comprising dimensions, materials, and functionality similar to electronic complementary metal−oxide−semiconductor (CMOS) components. Here we demonstrate such a modulator, based on field-effect modulation of plasmon waveguide modes in a MOS geometry. Near-infrared transmission between an optical source and drain is controlled by a gate voltage that drives the MOS into accumulation. Using the gate oxide as an optical channel, electro-optic modulation is achieved in device volumes of half of a cubic wavelength with femtojoule switching energies and the potential for gigahertz modulation frequencies.

The integrated circuits ubiquitous in modern technology were critically enabled by the invention of the metal−oxide−semiconductor field effect transistor (MOSFET) — a three-terminal device that modulates current flow between a source and drain via an applied electric field. Since the first successful demonstration of MOSFETs in the 1960s, silicon devices and circuits have continuously scaled according to Moore's law, increasing both the integration density and bandwidth of complementary metal−oxide−semiconductor (CMOS) networks. At present, microprocessors contain over 800 million transistors clocked at 3 GHz, with transistor gate lengths as small as 35 nm.[1,2] Unfortunately, as gate lengths approach the single-nanometer scale, MOS scaling is accompanied by increased circuit delay and higher electronic power dissipation — a substantial hurdle to Moore's law often referred to as the "interconnect bottleneck".

To circumvent the electrical and thermal parasitics associated with MOS scaling, new interconnect technologies are being considered. Particular attention has been given to optical technologies, which could achieve high integration densities without significant electrical limitations.[3−5] On-chip optical components would offer a substantially higher bandwidth, a lower latency, and a reduced power dissipation compared with electronic components.[3,4,6] Unfortunately, optical components are generally bulky relative to CMOS electronic devices, comprising dimensions on the order of the signal wavelength.

Use of plasmonic components offers a unique opportunity for addressing the size mismatch between electrical and optical components. Plasmonic devices convert optical signals into surface electromagnetic waves propagating along metal−dielectric interfaces. Because surface plasmons exhibit extremely small wavelengths and high local field intensities, optical confinement can scale to deep subwavelength dimensions in plasmonic structures.

Recent reports have demonstrated passive and active plasmonic components that combine low optical loss with high mode confinement. Metal−dielectric channels[7−9] and metal−insulator−metal slot structures[10−13] have formed the basis for subwavelength plasmonic waveguides, interferometers, and resonators.[14] In addition, plasmon modulators based on quantum dots,[15] ferroelectric materials,[16] or liquid crystals[17] have been proposed and demonstrated. However, in terms of integrating standard Si-based electronics with Si-based photonics, it would be highly desirable to develop a suite of plasmonic devices with Si as the active medium. This approach would allow for compatibility with standard CMOS processing techniques and potential integration into existing Si-based photonic networks. Unfortunately, unstrained Si exhibits an indirect bandgap and no linear electro-optic effect, yielding a continuous-wave optical response that is typically either slow or weak.[18,19] To date, neither a Si-based plasmonic waveguide nor plasmonic modulator have been demonstrated.

Here, we present an experimental demonstration of a field effect Si modulator based on multimode interferometry in a plasmonic waveguide. Like the Si-based modulators implemented by Lipson and colleagues,[20] this device utilizes high optical mode confinement to enhance electro-optical non-

* To whom correspondence should be addressed, haa@caltech.edu.
[†] These authors contributed equally to this work.
[‡] Present address: Department of Chemistry, University of California, Berkeley, Berkeley, CA 94720.
[§] Present address: Northrop Grumman Space Technology, One Space Park, Redondo Beach, CA 90278.

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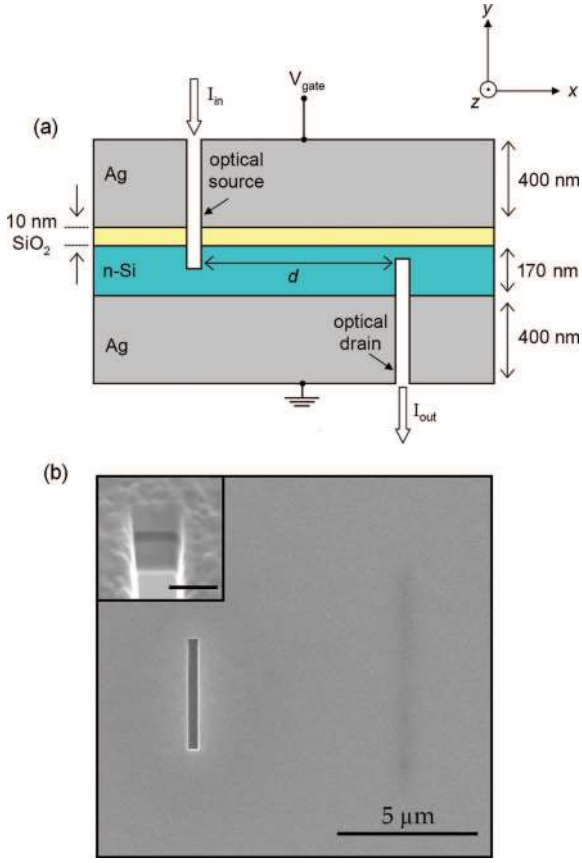
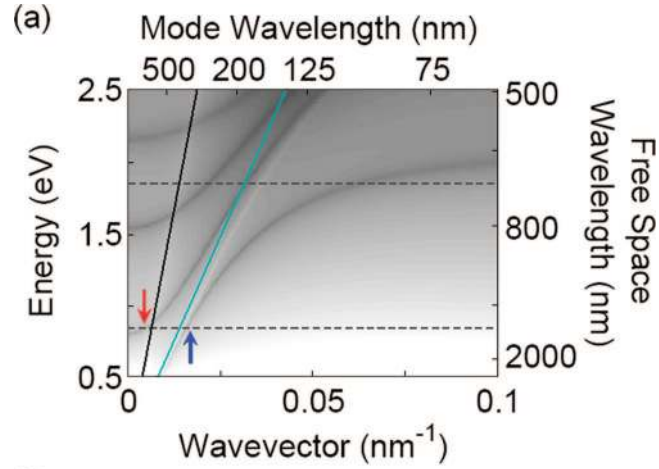


Figure 1. Geometry of the Si field effect plasmonic modulator (plasmostor). (a) Cross-sectional schematic of the modulator. A ~170 nm thick Si film is coated with a thin, 10 nm SiO_2 layer and clad with Ag. Subwavelength slits milled through the Ag cladding form the optical source and drain, through which light is coupled into and out of the modulator. (b) Scanning electron micrograph of the plasmostor as viewed from the optical source side. The optical drain is visible due to electron transparency. The inset shows a cross-sectional cut through the four-layer plasmostor waveguide (scale bar is 500 nm).



(b)

λ=1.55μm	|E| mode profile	Mode Index	Loss (dB/μm)
Off state (V=0) *depletion*	Ag / SiO_2 / Si / Ag	3.641	0.207
		0.375	2.37
On state (V>0.7V) *accumulation*	Ag / SiO_2 / Si / Ag	3.649	0.228
		0.033	28.14

Figure 2. Dispersion relations and tabulated mode properties of the plasmostor. (a) Calculated transverse-magnetic dispersion relation for the plasmostor in the voltage-off (depleted) state. The dark gray curves correspond to optimal dispersion relation solutions with the gray scale indicating the mode line width. Light lines for SiO_2 (black solid line) and Si (cyan solid line) are also included. The horizontal gray dashed lines indicate free-space wavelengths of $\lambda = 1.55$ μm and $\lambda = 685$ nm. Note that at a wavelength of $\lambda = 1.55$ μm, the depleted plasmostor supports two modes: a photonic mode lying to the left of the Si and SiO_2 light lines (red arrow) and a plasmonic mode lying to the right of the Si light line (blue arrow). (b) Tabulated mode profiles, refractive indices, and losses for the plasmostor in both depletion (voltage-off) and accumulation (voltage-on) states at a wavelength of $\lambda = 1.55$ μm. Properties of the photonic mode are denoted in red, while properties of the plasmonic mode are denoted in blue.

linearities in Si. Moreover, like the Si optical modulator of Liu and colleagues,[21] this device exploits the fast modulation of accumulation conditions in a metal−oxide−semiconductor (MOS) capacitor. In contrast with these and related[22] structures, our plasmonic modulator can achieve modulation ratios approaching 10 dB in device volumes of half a cubic wavelength. In particular, our device illustrates that conventional scaled MOSFETs can operate as optical modulators, by transforming the channel oxide into a plasmon slot waveguide.

Figure 1 illustrates the geometry of our plasmonic MOS modulator, called a "plasmostor". As seen in Figure 1a, the modulator consists of a four-layer metal−oxide−Si−metal waveguide. The plasmostor was prepared from single-crystalline, n-doped Si-on-insulator wafers. With standard etching and oxidation techniques, a large centimeter-scale suspended Si membrane was fabricated with a uniform thickness of approximately 170 nm and carrier concentrations of $\sim 9 \times 10^{16}/\text{cm}^3$. Subsequently, a thin 10 nm SiO_2 layer was thermally grown on the top surface of the Si. Thermal evaporation was used to deposit 400 nm thick Ag layers onto each side of the membrane, forming both the plasmostor cladding and the gate contact. Light was coupled into and out of the plasmostor via subwavelength slits etched into the top and bottom cladding layers (Figure 1b). This double-sided coupling configuration provides for a dark-field imaging configuration with minimal background signal, though end-fire excitation could also be used. Note that in this geometry, the slits function as the optical source (input) and drain (output) of the plasmostor. As seen in Figure 1b, the input slits are defined to a length of approximately 4 μm, which determines the lateral extent of waveguided modes.[12] To map transmission as a function of device length, the source−drain separation was varied from approximately 1 to 8 μm in 50 nm increments.

In the absence of an applied field at the gate, the plasmostor is fully depleted and light can be guided from the source to the drain through both the Si and SiO_2 layers. Figure 2 illustrates the dispersion diagram and mode profiles that characterize the unbiased plasmostor waveguide. Modal

properties were calculated via a numerical solution of Maxwell's equations and assume uniform coupling across the waveguide stack. For reference, the dispersion diagram also includes the light lines in Si and SiO_2, corresponding to light propagation through bulk media with refractive index $n = n_{Si}$ or n_{SiO_2}.

As seen in Figure 2a, the plasmostor supports a variety of transverse magnetic modes. In particular, at a wavelength of $\lambda = 1.55$ μm, the unbiased plasmostor supports two modes: a photonic mode lying to the left of the Si and SiO_2 light lines (red arrow) and a plasmonic mode lying to the right of the Si light line (blue arrow). Both modes will be generated at the plasmostor source and can interfere either constructively or destructively at the drain, depending on the source−drain separation. As seen in Figure 2b, the photonic mode (red) is characterized by an electric field localized predominately in the Si core and a mode index of $n = 0.375$. In contrast, the plasmonic mode (blue) exhibits maximal field intensities within the SiO_2 channel and a mode index of $n = 3.641$. While the high plasmonic mode index arises from mode overlap with the Ag and Si layers, propagation losses remain relatively low. At $\lambda = 1.55$ μm, losses of the plasmonic and photonic modes are 0.207 and 2.37 dB/μm, respectively. For both modes, fields in the metal cladding decay within approximately 20 nm of the Ag−Si and Ag−SiO_2 interfaces.

The nearly flat dispersion of the photonic mode around $\lambda = 1.55$ μm suggests that this mode will be extremely sensitive to changes in the Si complex index. For example, modifying the Si index through free-carrier absorption will push this mode into cutoff, such that the dispersion curve intercepts the energy axis just above $\lambda = 1.55$ μm. The remaining plasmonic mode will then propagate through the plasmostor without interference from the photonic mode.

In the plasmostor, such changes in the Si index are induced by applying a positive bias to the gate. For drive voltages above the flat-band voltage, electrons in the n-type Si form an accumulation layer characterized by a peak carrier concentration at the Si/SiO_2 interface and a spatial extent given by the Debye length. Figure 2b tabulates the theoretical change of mode index and propagation length with the onset of accumulation. To represent the spatially varying charge distribution predicted by Poisson's equation, the accumulation layer is modeled as five discrete Drude layers of varying conductivity, with an average plasma frequency of 7.94×10^{14} Hz and a Debye decay length of 14 nm. Note that both the Drude model and the Debye approximation were used for simplicity. As expected, the effective index and losses of the plasmonic mode exhibit very little change between the voltage-off (depletion) and voltage-on (accumulation) states. In particular, the plasmonic mode index varies from the off state by $\Delta n = 0.008$, and losses are only slightly increased to 0.228 dB/μm. However, the photonic mode is pushed into cutoff, as indicated by the near-zero mode index and substantially increased losses (i.e., the photonic mode becomes evanescent and can no longer propagate power through the device). Therefore, in the accumulation state, the plasmostor will guide near-infrared light almost exclusively through the SiO_2 channel,[23] solely via the plasmonic mode.

Modulation of the electric field distribution and outcoupled power is illustrated in the finite difference time domain simulations of Figure 3. In these simulations, the plasmostor is illuminated through the optical source with a Gaussian beam of wavelength $\lambda = 1.55$ μm or $\lambda = 685$ nm, and the source−drain separation is set to $d = 2$ μm. As seen in the left column of Figure 3a, in the absence of an applied field, plasmostor transmission at $\lambda = 1.55$ μm is distributed throughout the Si core with sparse regions of high electric field in the oxide slot. However, with the onset of accumulation, the field transmitted within the Si core is notably decreased. As seen in the right column of Figure 3a, plasmostor fields are localized predominately within the 10 nm thick oxide layer, which acts as a channel between the optical source and optical drain. Within the slot, pronounced maxima and minima within the resonator can be observed with a wavelength of approximately 225 nm.

By choosing the source−drain separation to correspond to a condition of destructive interference between the photonic and plasmonic modes, plasmostor transmission can be substantially increased by inducing accumulation. Figure 3b plots the total power transmitted through the plasmostor at $\lambda = 1.55$ μm, with $d = 2$ μm. On comparison of intensities at the optical drain between the voltage-off and voltage-on states, simulated modulation ratios exceeding +10 dB can be observed.

As wavelengths approach the visible range, the plasmostor begins to support a number of photonic and plasmonic modes (see Figure 2a). At $\lambda = 685$ nm, for example, the unbiased plasmostor exhibits three modes with effective indices of $n = 5.36$, 3.40, and 2.28. An applied field shifts these indices to $n = 5.35$, 3.34, and 2.15. Such multimode behavior is readily visualized in the simulated images of panels c and d of Figure 3. However, because Si is more absorbing in the visible region, the propagation lengths of these modes do not exceed 3 μm. The accumulation layer induces higher losses in the structure, and modulation between the voltage-off and voltage-off states results almost exclusively from absorption of all modes. The higher absorption and multimode behavior at visible wavelengths suggest that this particular plasmostor design is ideally suited for near-infrared operation.

Experimental capacitance−voltage (CV) curves were used to characterize the electrical response of our fabricated plasmostor. Figure 4a shows a high-frequency CV curve obtained with a driving frequency of 100 kHz, measured over an area of approximately 100 μm × 100 μm. As the figure reveals, the plasmostor is in a state of inversion for negative biases, depletion for biases between 0 and 0.7 V and accumulation for biases greater than 0.7 V. The flat-band voltage, where the Si layer is charge neutral, occurs around 0.5 V. From the total observed accumulation capacitance (35 pF) of this sample region A_{meas}, we infer the capacitance of a typical plasmostor with areal dimensions $A_{plasmostor} = 4$ μm^2 as $C_{plasmostor} = C_{meas}(A_{plasmostor}/A_{meas}) = 14$ fF.

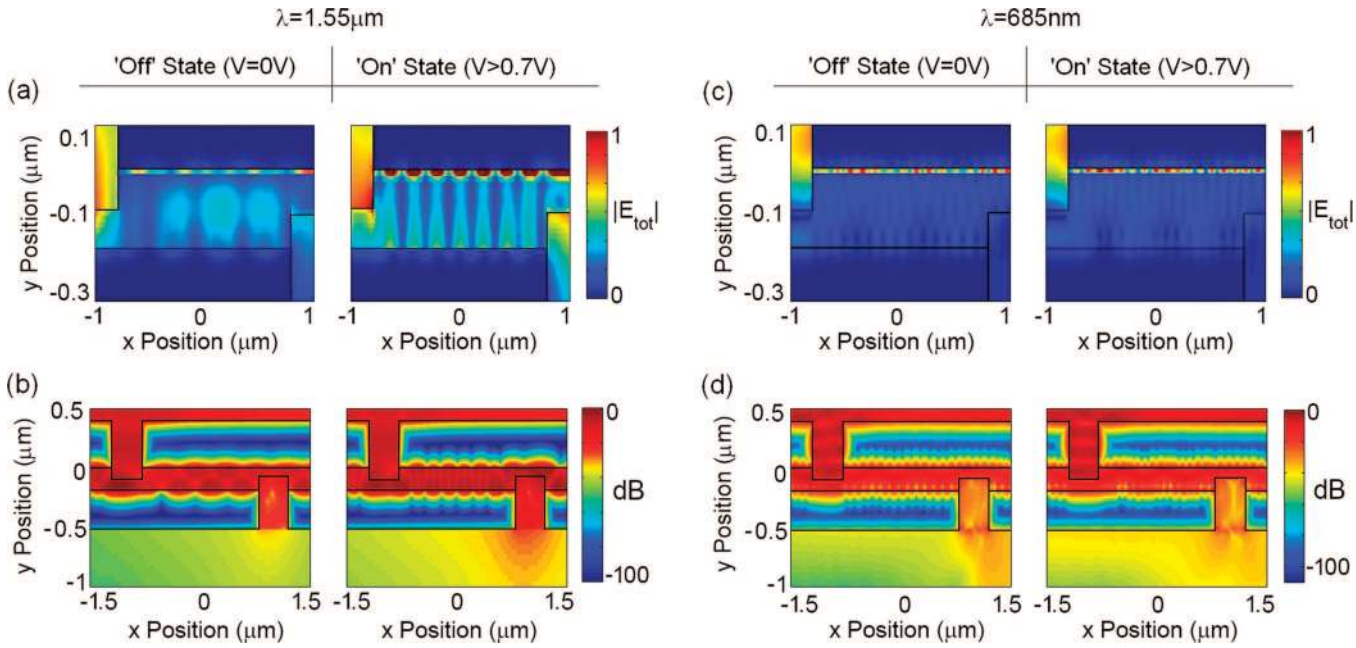


Figure 3. Finite difference time domain simulations of the plasmostor, showing the total electric field and the transmitted power for a 2 μm long optical source−drain separation. All panels correspond to the same plasmostor geometry, illuminated through the optical source with a Gaussian beam of wavelength $\lambda = 1.55$ μm (a, b) or $\lambda = 685$ nm (c, d). The slits are centered at $x = \pm 1$ μm, with the Ag/air interfaces located at $y \approx \pm 0.5$ μm. The electric field (a, c) and power (b, d) are monitored in both the voltage-off (depleted) and voltage-on (accumulated) states at each wavelength. The accumulated plasmostor state is modeled by modifying the unbiased Si permittivity with a spatially-varying Drude permittivity that reflects the increased charge concentration. (a) For plasmostor excitation with $\lambda = 1.55$ μm illumination and no applied gate bias (left column), fields are distributed throughout the Si core with sparse regions of high electric field in the oxide slot. However, with the onset of accumulation (right column), the Si-core mode is cutoff and fields are predominately confined to the thin SiO_2 slot. (b) When the power profiles are monitored in both the voltage-off (left column) and voltage-on (right column) states, a 10 dB increase in output power can be seen in the on (accumulated) state. (c and d) At $\lambda = 685$ nm, increased Si losses and multiple plasmostor modes decrease the observed field and power modulation between the voltage-off (left column) and voltage-on (right column) states.

To characterize the optical response, the out-coupled intensity from the plasmostor was monitored as a function of gate bias. An infrared laser source ($\lambda = 1.55$ μm) was focused onto a single device and transmission through the optical drain was imaged using a 50× microscope objective coupled to a Ge detector. Depending on the source−drain separation — and hence the interference condition of the photonic and plasmonic modes in the depleted state — transmitted intensity could increase or decrease with applied bias. As seen in Figure 4b, a modulator of length $d_1 = 2.2$ μm exhibits a pronounced intensity increase with increasing positive bias for $\lambda = 1.55$ μm. Consistent with the capacitance−voltage curves, modulation saturates around 0.7 V, corresponding to the onset of accumulation. In contrast, a modulator of length $d_2 = 7.0$ μm exhibits a 30% decrease in transmitted intensity for $\lambda = 1.55$ μm.

Full experimental optical characterization was achieved by varying the source−drain separation and the illumination wavelength, both with and without an applied bias. Panels c and d of Figure 4 show plasmostor transmission as a function of resonator length for source wavelengths of 685 nm and 1.55 μm, respectively. As seen in Figure 4c, at a wavelength of 685 nm, negligible modulation is observed for TM-polarized light between the voltage on and off states of the modulator. For shorter cavity lengths, transmission predominately decreases with applied bias. Cavities longer than 2.5 μm are dominated extinction, consistent with mode propagation lengths derived from calculations.

In contrast, the plasmostor exhibits pronounced modulation for near-infrared sources. As seen in Figure 4d, with no applied bias, plasmostor transmission at $\lambda = 1.55$ μm is characterized by an output signal comprised of both high- and low-frequency components. As illustrated by the dispersion diagram of Figure 2, these components correspond to the plasmonic and photonic waveguide modes, respectively. An applied bias of 0.75 V forces the photonic mode into cutoff, leaving only a single, high-frequency mode in the waveguide. Experimentally, the observed propagation length of this mode is in fair agreement the plasmonic mode losses predicted from calculations. The observed mode index is about half the calculated plasmon index, likely due to aliasing effects arising from the chosen optical source−drain separation step size. Still, source−drain separations ranging from 1 to 8 μm exhibit amplitude modulation ratios ranging between −3.15 dB (at $d = 7.5$ μm) and 4.56 dB (at $d = 2.6$ μm). Moreover, theoretical fits to the experimental data indicate that higher modulation ratios may be possible at shorter source−drain separations. Such observations are consistent with the simulations of Figure 3. To our knowledge, this plasmostor yields one of the highest reported near-infrared Si modulation depths in the smallest reported volume, with device volumes as small as one-half of a cubic wavelength.

Plasmostor modulation depths remain high for wavelengths spanning from 1.48 to 1.58 μm (the range of our infrared source), where changes in the complex refractive index of

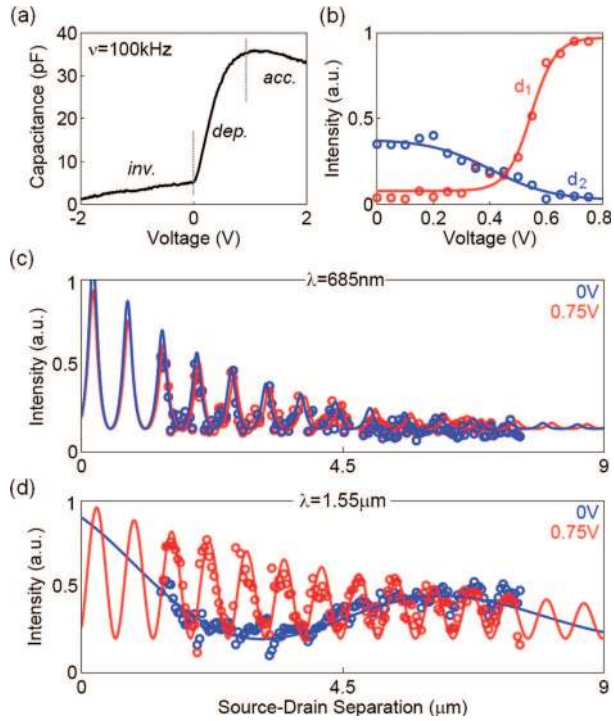


Figure 4. Experimental electrical and optical characterization of the plasmostor. (a) High-frequency (100 kHz) capacitance−voltage curve of the modulator over a ∼100 × 100 μm^2 area, showing that the plasmostor is in inversion for negative biases, depletion for biases between 0 and 0.7 V, and accumulation for voltages exceeding 0.7 V. The flatband voltage, where the Si is charge neutral, occurs around 0.5 V. From the accumulation capacitance of 35 pF, a device capacitance of 14 fF may be inferred for a typical 4 μm^2 plasmostor. (b) Optical drain intensity as a function of gate bias for two source−drain separations ($d_1 = 2.2$ μm and $d_2 = 7.0$ μm) at $\lambda = 1.55$ μm. The onset of significant modulation occurs around 0.5 V and saturates around 0.7 V, consistent with the accumulation-based operation of the device. (c and d) Optical drain intensity as a function of source−drain separation for the voltage-off state (blue, $V = 0$) and the voltage-on states (red, $V = 0.75$ V) at $\lambda = 685$ nm (c) and $\lambda = 1.55$ μm (d). Experimental points are shown as open circles, with the radius encompassing the experimental error. Best fits based on resonator theory are shown as solid lines.

Si induce cutoff of the photonic mode. For these wavelengths, significant modulation is preferentially observed in shorter resonator lengths ($d < 3$ μm), which in the depleted state produce destructive interference between the photonic and plasmonic modes. Previous Si modulators based on MOS capacitors, in contrast, require device lengths on the order of millimeters.[21] Interestingly, the internal waveguide propagation losses of the plasmostor are not significantly higher than 1 dB (for a source−drain separation of $d = 2.2$ μm, the plasmonic mode has a propagation loss of 0.5 dB). Thus, despite the higher losses generally associated with plasmonic components, the plasmostor exhibits propagation losses that are comparable with traditional Si- or dielectric-based modulators.[20−22]

We note that the prototype plasmostor reported here incurs additional losses from mode insertion and extraction through the "source" and "drain" slits employed in our device. Using full field electromagnetic simulations, we calculate an insertion loss of -12.8 ± 0.1 dB and an extraction loss of -3 ± 1 dB. Combined with the waveguide propagation losses, then, this prototype plasmostor exhibits a total on-chip loss of approximately −17 dB, in rough accord with the total experimentally determined loss of approximately −20 dB. However, we do not consider these high coupling losses intrinsic to device operation, since slit coupling is not fundamental to plasmostor modulation. In fact, our simulations indicate that by modifying the coupling geometry to simple, nonoptimized end-fire excitation from a Si-waveguide, an increased coupling efficiency of 36% (coupling losses of 4.4 dB) can be achieved. Moreover, as reported by Veronis and Fan,[24] optimization techniques have been proposed to achieve >90% incoupling efficiencies into plasmonic waveguides, corresponding to coupling losses as low as 0.3 dB. Thus, future plasmostors with a device length of approximately 2 μm and more optimal incoupling could achieve overall "on" state losses as low as 1.1 dB.

The frequency response of the plasmostor was characterized by applying a 4 V, 100 kHz pulse train to the modulator with a rise time of 10 ns. Plasmostor switching was determined to be at least as fast as 10 ns, which was limited by the frequency response of our pulse generator. We note, however, that modulation speeds of a plasmostor are likely to be fundamentally limited by the speed of formation of the MOS accumulation layer, as is true in a conventional small-geometry MOSFET; accordingly, plasmostor operation should be compatible with gigahertz modulation frequencies.

To explore the potential for gigahertz modulation in more detail, we conducted circuit simulations of our plasmostor driven into accumulation by *optical* means. For example, a photodiode connected to the plasmostor gate could provide sufficient power to modulate the channel properties.[25] Provided the photodiode could produce gate voltages exceeding 0.7 V, this coupled plasmostor−photodiode system could form the basis for all-optical MOS-based modulation. Figure 5 proposes such a scheme for all-optical modulation. As seen, a Ge p−i−n photodiode is connected to the plasmostor in parallel with a dielectric (a resistor). Here, the plasmostor is modeled using the experimentally inferred capacticance (14 fF) of a typical 4 μm^2 device. Similarly, the photodiode is modeled using circuit parameters from state-of-the-art small photodiodes[26] exhibiting quantum efficiencies of 10% under 6 mW optical illumination. Using a photodiode with an active area of 75 μm^2 and an ∼40 GHz bandwidth,[26] circuit simulation indicates coupled plasmostor–photodiode bandwidths of 3 GHz (Figure 5a). Scaling the photodiode active area to 4 μm^2 (and thereby increasing the photodiode bandwidth[26]), coupled plasmostor−photodiode bandwidths increase to 15 GHz. Further improvements could be achieved by varying the oxide thickness or the plasmostor gate length. Moreover, by tuning the magnitude of the optical carrier (λ_1) and signal (λ_2) sources, this coupled photodiode−plasmostor system could exhibit signal gain at the plasmostor drain.[25] This three-terminal, integrated optical device requires no electronic conditioning and can be fabricated from SOI waveguide technology, using, for instance, local oxidation of silicon (LOCOS) processing. Such processing would

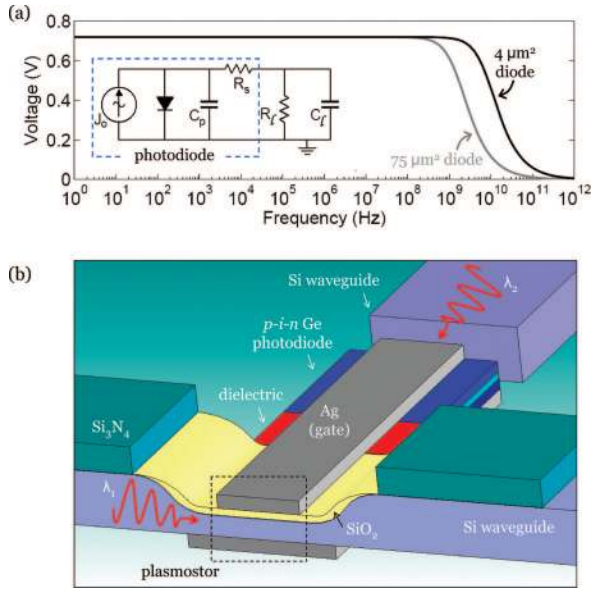


Figure 5. An all-optical, SOI-based plasmostor. An ideal photodiode is connected to a load resistor and the plasmostor, forming a three-terminal device capable of gigahertz operation. (a) Circuit analysis of the coupled photodiode−plasmostor system, modeling the photodiode after ref 26 and the plasmostor as a MOS capacitor with a capacitance of 14 fF. The load resistance was chosen so that the photodiode provides the appropriate gate bias to the plasmostor. Photodiodes with active areas of 75 μm^2 (gray curve) and 4 μm^2 (black curve) allow system bandwidths (3 dB roll-off frequencies) of 3 and 15 GHz, respectively. Bandwidths could potentially be improved by further decreasing the photodiode size or the modifying the channel thickness. Circuit parameters for the 75 μm^2 diode, load resistor (R_l), and plasmostor MOS capacitor (C_l) are $J_o = 0.6$ mA, $C_p = 66$ fF, $R_s = 32\ \Omega$, $R_l = 1200\ \Omega$, $C_l = 14$ fF. Parameters for the 4 μm^2 diode, resistor, and plasmostor are $J_o = 0.6$ mA, $C_p = 2$ fF, $R_s = 50\ \Omega$, $R_l = 1200\ \Omega$, $C_l = 14$ fF. (b) Schematic of an SOI-based all-optical plasmostor. Note that the dimensions of this device could reach subwavelength scales.

facilitate CMOS compatibility while minimizing optical insertion losses.

The plasmostor offers a unique opportunity for compact, Si-based field effect optical modulation using scaled electronic MOSFET technology. The empirically determined switching voltage (0.7 V) and capacitance (14 fF) yield a required switching energy of $E = CV^2 = 6.8$ fJ for a typical 4 μm^2 plasmostor device, commensurate with existing CMOS and optical logic gates.[27] To our knowledge, the plasmostor achieves the first electrical amplitude modulation of light in a plasmon waveguide. Furthermore, by modulating optical signals with a photodiode coupled to the gate, the plasmostor promises potential for opto-electronic and perhaps even all-optical Si-based modulation.

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(27) For comparison, existing Si-based optical logic gates require switching energies that range from 30 to 2.8 × 10^4 fJ per bit and span lateral areas ranging from 30 to 6000 μm^2. Tabulated properties of state-of-the-art Si-based modulators may be found in ref 22.

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