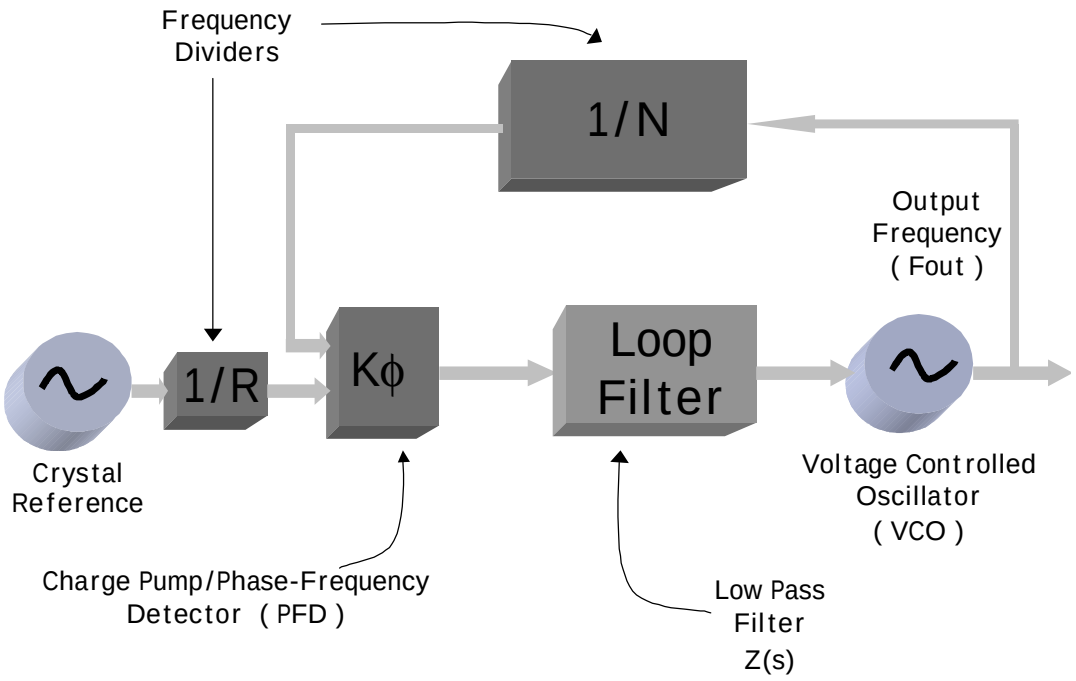
PLL Performance, Simulation, and Design



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i. Preface

Who This Book is Intended For

This book assumes experience working with passive loop filters. The basic design equations for the passive loop filter is in National Semiconductor's Application Note AN-1001 "An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops". Many of the basic concepts and design equations are given in this application note. This is available on the web at http://www.national.com/. It is also true that some of these papers are very specific to National Semiconductor's PLLs. However, most of the concepts apply to all PLLs. As the author of this book, I endorse National Semiconductor PLLs for reasons including their high quality, extensive portfolio, and excellent phase noise performance

How this Book Came to Be

I first became familiar with PLLs when I started working for National Semiconductor as a wireless applications support person. When dealing with customer support, I have noticed that many questions are asked over and over. Instead of creating the same response over and over, it made more sense to create a document, worksheet, or program to address the question in greater detail and just re-send the file. These files have evolved into a massive collection of papers, programs, excel worksheets, and mathcad programs. This is a collection of papers that have been used to explain many of the things that were observed in practice that were previously not understood.

The Value of a Rigorous Mathematical Approach

Many of these questions can be answered with a greater understanding of the problem and the mathematics involved. By approaching problems in a rigorous mathematical way one gains a greater level of understanding, a greater level of satisfaction, and the ability to apply the concepts learned to other problems. An excellent online mathematical reference is Eric's Treasure trove of mathematics at: http://www.astro.virginia.edu/~eww6n/math/math0.html

Many of the formulas that I have seen used before contain many approximations and are hard to find a justification of how they were derived. Also, many of these formulas are from textbooks that are out of date and make assumptions not true of the PLL system today. From these, rules of thumb are born that work only under certain conditions. All of these papers have some sort of computer simulation tool associated with them. I have also compared a lot of these simulated results against real results.

Credits

This book is a collection of my learnings on PLLs. There are other people who I have worked with in National Semiconductor who have aided in my understanding of PLLs and also in the editing of this book.

I would like to thank Ian Thompson for the insights that he has provided, particularly in the area of phase noise and the noise characteristics of the phase-frequency detector. I would lend special thanks Bill Burdette for all the editing, commenting, and RF insights that he has provided that has made this book possible. I would also like to thank Bill Keese for his insights, particularly in AN-1001, which serve as a basis for a lot of these documents. I would also like to thank Yuko Kanagy for her helpful insights.

ii. What's All of this PLL Stuff?

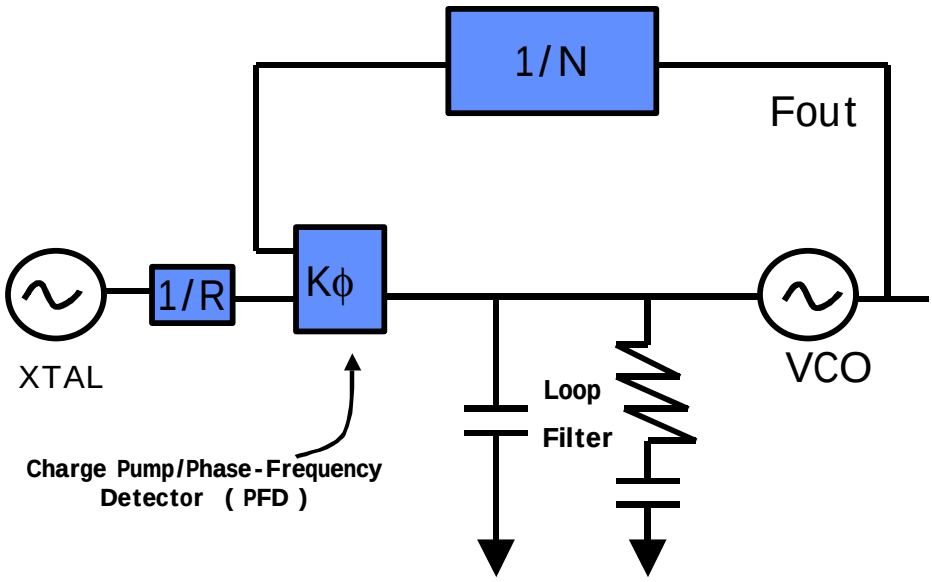


Figure 1 *The Basic PLL*

Basic PLL Operation

The PLL (Phased Locked Loop) starts with a stable crystal reference frequency. This frequency is divided by R to a lower frequency, which is called the comparison frequency. This is one of the inputs to the phase detector. The phase-frequency detector outputs a current which has an average DC value that is proportional to the phase error between the comparison frequency, and the output frequency after it is divided by the N divider.

If one takes this average DC current value and multiplies it by the impedance of the loop filter, then the input voltage to the VCO (Voltage Controlled Oscillator) can be found. Note that the loop filter is a low pass filter, often implemented with discrete components. This loop filter is application specific, and much of this book is devoted to the loop filter. This tuning voltage adjusts the output phase of the VCO, such that when divided by N, is equal to the phase of the comparison frequency. Since phase is the integral of frequency, this implies that the frequencies will also be matched, and the output frequency will be given by:

$$\textit{Output Frequency} = \frac{N}{R} \bullet XTAL \qquad (1)$$

This applies only when the PLL is in the locked state, and does not apply during the time when the PLL is adjusting to the locked state. For a given application, R is typically fixed, and the N value can easily be changed.

Note that the PLL technically refers to the entire system shown in figure 1, however, sometimes the PLL is meant to refer to the entire system except for the crystal and VCO. This is because these components are difficult to integrate on a PLL synthesizer chip.

iii. The Charge Pump PLL with a Passive Loop Filter

Why this Book Focuses on Charge Pump PLLs

This book focuses all of it's effort's on charge pump PLLs. The reason for doing so is that these are the vast majority of the PLLs in the market today, and that is what I have experience in dealing with. The charge pump PLL offers many advantages over the classical voltage phase detector PLL including an infinite pull in range and zero steady state phase error. There is also a considerable amount of literature that discusses in great detail features that are specific only to the voltage phase detector. This allows more time to discuss other features of the PLL, without getting caught up in the details of the phase detector. The charge pump PLL also allows one to use a passive filter and still have many of the benefits of using the active filter with the voltage phase detector. I have always recommended passive filters because they are lower cost and have no added noise. The exception to this case is when the VCO tuning voltage needs to be higher than the PLL can supply – in this case, an active filter is necessary.

The Classical Voltage Phase Detector

In the past, active filters have been emphasized for several reasons that are explained in depth in Floyd Gardner's classical book "Phaselock Techniques. Many of these concepts still apply to the charge pump PLL, while many others, such as the steady state phase error do not. The XOR gate and the mixer are both discussed as practical ways to implement a phase detector. In Gardner's book, the following classical active loop filter topology is presented.

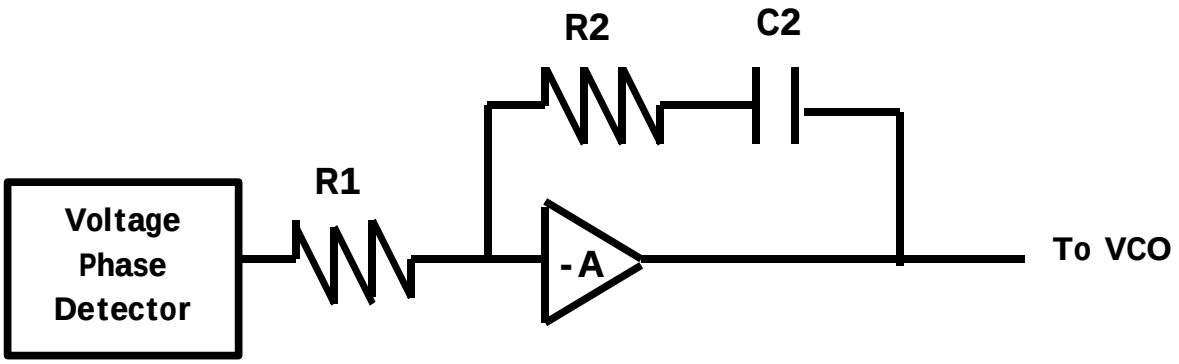


Figure 1 *Classical Active Loop Filter Topology for a Voltage Phase Detector*

The Modern Phase Frequency Detector with Charge Pump and it's Advantages

The phase frequency detector with charge pump combination offers several advantages over the voltage charge pump and has all but replaced it. The phase-frequency detector and charge pump are usually integrated on the PLL chip. Using this approach completely bypasses issues of steady state phase error and hold in range. The PLL with this combination can be compared to it's predecessor as is done in figure 2. Note that the circuit shown below with the box drawn around it integrates the functionality of the OP AMP. Note it is necessary to divide the phase detector voltage gain by R1 in order convert the voltage gain to a current gain.

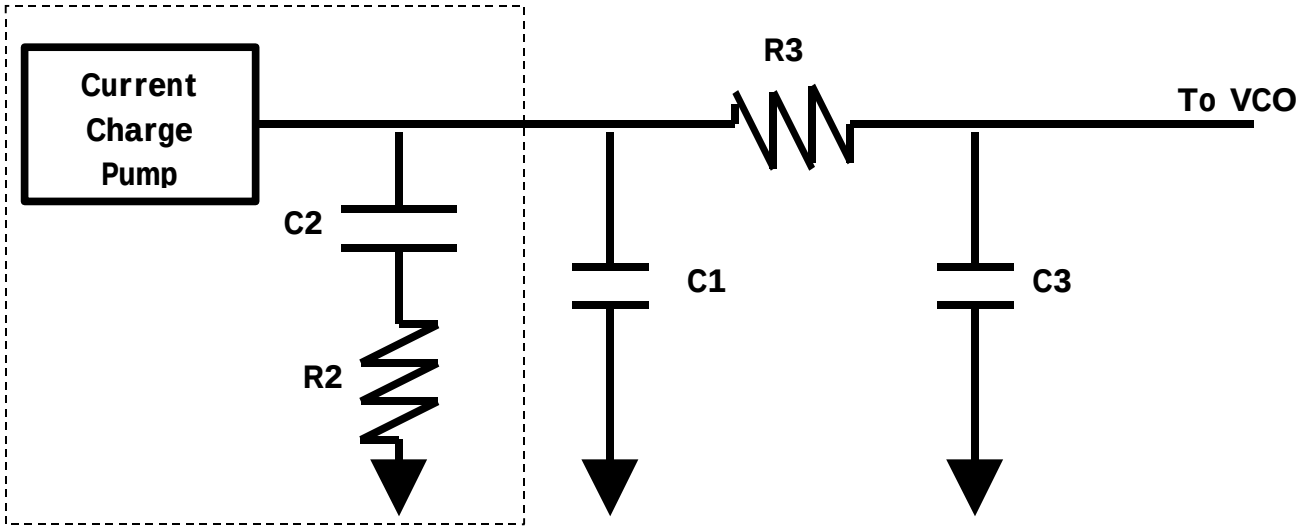


Figure 2 *Passive Loop Filter with Charge Pump*

The capacitor C1 is added, because it reduces the spur levels significantly. Also, the components R3 and C3 can optionally be added in order to further the reference spur level. Note that this passive filter has the OP AMP functionality included. Instead of the phase detector delivering a voltage proportional to the phase error, the charge pump delivers a current with average value proportional to the phase error. This current is actually a constant amplitude with variable duty cycle. It is usually sufficient to model this current as an analog current with the average value proportional to the phase error. This is called the continuous time approximation and is used in most of the chapters in this book.

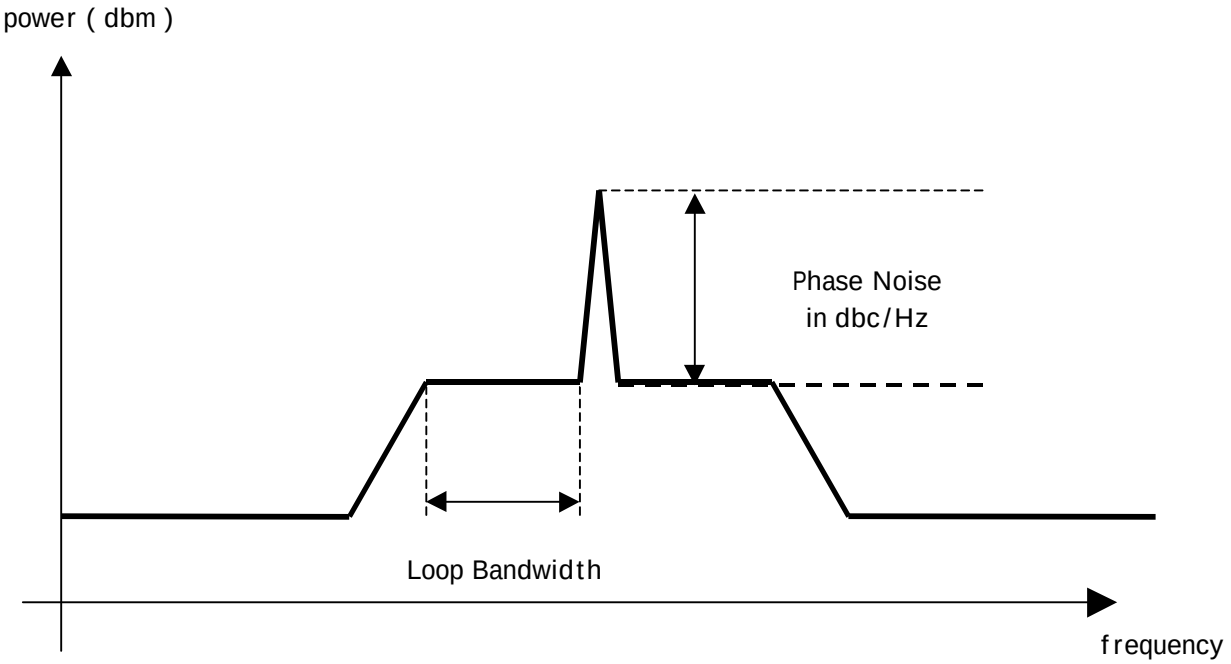
References

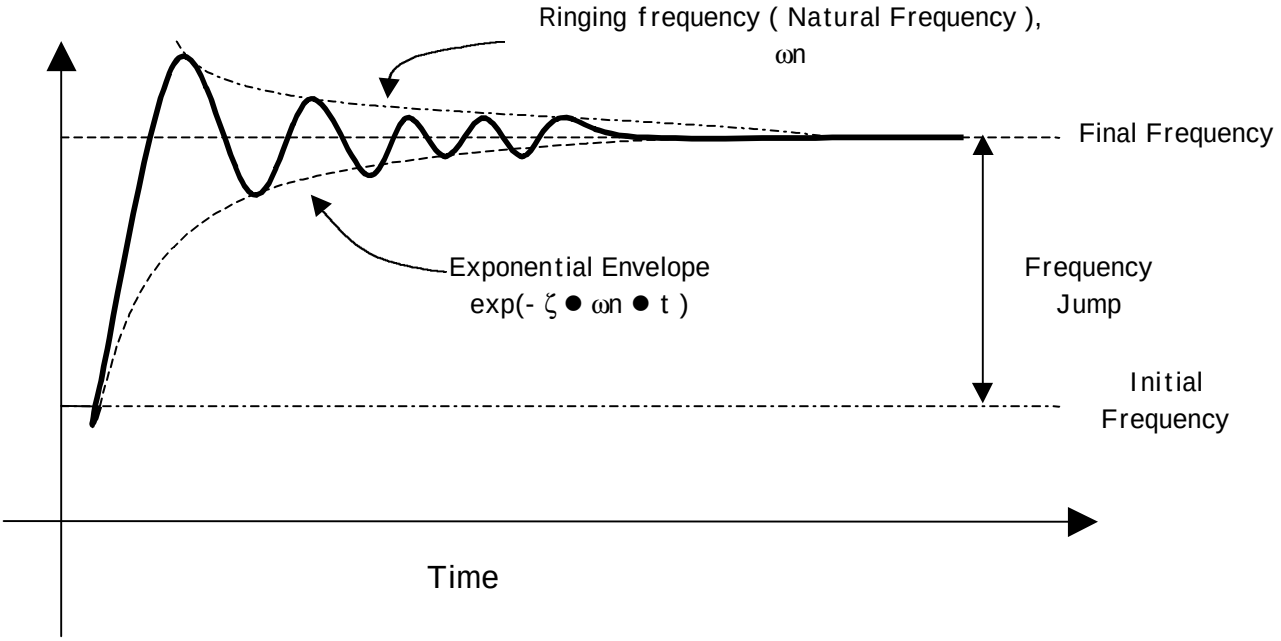
[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[2] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

[3] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

PLL Performance and Simulation





1. On Noise Sources in a PLL System

Introduction

This paper investigates phase noise sources and phase noise floor. The first part gives the theoretical derivations of the noise contributions to the PLL spectra. Whether the user is comfortable with these derivations or not, the second part shows an easy and simple way to apply these concepts to make reasonably accurate estimations of phase noise which are accurate to within a few db most of the time.

PLL Basic Structure

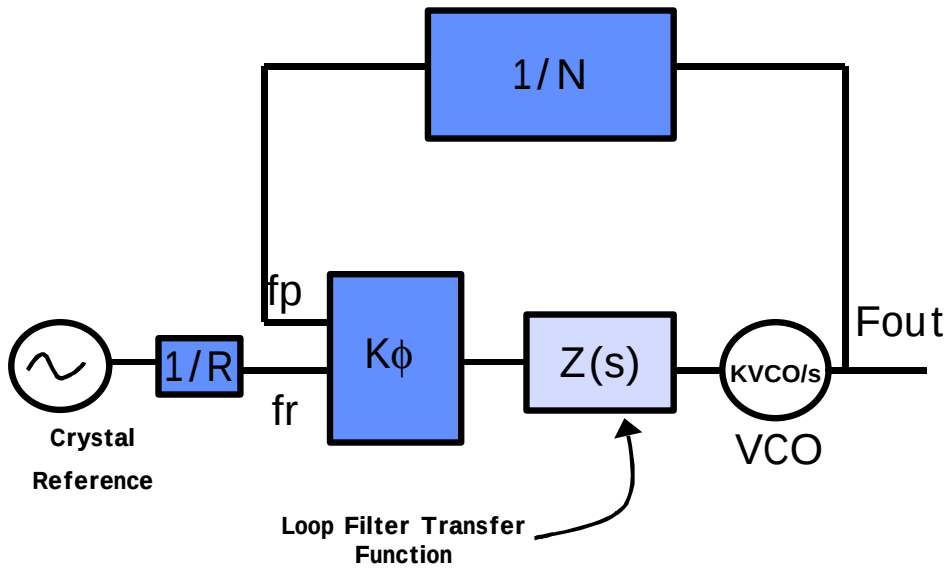


Figure 1 *Basic PLL Structure*

Continuous Time Approximation

In order to derive the transfer functions, it is necessary to introduce one approximation. It is the continuous time approximation, which approximates discrete current pulses from the phase detector as a continuous signal that has the same average value as the discrete pulses. This approximation becomes more rough as the comparison frequency approaches the loop bandwidth of the system. So, since the PLL charge pump puts out current pulses of magnitude $K\phi$ mA, the time averaged output of the charge pump would be $K\phi/2\pi$ mA/radian. Since the charge pump output $K\phi/2\pi$ multiplies the output of the VCO, KVCO●2π in all of the equations involved in this paper, the these factors of 2π cam be disregarded and pump output has been labeled as $K\phi$ and the VCO output has been labeled as KVCO in Figure 1.

Derivation of Transfer Functions

For the purposes of this paper it is easier to define the following transfer functions:

$$G(s) = \frac{K\phi \cdot Kvco \cdot Z(s)}{s} \tag{1}$$

$$H = \frac{1}{N} \tag{2}$$

Below is a chart showing various noise sources and the transfer functions that multiply each one.

Source	Transfer Function
Crystal Reference	$\frac{1}{R} \bullet \frac{G(s)}{1 + G(s) \bullet H}$
R Divider	$\frac{G(s)}{1 + G(s) \bullet H}$
N Divider	$\frac{G(s)}{1 + G(s) \bullet H}$
Phase Detector	$\frac{1}{Kf} \bullet \frac{G(s)}{1 + G(s) \bullet H}$
N Divider	$\frac{G(s)}{1 + G(s) \bullet H}$
VCO	$\frac{1}{1 + G(s) \bullet H}$

Table 1 *Transfer functions for various noise sources*

Analysis of Transfer Functions

In other words, if a noise source is introduced at the source labeled in Table 1, the noise is multiplied by the corresponding transfer function. Note that the crystal has a factor of 1/R multiplying it and the phase detector has a factor of 1/Kϕ multiplying it. It should be apparent that the phase detector noise, N divider noise, R divider noise, and the crystal noise all contain a common factor in their transfer functions. This function is given below.

$$\frac{G(s)}{1 + G(s) \bullet H} \tag{3}$$

For this reason, all of these noise sources will be referred to as in band noise sources. The loop bandwidth, ωc, and phase margin, ϕc, are defined as follows:

$$\left\| G(j \bullet \omega c) \bullet H \right\| = 1 \tag{4}$$

$$180 - \angle G(j \bullet \omega c) \bullet H = \phi c \tag{5}$$

Using these definitions, equations (1) and (2), and the fact that G(s) is monotonically decreasing in s yields the following:

$$\frac{G(s)}{1+G(s)\bullet H} \approx \begin{cases} N & \text{For } \omega << \omega c \\ G(s) & \text{For } \omega >> \omega c \end{cases} \tag{6}$$

However, the VCO noise is multiplied by a different transfer function:

$$\frac{1}{1+G(s)\bullet H} \tag{7}$$

Note that this transfer function (7) can be approximated by:

$$\frac{\mathbf{1}}{\mathbf{1}+\boldsymbol{G(s)}\bullet \boldsymbol{H}} \approx \begin{cases} \dfrac{\boldsymbol{N}}{\boldsymbol{G(s)}} & \textit{For } \boldsymbol{w << wc} \\ \mathbf{1} & \textit{For } \boldsymbol{w >> wc} \end{cases} \tag{8}$$

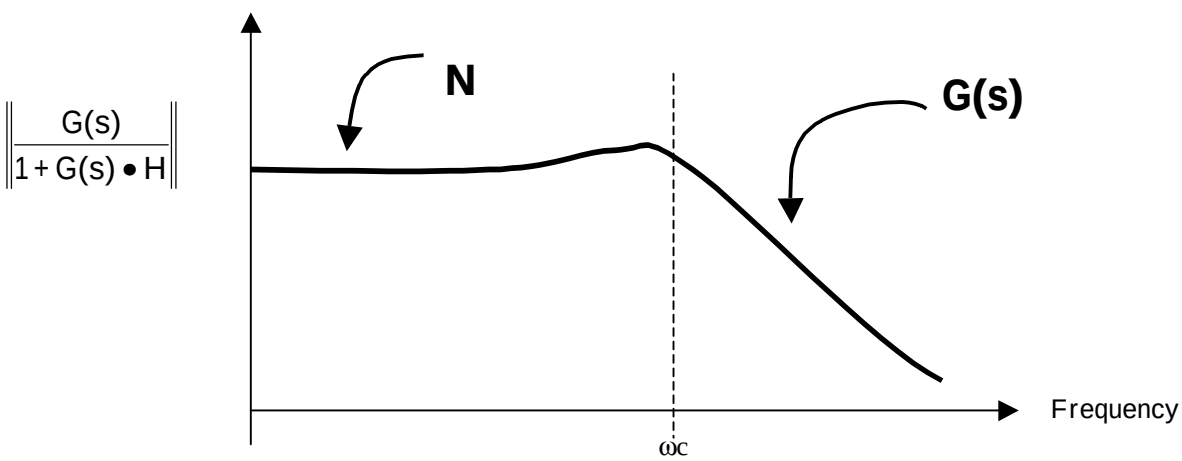


Figure 2 *Transfer Function Multiplying all Noise Sources Except the VCO*

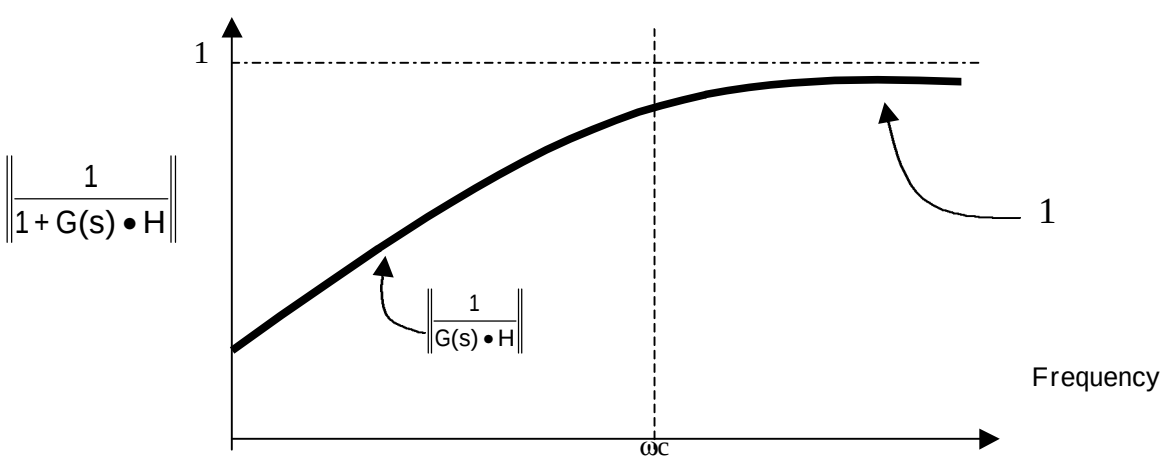


Figure 3 Transfer Function Multiplying the VCO Noise

Design for Optimal Loop Bandwidth

It should be noted from this discussion that the in band sources dominate within the loop bandwidth, that is for $\omega \ll \omega c$ and the VCO noise dominates outside of the loop bandwidth, that is for $\omega \gg \omega c$. This can be seen in figure 4. The phase noise measured at an offset that is close to the carrier is basically independent of loop bandwidth, provided that the loop bandwidth is sufficiently wide to eliminate the VCO noise. However, the RMS phase error is more dependent on the loop bandwidth. To theoretically design for the lowest RMS phase error, this means that one needs to design such that the VCO noise contribution at $\omega = \omega c$ is equal to the total noise contribution from the other sources at $\omega = \omega c$. Typically this number is in the ballpark of a few kilohertz. If the VCO is noisy relative to the PLL, then this number would be smaller, and if the PLL is noisy relative to the VCO, then this number would be larger.

Note that although the noise within the loop ($\omega \ll \omega c$) is dominated by the in band sources, there may be some slight contribution to this noise from the VCO. This is most noticeable for narrow loop bandwidths, which are less than the theoretical optimal loop bandwidth.

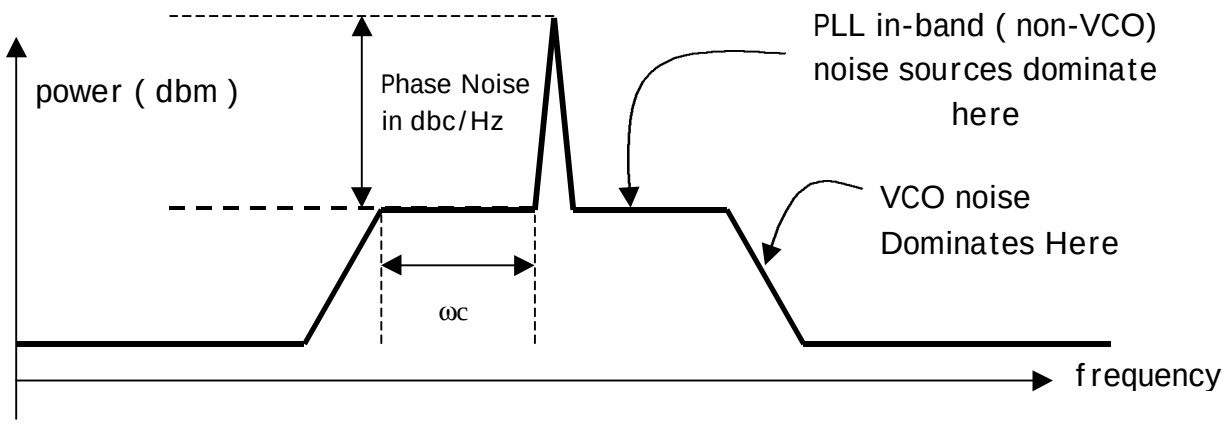


Figure 4 *Typical Phase Noise Spectral Plot for a PLL*

Phase Noise and Phase noise Floor

From the equations in the previous sections, one could notice that within the loop bandwidth, the VCO noise contribution should be small, and the in band noise sources are multiplied by N. Since this is a noise voltage, the noise power would be proportional to N^2, hence the common misconception that the phase noise will vary with 20●log(N). There is nothing wrong with this theory, however, it disregards the effects of the phase detector.

Phase Noise Floor

Phase noise floor is defined as follows:

PhaseNoiseFloor = **PhaseNoise** *(Accounting For Resolution Bandwidth)* – **20● log(N)** (9)

Noise Contribution Due to the Discrete Sampling Action of the Phase Detector

Assuming a digital 3-state phase-frequency detector, this will put out more noise at higher comparison frequencies. The phase-frequency noise also tends to be the dominant noise source, which is proportional to the comparison frequency. However, the comparison frequency

is inversely proportional to N. So the bottom line is that the noise due to the phase detector degrades in accordance with 10●log(N).

Prediction of Close in Phase Noise as a function of N

Combining the 20●log(N) noise improvement due to the transfer function and the 10●log(N) degradation due to the added phase detector noise, the net effect on phase noise is:

$$10 \bullet \log(N) \qquad (10)$$

In other words, if N were increased by 10, there would be a 10 db degradation in the phase noise. This completely describes the variation of phase noise floor in AN-1052. This is why phase noise floor is not a very meaningful without also knowing the comparison frequency.

Prediction of Close in Phase Noise in General

National's PLLs have different phase noise performance for different parts. Here is some data for each of these parts. Note that this information is subject to change and is not guaranteed. It is true that the dividers, Crystal Reference, and VCO contribute to the in-band phase noise, but these are typically dominated by the noise of the phase detector. Since the phase detector noise is dependent on the comparison frequency, this table is normalized for what the phase detector noise would theoretically be for a 1 Hz comparison frequency. This table is based on sample data taken from evaluation boards.

PLL	1 Hz Normalized Phase Detector Noise Floor (dbc/Hz)
LMX233x LMX233xL	-211
LMX23x6 single	-210
LMX15x1,23x5	-206
LMX2350/52	-201
LMX 1600 family	-199

Table 2 *1 Hz Normalized Phase Noise Floor for Various National PLLs*

To predict the phase noise, use:

Phase Noise = **(1 Hz Normalized Phase Noise Floor from Table)**
+ **10●** log*(* **Comparison Frequency** *)* + **20●** log(**N**) (11)

For example, for a 900 MHz VCO with a 200 KHz comparison frequency (N=4500), using an lmx2315, the predicted phase noise would be:

-206 + **10** ● log(**200000**) + **20●** log(**4500**) = **- 80** dbc/Hz (12)

Table 2 gives a rough indication of how one PLL will perform against another, and the expected db difference is simply the difference in the numbers from the table. Note for the fractional N PLL (lmx2350/52), the phase noise floor can be deceptive. Since the fractional N capability allows one to use a higher reference frequency, the actual phase noise tends to be better, despite the fact that the phase noise floor is degraded. This is because the value of N will

be smaller. So one should be cautious about comparing the noise floor of this part directly to other parts.

Adjustments to the Above Phase Noise Calculations

The phase noise numbers in the table give reasonably accurate estimates for phase noise in most cases. There will be some part to part variation and layout dependency, although these tend to not be very much. The numbers in the chart assume that the in-band phase noise is dominated by the charge pump, which is usually (but not always) the case. There are several other factors that could have an impact on the phase noise.

1. In-Band VCO Phase Noise Contribution

For the purposes of the phase noise calculations presented, the VCO noise contribution within the loop bandwidth is considered to be negligible. Referring back to figure 3 indicates that the VCO actually does contribute noise within the loop bandwidth. This transfer function is increasing within the loop bandwidth, however the VCO noise is a decreasing function. When these two functions are multiplied together, the result is relatively flat. The VCO tends to contribute more noise within the loop bandwidth in the cases where the loop bandwidth is narrow or in the case of a noisy VCO.

2. Lower Charge Pump Gain Phase Noise Adjustment

The PLL noise chart assumes that the PLL is in the highest charge pump gain. Note from the transfer functions that the charge pump noise is divided by the charge pump gain. However, it is usually the case that when the charge pump gain is increased, the charge pump noise is increased as well. In some cases, there is no difference in phase noise when the charge pump is used in different gains, and in others, the phase noise is better when the charge pump is used in the higher gains. For this reason, all of the numbers specified in the table are for when the charge pump is in it's highest gain state. If this is not the case then the phase noise may be degraded. The influence of the charge pump gain on the phase noise is therefore specific to the PLL chip used. In the case of National Semiconductor parts, a rough rule of thumb is that below 1 mA of charge pump gain, the gain of the charge pump has little effect on the phase noise, but above 1 mA, the charge pump gain does impact the phase noise. Going from a 4 mA to a 1 mA charge pump gain has been measured to cause a typical degradation in phase noise of about 4 db in the lmx233x family. Going from a 2 mA to a 1 mA mode charge pump gain typically can cause about a 2 db degradation in the phase noise. This characteristic of having the best phase noise performance at higher charge pump gains is a characteristic of National PLLs along with other manufacturers PLLs as well.

3. Dual PLL Adjustment

In the dual PLL, it has been found that the optimal phase noise performance is when the other side of the PLL is unused, powered down, and with no VCO connected. If this is the case, then this results in a 2 db improvemen*t* from what the table predicts. The table assumes that the other PLL is powered down, but the VCO is connected. If the other side is powered up and running, then the degradation in phase noise may be a db or two worse than the table predicts. The closer the output frequencies of the two PLLs are, the more severe the phase noise degradation.

4. Noisy Crystal Reference Consideration

It is assumed that the charge pump noise dominates. However, this may not be the case if the crystal reference is noisy. The crystal noise is divided by R and multiplied by N. One way to see if the crystal noise is dominating is to double the crystal frequency and double the R value, if the phase noise changes, then this suggests that the crystal noise is dominating.

Conclusion

This paper has investigated the causes of phase noise and has provided a somewhat accurate model of how to predict it. This model has been predicted in practice. Phase noise can vary from board to board and part to part, but typically this variation is in the order of a few dbs. However, it is foolish to rely too heavily on this mathematical model, since there are cases where the model is substantially off.

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[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[2] Franklin, F. , Powell, D., and Emami-Naeini, A. *Feedback Control of Dynamic Systems*, 3rd ed. , Addison-Wesley, 1994

Measured Phase Noise For Various National PLLs

Part	Title	Fout	Fcomp	N	CP	CP	Dual	Noise Floor (dbc/Hz)			Phase Noise		
		(MHz)	(KHz)		%	Adj	Adj	Base	Adj	Actual	Predicted	Actual	
Evaluation Boards													
lmx1600	1600eval	1780	200	8900	100	0	0	-199	-199	-197.4981	-67.0019	-65.5	2
lmx1601/02	1601eval	889	200	4445	10	2	0	-199	-197	-197.0677	-71.03226	-71.1	1,2
lmx2306	demo2306	235	50	4700	100	0	0	-210	-210	-210.1317	-89.56834	-89.7	
lmx2316	demo2316	889	200	4445	100	0	0	-210	-210	-207.2677	-84.03226	-81.3	
lmx2326	demo2326	1930	200	9650	100	0	0	-210	-210	-209.7008	-77.29915	-77	
lmx2301	lmx2301g	137.5	100	1375	100	0	0	-206	-206	-182.2661	-93.23395	-69.5	3
lmx1501	lmx1501g	900	200	4500	100	0	0	-206	-206	-196.0746	-79.92545	<-70	
lmx1511	lmx1511g	900	200	4500	100	0	0	-206	-206	-206.0746	-79.92545	-80	
lmx2315	lmx2315g	900	200	4500	100	0	0	-206	-206	-206.0746	-79.92545	-80	
lmx2325	lmx2325g	2425	1000	2425	100	0	0	-206	-206	-206.8942	-78.30577	-79.2	
lmx2330	2330aevl	2425	1000	2425	100	0	0	-211	-211	-207.6942	-83.30577	-80	2
lmx2330l	2330levl	2425	1000	2425	100	0	0	-211	-211	-207.2942	-83.30577	-79.6	2
lmx2331	2331evl	1775	200	8875	100	0	0	-211	-211	-211.7737	-79.02633	-79.8	2
lmx2331L	2331levl	1775	200	8875	100	0	0	-211	-211	-211.7737	-79.02633	-79.8	2
lmx2332	2332aevl	900	200	4500	100	0	0	-211	-211	-207.0746	-84.92545	-81	2
lmx2332L	2332leval	900	200	4500	100	0	0	-211	-211	-207.0746	-84.92545	-81	2
lmx2336	2336eval	1830	200	9150	25	4	0	-211	-207	-207.0387	-74.76128	-74.8	2
lmx2336	2336evla	1780	200	8900	100	0	0	-211	-211	-210.6981	-79.0019	-78.7	2
lmx2350	2350eval	1960	160	12250	100	0	0	-201	-201	-200.2039	-67.19608	-66.4	2
lmx2352	2352eval	902	160	5638	100	0	0	-201	-201	-200.2629	-73.93707	-73.2	2
Characterization Data													
lmx2331A	LowPwr	1653	300	5510	100	0	-2	-211	-213	-213.0942	-83.40576	-83.5	2
lmx2331L	LowPwr	1653	300	5510	100	0	-2	-211	-213	-212.8942	-83.40576	-83.3	2
lmx2332A	LowPwr	1017	25	40680	100	0	-2	-211	-213	-211.767	-76.83298	-75.6	2
lmx2332L	LowPwr	1017	25	40680	100	0	-2	-211	-213	-211.467	-76.83298	-75.3	2
lmx1600	LowCost	903	25	36120	100	0	-2	-199	-201	-199.3344	-65.86565	-64.2	2
lmx1600	LowCost	903	200	4515	100	0	-2	-199	-201	-200.8035	-74.89654	-74.7	2
lmx1601	LowCost	903	25	36120	100	0	-2	-199	-201	-199.1344	-65.86565	-64	2
lmx1601	LowCost	903	200	4515	100	0	-2	-199	-201	-200.6035	-74.89654	-74.5	2
lmx1602	LowCost	903	25	36120	100	0	-2	-199	-201	-199.5344	-65.86565	-64.4	2
lmx1602	LowCost	903	200	4515	100	0	-2	-199	-201	-200.4035	-74.89654	-74.3	2
lmx2306	LowPwr	235	50	4700	100	0	0	-210	-210	-207.2317	-89.56834	-86.8	
lmx2306	LowPwr	245	50	4900	100	0	0	-210	-210	-202.7936	-89.20638	-82	
lmx2306	LowPwr	250	50	5000	100	0	0	-210	-210	-208.4691	-89.0309	-87.5	
lmx2316	LowPwr	889	200	4445	100	0	0	-210	-210	-207.2677	-84.03226	-81.3	
lmx2316	LowPwr	902	200	4510	100	0	0	-210	-210	-206.7938	-83.90617	-80.7	
lmx2316	LowPwr	915	200	4575	100	0	0	-210	-210	-207.9181	-83.78188	-81.7	
Databook													
lmx1511	DataSheet	886	25	35440	100	0	0	-206	-206	-210.4693	-71.03073	-75.5	
lmx2320	DataSheet	1669	300	5563	100	0	0	-206	-206	-210.7779	-76.32209	-81.1	
lmx2315	AN-1001	900	200	4500	100	0	0	-206	-206	-205.6746	-79.92545	-79.6	
lmx2332A	AN-1052	900	31.25	28800	100	0	-2	-211	-213	-213.9363	-78.86365	-79.8	2

Comments

1. For the LMX233x, 4X current mode is 4 db better than 1X.
2. Best performance is with IF VCO disconnected, 2nd best with IF poweroff, 3rd IF running.
3. These boards have discrete VCOs and narrow loop bandwidths, thus their bad in-band phase noise.

2. On RMS Phase Error

Introduction

This chapter discusses RMS Phase error, how to calculate it, the relevance it has in digital communications, and how to minimize it.

What is RMS Phase Error?

There are three different ways of visualizing RMS phase error. It can be visualized in the time domain, in the frequency domain, or in a constellation diagram. These different interpretations of RMS phase error are all related and discussed below.

RMS Phase Error In the Time Domain

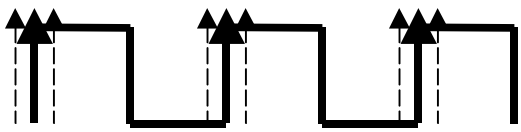


Figure 1 *Illustration of RMS Phase Error on a signal in the Time Domain*

The above figure shows a square wave Note on the rising edges of the square wave do not always occur at exactly the time they should, but have a random phase error that can be either positive or negative. Now the average value of this phase error is zero, but the variance is nonzero and is called the RMS phase error. Recall for the normal distribution, approximately 68% of the area of the normal distribution curve is within one standard deviation of the mean. This means that that if one was to take a random sample of the starting phase, 68 % of the time it would be within the RMS phase error. Notice how the rising edges of the signal do not always start at the time they should, but sort of jitters. For this reason, RMS phase error and phase noise are often referred to as "phase jitter". Although the output of a PLL tends to be a sine wave (instead of a square wave), there is little loss of generality here, because the sine wave is run through counters that turn it into a square wave.

For an example, consider a 10 MHz signal with 5 degrees RMS phase error. Since the period of this signal is 0.1 uS, a 5 degree RMS phase error imply a normally distributed random phase shift which has a standard deviation of 1.339 nS.

RMS Phase Error Calculation from Frequency Domain

Formula for Relating Spectral Density to RMS Phase Error

RMS Noise is calculated by integrating the phase noise, taking the square root, and then converting from radians to degrees.

$$\boldsymbol{RMS\ \ Phase\ \ Error = \frac{180}{p} \bullet \sqrt{\int_0^{\infty} L(f) \bullet df}} \qquad (1)$$

Why this Formula Works

It will now be explained why RMS phase error is calculated in this way. Refer to figure 2 for clarification. Phase Noise is measured in dbc/Hz on a spectrum analyzer, which shows the output power vs. frequency. Since phase noise is measured at a particular frequency output, it can be thought of as the ratio of the power of the carrier frequency to the power of an unwanted noisy frequency, expressed in a decibel scale. This can also be thought of as a phase noise density, which is actually a more accurate name for it than phase noise at a particular offset, as it is commonly called. This book, and many other sources use the term phase noise, but what is really being referred to is phase noise density. In other words, phase noise density is the same thing as a noise concentrated at a particular frequency, since phase is the integral of frequency. To obtain the total phase error, it is therefore necessary to integrate the phase noise (density) over the whole frequency spectrum.

Since the spectrum analyzer displays power vs. frequency, and not voltage vs. frequency, it is necessary to take the square root of the integrated product to obtain an RMS (Root Mean Square) error. Since number obtained is a dimensionless value in radians, it is necessary to convert this to degrees. This is the logic behind formula (1).

Approximate RMS Phase Error Calculation

To calculate the RMS noise correctly, the spectral density needs to be known. This requires knowledge of the PLL and VCO. Methods for predicting phase noise are in this book, but the VCO noise is unknown, and can be very relevant. One way to estimate the VCO noise is to assume that it decreases 20 db/decade from the PLL loop bandwidth. This approximation is shown below.

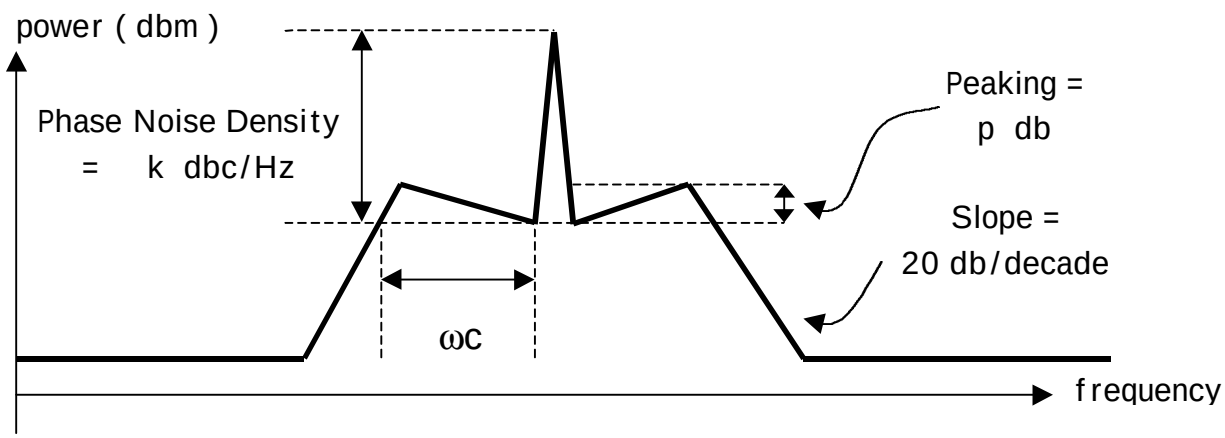


Figure 2 *Typical Phase Noise Spectral Plot for a PLL*

Approximate Calculation of RMS Phase Error

To calculate the RMS Phase Error, formula (1) will now be applied. Since the phase noise density, k, is expressed in dbc/Hz, it is necessary to convert this from decibels to scalar units before the integration is performed.

$$RMSnoise = 2 \bullet \frac{180}{p} \sqrt{\int_0^{fc} 10^{k/10} \bullet \left(1 + \left[10^{p/10} - 1\right] \bullet \frac{f}{fc}\right) \bullet df + \int_{fc}^{\infty} 10^{(k+p)/10 - 20 \bullet \frac{\log(f - fc + 1)}{10}} \bullet df}$$

$$= \frac{360}{p} \bullet 10^{k/20} \sqrt{\frac{fc}{2} \bullet \left(1 + 10^{p/10}\right) + 10^{p/10}}$$

Note that for the purposes of simplifying calculations, it was assumed that the phase noise peaks at the loop bandwidth, but in actuality, the peaking occurs slightly before the loop bandwidth as shown in figure 2. The impact of this is to cause these estimations to be slightly lower than actual. 3 db is a typical value for the peaking which would be typical for a 45 degree phase margin, however, it makes sense to use a value slightly higher, since this will help compensate for the fact that the estimates are slightly low. A good value to use is about 4 db.

Since this model makes some assumptions about the VCO, it makes sense to introduce approximations. Note that the second term under the square root is very small compared to the first term for any loop bandwidth that is reasonable. If one neglects the second term and assumes 4 db of peaking, an easier to use formula can be generated.

$$RMSnoise = 150 \bullet 10^{k/20} \sqrt{fc}$$

If 0 db of peaking, then multiply this result by 75%, if 3 db of peaking is assumed, then multiply this result by 92%, and if 10 db of peaking is assumed, multiply this result by 177%.

For a System with 10 KHz loop bandwidth, and –80 dbc/Hz phase noise, (assume 4db peaking):

$$RMS\ Phase\ Error = 150 \bullet 10^{-80/20} \bullet \sqrt{10000} = 1.5\ degrees$$

Choice of Loop Bandwidth for Optimal RMS Phase Error

This formula implies that a narrower loop bandwidth implies less RMS phase error, but in fact this is only true to a point. The validity of the approximations used in the above formula degrade if the loop bandwidth is too narrow. After decreasing the loop bandwidth beyond this point (where the PLL noise equals the VCO noise), the phase error actually starts to increase. It follows that for optimal RMS phase error, one should choose the loop bandwidth of the system such that the PLL noise is equal to the free-running VCO noise at that point. This is because within the loop bandwidth, the main noise contribution is from the PLL (everything except for the VCO), while outside of the loop bandwidth, the main noise contribution is the VCO.

RMS Phase Error Interpretation in the Constellation Diagram

If one visualizes the RMS error in the time domain, then it can be seen why this may be relevant in clock recovery applications, or any application where the rising edges of the signal need to occur in a predictable fashion. However, the it's relevance is more obvious when considering a constellation diagram.

The constellation diagram shows the relative phases of the I (in phase) and Q (in quadrature -– 90 degrees phase shift) signals. Each point on the constellation diagram corresponds to a different symbol, which could represent multiple bits. Below is a constellation diagram for QPSK.

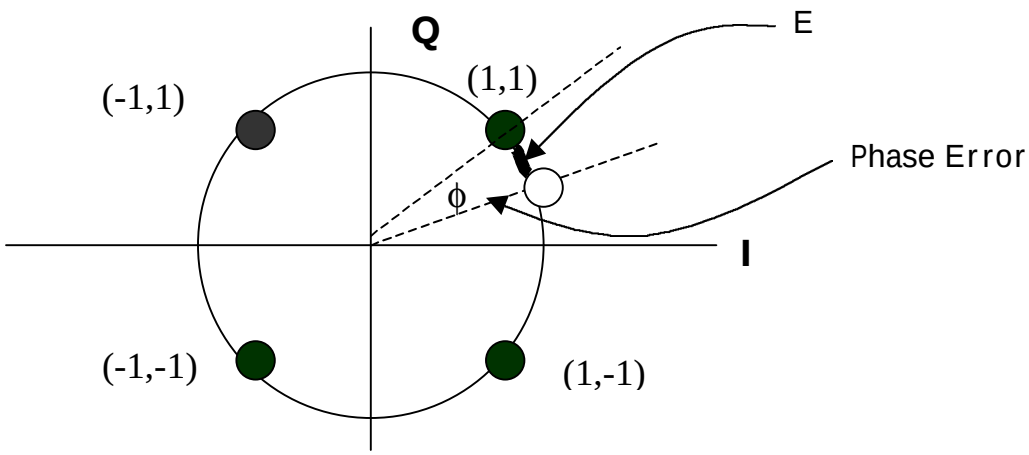


Figure 3 *Impact of RMS phase Error Seen on a Constellation Diagram*

Consider an ideal system in which the only noise-producing component is the PLL in the receiver. In this example, the symbol corresponding to the bits (1,1) is the intended message indicated by the darkened circle. However, because the PLL has a non-zero RMS phase error contribution, the received signal is actually the non-filled circle. If this experiment was repeated, then it would be found that the phase error between the received and intended signal was normally distributed with a standard deviation equal to the RMS phase error. It should be clear that if the RMS phase error of the system was too large, it could actually cause a the message to be interpreted as (-1, 1) or (1,-1). It should also be clear from this constellation diagram interpretation of RMS phase error that higher order modulation schemes are more subject to the RMS phase error of the PLL. If one considers that a real communications system will have a noisy channel and other noisy components, it should be clear why RMS phase error of the PLL is also relevant when compounded with these other effects.

Other Interpretations of RMS Phase Error

Eye Diagram

One popular way of viewing RMS phase error is the eye diagram. The impact of the RMS phase error on the eye diagram is that it causes it to close up. This means that the decision region is smaller and it is more likely to make an error in which bits were sent.

Error Vector Magnitude (EVM)

Error Vector Magnitude is the magnitude of the vector formed from the intended message and the actual message received (refer to figure 3). This is commonly expressed as a percentage of the error vector relative to the vector formed between the origin and intended message. Referring to figure 3, assuming the circle has radius R, and applying the law of cosines yields the magnitude of the error vector (E) to be:

$$E = 2 \bullet R^2 - 2 \bullet R^2 \bullet \cos(f)$$

Assuming that ϕ is small, and using the taylor series expansion $\cos(\phi) = 1 - \phi^2/2$, yields the following relationship between RMS phase error and EVM:

$$EVM = 100\% \bullet \left(\frac{p}{180}\right) \bullet \left(RMS\ \ Phase\ Error\ in\ Degrees\right)$$

Conclusion

The meaning, calculation, and relevance of the RMS phase error have been discussed. Lower phase noise in the PLL implies a lower RMS error. Unlike the phase noise discussed in the previous chapter, the RMS phase error is very dependent on the loop bandwidth of the system.

3. Reference Spurs and their Causes

Introduction

In PLL frequency synthesis, reference sidebands and spurious outputs are an issue in design. There are several types of these spurious outputs and they can be caused by many different causes. However, by far, the most common type of spur is the reference spur. These spurs appear at multiples of the comparison frequency.

This paper investigates the causes of these reference spurs and how they can be minimized. These spurs are mainly caused by mismatches and leakages in the charge pump of the PLL. At lower comparison frequency, there is a tendency for leakage to dominate. 30 KHz is considered low. At higher comparison frequencies, mismatch tends to dominate. 200 KHz is considered higher. This paper investigates all three of these issues independently.

Causes of Reference Spurs

Leakages of components and mismatches in the charge pump can cause an AC modulation on the tuning line of the VCO, which can be viewed as FM modulation. This FM modulation gives rise to reference spurs. This is discussed in detail in the appendix.

<u>Leakage Related Spurs</u>

At lower comparison frequencies, leakage effects are the dominant cause of reference spurs. When the PLL is in the locked condition, the charge pump will put out short alternating pulses of current with long periods in between in which the charge pump is tri-stated. See figure 1 for a description of this.

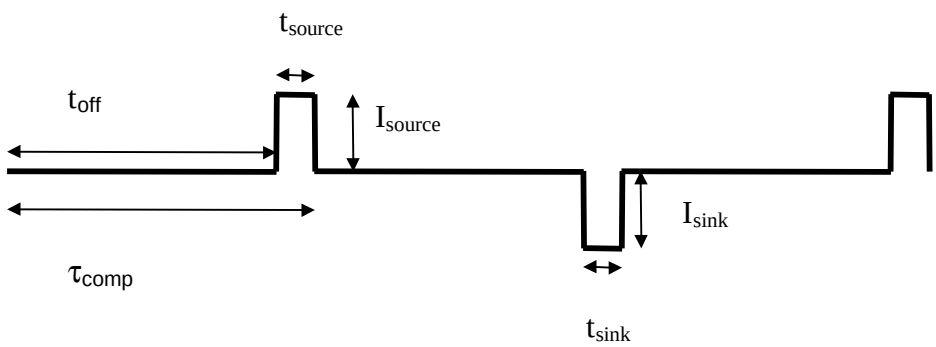


Figure 1 *Output of the charge pump in when the PLL is in the locked condition*

When the charge pump is off for a period of time equal to t_{off} there would ideally be an infinite impedance of the charge pump. However, there will be in fact be some leakage through the charge pump. One must also be aware that there will also be leakage through the VCO, capacitors in the loop filter, and even the board. To protect against leakages not due to the PLL, it is good to lay out components in the loop filter farther apart, make sure that the board is clean, use sealants if necessary to protect the board against humidity, use capacitors with good leakage properties, and use VCOs with low leakage. Leakage has a tendency to dominate at lower reference frequencies because the period that the charge pump has to leak is longer, since the comparison frequency period, τ_{comp} is longer.

The leakage due to the PLL charge pump is temperature dependent and is often given guaranteed ratings as well as typical ratings and graphs in performance. The leakage of the charge pump increases with temperature, so spurs caused by leakage of the charge pump tend to increase when the PLL is heated.

Theoretical predictions for spur levels can be made on the assumption of charge pump leakage alone such as the one given below (see appendix), however these models do not consider charge pump mismatch which is a very relevant factor.

$$S1 = 20 \bullet \log\left[\frac{KVCO \bullet leakage}{Fcomp^2 \bullet (C1 + C2) \bullet \sqrt{1 + (2p \bullet Fcomp \bullet R3 \bullet C3)^2}}\right] \quad (1)$$

What can be inferred from this is that leakage related spurs are more of an issue at lower comparison frequencies, higher VCO gains, and higher tuning voltages to the VCO (since leakage is more at these voltages). Below is some empirical data taken from boards that were heated.

Temperature	Spur Level
-40 C	Not visible
+25 C	Not visible
+50 C	-46 dbc/Hz
+85 C	-33 dbc/Hz

Table 1 *Board with 10 KHz reference frequency*

Output Frequency MHz	Temperature Celsius	Spur Level dbc/Hz
985	25	-51.12
	65	- 51.39
995	25	- 65.24
	65	- 61.92
1005	25	- 66.21
	65	-60.94

Table 2 *Spur Level with 25 KHz comparison frequency*

From these results, it should be clear that the reference spurs increase with higher temperatures, but for Table 2 shows that heating the board with Fout = 985 MHz had negligible

effect, while heating the board with Fout = 1005 MHz made a difference of 6 db. This may seem perplexing at first, but that is because for this case, charge pump mismatch is also an issue. Note that at 985 MHz, the VCO is at its lower rail, and the charge pump mismatch dominates, this is why the spur level is so much worse here than at 1005 MHz. At 985 MHz, the charge pump mismatch is dominating, thus increasing the leakage has a negligible effect, however, at 1005 MHz, mismatch is much less of an issue and therefore heating the board has a much more noticeable effect. This shows that it is inadequate to model the reference spurs based only on leakage at these frequencies.

Mismatch Related Spurs

As seen from table 2, modeling reference spurs based on leakage currents alone is usually not adequate. Another relevant cause of reference spurs is the charge pump mismatch. This is nonzero when the current that the charge pump sinks, I_{sink} is not equal to the source current , I_{source} . It is defined as:

$$mismatch(\%) = 200\% \frac{(I_{source} - I_{\sin k})}{I_{source} + I_{\sin k}} \tag{2}$$

Variation of Mismatch Over Tuning Voltage

Referring to figure 1, the net charge delivered when the charge pump is sourcing current will be equal to the net charge delivered when the charge pump is sinking current. In other words, $I_{sink}\, t_{sink} = I_{source}\, t_{source}$. The current is sourced by a PMOS device and sunk by a NMOS device. The currents that are sourced and sunk are not constant. The sourced current decreases as the tuning voltage is increased while the current sunk by the NMOS device sinks more current. The net effect of this is that the mismatch varies as a function of the tuning voltage and increases with increasing tuning voltage. Furthermore note that not every part will be exactly the same, but rather the mismatch properties can change from part to part and date code to date code. National currently guarantees mismatch within - 10% and + 10% when the tuning voltage is at Vp/2 for most of it's PLLs.

Effects of Unequal Turn On Times on Reference Spurs

Another relevant understanding about mismatch is that optimal performance does not occur at 0% mismatch. This is because the turn on time for the PMOS (source) device is slower than that for the turn on time for the NMOS (sink) device. Recall that the PMOS technology is theoretically half the speed of the NMOS technology. Since the PMOS (source) transistor has the slower turn on time, it is desirable to have this transistor source a little bit more than the NMOS transistor sinks. If one also considers that leakage currents are always sinking current, this is another reason for it to be desirable for the mismatch to be slightly positive. From empirical measurements, it follows that the optimal number for mismatch is around + 4 %. In other words, having - 2 % mismatch would be just as bad as having + 10 % mismatch, with all other factors held constant. Note that these numbers for optimal mismatch can be very part specific. Since the mismatch can vary as a function of the tuning voltage to the VCO, there will be a certain tuning voltage V_{opt} that will yield optimal spur performance. Below is some data taken at 200 KHz reference frequency.

Vtune (Volts)	1	1.5	2.2	3	4	4.5
Source (mA)	5.542	5.624	5.711	5.793	5.901	5.986
Sink (mA)	6.062	5.998	5.903	5.772	5.526	5.118
mismatch (%)	- 9.0	- 6.4	- 3.3	0.4	6.6	15.6
200 KHz Spur (dbc/Hz)	- 66.4	-68.7	-72.1	-79.6	-79.8	-66.9

Table 3 *200 KHz Mismatch Dominated Reference Spurs*

From table 3 it can be seen that the spur level for this particular design can be predicted reasonably well via the relationship:

$$\textit{spur level (dbc/Hz)} = -83.6 - 1.41 \bullet |\ \%Mismatch - 3.9\%\ | \qquad (3)$$

Note also that this table suggests that V_{opt} is somewhere around 3.7 volts. Compare this to another part measured on the same board under the same conditions.

Vtune (Volts)	1	1.5	2.2	3	4	4.5
Source (mA)	5.099	5.169	5.241	5.308	5.397	5.455
Sink (mA)	5.308	5.253	5.166	5.047	4.828	4.517
mismatch (%)	- 4.0	- 1.6	1.4	5.0	11.1	18.8
200 KHz Spur (dbc/Hz)	- 73.1	- 76.6	- 83.3	- 83.2	- 72.8	- 65.7

Table 4 *Sample variation of spur levels and mismatch with Do voltage*

Note that although the spur levels are different, it seems that the best spur performance is somewhere around 2.6 volts this time as opposed to 3.7 volts in the last example. This data can be reasonably modeled as:

$$\textit{spur level (dbc/Hz)} = -84 + 1.28 \bullet |\ \%mismatch - 3.2\%\ | \qquad (4)$$

Although not exact, this shows a reasonable correlation between mismatch and reference spurs for this application. Note that both sets of data in table 3 and table 4 suggest an optimal spur level of – 84 dbc/Hz.

For mismatch related spur issues, it is important to be aware of the mismatch properties and to base the design around several different parts to get an idea of the full variations. Mismatch properties of parts can vary from date code to date code, so it is important to consider that in the design process. Also, in designs where an OP amp is used in the loop filter, it is best to use all of the range of Vdo and to also center the op amp around Vp/2 or slightly higher.

Prediction of Reference Spur Level

Accurate prediction of reference spurs is a real challenge and beyond the scope of this book. There are some formulas given in the appendix, but they are not very useful in practice. Some insight is gained from the formulas in the appendix, but these formulas are in no way presented as accurate models – but rather as mathematical insights. Also recall that mismatch dominated spurs are VCO tuning voltage dependent.

However, if one looks at the bode plot for the closed loop gain of the PLL system (which at the reference frequency is well approximated by the open loop gain), then this gives insight in how the spur level of one filter may compare to another. Note that it is necessary to multiply the closed loop transfer function by a factor of s, since it is the frequency response, not the phase response that is sought. The magnitude of the bode plot is observed for one loop filter. If another loop filter is designed using the same PLL synthesizer chip and at the same frequency, then the best way to anticipate the difference in the spur levels would be to compare toe bode plots. Of course, if these spurs are layout related or really caused by leakage in the VCO, then this type of analysis will not work. Loop bandwidth is definitely the most important factor, but the added attenuation from R3 and C3 in the loop filter, and the phase margin can also have some influence. Some typical data is shown below. From this data, it can be seen that reference spur prediction is quite a challenge.

Source	Part lmx	Output MHz	Fcomp KHz	ωc KHz	Fcomp/ ωc	Spur dbc/Hz
AN1001	2315	900	200	11	18.2	-74.7
eval inst	2301	135	100	0.4	250.0	-91
eval inst	2301	137.5	100	0.4	250.0	-82.7
eval inst	2301	140	100	0.4	250.0	-80
eval inst	2325	2425	1000	20	50.0	-68.9
eval inst	2320	1780	200	17	11.8	-80
eval inst	2326	1800	200	12	16.7	-68.68
eval inst	2316	900	200	8	25.0	-63.1
eval inst	2306	889	200	10	20.0	-82.3
eval inst	2306	902	200	10	20.0	-84.1
eval inst	2306	915	200	10	20.0	-83.5
eval inst	2332	915	200	20	10.0	-77.4
eval inst	2331	1775	200	10	20.0	-82
eval inst	2335	900	31.25	3	10.4	-77.6
eval inst	2336	1830	200	12	16.7	-74.4
eval inst	2330	2425	200	30	6.7	-75.6
eval inst	2352	900	160	0.6	266.7	-83.9

Table 5 *Reference Spur Level Data for Various PLLs*

Additional Remedies for spur problems

When designing the loop filter, much can be done in eliminating spur problems, such as using the highest current mode, using a VCO with a lower gain and lower leakage, increasing the value of ATTEN (within certain limits), designing a higher order loop filter, and adding a notch filter. The optimal choice for the value of ATTEN and also a design for a higher order (4th) loop filter are other things that can be considered and are discussed elsewhere in this book.

Conclusion

This paper has discussed reference spurs that occur in the PLL system. They can be caused by many things such as charge pump mismatch, charge pump leakage, transistor turn on times, dead zone elimination circuitry, and many other factors. These factors cause an AC component on the tuning line of the VCO, which causes the output of the VCO to be FM modulated. These factors can vary over many conditions such as temperature, tuning voltage, and date code of part. In PLLs with higher leakages, it is possible to make reasonable predictions about spur levels, but in parts with very low leakage, such as those made by National Semiconductor, there could very well be other factors that are very hard to predict. Spurs are a fact of PLL design, and the best defense is good loop filter design.

Appendix: Spectra of Spurious Signals

Introduction

This section investigates the causes of spurs and their spectral density for an arbitrary time-varying signal that is fed to a VCO.

Derivation of Spurious Spectrum

Spurs caused by the PLL when a signal with an AC component is presented to the tuning line of the VCO.

Assume that the tuning voltage to the VCO has the form:

$$V_{tune} = c + f_{ac}(t)$$

Where

V_{tune}	=	tuning voltage to the VCO
c	=	DC component of tuning voltage to the VCO
f_{ac}	=	AC component of tuning voltage to the VCO

The VCO has an output voltage of the form.

$$Vout(t) = A \bullet \cos\left([c_1 + KVCO \bullet c_0 \;] \bullet t + \int_0^t KVCO \bullet f_{ac}(x) \bullet dx \right)$$

$$= A \bullet \cos\left(c_2 \bullet t + \int_0^t KVCO \bullet f_{ac}(x) \bullet dx \right)$$

Where

A, c_0 , c_1, and c_2	=	constants
KVCO	=	VCO gain

The output spectral density of the VCO is given by the Fourier transform of the output voltage:

$$Pout(w) = \int_{-\infty}^{\infty} e^{j \bullet w \bullet t} \bullet A \bullet \cos\left(c_2 \bullet t + \int_0^t KVCO \bullet f_{zc}(x) \bullet dx \right) \bullet dt$$

Consider the special case of FM modulation, which is a good approximation to the voltage at the VCO. That is[4]:

$$f_{ac}(t) = a_m \bullet \cos(w_m \bullet t)$$

$$b = \frac{F_{dev}}{w_m} = \text{modulation index}$$

$$Pout(w) = A \bullet \sum_{-\infty}^{\infty} J_n(b) \bullet \cos(w_c \bullet t + n \bullet w_m \bullet t)$$

So the first few sideband levels are:

***fundamental*:** $J_0(b) \approx 1$

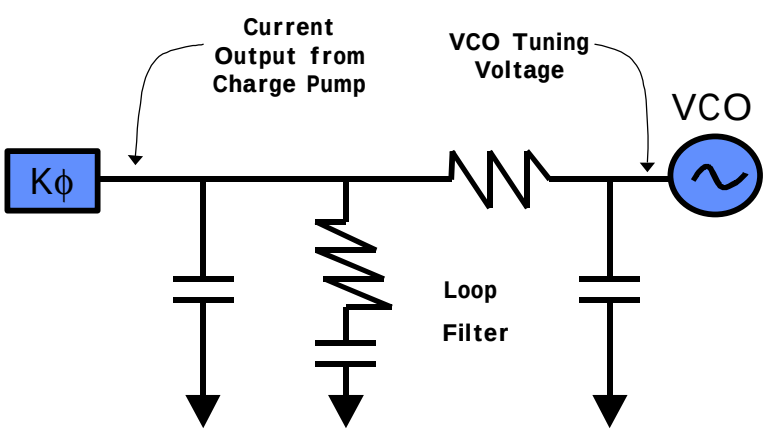
***first*:** $J_1(b) \approx \frac{b}{2}$

second: $J_2(b) \approx \frac{b^2}{8}$

Below is a table of first sideband level versus frequency deviation from 0, for various comparison frequencies:

Spur Level (dbm)	Modulation Index (β)	Frequency Deviation for Various Comparison Frequencies (Hz)					
		Fref 10 KHz	Fref 30 KHz	Fref 50 KHz	Fref 100 KHz	Fref 200 KHz	Fref 1000 KHz
-30	6.32e-2	632	1900	3160	6320	12600	63200
-40	2.00e-2	200	600	1000	2000	4000	20000
-50	6.32e-3	63	190	316	632	1260	6320
-55	3.56e-3	36	107	178	356	712	3560
-60	2.00e-3	20	60	100	200	400	2000
-65	1.12e-3	11	34	56	112	224	1120
-70	6.32e-4	6	19	32	63	126	632
-75	3.56e-4	4	11	18	36	71	356
-80	2.00e-4	2	6	10	20	40	200
-85	1.12e-4	1	3	6	11	22	112
-90	6.32e-5	0.6	2	3	6	13	63

Table 6 *Relationship Between Spur Level, Modulation Index, and Frequency Variation*



Causes of Modulation on the Tuning Line

The rest of this paper will investigate the causes of FM modulation on the tuning line and use the above model to predict the sidebands. The things considered will be:

1. Leakage into the Charge Pump (and other components, like the VCO)
2. Mismatch of the Charge Pump
3. Additional mismatch caused by the fact that the NMOS transistor that sinks current has ½ the turn on time of the PMOS transistor that sources current.

Calculation of Reference Spurs Based on Leakage

Now it will be approximated that the loading effects due to R3 and C3 are small. So the voltage at the junction of C2 and R3 needs to be calculated. On the average, the voltage to the tuning line is correct, but there is an instantaneous error.

For this, the voltage will be computed at the junction of C2 and R3, and then it will be multiplied by the transfer function of R3 and C3. Let V1(t) be this voltage, and i be a constant equal to the leakage into the PLL. It therefore follows that:

$$\frac{d^2V1}{dt^2} \bullet R2 \bullet C1 \bullet C2 + \frac{dV1}{dt} \bullet (C1+C2) = i$$

But actually, the quantity of interest is the derivative of this voltage with respect to time.

$$\frac{dX}{dt} \bullet R2 \bullet C1 \bullet C2 + X \bullet (C1+C2) = i$$

$$X \equiv \frac{dV1}{dt}$$

Imposing the restriction that the voltage is not changing at time t = 0 gives:

$$\frac{dV}{dt} = \frac{i}{C1+C2} \bullet \left[1 - \exp\left(-\frac{C1+C2}{R2 \bullet C1 \bullet C2} \bullet t\right)\right]$$

Since this is based on approximations anyways, it will be assumed that the time period is large compared to the exponential part multiplying it. It is also fair to assume C1 to be within an order of magnitude of C2, which justifies this. This simplifies things to:

$$\frac{dV1}{dt} = \frac{i}{C1+C2}$$

So the maximum frequency deviation can be determined by:

$$V1_{dev} = \int_0^{\frac{1}{Fcomp}} \frac{i}{C1+C2} = \frac{i}{Fcomp \bullet (C1+C2)}$$

Using this as a peak to peak voltage for a model sinusoid, the Voltage V can be determined by:

$$V_{dev} = \frac{i}{Fcomp \bullet (C1+C2) \bullet \sqrt{1+(2p \bullet Fcomp)^2}}$$

So finally the modulation index can be calculated:

$$b = \frac{KVCO \bullet V_{dev}}{Fcomp} = \frac{KVCO \bullet i}{Fcomp^2 \bullet (C1 + C2) \bullet \sqrt{1 + (2p \bullet Fcomp \bullet R3 \bullet C3)^2}}$$

and all of the sidebands can be determined.

Some rough rules of thumb that can be inferred from this are:

1. Doubling the VCO gain results in a 6 db spur increase. However, this is because doubling the VCO gain also increases the loop bandwidth. In actuality, if the loop filter is redesigned, then it turns out that the spurs are independent of VCO gain (theoretically).
2. Doubling the leakage results in a 6 db spur increase
3. Doubling the Comparison Frequency results in a 18 db spur decrease if a spur attenuator , R3 and C3 are used, otherwise it results in a 12 db spur decrease.

Spurs Based on Mismatch, Unequal Transistor Turn on Times, and Dead Zone Elimination Circuitry

The previous model above assumes a perfectly balanced charge pump, when in fact, it is not. The mismatch of the charge pump and the turn on times of the MOS devices also are a relevant factor in spurious calculations.

Charge Sourced Per 2 reference Cycle

$$Q_{source} = t_{source} \bullet Kf_{source} - \frac{1}{2} \bullet s_{source} \bullet Kf_{source}$$

Charge Sunk Per 2 Reference Cycle

$$Q_{\sin k} = t_{\sin k} \bullet Kf_{\sin k} - \frac{1}{2} \bullet s_{\sin k} \bullet Kf_{\sin k}$$

Now these 2 quantities are equal. The real challenge is to calculate the on time of the charge pump. This is highly part specific, and is dependent on the mismatch, dead zone elimination circuitry, and even the on times of the transistors. For the purposes of these calculations, it will be assumed that the on time of the charge pump is known. Typically, these pulses are on the order of 20 nS in the high current mode and 40 nS in the low current mode. In the case of the mismatch related spur, the Voltage deviation can be approximated as:

$$V_{dev} = \frac{t_{on} \bullet i_{cp}}{(C1 + C2) \bullet \sqrt{1 + (2p \bullet Fcomp)^2}}$$

This implies a modulation index of:

$$b = \frac{KVCO \bullet V_{dev}}{Fcomp} = \frac{KVCO \bullet i_{cp} \bullet t_{on}}{Fcomp \bullet (C1 + C2) \bullet \sqrt{1 + (2p \bullet Fcomp \bullet R3 \bullet C3)^2}}$$

Although a lot of assumptions went into this calculation, it implies the following rules of thumb.

1. Spurs increase 6 db for every doubling of the VCO gain. However, this is because doubling the VCO gain also increases the loop bandwidth. In actuality, if the loop filter is redesigned, then it turns out that the spurs are independent of VCO gain (theoretically).
2. Spurs decrease 12 db for every doubling of the comparison frequency, 6 db if R3=C3=0
3. This type of spur is very difficult to predict, since the charge pump on time is unknown and needs to be measured.

4. On Non-Reference Spurs and their Causes

Introduction

Much has been said about reference spurs which occur at the reference frequency away from the carrier. This paper investigates other types of spurs and their causes. The value of doing this is so that when a spur is seen, its causes and fixes can be investigated. Although many types of spurs are listed, most often, these spurs are never seen. These spurs are listed in order to aid in troubleshooting. Since a lot of these spurs occur in dual PLLs, the main PLL will always refer to the side of a dual PLL on which the spur is being observed, and the auxiliary PLL will refer to the side of a dual PLL that is not being observed. This paper discusses general good tips for dealing with spurs, and then goes into categorizing the most common types, their causes, and their cures.

Tips for Good Decoupling and Good Layout

To deal with board-related crosstalk, there are several steps that can be taken. Be sure to visit http://www.national.com/ and download the evaluation board instructions to see typical board layouts. In addition to this, there are the following additional suggestions:

Good Decoupling By this it is meant to have several capacitors on both the VCC and Vpp lines. The Vpp lines are the most vulnerable to noisy signals. Place a 100 pF, 0.01 uF, and a 0.1 uF capacitor on each of these lines to deal with noise at a wide range of frequencies. It may seem that these capacitances simply add in parallel to form a 0.111 uF capacitor, but in fact, they are all necessary since the larger capacitors have more problems responding to high frequency signals. It is also good to place these components as close to the PLL chip as possible. Also it is often good to isolate the power supply pins with a small resistor of about 18 Ω to isolate the power supply pins.

Good Layout Be sure to protect the Vpp lines and the VCO tuning voltage lines from noisy signals. This can be done by making these traces short and as close as possible to the PLL chip. When 2 high frequency traces must be placed together, try to make them so that they are not parallel (i.e. try to make them perpendicular) in order to minimize the crosstalk effects. Also try to minimize ground looping, which occurs when there is a small impedance (such as the inductance caused by a via) which connects two traces to ground. In the instance of ground looping noise can travel from one trace to another.

Tips for Good Loop Filter Design

Other papers in this book discuss the optimal value for attenuation to use and a fourth order loop filter. In addition to these ideas, notch filters can be used. Notch filters tend to be very effective in eliminating an unwanted spur, but not very effective at eliminating higher harmonics of the spur.

Crosstalk vs. Non-Crosstalk Related Spurs

For the purposes of this discussion, the spurs will be divided into two categories. Crosstalk related spurs refer to any spur that is caused by some other signal somehow finding its way to the VCO output. Non-Crosstalk related spurs refer to spurs that are caused by some inherent behavior in the PLL. Perhaps one of the first diagnostic things to do when dealing with

a spur of unknown origin is to determine whether or not it is Crosstalk related. This can be done by eliminating other signal sources and checking if the spur goes away. Some common sources of crosstalk related spurs are: the other side of a dual PLL, computer monitors, other frequencies on the board, and the crystal oscillator and its harmonics.

Crosstalk Related Spurs

The crosstalk related spur is caused by some extraneous signal. In general, crosstalk of two signals is most severe when the signals are close together. For this reason, the harmonics of these spurious sources are sometimes more of a problem than the fundamental. These spurs are categorized below:

Auxiliary PLL Crosstalk Spur

Description

This spur only occurs in dual PLLs and is seen at a frequency spacing from the carrier equal to the difference of the frequencies of the main and auxiliary PLL (or sometimes a higher harmonic of the auxiliary PLL). This spur is most likely to occur if the main and auxiliary sides of a dual PLL are close in frequency. It can also happen if one of the PLLs is close to a higher harmonic of the other PLL.

Cause

Parasitic capacitances on the board can allow high frequency signals to travel from one trace on the board to another. This happens most for higher frequencies and longer traces. There could also be crosstalk within the chip. The Vpp1 and Vpp2 lines are vulnerable to high frequency noise.

Diagnosis

One of the best ways to diagnose this spur is to try to tune the auxiliary side of the PLL while observing the main side. If the spur moves around, that is a good indication that the spur being observed is of this type. Once this type of spur is diagnosed, then it needs to be determined if the spur is related to crosstalk on the board, or crosstalk in the PLL. Most of National's PLLs have a powerdown function that allow one to power down the auxiliary side of a PLL, while keeping the main side running. If the auxiliary side of the PLL is powered down, and the spur reduces in size substantially, this indicates crosstalk in the PLL chip. If the spur stays about the same magnitude, then this indicates that there is crosstalk in the board.

Cure

Read the section on how to deal with board related crosstalk.

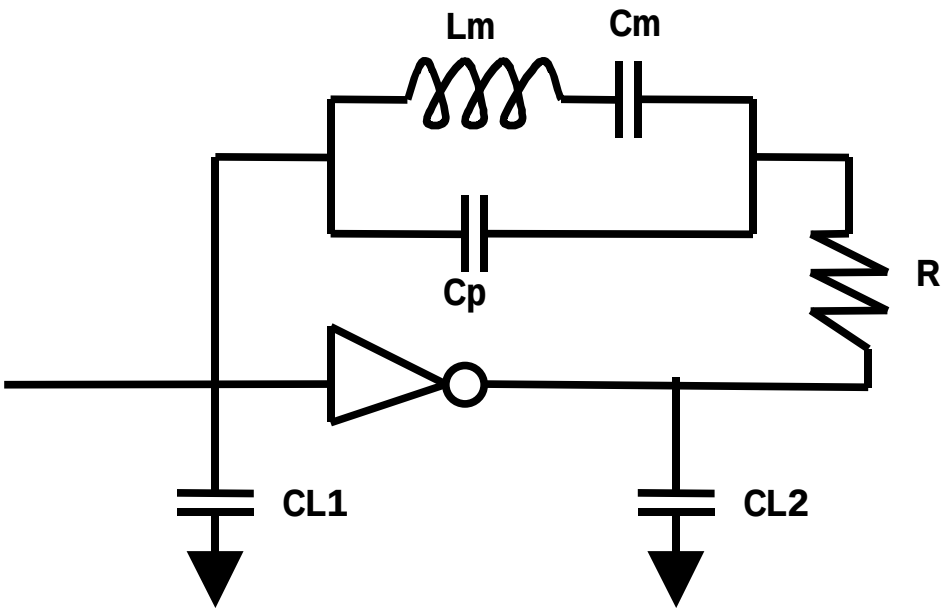
Crystal Reference Crosstalk Spur

Description

This spur is visible at a distance from the carrier equal to the crystal reference frequency. Often times, there is a whole family of spurs that often occur at harmonics of the crystal reference frequency. In this case, the odd harmonics are often stronger than the even harmonics.

Cause

One possible cause of this spur is crosstalk on the board. If this is the case, be sure to read the section on tips on how to deal with board related crosstalk. In addition to this, it may have something to do with excessive gain in the crystal inverter structure. Note that a square wave has only odd harmonics, which is why the odd harmonics tend to be stronger. When the inverting buffer in the crystal oscillator circuit has excessive gain, then it can cause these higher harmonics to occur. Below is a general circuit for a crystal oscillator.



Diagnosis

Try driving the chip with a signal generator, if this reduces these spurs, then this could be indicative that the oscillating buffer has excessive gain. Note that on some of National's PLLs, the inverting buffer is included on the PLL chip, while on others, it is not. If the power level to the chip is reduced, then this decreases the gain of the buffer, which theoretically should decrease the level of this type of spur.

Cure

In addition to the suggestions about good decoupling and layout, there are several things that can be attempted to help these spur levels. However, none of these is guaranteed to work.

1. *Decrease the gain of the inverting buffer.*
   This may sound sort of ridiculous at first, but if the part is run at a lower VCC power supply voltage, then the gain of the inverter is decreased. Also, some of National's PLLs, such as the LMX160x family have only a single inverter stage as opposed to a triple inverter stage.
2. *Supply an external inverter*
   Using a separate inverter for the crystal, or using the inverter from some other component, such as the microprocessor could also be a fix.

3. *Increase the value of R*
   In the above diagram, increasing the value of R can account a little bit for the excessive inverter gain. If R is increased too much, the circuit simply will not oscillate. Note that in many inverter circuits R = 0.
4. *Try unequal load capacitors*
   Usually, the load capacitors, CL1, and CL2 are chosen to be equal, but in this case it might improve the spur level to make CL2 > CL1. This is because the output of the inverter is a square wave, so anything to round out the edges can help.
5. *Layout and filtering*
   Be sure to read the layout tips and also consider filtering the noisy signal on the board.

External Crosstalk Spur

Description

This spur appears and is unrelated to the auxiliary PLL output. Often times, when the main PLL is tuned to different frequencies, this spur moves around.

Cause

This type of spur is caused by some frequency source external to the PLL. This could be things such as the 31.25 KHz refresh rate on some computer monitors or a high frequency output elsewhere on the board. This spur is caused by parasitic capacitances on the board, and long traces on the board, that can act as an antenna for noise.

Diagnosis

The first step in diagnosing this spur is to be sure it is not caused by the Auxiliary side of the PLL. Try powering down the Auxiliary PLL and VCO. If the spur goes away, then it was most likely caused by some sort of crosstalk with the auxiliary side of the PLL. If the spur persists, then it may be caused by some other high frequency signal. In this case, the best way to diagnose these is to disconnect frequency sources and see if the spur goes away.

Cure

To eliminate this spur, remove or isolate the PLL from the signal source. As usual, these spurs are layout dependent, so be sure to read the section on good layout. Also consider using RF fences.

Non-Crosstalk Related Spurs

These spurs are caused by something other than crosstalk on the board. Some common examples are discussed below:

Fractional N Spurs

Description

These spurs only occur in the fractional N PLL. They occur at multiples of the fractional modulus M. The 1/M th and (M-1)/M th fractional spurs tend to be the most severe. They are very dependent of the fractional modulus used. For instance, if there was a fractional N PLL with N = 915.2, and a comparison frequency of 1 MHz, there could potentially be spurs at 200 KHz ($1/5^{th}$ fractional spur), 400 KHz ($2/5^{th}$ fractional spur), 600 KHz ($3/5^{th}$ fractional spur), 800 KHz ($4/5^{th}$ fractional spur), and 1 MHz (main spur) from the carrier.

Cause
In any fractional N PLL, fractional N averaging is employed. Fractional N averaging involves switching the N counter value between 2 different values. This gives rise to fractional spurs due to an instantaneous phase error introduced by the fractional N averaging. For this reason, compensation circuitry is included on the chip to account for this instantaneous phase error. Since this circuitry is not perfect, there will usually be fractional N spurs on any sort of fractional PLL.

Diagnosis
These spurs occur at the fractional modulus times the comparison frequency from the carrier and are very dependent on the fractional modulus and this spur is typically easy to identify.

Cure
Fractional N parts have a lot of part-specific spur causes. In the Philips 7025/8025 fractional N PLL, these spurs are due to imperfections in the compensation circuitry. They can be dependent on supply voltage, output frequency, and a lot of other features. Given a certain part under certain conditions, the only thing that can be done about this is in the loop filter. However, these spurs can be dependent on things that may not be suspected, such as power supply voltage. If there is flexibility in playing with the power supply voltage, then this provides one degree of freedom. The other way to deal with these fractional spurs is to use a different fractional N part, since they are specific to each family of fractional N parts.

Greatest Common Multiple Spur

Description
This spur occurs in a dual PLL at the greatest common multiple of the two comparison frequencies. For example, if one side was running with a 25 KHz comparison frequency, and the other side was running with a 30 KHz comparison frequency, then this spur would appear at 5 KHz. In some cases, this spur can be larger on certain output frequencies.

Cause
The reason that this spur occurs is that the greatest common multiple of the two comparison frequencies corresponds to the event that both charge pumps come on at the same time. This result can be derived by considering the periods of the two comparison frequencies. When both charge pumps come on, they produce noise, especially at the Vpp lines, which gives birth to this spur.

Diagnosis
A couple telltale signs of this type of spur is it is always spaced the same distance from the carrier, regardless of output frequency. However, keeping the output frequency the same, but changing the comparison frequency causes this spur to move around. Just be sure that when changing the comparison frequencies for diagnostic purposes, you are also changing the greatest common multiple of the two comparison frequencies.

Cure

This spur can be treated effectively by putting more capacitors on the Vcc and Vpp lines. Be sure that there is good layout and decoupling around these pins. Also consider changing the comparison frequency of the auxiliary PLL.

Phantom Reference Spur

Description

The phantom reference spur is characterized by a ghastly increase in the reference spurs right after switching frequencies. After the frequency is changed, it takes an excessively long time for the reference spurs to settle down. They are more common at lower comparison frequencies.

Cause

Some of this can be possibly explained by deceptive measurements from the equipment, such as using the video averaging function on a spectrum analyzer. It can also be caused by leaky capacitors in the loop filter. Other theories suggests that it is related to the capacitors developing some sort of polarization. The reason that these spurs are more common at lower comparison frequencies is that at lower comparison frequencies, leakage effects have a stronger affect on reference spurs.

Diagnosis

This can be observed on a spectrum analyzer. Just be very careful that it is not some sort of averaging effect of the spectrum analyzer. The output of the spectrum analyzer is power vs. frequency, which is really intended to be a still time sort of measurement. It may be helpful to test the equipment measuring some other spur to make sure that this is really the PLL and not the equipment.

Cure

Designing with less leaky capacitors helps a lot. Common capacitor types listed in order of decreasing leakage currents are: tantalum, X7R, NP0, and polypropeline. Also, using a fractional N PLL can possibly help, since the fractional spurs tend to be less leakage dominated.

Prescaler Miscounting Spur

Description

This spur typically occurs at half the comparison frequency. However, it can also occur at one-third, two-thirds, or some fractional multiple of the comparison frequency. It can have mysterious attributes, such only occurring on odd channels.

Cause

This spur is caused by the prescaler miscounting. Things that cause the prescaler to miscount include poor matching to the high frequency input, violation of sensitivity specifications for the PLL, and VCO harmonics. Be very aware that although it may seem that the sensitivity requirement for the PLL is being met, poor matching can still cause sensitivity to be a problem. Note also that there is an upper sensitivity limitation on the part.

To understand what the prescaler miscounting has to do with spurs, consider fractional N averaging. Since the prescaler is skipping counts on some occasions and not skipping counts on another, it produces spurs similar to fractional spurs.

Diagnosis

Since miscounting ties in one way or another to sensitivity, try varying the voltage level to the PLL. The sensitivity is very voltage dependent, and dependency of these spurs on the PLL supply voltage point to prescaler miscounting as the cause of the spur. It is also possible to change tinker with the temperature. Changing the N counter value can also sometimes have an impact on this type of spur caused by the N counter miscounting.

Also be aware that it is also theoretically possible for the R counter to have sensitivity problems as well. One way diagnose R counter miscounting is to change the R counter value just slightly. If the spur seems sensitive to this, then this may be the problem. If a signal generator is connected to the reference input, and the spur mysteriously disappears, then this suggests that the R counter miscounting may be causing the spur.

Cure

To cure this problem, it is necessary to fix whatever problem is causing the prescaler to miscount. The first thing to check is that the power level is within the specifications of the part. After that, consider the input impedance of the PLL. For National's PLLs, this tends to be capacitive. Putting an inductor to match the imaginary part of the PLL input impedance at the operating frequency can usually fix impedance matching issues. Be also aware of the sensitivity and matching to the VCO harmonics, since they can also cause a miscount. Try to keep the VCO harmonics –20 dbm or lower in order to reduce the chance of the PLL miscounting the VCO harmonic.

Reference Spurs and their Harmonics

Description

These spurs occur at the reference (comparison) frequency from the carrier, and harmonics thereof.

Cause

These are mainly caused by mismatches and leakages in the charge pump. At lower comparison frequencies, the charge pump leakage tends to be the dominant cause of these. At higher comparison frequencies, the charge pump mismatch tends to be the dominant cause of these. Be aware that leaky VCOs and capacitors can also cause these spurs. These mismatches and leakages put an AC component on the VCO tuning line, which can be analyzed as FM modulation on the VCO output. FM modulation gives rise to spurious sidebands. This type of spur is discussed in depth in other sections of this book.

Diagnosis

These spurs are very common and appear at the comparison frequency away from the carrier. Be aware that mismatch of the charge pump can change vs. tuning voltage.

Cure

These spurs are best dealt with through good loop filter design.

VCO Harmonic Spurs

Description

This spur occurs at multiples of the output frequency. All VCOs put out harmonics of some kind. This spur can cause problems if there is very poor matching to the high frequency input of the PLL. Note also in some cases, the higher harmonic has better matching and sensitivity performance than the fundamental. This can cause mysterious noisy behavior. In general, it is good to have the second harmonic 20 db down if possible, but that is very dependent on the matching and the sensitivity of the PLL.

Cause

VCOs are part specific in what kind of harmonics they produce, but they tend to be the cause of the spurs.

Diagnosis

These spurs appear at the VCO frequency and multiples thereof. Change the VCO frequency, and see if the spurs still appear at multiples of the VCO output.

Cure

If the VCO harmonics cause a problem there are several things that can be done to reduce their impact. They can be lowpass filtered with LC or RC filters. A resistor or inductor can be placed in series at the fin pin to prevent them from causing the prescaler to miscount. Just make sure that there is good matching and that the spur level at the fin pin is as low as possible. Note also that the National PLLs do not have a 50 Ω input impedance. Treating it as such often creates big problems with the VCO harmonics.

Conclusion

In this paper some, but not all causes of spurs have been investigated. Although very difficult to predict the levels of reference spurs, their diagnosis and what is really important anyways. Spurs tend to be a thing that requires a lot of hands on type of diagnostics and process of elimination is sometimes the only way to figure out what is the real cause.

5. Transient Response of PLL Frequency Synthesizers

Introduction

This paper considers the frequency response of a PLL when the N divider is changed. In addition to giving a fourth order model of this event, whose only approximation is the continuous time approximation for the phase detector, it also gives derivations for natural frequency and damping factor which are used in a second order approximation. It further relates them to loop bandwidth and phase margin. This paper is intended to give a rigorous mathematical foundation for the transient response of PLL synthesizers and in doing so provide a universal model which can be used in place of all of the various rules of thumb, since rules of thumb only work under certain conditions or for certain applications.

PLL Basic Structure

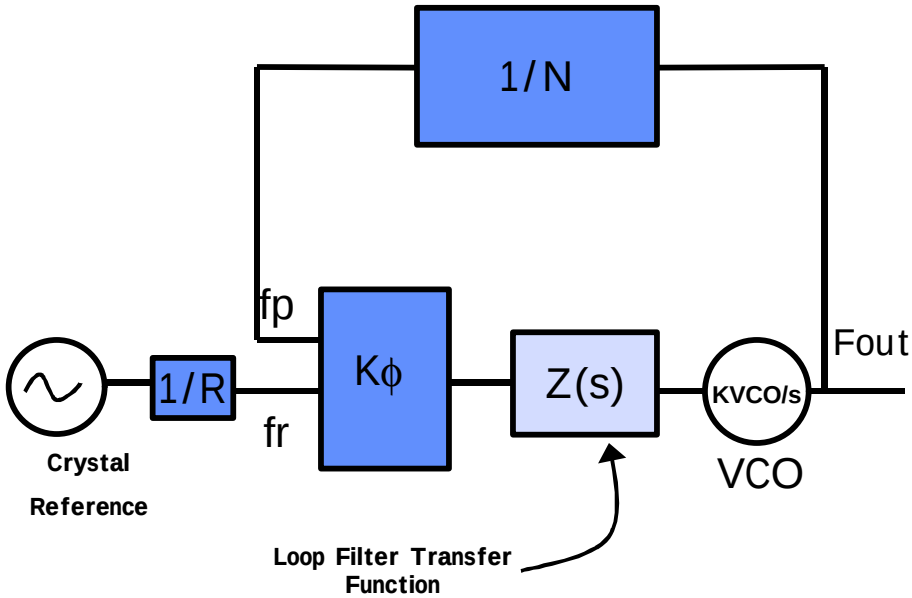


Figure 1 *Basic PLL Structure*

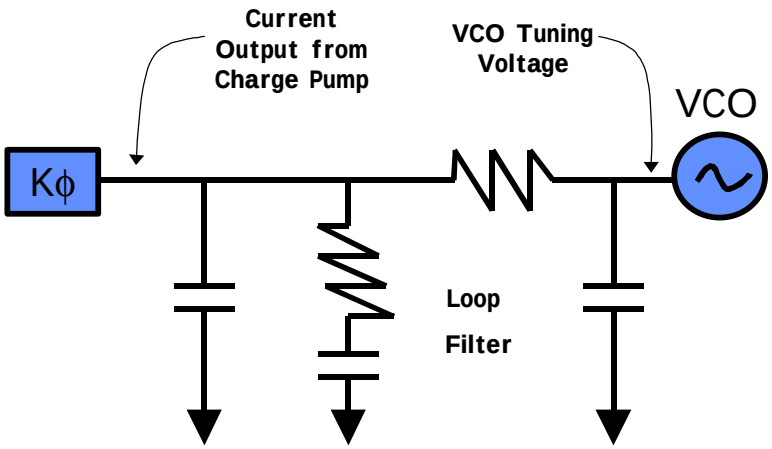


Figure 2 *Assumed Passive Third Order Loop Filter Topology*

Continuous Time Approximation

In order to derive the transfer functions, it is necessary to introduce one approximation. It is the continuous time approximation, which approximates discrete current pulses from the phase detector as a continuous signal that has the same average value as the discrete pulses. This approximation becomes more rough as the comparison frequency approaches the loop bandwidth of the system[4]. So, since the PLL charge pump puts out current pulses of magnitude Kϕ mA, the time averaged output of the charge pump would be Kϕ/2π mA/radian. Since the charge pump output Kϕ/2π multiplies the output of the VCO, KVCO●2π in all of the equations involved in this paper, the these factors of 2π cam be disregarded and pump output has been labeled as Kϕ and the VCO output has been labeled as Kvco in Figure 1.

Derivation of Transfer Function

Define the following constants:

$$\begin{aligned} k0 &= R2 \bullet C2 \\ k1 &= R2 \bullet R3 \bullet C1 \bullet C2 \bullet C3 \\ k2 &= C2 \bullet C3 \bullet R2 + C1 \bullet C2 \bullet R2 + C1 \bullet C3 \bullet R3 + C2 \bullet C3 \bullet R3 \\ k3 &= C1 + C2 + C3 \end{aligned} \tag{1}$$

Then the transfer function of the loop filter is given by:

$$Z(s) = \frac{1 + s \bullet k0}{s \bullet \left[s^2 \bullet k1 + s \bullet k2 + k3 \right]} \tag{2}$$

This leads to the following closed-loop transfer function:

$$\boldsymbol{CL(s) = \frac{Kf \bullet Kvco \bullet N \bullet (1 + s \bullet k0)}{s^4 \bullet N \bullet k1 + s^3 \bullet k2 \bullet N + s^2 \bullet k3 \bullet N + s \bullet Kf \bullet Kvco \bullet k0 + Kf \bullet Kvco}} \tag{3}$$

Second Order Approximation to Transient Response

To this point, no approximations have been made. In this section, CL(s) will be approximated by a second order expression, CL1(s), in order to derive results that give an intuitive feel of the transient response.

It is assumed that these higher order terms are small relative to the lower order terms. The initial value theorem (4) shows the initial value theorem which suggests that the consequences of ignoring these terms are more on the initial characteristics, such as overshoot, and less on long time behavior, such as lock time.

$$\boldsymbol{\lim_{s \to \infty} s \bullet Y(s) = \lim_{t \to 0} y(t)} \tag{4}$$

The simplified second order expression is:

$$\boldsymbol{CL1(s) = \frac{\left(\frac{Kf \bullet Kvco}{n \bullet k3}\right) \bullet \left(1 + s \bullet k0 \bullet N\right)}{s^2 + s \bullet \left(\frac{Kf \bullet Kvco \bullet k0}{k3 \bullet N}\right)}} \tag{5}$$

Defining

$$z = \frac{R2 \bullet C2}{2} \bullet \sqrt{\frac{Kf \bullet Kvco}{N \bullet (C1 + C2 + C3)}} \tag{6}$$

$$wn = \sqrt{\frac{Kf \bullet Kvco}{N \bullet (C1 + C2 + C3)}} \tag{7}$$

it can be seen that the poles of this function are at:

$$-z \bullet wn \pm jwn \bullet \sqrt{1 - z^2} \tag{8}$$

Now consider a PLL which is initially locked at frequency f1, and then the N counter is changed such to cause the PLL to switch to frequency f2. It should be noted that the value for N that is used in all of these equations should be the value of N corresponding to f2. This event is equivalent to changing the reference frequency from f1/N to f2/N. The first term in the numerator of (5) shows the primary effects, and the second expression shows the secondary effects due to the zero. The zero in the transfer function has a lot of effect on the overshoot and the rise time, but has little effect on the lock time. Using inverse Laplace transforms it follows that the time frequency response is:

$$F(t) = f2 + (f1 - f2) \bullet e^{-z \bullet wn \bullet t} \bullet \left[\cos(wn \bullet \sqrt{1-z} \bullet t) + \frac{z - R2 \bullet C2 \bullet wn}{\sqrt{1-z^2}} \bullet \sin(wn \bullet \sqrt{1-z^2} \bullet t)\right] \tag{9}$$

Since the term in brackets has a maximum value of:

$$\frac{1 - 2 \bullet R2 \bullet C2 \bullet z \bullet wn + R2^2 \bullet C2^2 \bullet wn^2}{\sqrt{1-z^2}} \tag{10}$$

It follows that the lock time is given by:

$$LockTime(s) = \frac{-\ln\left(\frac{tol}{f2 - f1} \bullet \frac{\sqrt{1-z^2}}{1 - 2 \bullet R2 \bullet C2 \bullet z \bullet wn + R2^2 \bullet C2^2 \bullet wn^2}\right)}{z \bullet wn} \tag{11}$$

Many times, this is approximated by:

$$LockTime(s) = \frac{-\ln\left(\frac{tol}{f2 - f1} \bullet \sqrt{1-z^2}\right)}{z \bullet wn} \tag{12}$$

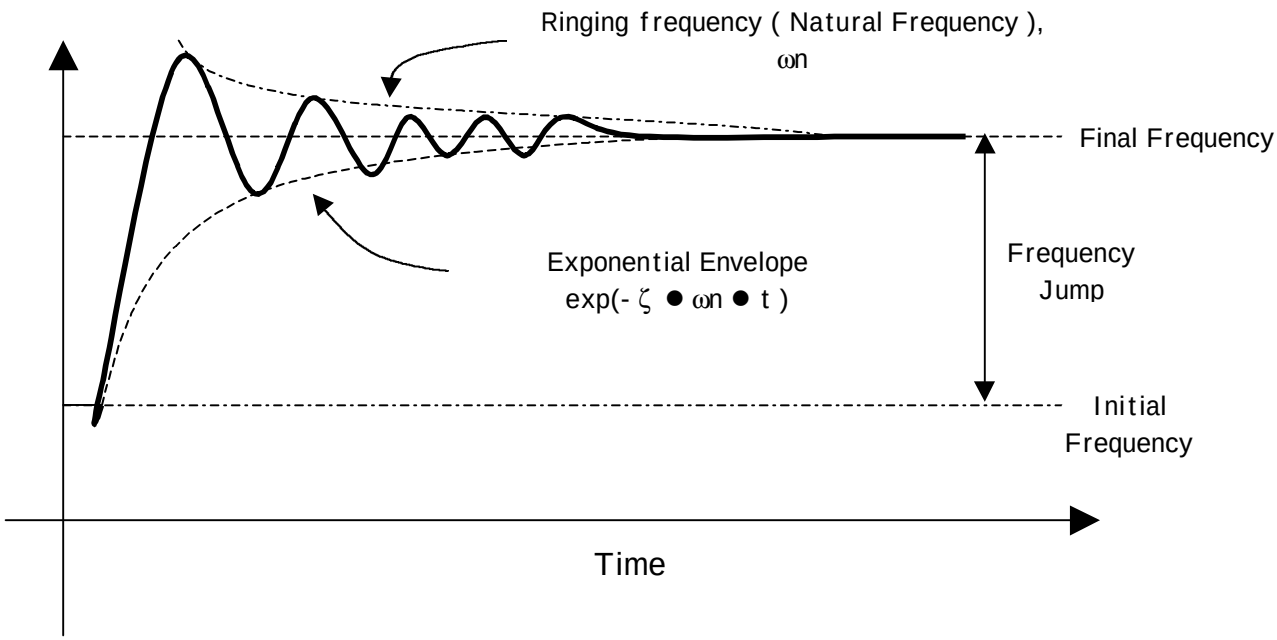


Figure 3 *Classical Model for the Transient Response of a PLL*

Figure 3 shows the classical second order model for the frequency response. For a second order filter, that is a filter with R3=C3=0, the following relationships exist for loop filters designed with AN-1001. These formulas are proven in the Appendix.

$$wp = 2 \bullet z \bullet wn$$

$$\sec fp - \tan fp = \frac{1}{4 \bullet z^2} \tag{13}$$

Note here that ωp is defined as the point where the magnitude of the open loop transfer function is equal to 1.

$$\left|\frac{Kf \bullet Kvco \bullet Z(s)}{N \bullet s}\right| = 1 \tag{14}$$

The reader should be careful not to confuse the loop bandwidth with the noise bandwidth. The relationships between the noise bandwidth.[1]

$$B_L = \int_0^{\infty} \left|H(2p \bullet f)\right|^2 df \tag{15}$$

It can be shown that:

$$B_L = \frac{wn}{2} \bullet \left(z + \frac{1}{4z}\right) \tag{16}$$

The reader should be even more careful as to confuse the loop bandwidth with the 3db noise bandwidth, which is given below[1] :

$$B_{3db} = \frac{wn}{2} \bullet \sqrt{1 + 2 \bullet z^2 + \sqrt{2 + 4 \bullet z^2 + 4 \bullet z^4}} \tag{17}$$

So by specifying a the loop bandwidth, ωp, and the phase margin, ϕp, the damping factor and natural frequency can be determined, and vise versa. The formulas (15) – (17) show other formulas that are commonly used[3], but these use a different definition of loop bandwidth and also assume a different loop filter topology.

Fourth Order Transient Analysis

This analysis considers all the poles and zeros of the transfer function and gives the most accurate results. It does require finding the roots of a fourth order polynomial. An explicit formula does exist for this and is given in [6]. There also exist software, such as Mathcad, which is ideal for dealing with a problem such as this. The aim of this section is to derive an expression for the transient analysis that can be graphed and properties such as the lock time, rise time, overshoot, ringing, and damping factor can be seen from the graph. To start with, the transfer function in (3) is multiplied by (f2-f1)/(Ns). However, since these formulas are really referring to the phase response, and it is the frequency response that is sought, the whole transfer function is also multiplied by s to perform differentiation (frequency is the derivative of phase). The resulting expression is rewritten in the following form

$$\overline{F(s)} = s \bullet H(s) \bullet \frac{f2 - f1}{N \bullet s} = \frac{n1 \bullet (1 + s \bullet k0)}{s^4 + d3 \bullet s^3 + d2 \bullet s^2 + d1 \bullet s + d0} \tag{18}$$

where

$$n1 = \frac{Kf \bullet Kvco \bullet (f2 - f1)}{N \bullet C1 \bullet C2 \bullet C3 \bullet R2 \bullet R3} \tag{19}$$

$$d3=\frac{k2}{k1}=\frac{C2\bullet C3\bullet R2+C1\bullet C2\bullet R2+C1\bullet C3\bullet R3+C2\bullet C3\bullet R3}{R2\bullet R3\bullet C1\bullet C2\bullet C3} \tag{20}$$

$$d2=\frac{k3}{k1}=\frac{C1+C2+C3}{R2\bullet R3\bullet C1\bullet C2\bullet C3} \tag{21}$$

$$d1=\frac{Kf\bullet Kvco}{N\bullet C1\bullet C3\bullet R3} \tag{22}$$

$$d0=\frac{Kf\bullet Kvco}{N\bullet R2\bullet R3\bullet C1\bullet C2\bullet C3} \tag{23}$$

Note that the zeroes of the denominator are the poles of the transfer function. Since this is a fourth order polynomial, the zeroes of this function can be found analytically, although it is much easier to find them numerically. At least 2 of these poles will be complex, and they will be close to 2 of the poles of the second order approximation. The transfer function can be rewritten as:

$$H(s)\bullet\frac{f2-f1}{N\bullet s}=\sum_{i=0}^{3}A_i\bullet\left[\frac{1}{s\bullet(s-p_i)}+\frac{R2\bullet C2}{s-p_i}\right] \tag{24}$$

$$\boldsymbol{A_i=n1\bullet\prod_{k\neq i}\frac{1}{p_i-p_k}} \tag{25}$$

Finally, this leads to the transient response. Note that some of the coefficients A_i will be complex, however, they will combine in such a way that the final solution is real. Now since the poles need to be calculated for this, it will be assumed that they all have negative real parts. If this is not the case, then the design is unstable. Using this assumption that the design is stable, the transient response can be simplified. Also, if the simulator does not do this, the solution can be expressed with all real variables by applying Euler's formula:

$$e^{a+j\bullet b}=e^{a}\bullet(\cos b+j\bullet\sin b) \tag{26}$$

Assuming a stable system, the transient response is:

$$\boldsymbol{F(t)=f2+\sum_{i=0}^{3}A_i\bullet e^{p_i\bullet t}\bullet\left(\frac{1}{p_i}+R2\bullet C2\right)} \tag{27}$$

Simulation Results

Below are simulation results for the GSM example used in the databook for Figures 10 and 12 in AN-1001. Although these are a little distorted distorted from the actual graphs, since they do not account for the discrete effects of the phase detector and the nonlinear behavior of the VCO, they still provide a reasonably accurate prediction of lock time.

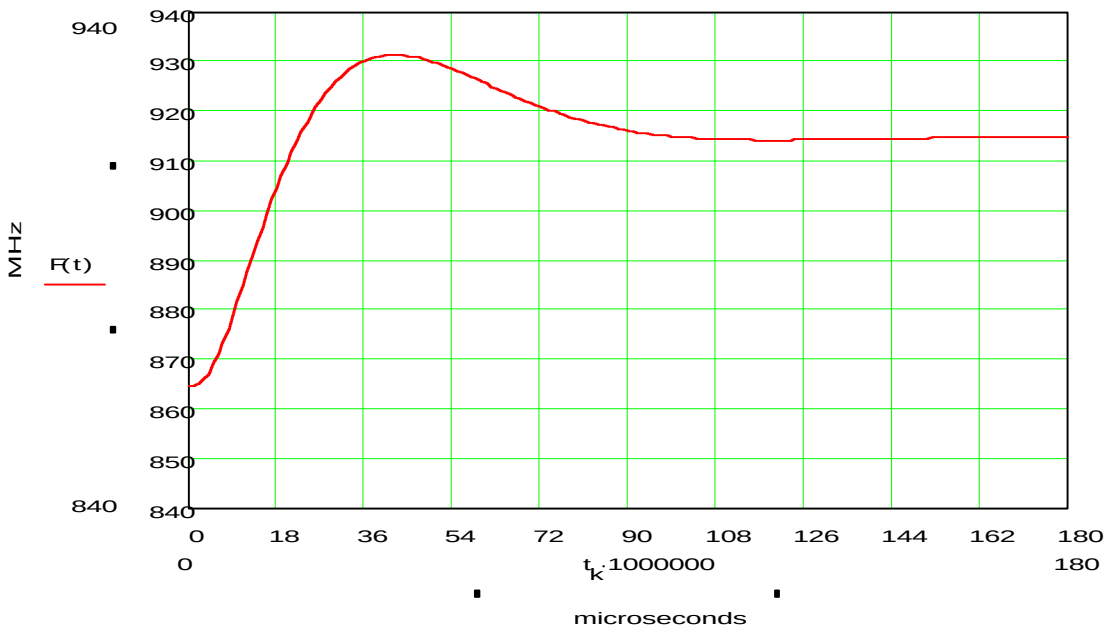


Figure 4 *Wide span view for a 50 MHz Jump to a tolerance of 500 Hz*

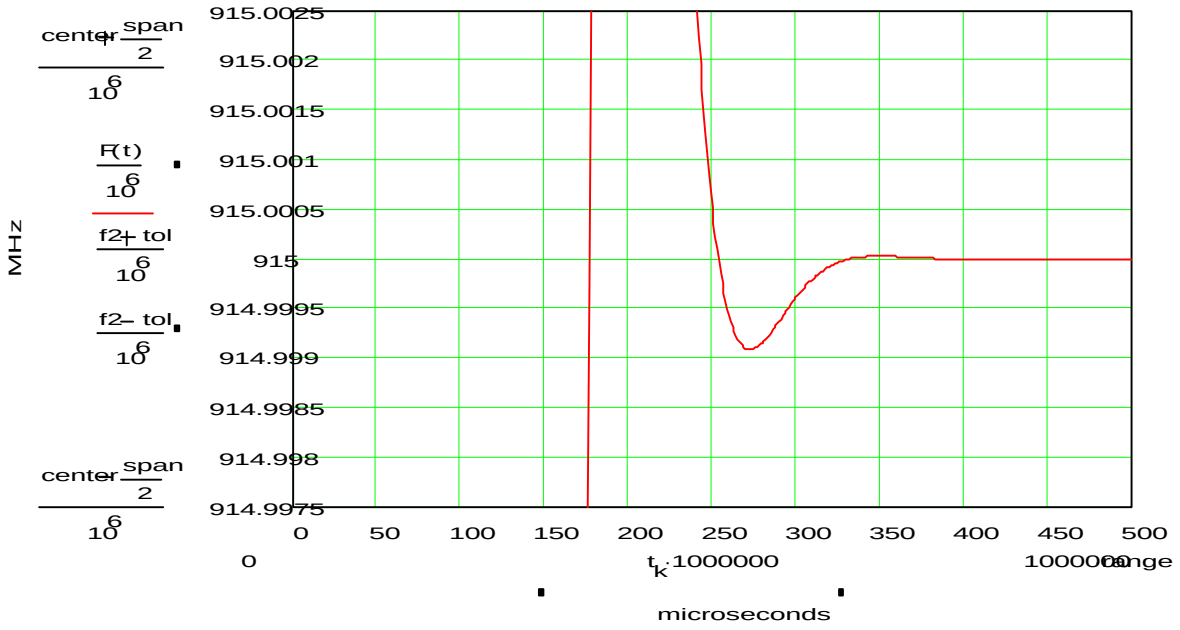


Figure 5 *Transient Response showing a lock time to 500 Hz of about 300 uS*

Conclusion

Accuracy of Mathematical Calculations

This paper has gone through a rigorous derivation of the equations involved in predicting lock time and the transient response of the PLL when the N divider is changed. A second order and a fourth order model were presented. The second order model is good for a rough guess at the lock time and is easier to use. The fourth order analysis uses no mathematical approximations other than the continuous time approximation for the phase detector.

Other Factors that Could Cause Theoretical Lock Time Predictions to be Off

VCO Non-linearity

Perhaps the biggest real world thing that could throw off this analysis is the VCO non-linearity. VCOs tend to have a frequency specification within a certain range. When switching from one frequency to another, there is typically overshoot in the order of one third of the frequency jump. This overshoot is dependent on the phase margin/damping factor. At the higher tuning voltages of the VCO, the VCO gain typically is less. The effect of this is that it rounds off the first lobe of the transient response and increases the lock time. The designer should be aware that if overshoot causes the frequency to go outside the tuning range of the VCO, the modeled prediction could lose accuracy. To deal with this, design for a higher phase margin in order to decrease the overshoot.

Charge pump Non-linearity

The charge pump current output does have some dependence on the VCO tuning voltage, especially around the supply rails.

VCO Input Capacitance

The VCO input capacitance adds in parallel with the capacitor C3. If not accounted for, this could throw change the results. This tends to decrease the loop bandwidth, and therefore increase the lock time.

Phase Detector Discrete Sampling Effects

The discrete sampling effects of the phase detector tend to have little bearing on the lock time, provided that the comparison frequency is large (10 X) compared to the loop bandwidth. The fourth order model was compared to another model that did take into account these effects, and the difference in the lock time was very small. In an actual transient response for a PLL with a digital phase detector, there will be small jagged corrections corresponding to these corrections of the phase detector.

Other Factors

There are also charge pump mismatch, charge pump leakage, board paracitics, and component leakages that could throw these results off.

Final Remarks

Despite that this model has not accounted for everything, it is perfect in the sense that it is exactly the response of the system that is modeled. The only reasons why the fourth order calculations would be different from the actual results is that there are some factors that were not accounted for. Many previous rules of thumb had additional errors, which could be quite large, that were introduced by mathematical approximations.

Appendix

Proof of relation between Natural Frequency (ωn), Damping Factor (ζ), Loop Bandwidth (ωp) , and Phase Margin (ϕp)

Note that this is for a second order filter, so recall that for all expressions involving C3, C3=0

Recall from AN1001[2] for a second order filter

$$T1 = \frac{\sec fp - \tan fp}{wp} \tag{28}$$

$$T2 = R2 \bullet C2 = \frac{1}{wp^2 \bullet T1} \tag{29}$$

Combining (5) , (6) , (28), and (29) in order to eliminate T1 and T2 yields the following:

$$\frac{wn}{z} = 2 \bullet wp \bullet (\sec fp - \tan fp) \tag{30}$$

Recall Also from AN 1001 [2]

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \tag{31}$$

This can be restated as follows,

$$C1 + C2 = \frac{T2}{T1} \bullet C1 \tag{32}$$

By AN 1001[2]

$$C1 = \frac{T1}{T2} \bullet \frac{Kf \bullet Kvco}{N \bullet wp^2} \sqrt{\frac{1 + (wp \bullet T2)^2}{1 + (wp \bullet T1)^2}} \tag{33}$$

Substituting this expressing for C1 in the right hand side of (32), and equating this derived expression for C1+C2 for C1+C2 obtained from equation (6) yields the following:

$$\frac{Kf \bullet Kvco}{N \bullet wp^2} \sqrt{\frac{1 + (wp \bullet T2)^2}{1 + (wp \bullet T1)^2}} = C1 + C2 = \frac{Kf \bullet Kvco}{N \bullet wn^2} \tag{34}$$

Using expressions (28) , (29) , and (30) in order to express T1 and T2 in terms of ζ, ωn, and ωp, yields the following equation:

$$\left(\frac{wp}{wn}\right)^4 = \frac{1+\left(\frac{2 \bullet z \bullet wp}{wn}\right)^2}{1+\left(\frac{wn}{2 \bullet z \bullet wp}\right)^2} \tag{35}$$

This equation can be simplified to an equation that is quadratic in ωp^2 and can be solved using the quadratic formula for the following elegant relationship:

$$wp = 2 \bullet z \bullet wn \tag{36}$$

By substituting this into (30), the other relationship can be obtained

$$\sec fp - \tan fp = \frac{1}{4 \bullet z^2} \tag{37}$$

Note that no approximations were made for a second order filter. For a third order filter, these relationships are not exact, but serve as good approximations.

References

[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[2] Franklin, F. , Powell, D., and Emami-Naeini, A. *Feedback Control of Dynamic Systems*, 3rd ed. , Addison-Wesley, 1994

[3] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

[4] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

[5] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops*

Application Example for "Transient Response of PLL Frequency Synthesizers"

USER NEEDS TO ENTER THESE:

$Kvco := 20 \cdot \frac{MHz}{volt}$ Enter the Tuning Constant Here

$K\phi := 5 \cdot mA$ Enter the Phase Detector gain do not divide by 2*π

$Fout := 900MHz$ RF output frequency. Choose equal to sqrt(Fmax*Fmin)

$Fcomp := 200kHz$ Comparison Frequency

$Fc := 11.2110694 \cdot kHz$ Enter the True Loop Bandwidth in KHz. Do not put Fp.

$\phi p := 45 \cdot deg$ Phase margin. Default is 50 degrees.

$ATTEN := 10$ Reference spurious attenuation in dB added by R3 and C3. This value is 1/2 of what is used in AN1001.

CALCULATIONS

$$N := \frac{Fout}{Fcomp} \qquad \omega c := 2 \cdot \pi \cdot Fc$$

$$T3 := \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{2 \cdot \pi \cdot Fcomp}$$

$$f(\omega p) := \tan(\phi p) \cdot \frac{\frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} + T3}{\left(\frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} + T3\right)^2 + \frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} \cdot T3} \cdot \left[\sqrt{1 + \frac{\left(\frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} + T3\right)^2 + \frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} \cdot T3}{\left[\tan(\phi p) \cdot \left(\frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} + T3\right)\right]^2}} - 1\right]$$

$$x := 2 \cdot \pi \cdot Fc \qquad \omega p := root(f(x) - 2 \cdot \pi \cdot Fc, x) \qquad Fp := \frac{\omega p}{2 \cdot \pi}$$

$$T1 := \frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega p} \qquad T2 := \frac{1}{(\omega c^2 \cdot (T1 + T3))}$$

$$C1 := \frac{T1}{T2} \cdot \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \left[\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)}\right]^{\frac{1}{2}}$$

$$C2 := C1 \cdot \left(\frac{T2}{T1} - 1\right)$$

$$C3 := \frac{C1}{10} \cdot min\left(\begin{bmatrix} ATTEN \\ 1 \end{bmatrix}\right)$$

$$R2 := \frac{T2}{C2}$$

$R3 := \frac{T3}{C3}$

DERIVED QUANTITIES

Parameters

$Fp = 2 \cdot 10^{4} \cdot sec^{-1}$ $N = 4.5 \cdot 10^{3}$

Time Constants

$T1 = 3.296 \cdot 10^{-6} \cdot sec$

$T2 = 3.546 \cdot 10^{-5} \cdot sec$

$T3 = 2.387 \cdot 10^{-6} \cdot sec$

Filter Poles

$\frac{1}{T1 \cdot 2 \cdot \pi} = 4.829 \cdot 10^{4} \cdot kHz$

$\frac{1}{T3 \cdot 2 \cdot \pi} = 6.667 \cdot 10^{4} \cdot kHz$

Filter Zero

$\frac{1}{T2 \cdot 2 \cdot \pi} = 4.488 \cdot 10^{3} \cdot kHz$

CALCULATED VALUES:

$C1 = 1.076 \cdot 10^{3} \cdot pF$ $C2 = 1.05 \cdot 10^{4} \cdot pF$ $C3 = 107.59 \cdot pF$

$R2 = 3.377 \cdot k\Omega$ $R3 = 22.189 \cdot k\Omega$

ACTUAL VALUES

$C1 := 1000 \cdot pF$ $C2 := 10 \cdot nF$ $C3 := 98 \cdot pF$

$R2 := 3.3 \cdot k\Omega$ $R3 := 22 \cdot k\Omega$

DESIGN CHECK

Ensure

C3/C1< 1/10 $\frac{C3}{C1} = 0.098$ R3 / R2 > 2 $\frac{R3}{R2} = 6.667$

SIMULATION

$\zeta := \frac{R2 \cdot C2}{2} \cdot \sqrt{\frac{K\phi \cdot Kvco}{N \cdot (C1 + C2 + C3)}}$ $\omega n := \sqrt{\frac{K\phi \cdot Kvco}{N \cdot (C1 + C2 + C3)}}$

100 points

$j := 20 .. 120$ $f_j := 10^{\frac{j}{20}} \cdot Hz$

Generates 5 decades from 10 Hz to 1 MHz

$S_j := 2 \cdot \pi \cdot f_j \cdot i$

S = iω

$$Z(S) := \frac{1 + (C2 \cdot R2) \cdot S_j}{(C1 + C2 + C3) \cdot (S_j) + (C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3) \cdot (S_j)^2 + C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \cdot (S_j)^3}$$

Forward Loop Gain

$$G(S) := \frac{K\phi \cdot Kvco \cdot Z(S)}{S_j}$$

Reverse Loop Gain

$$H(S) := \frac{1}{N}$$

Open Loop Gain

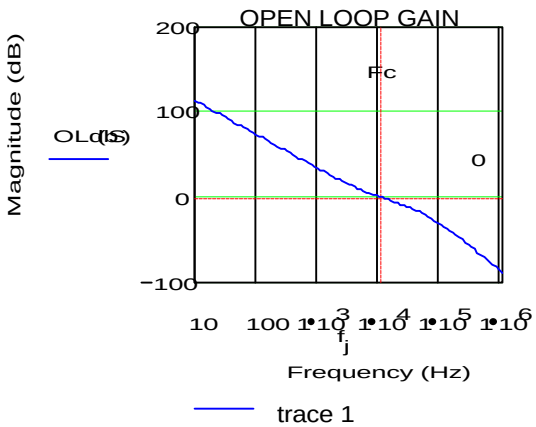
$$OL(S) := H(S) \cdot G(S)$$

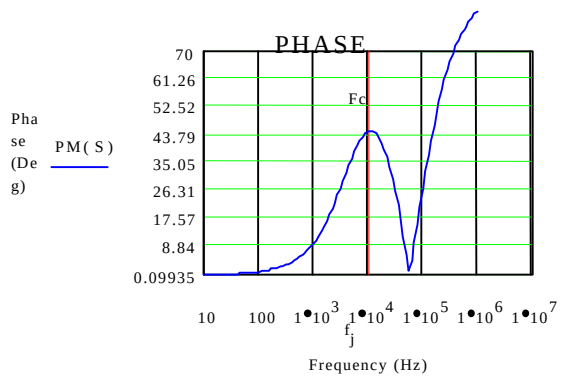
Closed Loop Gain

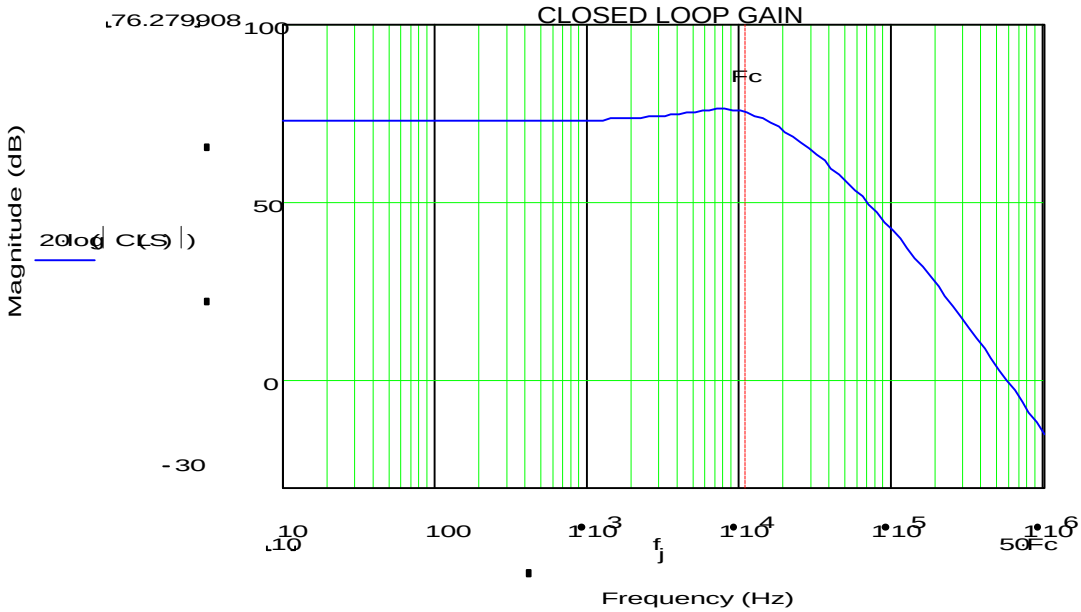
$$CL(S) := \frac{G(S)}{1 + H(S) \cdot G(S)}$$

Calculated Results

ATTEN = 9.212 $Fc = 1.104 \cdot 10^{4} \cdot sec^{-1}$ $\phi p = 45.264$ $\zeta = 0.738$ $\frac{\omega n}{2 \cdot \pi} = 7.122 \cdot 10^{3} \cdot sec^{-1}$







TRANSIENT ANALYSIS

User Enters these

$f2 := 915MHz$ Final Frequency

$f1 := 865MHz$ Starting Frequency

Calculations

$N := \frac{f2}{Fcomp}$ N value for f2

$den4 := R2 \cdot R3 \cdot C1 \cdot C2 \cdot C3$

$den3 := C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3$

$den2 := C1 + C2 + C3$

$den1 := \frac{K\phi \cdot Kvco \cdot C2 \cdot R2}{N}$

$num0 := \frac{K\phi \cdot Kvco \cdot (f2 - f1)}{N}$

$den0 := \frac{K\phi \cdot Kvco}{N}$

$num1 := num0 \cdot R2 \cdot C2$

$$v := \begin{bmatrix} \frac{den0}{den4} \cdot sec^4 \\ \frac{den1}{den4} \cdot sec^3 \\ \frac{den2}{den4} \cdot sec^2 \\ \frac{den3}{den4} \cdot sec \\ 1 \end{bmatrix} \qquad v = \begin{bmatrix} 3.072176 \cdot 10^{20} \\ 1.013818 \cdot 10^{16} \\ 1.559847 \cdot 10^{11} \\ 8.426097 \cdot 10^{5} \\ 1 \end{bmatrix}$$

These are the poles

$$p := polyroots(v) \cdot sec^{-1} \qquad p = \begin{bmatrix} -6.141915 \cdot 10^{5} \\ -1.432499 \cdot 10^{5} \\ -4.258418 \cdot 10^{4} + 4.096810^{4} i \\ -4.258418 \cdot 10^{4} - 4.096810^{4} i \end{bmatrix} \cdot sec^{-1}$$

$$A_o := \frac{\frac{num0}{den4}}{(p_o - p_1) \cdot (p_o - p_2) \cdot (p_o - p_3)} \qquad A_o = -9.932 \cdot 10^{10} \cdot sec^{-2}$$

$$A_1 := \frac{\frac{num0}{den4}}{(p_1 - p_o) \cdot (p_1 - p_2) \cdot (p_1 - p_3)} \qquad A_1 = 2.761 \cdot 10^{12} - 433.706i \cdot sec^{-2}$$

$$A_2 := \frac{\frac{num0}{den4}}{(p_2 - p_0)\cdot(p_2 - p_1)\cdot(p_2 - p_3)} \qquad A_2 = -1.331\cdot10^{12} - 2.7\cdot10^{12}i \cdot sec^{-2}$$

$$A_3 := \frac{\frac{num0}{den4}}{(p_3 - p_0)\cdot(p_3 - p_1)\cdot(p_3 - p_2)} \qquad A_3 = -1.331\cdot10^{12} + 2.7\cdot10^{12}i \cdot sec^{-2}$$

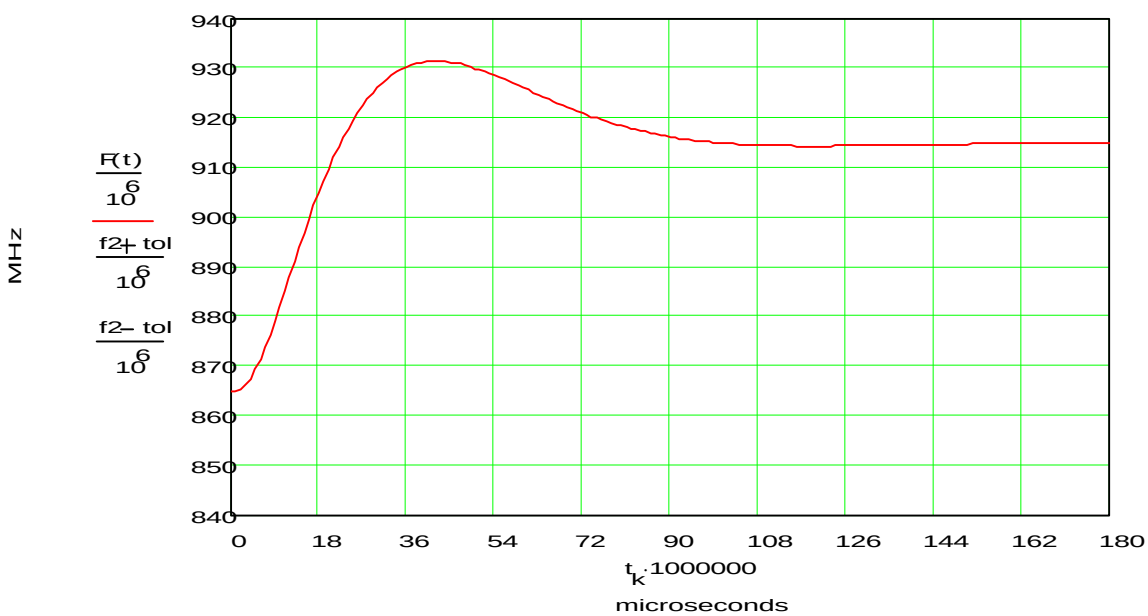
4 Pole Analysis

$k := 0..4500 \qquad t_k := \frac{k}{1000000}\cdot sec \qquad i := 0..3$

$$F(t) := f2 + \sum_i A_i \cdot e^{p_i \cdot t_k} \cdot \left(\frac{1}{p_i} + \frac{num1}{num0}\right)$$

Enter these to adjust the setting

$range := 180\cdot10^{(-6)}\cdot sec$	Maximum Range of the X axis
$tol := 0\cdot Hz$	Tolerance Marker for Lock Time Measurements
$span := 100MHz$	Vertical Span of the Plot
$center := 890MHz$	Center Frequency



4. Discussions of the Phase/Frequency Detector for the Armchair Philosopher

Introduction

Perhaps the most difficult component to understand in the PLL system is the phase/frequency detector. It puts out a signal that is proportional to the phase error. Since phase is the integral of frequency, it also gives some indication of the frequency error as well. In many older classical texts, devices such as mixers and XOR gates are mentioned as phase detectors. The mixer and XOR gate only worked within a limited range. This has caused a lot of confusion with the modern day phase frequency detector (PFD), which has no limitations on the operating range.

Looking carefully at figure 1, it should be clear that the output is actually a phase and not a frequency. The VCO gain is divided by s, which corresponds to integration. Recall this is done because phase is the integral of frequency If the frequency output is sought, then it only necessary to multiply the transfer function by a factor of s, which corresponds to differentiation. Now the phase-frequency detector not only causes the input phases to be equal, but also the input frequencies, because they are related.

Since phase is a little more abstract, many are interested in what the PFD does for two signals differing in frequency. This question is also if interest in the construction of some lock detect circuits, where the average duty cycle of the phase detector is sought for a given frequency error. The reason that this paper is directed at the armchair philosopher is that thinking of the phase-locked loop in terms of frequencies is good enough for most analysis, and many questions regarding phase tend to be very academic. This paper investigates this question with an ideal phase/frequency detector with charge pump attached.

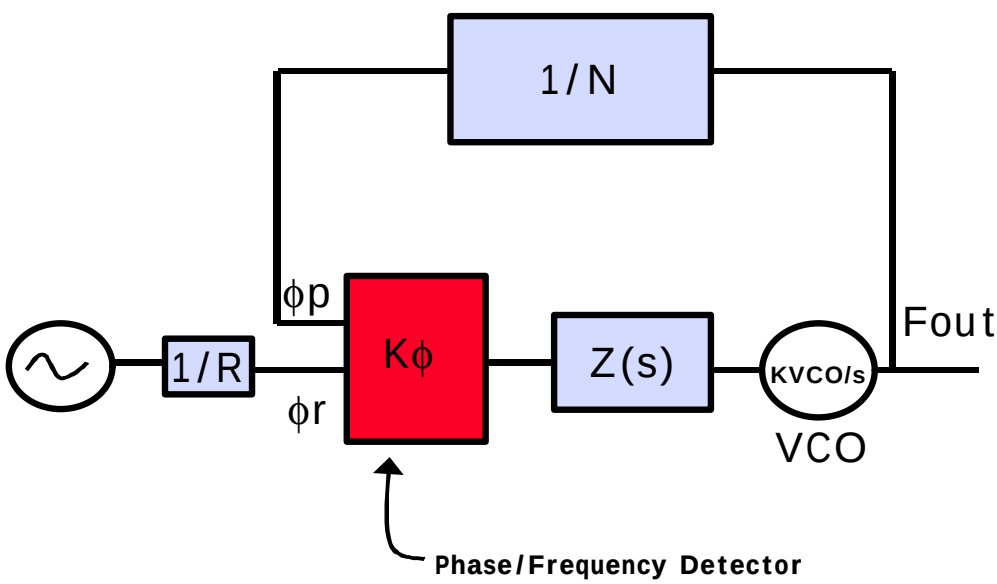


Figure 1 *The Basic PLL Structure Showing the Phase/Frequency Detector*

Analysis of the Phase/Frequency Detector

The output phase of the VCO is divided by N, before it gets to the Phase-Frequency Detector (PFD). Let ϕp represent the phase of this signal, and Fp represent the frequency of this signal. The output phase of the crystal reference is divided by R before it gets to the PFD. Let ϕr be the phase of this signal and Fr be the frequency of this signal. The PFD is only sensitive to the rising edges of ϕr and ϕp. The 3 state PFD has the following 3 states:

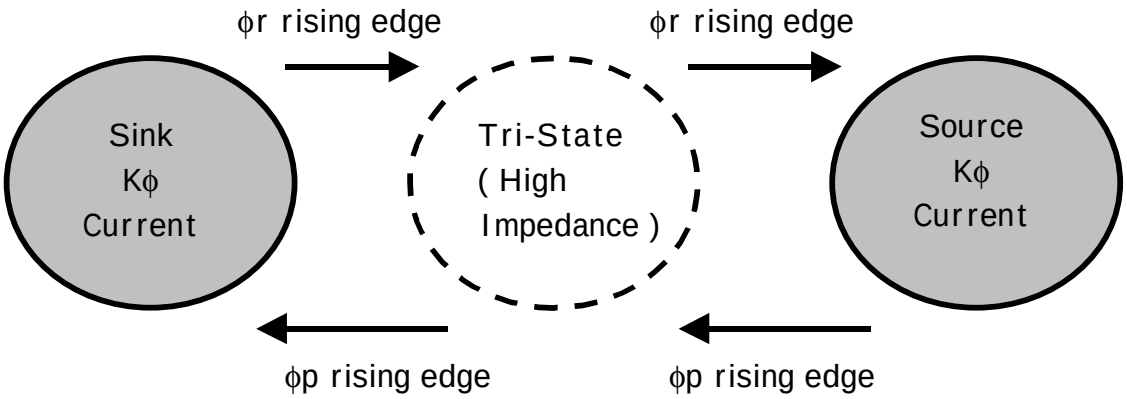


Figure 2 *States of the Phase Frequency Detector (PFD)*

Below is shown an actual example

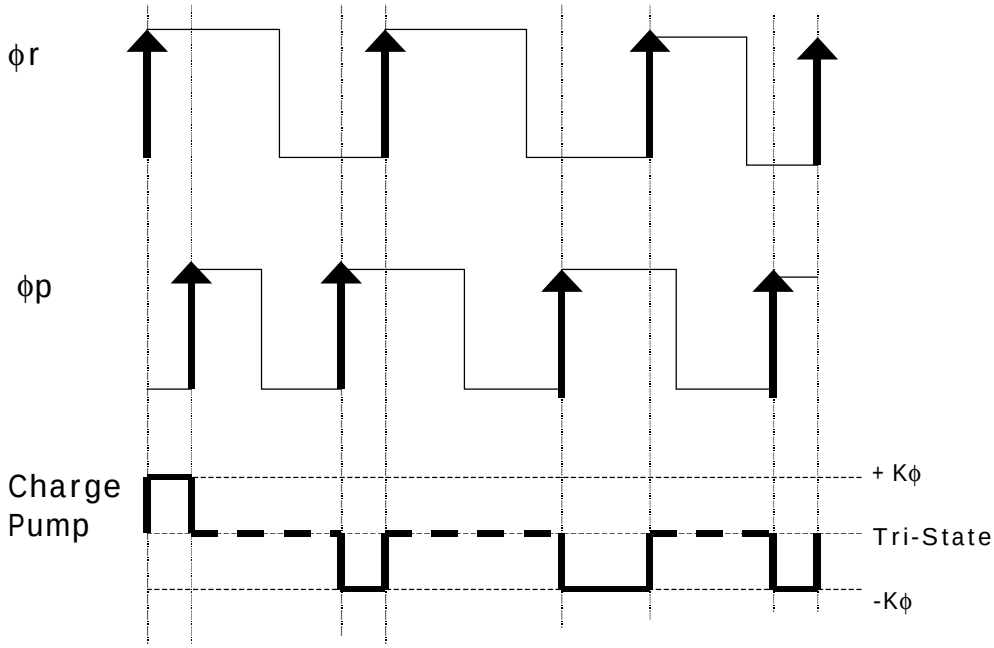


Figure 3 *Example of how the PFD works*

Analysis of the PFD for a Phase Error

Suppose that ϕp and ϕr are at the exact same frequency but off in phase such that the leading edge of ϕr is leading the leading edge of ϕp by a constant time period equal to τ. There are several possibilities:

$$\underline{\tau = 0}$$

For this case, there is no phase error, and the signals are synchronized in frequency and phase, therefore there would theoretically be no output of the phase detector. In actuality, there wound be some very small outputs from the phase detector due to dead zone elimination circuitry and gate delays of components. This is usually a series of positive and negative pulses, alternating in polarity.

$$\underline{\tau > 0}$$

The charge pump will be on for a period of τ for every reference period, 1/Fr. Thus the average output of the charge pump would be:

$$\boldsymbol{t \bullet Fr \bullet Kf} \qquad (1)$$

But this delay period can be associated with a phase delay by multiplying by 2π. So it can be seen that the time averaged output of the PFD is proportional to the phase error. Note that for 2 signals of the same frequency, their phase difference can always be expressed as a number between 0 and 2π. Therefore, the difference, τ, should always be less than 1/Fp in this case.

Phase Detector Gain

To calculate the phase detector gain note that it sources $K\phi$ current when the phase error is $+ 2\pi$ and sinks $K\phi$ current when the phase error is $- 2\pi$ and within this range, the curve is linear. This means that the proper phase detector gain is $K\phi/2\pi$ (mA/rad). In design equations, the factor of 2π is often omitted because it is multiplied by another of 2π which is used to convert the VCO gain from MHz/volt to Mrad/volt.

Analysis of The PFD for 2 signals differing in Frequency and Phase

The phase detector has been analyzed for two signals differing in phase, but not for two signals differing in frequency. This type of analysis is sufficient for most situations. However, some may be interested in how the phase detector behaves for two signals differing in frequency. This is of particular interest in the construction of lock detect circuits. For the purposes of this analysis, the following terms will be defined:

Fr	The frequency of the signal coming from the crystal reference and then divided by R
ϕp	The phase of the fr signal at any given time
α	The initial phase of the fr signal
Fp	The frequency of the signal coming from the VCO and then divided by N
ϕp	The phase of the fp signal at any given time
β	The initial phase of the fr signal
t	Elapsed time.

Since frequency is the rate of change of the phase, it can be shown that:

$$fr = a + Fr \bullet t \tag{2}$$
$$fp = b + Fp \bullet t \tag{3}$$

Looking in this perspective, the phase difference is obvious, therefore the output of the phase detector for a given time, t would be:

$$Kf \bullet \left(a - b + (Fr - Fp) \bullet t\right) \tag{4}$$

Now the choice of T depends on whether or not Fr>Fp or Fr<Fp. It will be assumed that Fr>Fp, if it is the other case, then a similar reasoning can be used. If one considers the average current output over P periods, this is shown below.

$$\begin{cases} \dfrac{Kf}{P} \bullet \left(a - b + (Fr - Fp) \bullet \dfrac{P}{Fr} \right) & Fr > Fp \\ \dfrac{Kf}{P} \bullet \left(a - b + (Fp - Fr) \bullet \dfrac{P}{Fp} \right) & Fr > Fp \end{cases} \tag{5}$$

Taking the limit as P approaches infinity gives the averaged output of the phase detector:

$$\begin{cases} Kf \bullet \left(1 - \dfrac{Fp}{Fr}\right) & Fr > Fp \\ -Kf \bullet \left(1 - \dfrac{Fr}{Fp}\right) & Fr < Fp \end{cases} \tag{6}$$

When Fr is an integer multiple of Fp, these results in (6) have been verified by computer simulation, however, for smaller frequency errors, it has been verified that the charge pump output is a function of the ration of Fr to Fp, and that this increases linearly with the frequency error for small frequency errors only. In a real situation, the PLL is tracking the phase error, which causes some of these simulations to be unrealistic. The equations above serve as a rough guess at the duty cycle of the phase detector for a given frequency error. However, in the closed loop system, the PLL is tracking the phase error, and this can cause these estimates to be a little different than theoretically predicted. For more accurate predictions on how the loop frequency response will be, the phase response can be calculated by taking the integral of the frequency response.

Other Information About the PFD

Discrete Sampling Effects on Loop Stability and Transient Response

The continuous time approximation is mentioned in several chapters and is an approximation which is commonly made. When the loop bandwidth is small relative to the comparison frequency, then these effects are small. If it is not, then this can throw off calculations and introduce instability. Choosing the loop bandwidth to be 1/10th of the comparison frequency is enough to keep one out of trouble, and when the loop bandwidth approaches around 1/3rd the comparison frequency, simulation results show that this causes

instability and the PLL to lose lock. In general, these effects should not be that much of a consideration.

Discrete Sampling Effects on Phase Noise

In terms of loop parameters and stability, these sampling effects are usually not that much of a concern, but they are very relevant in regards to phase noise. Recall that the phase detector/ charge pump tends to be the dominant noise source in the PLL and it is these discrete sampling effects that cause the PFD to be nosier at higher comparison frequencies. Since a PFD with a higher comparison frequency has more corrections, it also puts out more noise, and this noise is proportional to the number of corrections. It is for this reason that the PFD noise increases as 10xlog (Comparison Frequency).

Dead Zone Elimination Circuitry and Component Delays

The dead zone of the phase detector occurs around zero phase error. The problem that occurs here is that when the phase error is very small, the PFD is very non-responsive. There are also component delays. The dead zone elimination circuitry ensures that the phase detector always comes on for some amount of time to avoid operating in the dead zone.

Conclusion

This paper has discussed the PFD (Phase Frequency Detector) and given some characterization on how it performs for both frequency and phase errors. For the phase error, it can be seen that the output is proportional to the phase error, and for frequency errors, it can be seen that there is some output that is positively correlated with the frequency error.

The PFD is named so because it can detect differences in both phase and frequency. It also bypasses many limitations that are part of using a mixer or XOR phase detector, such as pull in range, hold in range, and steady state phase error.

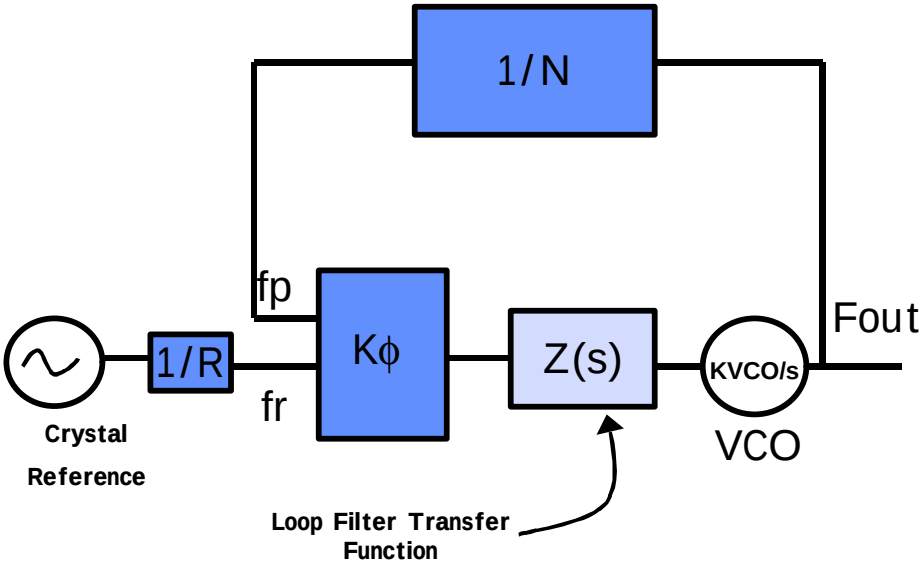
References

[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[3] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

[4] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

PLL Design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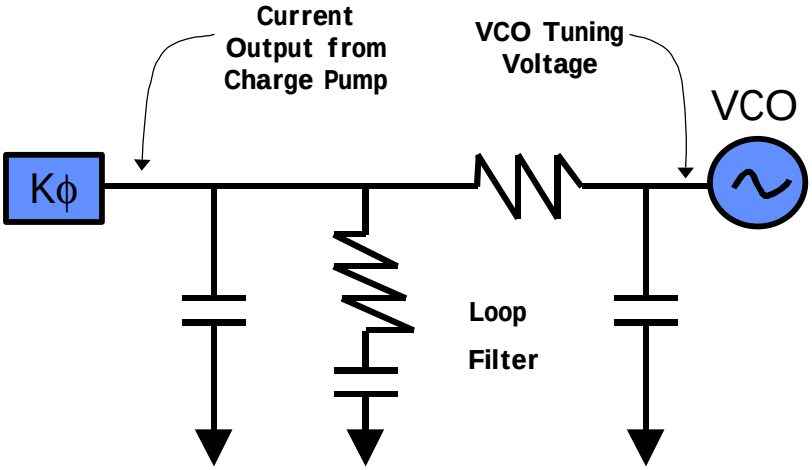
Kϕ
Z(s)
KVCO/s
Fout
1/R
fr
Crystal
Reference
VCO
Loop Filter Transfer
Function


Current
Output from
Charge Pump
VCO Tuning
Voltage
VCO
Kϕ
Loop
Filter

7. Exact Equations for PLL Design

Introduction

This paper has 2 sections. The first section shows a simplified approach that presents a modification that can be made to the equations in AN-1001 that both simplifies the math and also allows the user to specify the true closed loop bandwidth.

The second section allows the user to specify everything EXACTLY, so that simplifying assumptions such as R3>2 ● R2 and C3<C1/10 can be relaxed. The value is that this allows the user to increase the value of C3 which in turn decreases thermal noise due to R3 and decreases the impact of the input capacitance of the VCO that adds in parallel with C3.

Simplified approach

The first assumption, is the continuous time approximation, which approximates the phase detector/charge pump output as it's time-averaged output. The transfer function for the loop filter topology shown in figure 1 is:

$$Z(s) = \frac{1 + s \bullet T2}{(1 + s \bullet T1) \bullet (1 + s \bullet T3)} \bullet \frac{T1}{C1 \bullet T2} \tag{1}$$

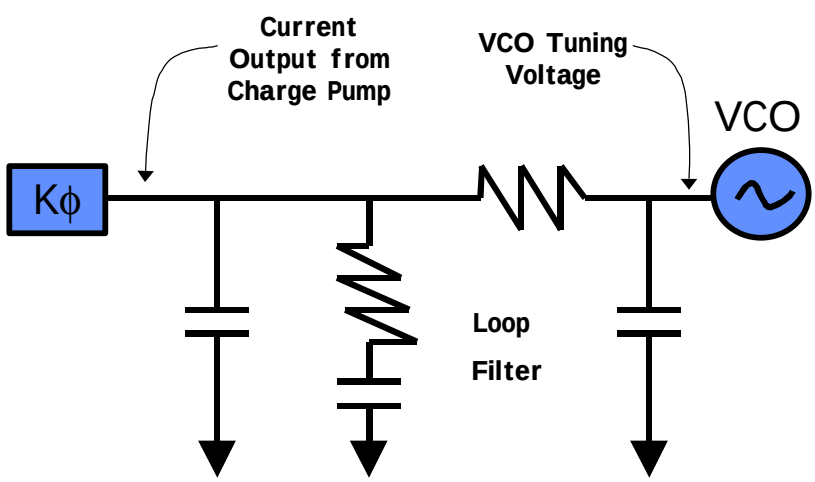


Figure 1 *Passive Third Order Loop Filter*

Phase Margin Derivation

The phase margin is given by:

$$fc = tan^{-1}(wc \bullet T2) - tan^{-1}(wc \bullet T1) - tan^{-1}(wc \bullet T3) + 180 \tag{2}$$

Taking the tangent of both sides yields the following:

$$tan(fc) = \frac{wc \bullet T2 - wc^3 \bullet T1 \bullet T2 \bullet T3 - wc \bullet T1 - wc \bullet T3}{1 - wc^2 \bullet T1 \bullet T3 - T2 \bullet wc^2 \bullet (T1 + T3)} \tag{3}$$

This can be rewritten in the form

$$tan(fc) = \frac{wc \bullet T2 - wc^2 \bullet T1 \bullet T3(tan(fc) - wc \bullet T2) - wc \bullet T1 - wc \bullet T3}{1 - T2 \bullet wc^2 \bullet (T1 + T3)} \tag{4}$$

Recall the relationship that was derived in AN-1001:

$$T2 = \frac{1}{wc^2 \bullet (T1 + T3)} \tag{5}$$

Assuming

$$wc^2 \bullet T1 \bullet T3 \bullet (tan(fc) - wc \bullet T2) \approx 0 \tag{6}$$

Substituting (5) and (6) into (4) yields the following elegant relationship

$$T1 + T3 = \frac{sec(fc) - tan(fc)}{wc} \tag{7}$$

From equations (5) and (7), it can also be inferred.

$$T2 = \frac{1}{wc \bullet (\ sec(fc) - tan(fc)\ )} \tag{8}$$

So T3 and T1 can be solved for in a straightforward manner, and then T2 can also be solved for from (8).

$$T1 = \frac{sec(fc) - tan(fc)}{wc} - T3 \tag{9}$$

Now, this sets a maximum bound on T3, in order to make T1>0

$$T3 < \frac{sec(fc) - tan(fc)}{wc} \tag{10}$$

However, this will always be satisfied, for from the optimal attenuation choice, which is T1 = T3, and the maximum attenuation choice is T1 = 0

Exact Solution of Loop Filter Components

This section derives the exact solution for the filter components. The only assumption here is that the discrete sampling action of the phase detector is approximated by a continuous signal. The assumptions that C3<C1/10 and R2>2 ● R3 have been completely relaxed.

Note that the time constants, T1 and T3, now correspond to the true poles of the filter, as was not the case before. It is also possible to use the method in the previous section to solve approximately for the time constants, and then the method in this section to solve for the loop filter components and relax the restrictions C3>C1/10 and R2>2 ●R3.

True Loop Filter Impedance
The impedance of the filter is given by:

$$\frac{1+s\bullet T2}{s\bullet(1+s\bullet T1)\bullet(1+s\bullet T3)}\bullet\frac{1}{C1+C2+C3} \tag{11}$$

$$T2 = R2\bullet C2$$
$$T1+T3 = \frac{C2\bullet C3\bullet R2+C1\bullet C2\bullet R2+C1\bullet C3\bullet R3+C2\bullet C3\bullet R3}{C1+C2+C3} \tag{12}$$
$$\frac{T1\bullet T3}{T2} = \frac{C1\bullet C3\bullet R3}{C1+C2+C3}$$

Exact Method for Solving for the Time Constants T1 and T2
Choosing the loop bandwidth to maximize the phase margin yields

$$\frac{wc\bullet T2}{1+(wc\bullet T2)^2} = \frac{wc\bullet T1}{1+(wc\bullet T1)^2} + \frac{wc\bullet T3}{1+(wc\bullet T3)^2} = f(wc\bullet T1) \tag{13}$$

$$wc\bullet T2 = \frac{1\pm\sqrt{1-4\bullet f(wc\bullet T1)^2}}{2\bullet f(wc\bullet T1)} = g(wc\bullet T1) \tag{14}$$

In (14) it has been found by trial and error that the positive root usually makes the math work out in the end. However, it is possible that using the negative root could yield better results in some cases.

Using (14) to eliminate $\omega c\bullet T2$ yields in equation (3) yields:

$$\frac{g(x)-x\bullet g(x)\bullet wc\bullet T3-x-wc\bullet T3}{1-x\bullet wc\bullet T3+g(x)\bullet(x+wc\bullet T3)} - tan(fc) = 0 \tag{15}$$

$$T1 = \frac{x}{wc} \tag{16}$$

Once T1 is known, T2 can be found by

$$T1 = \frac{g(wc\bullet T1)}{wc} \tag{17}$$

Defining the proper loop bandwidth
Now, by definition, the gain of the open loop transfer function is equal to one at the loop bandwidth. Therefore ...

$$C1+C2+C2 = \frac{Kf\bullet Kvco}{wc^2\bullet N}\bullet\sqrt{\frac{1+(wc\bullet T2)^2}{(1+(wc\bullet T1)^2)\bullet(1+(wc\bullet T3)^2)}} \tag{18}$$

Defining a system of 4 equations and 4 unknowns
This leads to a system of 4 equations and 4 unknowns:

Constants

$$k1 = \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1+(wc \bullet T2)^2}{(1+(wc \bullet T1)^2) \bullet (1+(wc \bullet T3)^2)}}$$
$$k2 = (T1+T3) \bullet k1$$
$$k3 = \frac{T1 \bullet T3 \bullet k1}{T2} \tag{19}$$
$$k4 = \frac{C3}{C1} = \textit{To be calculated later}$$

Equations

$$\begin{aligned} &C1+C2+C3 &&= k1 \\ &T2 \bullet (C1+C3) + R3 \bullet C3 \bullet (C1+C2) &&= k2 \\ &R3 \bullet C1 \bullet C3 &&= k3 \\ &\frac{C3}{C1} &&= k4\ (\textit{To be specified later}) \end{aligned} \tag{20}$$

$$C1 \bullet (k4+1) + C2 = k1$$
$$T2 \bullet C1 \bullet (k4+1) + k3 + \frac{k3 \bullet C2}{C1} = k2 \tag{21}$$

Combining these leads to a quadric equation that can be solved for C1

$$T2 \bullet (k4+1) \bullet C1^2 + \left(k3 - k2 - k3 \bullet (k4+1)\right) \bullet C1 + k3 \bullet k1 = 0 \tag{22}$$

Determining the proper value for k4

Note that the larger k4 is chosen, the larger C3 will be, and this will be assumed to be desirable. This section shows how to compute the largest possible value for k4.

The discriminant for equation (22) is:

$$A \bullet k4^2 + B \bullet k4 + C \tag{23}$$

Where

$$A = k3^2$$
$$B = 2 \bullet k2 \bullet k3 - 4 \bullet T2 \bullet k3 \bullet k1 \tag{24}$$
$$C = k2^2 - 4 \bullet T2 \bullet k3 \bullet k1$$

When the discriminant is equal to zero and solved for k4, one will get the restriction (r1 and r2 are the roots, and r1<r2):

$$\boldsymbol{k4 < r1} \quad \textbf{\textit{or}} \quad \boldsymbol{k4 > r2} \tag{25}$$

From trial and error, it usually turns out that k4 = r1 is the largest possible choice for k4 which will yield component values that are both real and non-negative. Once that k4 is selected, the equation (22) can be solved for C1. Once C1 is solved for, then C1, C2, R2, and R3 can be solved for in that order by applying equations (20). If the component values come out to be complex or negative, it may be necessary to adjust k4 or Atten.

Conclusion

This paper has presented two approaches to a third order passive loop filter design. The first is a simple approximation that is quite accurate under normal circumstances. The second approach is best used with a program like mathcad, so that the numerical routines can be taken advantage of. It is more work, but allows the user to specify the filter parameters without any approximations, and allows the user to violate the approximations previously used that C3>C1/10 and R3>2● R2. It is also possible to use the first method to solve for the time constants and then the second method to solve for the components. This approach is a little easier than using the second (exact) approach.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops*

EXACT PLL DESIGN
by
Dean Banerjee

This program calculates a third order filter exactly with no approximations whatsoever (Except for the continuous time approximation for the phase detector).
The program automatically picks the ratio of C3/C1. The user can tinker with this also.
If the component values come out negative or complex, try tinkering with the ATTEN value and also with the value of k4.

USER NEEDS TO ENTER THESE:

$\phi c := 45.000001 \cdot deg$ — Phase margin. Default is 50 degrees.

$Fc := 10.000001 \cdot kHz$ — Enter the True Loop Bandwidth in KHz. Do not put Fp.

$Fcomp := 200kHz$ — Comparison Frequency

$Kvco := 20 \cdot \frac{MHz}{volt}$ — Enter the Tuning Constant Here

$K\phi := 5 \cdot mA$ — Enter the Phase Detector gain do not divide by 2*p

$Fout := 900MHz$ — RF output frequency. Choose equal to sqrt(Fmax*Fmin)

$ATTEN := 5$ — Reference spurious attenuation in dB added by R3 and C3. This value is 1/2 of what is used in AN-1001. Stay Below or at the Optimal Value $ATTENopt = 12.304$

CALCULATIONS

$N := \frac{Fout}{Fcomp}$ $\qquad N = 4.5 \cdot 10^{3}$

$T3 := \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{2 \cdot \pi \cdot Fcomp}$ $\qquad T3 = 1.17 \cdot 10^{-6} \cdot sec$

$\omega c := 2 \cdot \pi \cdot Fc$

SOLVE FOR T1 AND T2

$f(x) := \frac{x}{1 + x^2} + \frac{\omega c \cdot T3}{1 + (\omega c \cdot T3)^2}$

This function is the rhs of phase margin eq.

$k := -1$

$g(x) := \frac{1 - k \cdot \sqrt{1 - 4 \cdot f(x)^2}}{2 \cdot f(x)}$

This finds wcT2 as a function of wcT1 (or x)

$x := 3 \cdot 10^{-5}$

$T1 := \frac{root(g(x) - x \cdot g(x) \cdot \omega c \cdot T3 - x - \omega c \cdot T3 - \tan(\phi c)\,(1 - x \cdot \omega c \cdot T3 + g(x) \cdot (x + \omega c \cdot T3)), x)}{\omega c}$

$T1 = 5.057 \cdot 10^{-6} \cdot sec$

$T2 := \frac{g(\omega c \cdot T1)}{\omega c}$ $\qquad T2 = 3.719 \cdot 10^{-5} \cdot sec$

SET UP SYSTEM OF 4 EQUATIONS AND 4 UNKNOWNS

$$k1 := \left(\frac{K\phi \cdot Kvco}{N}\right) \cdot \sqrt{\frac{1 + (\omega c \cdot T2)^2}{(1 + (\omega c \cdot T1)^2) \cdot (1 + (\omega c \cdot T3)^2)}} \cdot \frac{1}{\omega c^2}$$

$k1 = 13.598\,nF$

$k2 := (T1 + T3) \cdot k1$ $\qquad k2 = 8.467 \cdot 10^{-5}\,sec \cdot nF$

$k3 := \frac{T3 \cdot T1 \cdot k1}{T2}$ $\qquad k3 = 2.164 \cdot 10^{-6}\,sec \cdot nF$

USE THESE EQUATIONS TO FIND THE MAXIMUM VALUE FOR k4

$A := k3^2$ $\qquad A = 4.681 \cdot 10^{-12}\,sec^2 \cdot nF^2$

$B := 2 \cdot k2 \cdot k3 - 4 \cdot T2 \cdot k1 \cdot k3$ $\qquad B = -4.01 \cdot 10^{-9}\,sec^2 \cdot nF^2$

$C := k2^2 - 4 \cdot T2 \cdot k3 \cdot k1$ $\qquad C = 2.793 \cdot 10^{-9}\,sec^2 \cdot nF^2$

$k4min := \frac{-B - \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A}$ $\qquad k4min = 0.697$

$k4max := \frac{-B + \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A}$ $\qquad k4max = 855.973$

CHOOSE THE VALUE OF k4 SUCH THAT EITHER k4<=k4min OR k4>=k4max YOU MUST ALSO BE SURE THAT THIS LEADS TO REALIZABLE COMPONENT VALUES (i.e. NO NEGATIVE OR COMPLEX VALUES)

$k4 := k4min$

This is C3/C1 specify as instructed above

NOW SOLVE FOR C1 AND THE OTHER COMPONENTS

$A := T2 \cdot (k4 + 1)$ $\qquad A = 6.311 \cdot 10^{-5}\,sec$

$B := -k2 - k3 \cdot k4$ $\qquad B = -0.086\,sec\,pF$

$C := k3 \cdot k1$ $\qquad C = 29.422\,sec \cdot pF^2$

THE DETERMINANT, D, OF A SYSTEM INDICATES IF THE ROOTS WILL BE REAL THIS OCCURRS IF D>=0

$D := B^2 - 4 \cdot A \cdot C$ $\qquad D = 0\,sec^2 \cdot pF^2$

$k := 1$

$C1 := \frac{-B + k \cdot \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A}$ $\qquad C1 = 682.778\,pF$

$C3 := k4 \cdot C1$ $\qquad C3 = 475.932\,pF$

$C2 := k1 - C3 - C1$ $\qquad C2 = 12.44\,nF$

$R2 := \frac{T2}{C2}$ $\qquad R2 = 2.99\,k\Omega$

$R3 := \frac{k3}{C1 \cdot C3}$ $\qquad R3 = 6.658\,k\Omega$

DERIVED QUANTITIES

Filter Zero

$$\frac{1}{T2 \cdot 2 \cdot \pi} = 4.28 \cdot kHz$$

Time Constants

$$T1 = 5.057 \cdot 10^{-6} \cdot sec$$

$$T2 = 3.719 \cdot 10^{-5} \cdot sec$$

True Filter Poles

$$\frac{1}{T1 \cdot 2 \cdot \pi} = 31.475 \cdot kHz$$

$$\frac{1}{T3 \cdot 2 \cdot \pi} = 136.013 \cdot kHz$$

CALCULATED VALUES:

$C1 = 682.778 \cdot pF$ $\quad C2 = 1.244 \cdot 10^{4} \cdot pF$ $\quad C3 = 475.932 \cdot pF$

$R2 = 2.99 \cdot k\Omega$ $\quad R3 = 6.658 \cdot k\Omega$

$$\zeta := \frac{R2 \cdot C2}{2} \cdot \sqrt{\frac{K\phi \cdot Kvco}{N \cdot (C1 + C2 + C3)}} \qquad \omega n := \sqrt{\frac{K\phi \cdot Kvco}{N \cdot (C1 + C2 + C3)}}$$

SIMULATION

$j := 20 .. 120$

100 points

$$f_j := 10^{\frac{j}{20}} \cdot Hz$$

Generates 5 decades from 10 Hz to 1 MHz

$$S_j := 2 \cdot \pi \cdot f_j \cdot i$$

S = iw

$$Z(S) := \frac{1 + (C2 \cdot R2) \cdot S_j}{(C1 + C2 + C3) \cdot \left(S_j\right) + (C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3) \cdot \left(S_j\right)^2 + C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \cdot \left(S_j\right)^3}$$

Forward Loop Gain

$$H(S) := \frac{1}{N}$$

Reverse Loop Gain

$$G(S) := \frac{K\phi \cdot Kvco \cdot Z(S)}{S_j}$$

$$OL(S) := H(S) \cdot G(S)$$

Open Loop Gain

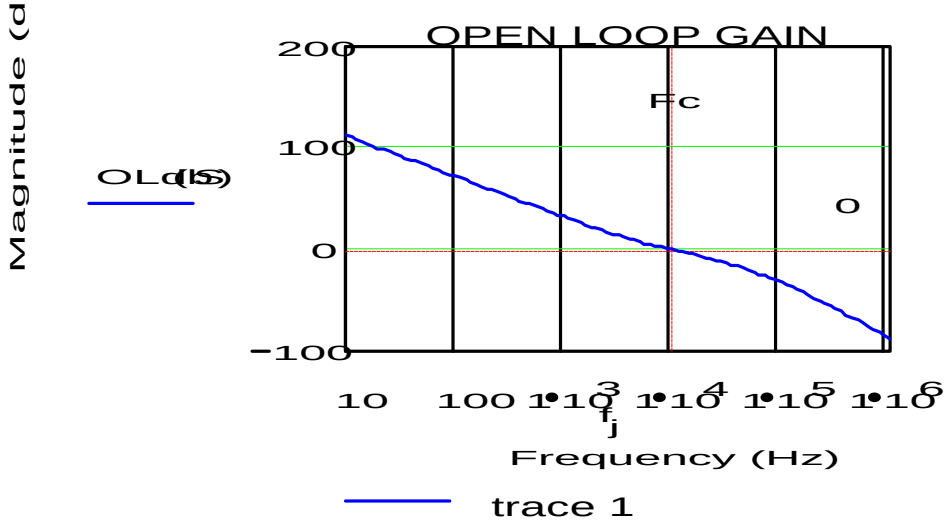
$$CL(S) := \frac{G(S)}{1 + H(S) \cdot G(S)}$$

Closed Loop Gain

Calculated Results

Fc = 10.000001 kHz ϕp = 45.0000011

ζ = 0.752 $\frac{\omega n}{2 \cdot \pi}$ = 6.434 kHz



8. Designing Loop Filters for Optimal Attenuation

Introduction

In accordance with AN-1001 the user specifies various variables, such as ωp (second order bandwidth), ωc (third order bandwidth), ϕp (second order phase margin), N, Fout, and ATTEN (added attenuation due to R3 and C3). When ATTEN = 0, ωc = ωp, however as ATTEN gets larger, ωc gets much smaller than ωp. Note that ωp is not the true bandwidth, but ωc. Note also that ATTEN is an index and is not the actual added attenuation. This paper investigates the actual added attenuation added for a filter of fixed loop bandwidth ωc, and investigates the value of ATTEN that maximizes the true added attenuation over a fixed loop bandwidth.

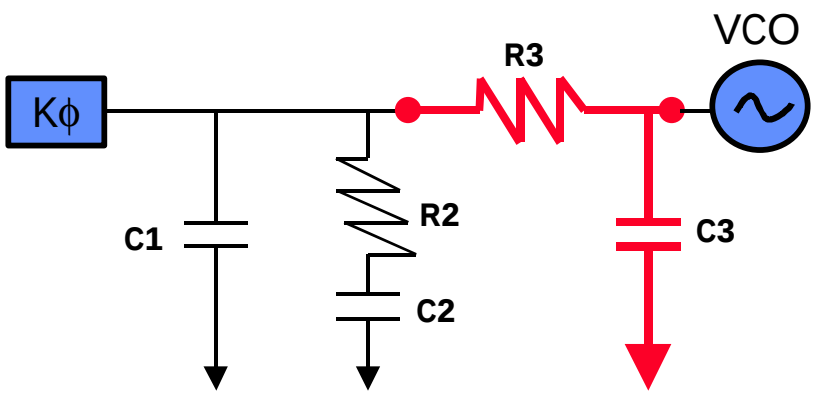


Figure 1 *Basic Passive Loop Filter Topology*

The Problem

The components R3 and C3 form an additional pole in the loop filter that can decrease the spurious attenuation. However, these components also cause the loop bandwidth to be narrowed. ATTEN refers twice of the theoretical added attenuation from these components. It may seem that one should choose ATTEN as large as possible for the best attenuation. However, by doing this other properties of the filter, namely the filter constant T1 get decreased, so the net effect could turn out to be different than once thought. For a fixed ωc, ATTEN can only be increased to a certain extent. When ωp becomes infinite this corresponds to this maximum value for ATTEN, however at this point, T1 becomes zero. This makes the loop filter simply R3 and C3 and nothing else. Clearly this is not the best choice for ATTEN and there are other factors at play. Likewise by experience and physical intuition, choosing ATTEN = 0 is not the best choice either. In other words, there exists some optimal choice of ATTEN.

$$ATTEN = 20 \bullet log\left|1 + (2 \bullet p \bullet fcomp)^2\right| \qquad (1)$$

True Added Attenuation Due to R3 and C3

Let G(s) represent the forward loop gain of the system. G(s) is the product of the phase detector gain, loop filter impedance, and VCO gain (divided by s). Now since we are interested in the spurs which are far outside the loop bandwidth, the closed loop transfer function which multiplies the spurs can be approximated as:

$$\left| s \bullet \frac{G(s)}{1+\frac{G(s)}{N}} \right| \approx \left| s \bullet G(s) \right| = \left| \frac{Kf \bullet Kvco}{C1 \bullet N \bullet wc} \bullet \frac{T2}{T1} \bullet \frac{(1+s \bullet T2)}{(1+s \bullet T1) \bullet (1+s \bullet T3)} \right| \tag{2}$$

Note the extra factor of s. This is because these transfer functions are phase transfer functions. To get the frequency, it is necessary to multiply by the s, which corresponds to differentiation (frequency is the derivative of phase). The magnitude of this can be expressed as:

$$\left| s \bullet G(s) \right| = \frac{Kf \bullet Kvco}{C1 \bullet N \bullet w} \bullet \frac{T1}{T2} \sqrt{\frac{1+w^2 \bullet T2^2}{(1+w^2 \bullet T1^2) \bullet (1+w^2 \bullet T3^2)}} \tag{3}$$

However C1 is not constant. Recall:

$$C1 = \frac{Kf \bullet Kvco}{N \bullet wc^2} \bullet \frac{T1}{T2} \bullet \sqrt{\frac{1+wc^2 \bullet T2^2}{(1+wc^2 \bullet T1^2) \bullet (1+wc^2 \bullet T3^2)}} \tag{4}$$

Substituting this in gives the following expression for G(s)

$$\left| s \bullet G(s) \right| = \frac{wc^2}{w} \bullet \sqrt{\frac{1+w^2 \bullet T2^2}{1+wc^2 \bullet T2^2} \bullet \frac{1+wc^2 \bullet T1^2}{1+w^2 \bullet T1^2} \bullet \frac{1+wc^2 \bullet T3^2}{1+w^2 \bullet T3^2}} \tag{5}$$

Now what is of real concern is the spurious attenuation that is added over a second order loop filter. Use the apostrophe (‘) to denote the values for the second order filter. To start, the following equations are needed [6].

$$T1 + T3 = \frac{sec(fc) - tan(fc)}{wc} = T1' \tag{6}$$

$$T2' = T2 = \frac{1}{wc^2 \bullet (T1+T3)} = \frac{wc}{sec(fc) - tan(fc)} \tag{7}$$

So the true added attenuation over the second order filter is given by:

$$A(T1,T3) = 10 \bullet log \left| \frac{1+wc^2 \bullet (T1+T3)^2}{1+fc^2 \bullet (T1+T3)^2} \bullet \frac{1+fc^2 \bullet T1^2}{1+wc^2 \bullet T1^2} \bullet \frac{1+fc^2 \bullet T3^2}{1+wc^2 \bullet T3^2} \right| \tag{8}$$

$$fc = 2 \bullet p \bullet fcomparison$$

Design for Optimal Attenuation

The problem is stated as follows. Of all loop filters with the following values constant:

ωc	(Third Order Closed Loop Bandwidth)
ϕp	(Second Order Phase Margin)
N	(High Frequency Divider Ratio)
Kvco	(VCO Gain)
Kϕ	(Charge Pump Gain)
Fcomp	(comparison Frequency)

maximize:

A(T1,T3) (9)

subject to the constraint:

$$T1 + T3 = constant = \frac{sec(fc) - tan(fc)}{wc} = K \quad (10)$$

Note that this makes **A(T1,T3)** symmetric in T1 and T3. That is that switching T1 and T3 make no difference. In other words:

A(x,y) = A(y,x) (11)

This will be solved using LaGrange multipliers. The problem will be restated as:

Minimize **Y(T1, T3, λ) = A(T1,T3) + λ● [K – T1 – T3]** (12)

This is done by setting:

$$\frac{\P Y}{\P T1} = \frac{\P Y}{\P T3} = \frac{\P Y}{\P l} = 0 \quad (13)$$

And finding the corresponding values of T1, T3, and λ that satisfy the equation. Proceeding from 12 yields:

$$\frac{\P A}{\P T1} = \frac{\P A}{\P T3} = l \quad (14)$$

$$K = T1 - T3 \quad (15)$$

Now equation (15) is satisfied since it is the constraint. Recalling from (11) the symmetry properties of A(T1,T3) which also apply to its derivatives, then it follows that (14) will be satisfied if:

T1 = T3 (15)

Substituting this back into (10) yields:

$$T3 = T1 = \frac{K}{2} = \frac{sec(fc) - tan(fc)}{2 \bullet wc} \quad (16)$$

This is the optimal choice of T3, of academic interest is also this result expressed using the design rules in AN-1001, which are very similar to (6).

$$T3 = \frac{2 \bullet tan(fp)}{5 \bullet wc} \bullet \left[\sqrt{1 + \frac{5}{4 \bullet tan^2(fp)}} - 1 \right] \quad (17)$$

Also of academic interest is the mathematical limit of ATTEN which occurs when T1 = 0. Note DO NOT USE THIS VALUE. This will attain the same attenuation as a second order filter and will violate design assumptions.

$$T3 = K \tag{18}$$

		Optimal Atten Index db	True Attenuation for this Index db	Attenuation Index Limit db
Fcomp/ωc	3	0.01	-0.90	0.06
	5	6.02	-0.58	14.47
	7	9.43	0.42	19.47
	10	13.98	2.19	25.18
	15	20.00	4.89	31.95
	20	24.61	7.07	36.86
	30	31.36	10.35	43.82
	40	36.26	12.77	48.80
	50	40.09	14.67	52.67
	80	48.20	18.71	60.82
	100	52.06	20.63	64.69
	500	80.00	34.60	92.65
	1000	92.04	40.62	104.69
	10000	132.04	60.62	144.69

Table 1 *Optimal Attenuation Index, Added Attenuation, and Attenuation Limits*

True Added Attenuation and the Optimal Attenuation Index

Table 1 shows the optimal choice for the attenuation index, the expected attenuation of reference spurs from this attenuation index, and the mathematical limit for the attenuation index. This also shows that it makes sense to design for a higher attenuation index when the comparison frequency is large relative to the loop bandwidth. These are the cases when the spurs tend to be less of a problem to begin with. Higher order filters and their effectiveness are also discussed in this book. Note that this table is for the true loop bandwidth ωc and not the approximate loop bandwidth ωp. When the optimal attenuation value is chosen it approximately holds that ωp = 2● ωc. This optimal attenuation index is intended as a limit, and it does make sense to design for slightly less than this index so as to avoid peaking in the loop filter and increase the required capacitor size for C3. As the attenuation index is increased, the capacitor C3 becomes smaller and smaller. When it gets less than about 100 pF, then the VCO input capacitance can start to throw the design off. The VCO input capacitance adds in parallel with C3.

Conclusion

This paper has investigated the true spurious attenuation added by R3 and C3 and also give a recommendation for optimizing this value. Note that these theoretical calculations also hold in the case of fractional spurs. These results were confirmed with a mathcad simulation and

a discrete time analysis, and this value seemed to indeed be an optimal value. Table 1 shows that it makes sense to design for a larger attenuation index (ATTEN), when the comparison frequency is large relative to the loop bandwidth. This is true because the added components, R3 and C3, have a lesser impact on the loop bandwidth.

In conclusion, one should be a little cautious about designing for exactly the optimal attenuation value. To be conservative, one could design a little less than this value to be safe. It makes no sense to design for a value larger than the optimal value.

References

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[3] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

[4] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

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9. Fourth and Higher Order Loop Filter Designs

Introduction

The order of a PLL system is defined as one plus the number of poles in the loop filter. This paper investigates the design of filters with three or more poles and also discusses the theoretical advantages. The motivation for doing higher order filter designs is that the reference spurs are attenuated more. Although this paper investigates the general case for the higher order filters, the fourth order will be used for most of the examples and diagrams, since this filter seems more practical than the higher order designs.

Circuit Topology

A fourth order loop filter is shown below. Higher order loop filters are possible by adding additional RC filters. Buffers can be put between the stages to improve the isolation.

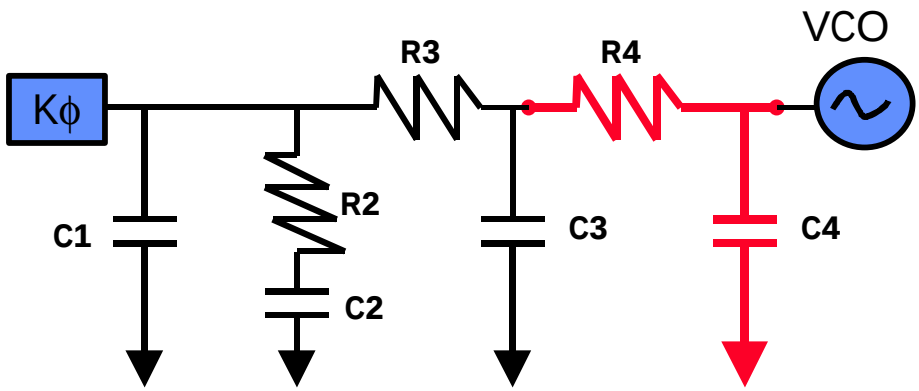


Figure 1 *Fourth Order Passive Filter*

Derivation of Equations

The forward loop gain for the general kth order loop filter is:

$$G(s) \bullet H(s) = \frac{-Kf \bullet Kvco \bullet (1 + s \bullet T2)}{w^2 \bullet N \bullet C1 \bullet (1 + s \bullet T1) \bullet \prod_{i=3}^{k} (1 + s \bullet T_i)} \tag{1}$$

where

$$T1 = R2 \bullet C2 \bullet \frac{C1}{C1 + C2} \tag{2}$$

$$T2 = R2 \bullet C2 \tag{3}$$

$$T_i = R_i \bullet C_i \qquad \mathbf{i = 3,4, \ldots k} \tag{4}$$

Now the equations (1) – (4) are reasonably good approximations. Note that equation (4) is only an approximation of the time constants of the filter, and not the true time constants of the filter. This approximation holds true as long as:

$$\mathbf{C_3 << C1} \tag{5}$$

$$1 << \left(\frac{C_i}{C_{i+1}}\right) + \left(\frac{R_{i+1}}{R_i}\right) \qquad i = 3,4,\ldots k \tag{6}$$

One possible way to ensure that the above constraints are satisfied is to choose:

$$T_i \geq 2 \bullet T_{i+1} \tag{7}$$

In a similar way is calculated in AN-1001, the phase margin is given by:

$$f = 180 + \tan^{-1}(wc \bullet T2) - \tan^{-1}(wc \bullet T1) - \prod_{i=3}^{k} \tan^{-1}(wc \bullet T_i) \tag{8}$$

From the Taylor Series, for small x it can be shown:

$$\begin{aligned} \tan(x) &\approx x \\ \tan^{-1}(x) &\approx x \end{aligned} \tag{9}$$

Applying the tan function, and using the two above identities yields the following simplification:

$$T1 + \sum_{i=3}^{3} T_i \approx \frac{\sec(f) - \tan(f)}{wc} \tag{10}$$

Note for the case that k = 3, this simplifies to the approach given in chapter describing exact equations. Referring back to equation (5), in a similar way as done in AN-1001, the derivative is taken and set to 0 in order to maximize the phase margin:

$$T2 = \frac{T1}{1 + wc \bullet T1} + \sum_{i=3}^{k} \frac{T_i}{1 + wc \bullet T_i} \tag{11}$$

Cross multiplying both sides yields

$$T2 + \ldots \approx wc^2 \bullet T2^2 \bullet (T1 + \sum_{i=3}^{k} T_i) + \ldots \tag{12}$$

Now a great many number of terms have been eliminated, and this simplification can be justified as long as:

$$T2 >> T1 + \sum_{i=3}^{k} T_i \tag{13}$$

Rearranging equation (12) yields the following:

$$T2 \approx \frac{1}{wc^2 \bullet (T1 + \sum_{i=3}^{k} T_i)} \tag{14}$$

$$T1 + \sum_{i=3}^{n} T_i \; \frac{sec(f) - tan(f)}{wc} \tag{15}$$

Now the choice of the time constants T1, T_3, ... T_k can all be chosen equal for optimal spurious attenuation, or can be chosen as in (7) to avoid too much error due to mathematical approximations. In the case of a 4th order filter, to satisfy (7) choose:

$$T1 = \frac{4}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

$$T_3 \equiv T3 = \frac{2}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

$$T_4 \equiv T4 = \frac{1}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

Once these time constants are known, the other components can be solved for

$$C1 = \frac{T1}{T2} \bullet \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1 + wc^2 \bullet T2^2}{(1 + wc^2 \bullet T1^2) \bullet \prod_{i=3}^{k} (1 + wc^2 \bullet T_i^2)}}$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right)$$

$$R2 = \frac{T2}{C2}$$

$$C3 = \frac{C1}{10}$$

$$R3 = R4 = ... = R_k = \frac{T3}{C3}$$

$$C_i = \frac{T_i}{R_i} \qquad i = 3,4,...k$$

Added Attenuation Due to Higher Order Filters

Now that the filter components can be solved for, this still leaves the question of how much spurious attenuation can be expected from these higher order filters. For the purposes of these calculations, it will be assumed that all of the time constants T1 = T3 = ... = Tk are equal. Using the same approach as done in the chapter for optimal spurious attenuation, the expected attenuation over a second order filter is given by:

$$A = 10 \bullet log \left| \frac{1 + wc^2 \bullet (T1 + T3 + ... + Tk)^2}{1 + fc^2 \bullet (T1 + T3 + ... + Tk)^2} \bullet \frac{1 + fc^2 \bullet T1^2}{1 + wc^2 \bullet T1^2} \bullet \frac{1 + fc^2 \bullet T3^2}{1 + wc^2 \bullet T3^2} \bullet ... \bullet \frac{1 + fc^2 \bullet Tk^2}{1 + wc^2 \bullet Tk^2} \right|$$

where fc is the comparison frequency. It turns out that the really relevant factor is the ratio of the comparison frequency to the loop bandwidth. Below is a chart showing the relative attenuation over a second order filter (1 Pole).

	Ratio of Comparison Frequency To Loop Bandwidth						
	1000	**100**	**50**	**20**	**10**	**5**	**3**
# of Poles in the Loop Filter							
1	0	0	0	0	0	0	0
2	40.63	20.64	14.68	7.08	2.20	-0.58	-0.9
3	76.51	36.57	27.72	10.09	1.75	-1.71	-1.5
4	109.37	49.53	31.94	11.01	0.57	-2.60	-1.95
5	140.02	60.33	37.16	10.79	-0.70	-3.25	-2.4

Table 1 *Added Spurious Attenuation for Various Order Filters*

Although the chart does contain some approximations, this should be intended as an upper bound on the attenuation that can be achieved. Notice that when the comparison frequency is large relative to the loop bandwidth, there is much more advantage in building higher order filters. Of course in these cases, spurs are often not as much of an issue. The chart also implies that a third order loop filter (2 poles) only makes sense if the comparison frequency is at least 10X the loop bandwidth. Note that this should be the case anyways, in order to satisfy the continuous time approximation. Although this much attenuation may be possible, it makes sense to design for T1 > T3 > ... > Tk, in order to avoid peaking in the loop response

4th Order (3 Pole) Loop Filter Design Example

The following are the design parameters of the filter

VCO Gain	=	20	MHz/Volt
Charge Pump Gain	=	5	mA
Phase Margin	=	55	degrees
Output Frequency	=	2000	MHz
Comparison Frequency	=	200	KHz
Loop Bandwidth	=	10	KHz

Choose

T1 = T3 = T4

In order to get maximum spurious attenuation from the filter, all of the time constants will be chosen equal. Note that this may cause a degradation in phase margin and peaking in the loop response by using this choice.)

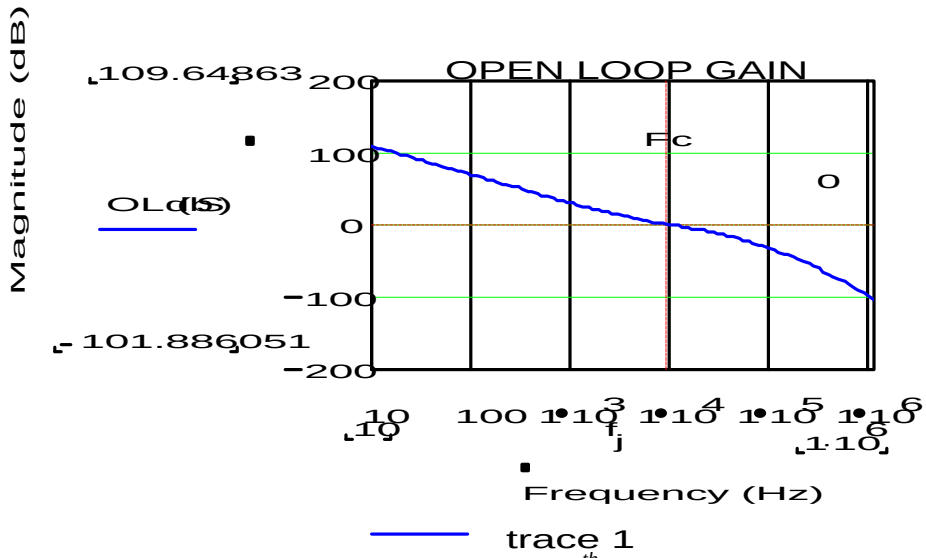


Figure 2 *Open Loop Gain for the 4th Order PLL Design*

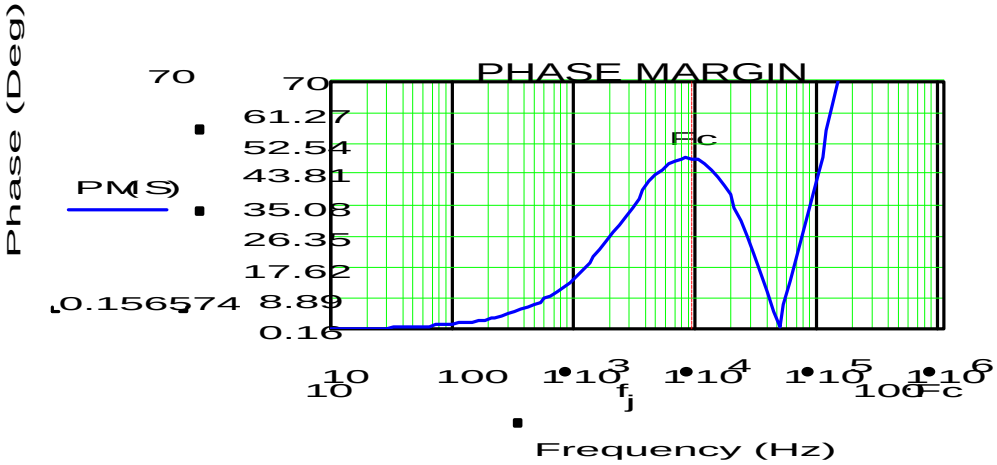


Figure 3 *Phase Margin for the 4th Order Design*

Now for this filter, it turns out that the true loop bandwidth turns out to be 9.05 kHz and the phase margin to be 48.4 degrees. Note that there was degradation in the phase margin due to the extra low pass filter, and this degradation was more because this particular filter was designed for optimal spurious attenuation.

Conclusion

The design and simulation of a fourth order filter has been presented. In most cases, the fourth order filter should be able to have better spurious attenuation. Table 1 shows theoretical advantages of using fourth and higher order filters. The design equations have been simulated and the parameters designed for seem close to those achieved.

PLL DESIGN

USER NEEDS TO ENTER THESE:

$Kvco := 20 \cdot \frac{MHz}{volt}$ Enter the Tuning Constant Here

$K\phi := 5 \cdot mA$ Enter the Phase Detector gain do not divide by 2*π

$Fout := 2000 MHz$ RF output frequency.

$Fcomp = 200 kHz$ Comparison Frequency

$Fc := 10 \cdot kHz$ Enter the True Loop Bandwidth in KHz. Do not put

$\phi := 55 \cdot deg$ Phase margin. Default is 50 degrees.

CALCULATIONS

$$N := \frac{Fout}{Fcomp}$$

$$\omega c := 2 \cdot \pi \cdot Fc$$

$$k := \frac{\left(\frac{1}{\cos(\phi)} - \tan(\phi)\right)}{\omega c}$$

$$T1 := \frac{k}{3} \qquad T3 := \frac{k}{3} \qquad T4 := \frac{k}{3}$$

$$T2 := \frac{1}{(\omega c^2 \cdot (T1 + T3 + T4))}$$

$$C1 := \frac{T1}{T2} \cdot \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \left[\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}\right]^{\frac{1}{2}}$$

$$C2 := C1 \cdot \left(\frac{T2}{T1} - 1\right) \qquad C3 := \frac{C1}{10} \qquad C4 := C3 \qquad R2 := \frac{T2}{C2}$$

$$R3 := \frac{T3}{C3} \qquad R4 := R3$$

CALCULATED VALUES:

$C1 = 274.578 pF$

$C2 = 8.011 \cdot 10^{3} \cdot pF$

$C3 = 27.458 pF$

$C4 = 27.458 pF$

$R2 = 6.301 k\Omega$

$R3 = 60.919 k\Omega$

$R4 = 60.919 k\Omega$

SIMULATION

$j := 20 .. 120$

100 points

$$\omega n := \sqrt{\frac{K\phi \cdot Kvco}{N \cdot (C1 + C2 + C3)}}$$

$$f_j := 10^{\frac{j}{20}} \cdot Hz$$

Generates 5 decades from 10 Hz to 1 MHz

$$S_j := 2 \cdot \pi \cdot f_j \cdot i$$

S = iω

$$Z1(S) := \frac{1 + (C2 \cdot R2) \cdot S_j}{S_j \cdot (C1 + C2) + (S_j)^2 \cdot C1 \cdot C2 \cdot R2}$$

$$Z(S) := \frac{Z1(S)}{S_j \cdot C4 \cdot \left[R3 + Z1(S) + \left(R3 + Z1(S) + \frac{1}{S_j \cdot C3} \right) \cdot \left(\frac{C3}{C4} \right) \cdot \left(1 + S_j \cdot C4 \cdot R4 \right) \right]}$$

Closed Loop Gain

Forward Loop Gain

$$H(S) := \frac{1}{N}$$

Reverse Loop Gain

$$G(S) := \frac{K\phi \cdot Kvco \cdot Z(S)}{S_j}$$

$$OL(S) := H(S) \cdot G(S)$$

Open Loop Gain

$$CL(S) := \frac{G(S)}{1 + H(S) \cdot G(S)}$$

Closed Loop Gain

Open Loop Gain

$$PM(S) := 180 - \left| \arg(OL(S)) \right| \cdot \frac{180}{\pi}$$

$\frac{\omega n}{2 \cdot \pi} = 5.52 \cdot kHz$ $\qquad$ $Fc = 9.051 \cdot kHz$ $\qquad$ $\phi p = 48.426$

10. The Effects Various Filter Parameters on Reference Spurs for a Second Order Filter

Introduction

This paper investigates the effects of various loop filter parameters, such as phase margin, loop bandwidth, and N value on the spur level. Without loss of generality, it is fair to assume a second order filter, because the effect of R3 and C3 as already been investigated. In the start of this chapter, the equations for the second order transfer function are expressed in different terms in order to enable one to see the effects of the different parameters directly on the loop filter components. Once this is known, influence of the design parameters on the reference spurs becomes more visible.

Reformulation of Equations

Recall in AN-1001, the equations were derived for the second order filter. This section simply reformulates these and eliminates the variables T1 and T2. Recall the formulas for the time constants T1 and T2.

$$T1 = \frac{sec(fp) - tan(fp)}{wp} \tag{1}$$

$$T2 = \frac{1}{wp^2 \bullet T1} \tag{2}$$

Combining these two expressions yields two more expressions that will be used later on.

$$\frac{T2}{T1} = \frac{cos^2(fp)}{(1 - sin(fp))^2} \tag{3}$$

Recall the expression for C1:

$$C1 = \frac{T1}{T2} \bullet \frac{Kf \bullet Kvco}{wp^2 \bullet N} \bullet \sqrt{\frac{1 + (wp \bullet T2)^2}{1 + (wp \bullet T1)^2}} \tag{4}$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \tag{5}$$

$$R2 = \frac{T2}{C2} \tag{6}$$

Combining equations (2) and (3) with (4), (5), and (6) yield the following

$$C1 = \frac{Kf \bullet Kvco}{wp^2 \bullet N} \bullet \frac{1 - sin(f)}{cos(f)} \tag{7}$$

$$C2 = \frac{2 \bullet Kf \bullet Kvco}{wp^2 \bullet N} \bullet tan(fp) \tag{8}$$

$$R2 = \frac{N \bullet w}{2 \bullet Kf \bullet Kvco} \bullet \frac{cos(fp)}{1 - sin(fp)} \tag{9}$$

Of some interest is the function $\frac{1 - sin(x)}{cos(x)}$ which is a gradually decreasing function in x.

Spur Levels

In the paper, "On Reference Spurs and their Causes", it was shown that for a second order filter, the spurs are multiplied by the following transfer function:

Leakage Dominated Spur	Mismatch Dominated Spur
$b = \frac{Kvco \bullet leakage}{Fcomp^2 \bullet (C1 + C2)}$	$b = \frac{Kvco \bullet Constant}{Fcomp \bullet (C1 + C2)}$

Taking the formulas in the table and making the following substitution:

$$\frac{1}{C1 + C2} = \frac{wp^2 \bullet N}{Kf \bullet Kvco} \bullet \left(\frac{1}{2 \bullet tan\, f} + \frac{cos\, f}{1 - sin\, f} \right) \tag{10}$$

Yields the fundamental relationships between the spur levels and the loop filter parameters.

Relationship to Parameter	Leakage Dominated Spurs	Mismatch Dominated Spurs
Charge Pump Leakage, i_{leak}	20 x log(i_{leak})	N/A
Mismatch, M	N/A	Correlated to abs(M - δ)
N Value, N	20xlog(N)	20xlog(N)
Phase Margin	Weak Inverse Correlation	Weak Inverse Correlation
VCO Gain, KVCO	Independent	Independent
loop Bandwidth, ωp	40 x log(ωp)	40 x log(ωp)
Added Attenuation, Atten	This is investigated separately in another paper	
Comparison Frequency	-40 x log(Fcomp)	-20 x log(Fcomp)
i = Fcomp/ωp	-40 X log(i)	-40Xlog(i) + 20Xlog(Fcomp)
Charge Pump Gain, Kϕ	-10 x log(Kϕ)	Independent

Table 1 Reference Spur Levels vs. Various Loop Filter Parameters

From Table 1, it follows that the loop bandwidth, comparison frequency, and N value have the largest influence on the spur level. If one considers the ratio of the comparison frequency to the loop bandwidth, then this is a rough indicator. The N value is also relevant, but is related to the comparison frequency. Larger charge pump gains yield lower leakage dominated spurs, because they yield larger capacitor values in the loop filter.

	Filter 1	Filter 2	Filter 3	Filter 4
Loop Bandwidth, ωc	7.6 KHz	3 KHz	7.6 KHz	15.8 KHz
Comparison Frequency, Fcomp	312.5 KHz	100 KHz	100 KHz	100 KHz
Fcomp/ωc	41.1	33.3	13.2	6.3
Frequency	**Spur Level (dbc)**			
1795 MHz	-72.0	X	-65.7	-54.8
1805 MHz	-76.0	X	-67.1	-56.8
1815 MHz	-78.0	X	-71.6	-58.5
1865 MHz	X	-	-75.6	-65.0
1875 MHz	-79.0	-	-70.5	-59.8
1885 MHz	-71.9	X	-64.2	-54.2
1895 MHz	-60.2	-69.7	-51.7	-41.0

Table 2 *Measured Spur Level For a Given PLL and VCO with Different Comparison Frequencies and Loop Filters*

Table 2 shows actual measured data on spur levels. For this data, the exact same PLL was used on the same board with the same VCO. Only the loop filter was changed. This was done for a 100 KHz comparison frequency and all filters were designed with about 45 degrees of phase margin. An X indicates that no spur was measured and the spur was below the noise. A dash indicates no measurement was taken.

Conclusion

This paper has investigated the various factors that influence spurs. The inferences about the spur level made in this paper assume a certain set of design requirements such as N value and loop bandwidth. Although this paper does show some general trends in reference spurs, spur prediction is very tricky because it involves several factors that could be part specific. The main purpose of this chapter is not to actually predict reference spurs but to give a better idea of how one loop filter design compares to another loop filter design.

11. A Simple Method for High Voltage Tuners

In many broadband tuning applications , it is necessary to supply a higher tuning voltage that the PLL is allowed to create. This necessitates the need for active devices in the loop filter. These active devices introduce noise, and it is important to minimize the effects of this noise. The third pole is placed after the op amp to reduce the op amp noise. This paper shows a possible topology and demonstrates that AN-1001 can be used to calculate the loop filter components.

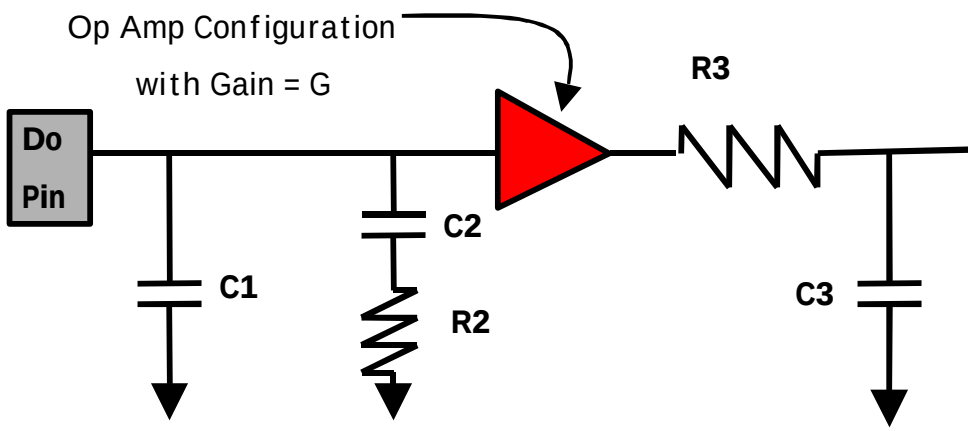


Figure 1. *Active loop filter topology*

In accordance with the methodology and terminology of AN-1001, it follows that impedance of this filter is given by

$$\frac{Vtune}{Ido} = \frac{(1+s \bullet T2)}{s \bullet C1 \bullet (1+s \bullet T1)} \bullet \frac{T1}{T2} \bullet \frac{G}{1+s \bullet T3} \tag{26}$$

The open loop gain is given by

$$G(s) \bullet H(s) = \frac{-Kpd \bullet Kvco \bullet (1+jw \bullet T2)}{w^2 \bullet C1 \bullet N \bullet (1+jw \bullet T1)} \bullet \frac{T1}{T2} \bullet \frac{G}{(1+jw \bullet T3)} \tag{27}$$

Note that it is not necessary to make any mathematical approximations, as was done in the case when no active device was placed in the loop filter. Also note that this formula is identical to (26) with the exception of the factor G. Since all of the component values are calculated from this formula, it follows that component values will be exactly the same as if one was to design for a VCO with the original gain times the gain of the Op amp stage. A possible choice for the op amp would be the LM6132/6142 or LM833. Note that if the op amp is used in the inverting configuration, it is necessary to invert the polarity of the phase detector.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops (AN-1001)*

12. Design of a Loop Filter Using the ϕr and ϕp pins

Introduction

This paper investigates the design of a loop filter and the behavior of a filter designed using the differential phase detector outputs , ϕr and ϕp. These were discussed in a previous chapter. This topology bypasses the charge pump and is most advantageous when used with a PLL with a bad charge pump. For PLLs with a well balanced and low-leakage charge pump, other active loop filter topologies are recommended that use the charge pump output. The reason for using an active filter is typically to get an increased tuning voltage to the VCO.

Loop Filter Topology

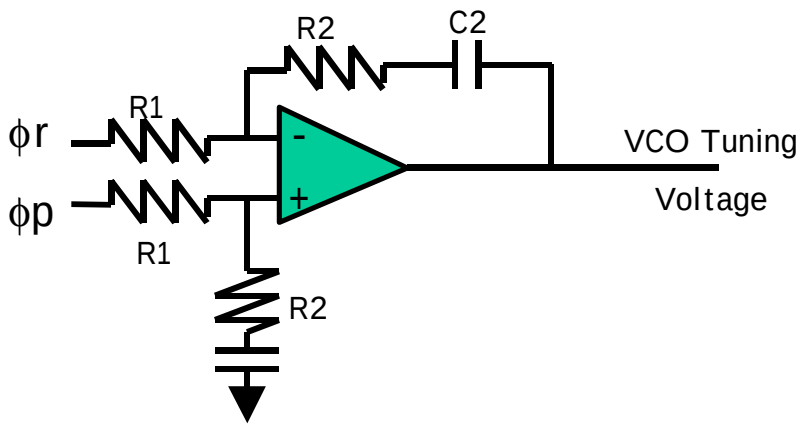


Figure 1 *Active Filter Topology Used*

The impedance of the filter is given by:

$$Z(s) = \frac{1 + s \bullet T2}{s \bullet T1}$$

where

T2 = R2●C
T1 = R1●C

The open loop response is given by:

$$G(s) \bullet H(s) = \frac{Kf \bullet Kvco \bullet (1 + s \bullet T2)}{N \bullet T1 \bullet s^2}$$

If the phase margin is specified to be ϕ , then

$$wc \bullet T2 = \tan f$$

where ωc is the closed loop bandwidth, that is the frequency where the open loop response is equal to 1. Substituting this back in yields the following

$$T1 = \frac{Kf \bullet Kvco}{N \bullet wc^2 \bullet \cos f}$$

So then the capacitor is chosen, and the resistors are determined by the time constants T1 and T2.

$$R1 = \frac{T1}{C}$$

$$R2 = \frac{T2}{C}$$

Transient Response

The transient response for this loop filter refers to the time it takes for the synthesizer to change from one frequency to another when the N divider is changed. To calculate this, the closed loop response is multiplied by a step response. This gives rise to a traditional second order model. For this loop filter topology, the second order model is the exact model, and not an approximation. These values for natural frequency and damping factor can be substituted into the second order model presented earlier in this book for lock time determination.

The closed loop response is given by:

$$\frac{\frac{Kf \bullet Kvco}{N} \bullet \frac{(1 + s \bullet T2)}{T1}}{s^2 + s \bullet \frac{Kf \bullet Kvco \bullet T2}{N \bullet T1`} + \frac{Kf \bullet Kvco}{N \bullet T1}}$$

Using traditional control theory and disregarding the effect of the zero, which has a large effect on the overshoot, but a minimal effect on the lock time, the transient response is characterized by:

$$h = \frac{wn \bullet R2 \bullet C}{2}$$

$$wn = \sqrt{\frac{Kf \bullet Kvco}{N \bullet C \bullet R1}}$$

Conclusion

The design equations are given for an op amp design using the differential outputs of the phase detector. There are other approaches to active loop filter design, but many like this particular design because it is something that they are more familiar with.

References

[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[2] Franklin, F. , Powell, D., and Emami-Naeini, A. *Feedback Control of Dynamic Systems*, 3rd ed. , Addison-Wesley, 1994

[3] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

[4] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

[5] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loop*

[6] AN535 *Phase-Locked Loop Design Fundamentals* Motorola Semiconductor Products, 1970

Example for "OP Amp Filter Design"

This program is for a design with resistors R1 going series from the ϕr and ϕp pins to the inputs of an op amp. There is R1 and C in series from the output of the op amp to the negative terminal.

Additional lowpass filtering by R11 and C1 of the ϕr and ϕp pins is provided for in the simulation,
but not the design

USER NEEDS TO ENTER THESE:

$Kvco := 10 \cdot \frac{MHz}{volt}$ Enter the Tuning Constant Here

$K\phi := 4 \cdot volt$ Enter the Phase Detector gain do not divide by 2*π

$Fout := 700MHz$ RF output frequency. Choose equal to sqrt(Fmax*Fmin)

$Fcomp := 100kHz$ Comparison Frequency

$Fc := 2 \cdot kHz$ Choose a Loop Bandwidth

$\phi := 45$ Phase Margin in degrees

CALCULATIONS

$N := \frac{Fout}{Fcomp}$ $N = 7 \cdot 10^3$

$\omega c := 2 \cdot \pi \cdot Fc$

$T1 := \frac{K\phi \cdot Kvco}{N \cdot \omega c^2 \cdot \cos\left(\frac{\pi}{180} \cdot \phi\right)}$ $T2 := \frac{\tan\left(\frac{\pi}{180} \cdot \phi\right)}{\omega c}$

Choose $C := 200pF$

$R1 := \frac{T1}{C}$ $R1 = 255.875kΩ$

$R2 := \frac{T2}{C}$ $R2 = 397.887kΩ$

SIMULATION

$j := 20 .. 120$

100 points

$\omega n := \sqrt{\frac{K\phi \cdot Kvco}{N \cdot C \cdot R1}}$ $\zeta := \frac{R2 \cdot C}{2} \cdot \omega n$

$f_j := 10^{\frac{j}{20}} \cdot Hz$

Generates 5 decades from 10 Hz to 1 MHz

$S_j := 2 \cdot \pi \cdot f_j \cdot i$ $S = i\omega$

$Z(S) := \frac{1 + (C \cdot R2) \cdot S_j}{R1 \cdot S_j \cdot C}$

$H(S) := \frac{1}{N}$ $\qquad$ $G(S) := \frac{K\phi \cdot Kvco \cdot Z(S)}{S_j}$

Open Loop Gain

$OL(S) := H(S) \cdot G(S)$

$CL(S) := \frac{G(S)}{1 + H(S) \cdot G(S)}$

ReCalculate Open Loop Gain in dB

$PM(S) := 180 - \left| \arg(OL(S)) \right| \cdot \frac{180}{\pi}$

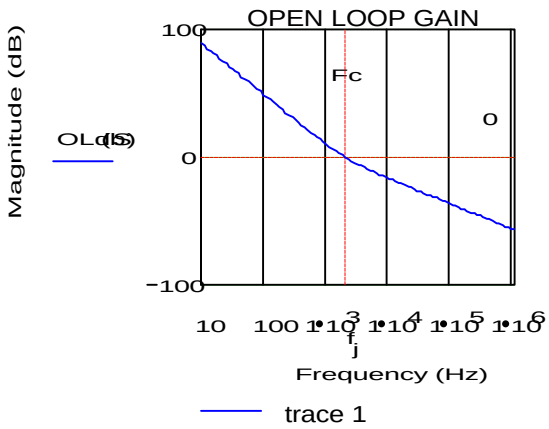
$Fc := \frac{\omega c}{2 \cdot \pi}$

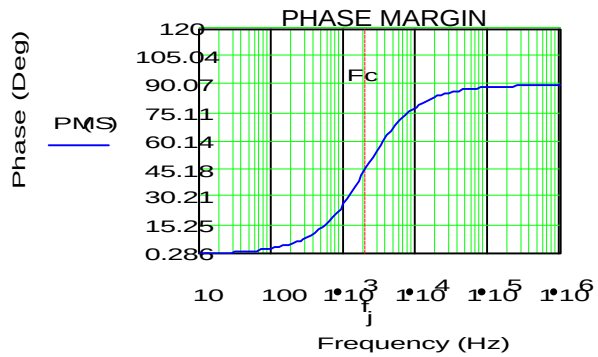
$\phi p := 180 - \left| \arg(G1(\omega c \cdot i)) \cdot \frac{180}{\pi} \right|$

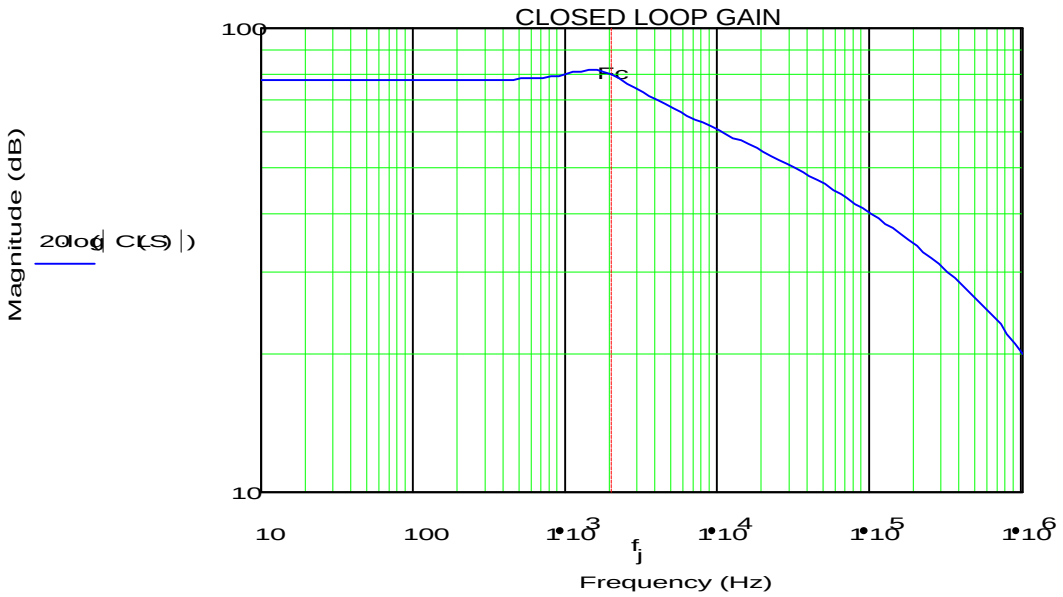
Calculated Results

$Fc = 2 \cdot 10^{3} \cdot sec^{-1}$ $\qquad$ $\phi p = 45$ $\qquad$ $\zeta = 0.42$ $\qquad$ $\frac{\omega n}{2 \cdot \pi} = 1.682 \cdot kHz$

Closed Loop Gain






CLOSED LOOP GAIN
100
10
Fc
Magnitude (dB)
20log(|C(S)|)
10
100
1·10^3
1·10^4
1·10^5
1·10^6
f_j
Frequency (Hz)

13. Alternative Active Filter Designs Using the Do Pin and OP AMP

Introduction

This approach is often used because it resembles a technique mentioned in older application notes which had a voltage charge pump. This method also has the advantage that it allows one to bias the voltage at the charge pump output to half of the power supply voltage. By doing this, the charge pump is better matched and the spurs are lower.

In this paper, two different approaches are used, both of which allow one to have a voltage output that swings to the rails of the OP AMP. The first method presented has the advantage that it is simple and it uses exactly the same design equations as presented in the beginning of this book. A second method is also presented, which is used because the topology is more familiar and also it may yield capacitor values that are easier to find.

Circuit Diagrams

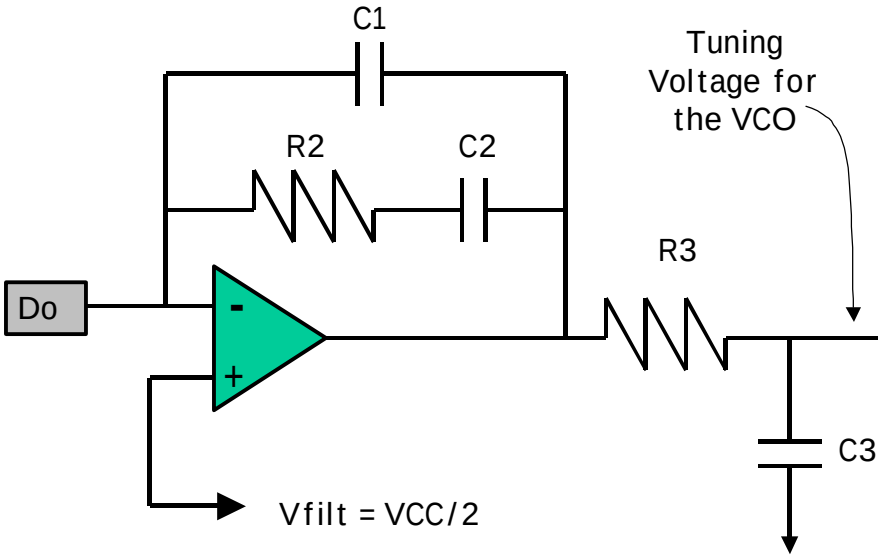


Figure 1 *First Active Filter Approach*

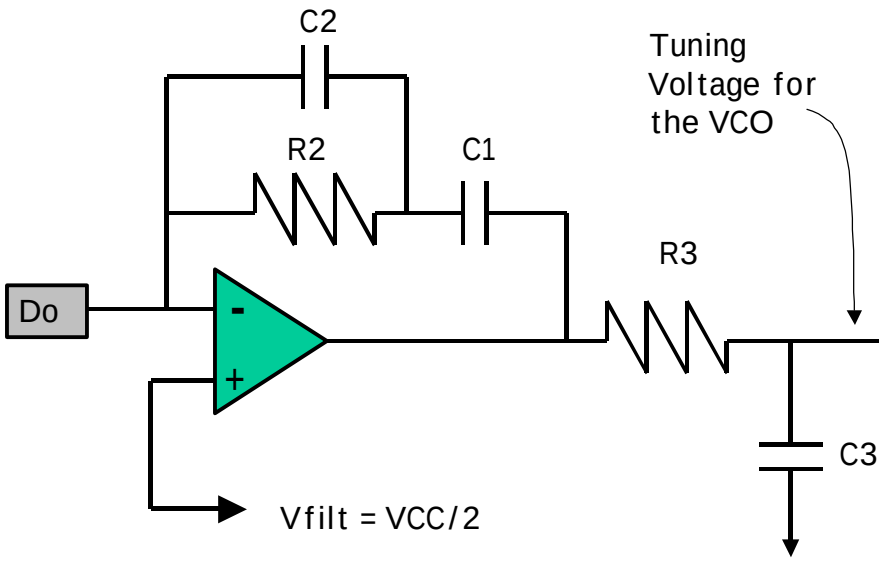


Figure 2 *A Second Active Filter Approach*

Solving for the Components

Vfilt

For Vfilt, choose this equal to Vcc/2 by using a resistive divider. The reason for this choice is that the mismatch of the charge pump should me minimized with this choice.

Transfer Function

Regardless of which filter topology is chosen, the transfer function can be expressed in the same form. For the case of the topology in figure 1:

$$Z(s) = \frac{1 + s \bullet C2 \bullet R2}{s \bullet C1 \bullet (1 + s \bullet C2 \bullet R2) \bullet (1 + s \bullet C3 \bullet R3)} = \frac{1 + s \bullet T2}{s \bullet C1 \bullet (1 + s \bullet T1) \bullet (1 + s \bullet T3)}$$

And in the case of the topology in figure 2:

$$Z(s) = \frac{1 + s \bullet (C2 \bullet R2 + C1 \bullet R2)}{s \bullet C1 \bullet (1 + s \bullet C2 \bullet R2) \bullet (1 + s \bullet C3 \bullet R3)} = \frac{1 + s \bullet T2}{s \bullet C1 \bullet (1 + s \bullet T1) \bullet (1 + s \bullet T3)}$$

but this is precisely the transfer function in AN-1001, however the time constants have different meaning. This means, by duality, the time constants can be solved for, and then the components. From the chapter on exact equations for PLL design and AN-1001:

$$T3 = \sqrt{\frac{10^{\frac{ATTEN}{20}}}{(2p \bullet fcomp)^2}}$$

$$T1 = \frac{\sec f - \tan f}{wc} - T3$$

$$T2 = \frac{1}{wc^2 \bullet (T1 + T3)}$$

$$C1 = \frac{T1}{T2} \bullet \frac{Kf \bullet Kvco}{N} \bullet \sqrt{\frac{1 + (wc \bullet T2)^2}{(1 + (wc \bullet T1)^2) \bullet (1 + (wc \bullet T3)^2)}}$$

$$C3 = \frac{C1}{10}$$ (Actually, C3 can be chosen larger, since there is an op amp)

$$R3 = \frac{T3}{C3}$$

The above formulas apply to both filter topologies. Below are shown formulas specific to the topology in figure 1.

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right)$$

$$R2 = \frac{T2}{C2}$$

Below are shown formulas specific to the topology in figure 2 which are derived by solving a system of equations.

$$R2 = \frac{T2 - T1}{C1}$$

$$C2 = \frac{T1}{R2}$$

Conclusion

Two loop filter topologies for active filters have been presented. These two approaches have the advantage that the OP AMP is centered at the middle of the charge pump supply, for optimal spur performance. The reason that one may choose to use one of these topologies over another is due to the capacitor sizes required. Note that although these approaches both yield the came component values for C1, C3, and R3, the second approach will always yield a smaller value for the capacitor C2 and a larger value for R2.

PLL DESIGN WITH OP AMP AND DO PIN

USER NEEDS TO ENTER THESE:

$Kvco := 20 \cdot \frac{MHz}{volt}$	Enter the Tuning Constant Here
$K\phi := 5 \cdot mA$	Enter the Phase Detector gain do not divide by 2*π
$Fout := 700MHz$	RF output frequency
$Fcomp := 200kHz$	Comparison Frequency
$Fc := 10 \cdot kHz$	Enter the True Loop Bandwidth in KHz. Do not put Fp.
$\phi p := 45 \cdot deg$	Phase margin. Default is 50 degrees.
$ATTEN := 10$	Reference spurious attenuation in dB added by R3 and C3. This value is in AN-1001

CALCULATIONS

$$N := \frac{Fout}{Fcomp}$$

$$\omega c := 2 \cdot \pi \cdot Fc$$

$$T3 := \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{2 \cdot \pi \cdot Fcomp}$$

$$T1 := \frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega c} - T3$$

$$T2 := \frac{1}{(\omega c^2 \cdot (T1 + T3))}$$

$$C1 := \frac{T1}{T2} \cdot \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \left[\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)} \right]^{\frac{1}{2}}$$

$$C3 := \frac{C1}{10} \qquad R3 := \frac{T3}{C3}$$

CALCULATED VALUES FOR BOTH APPROACHES:

$C1 = 1.979 \cdot 10^3 \cdot pF$

$C3 = 197.892 \cdot pF$

$R3 = 12.064 \cdot k\Omega$

CALCULATED VALUES FOR THE FIRST APPROACH

$$C2 := C1 \cdot \left(\frac{T2}{T1} - 1 \right) \qquad R2 := \frac{T2}{C2}$$

$C2 = 16.103 \cdot nF$ $\qquad R2 = 2.386 \cdot k\Omega$

CALCULATED VALUES FOR THE SECOND APPROACH

$$R2 := \frac{T2 - T1}{C1} \qquad C2 := \frac{T1}{R2}$$

$R2 = 17.291 \cdot k\Omega$ $\qquad C2 = 0.243 \cdot nF$

14. A Design for a High Voltage Tuner

Introduction

This paper investigates the design of a high voltage tuner. High voltage is considered to be any voltage that is higher than the Vp pin on the PLL can be used. This maximum rating is 6.5 Volts and is restricted because of process. However, it is sometimes desirable to have this voltage higher for wide band tuning applications or applications which have VCOs that require a higher tuning voltage for better phase noise performance. The insertion of any active device in the loop filter will introduce some noise. Vpp is used to signify the increased voltage, which can be up to 30 volts or possibly.

Circuit Topology

This design uses the Do pin and does not require ϕr and ϕp outputs on the PLL and is shown below:

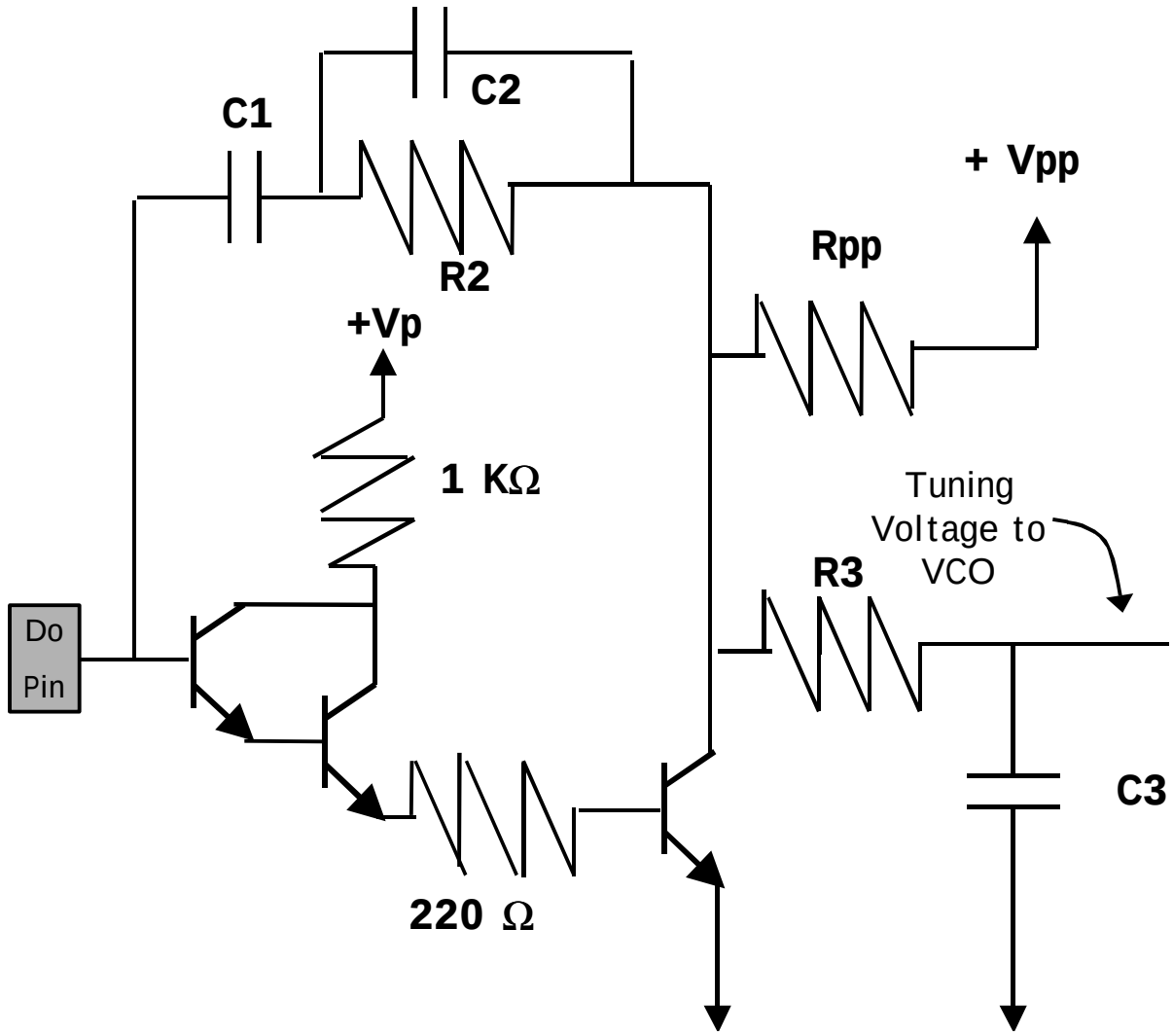


Figure 1 *Active Filter Topology*

The Expression for the Open Loop gain is given Below:

$$\boldsymbol{G(s) \bullet H(s) = \frac{-Kf \bullet Kvco \bullet (1 + s \bullet T1)}{w^2 \bullet N \bullet C1 \bullet (1 + s \bullet T2) \bullet (1 + s \bullet T3)}}$$

where

$T1 = (C1 + C2) \bullet R2$

$T2 = C2 \bullet R2$

$T3 = R3 \bullet C3$

Notice that this is the same as (20) in AN-1001 with the following substitutions:

T1 ==> ***T2*** T2 ==> ***T1*** T3 ==> ***T3***

Kvco = ***Kvco*** ● ***T1/T2*** ==> ***Kvco*** ● T2/T1

where the bold italicized figures represent the nomenclature used in AN-1001. Find the bold italicized symbol on the right side of each equation above in AN-1001. Then go substitute the left hand expression in. Note that this will give the correct results, but it is necessary to realized that the time constants have different definitions in terms of component values. So when the component values are solved for, one must use the definitions in this paper. By duality, using the same equations used in AN-1001, the following are derived:

$$T2 = \frac{\sec f - \tan f}{wp}$$

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2p \bullet Fref)^2}}$$

$$wc = \frac{\tan f \bullet (T2 + T3)}{[(T2 + T3)^2 + T2 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T2 + T3)^2 + T2 \bullet T3}{[\tan f \bullet (T2 + T3)]^2}} \right]$$

$$T1 = \frac{1}{wc^2 \bullet (T2 + T3)}$$

$$C1 = \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1 + wc^2 \bullet T1^2}{(1 + wc^2 \bullet T2^2) \bullet (1 + wc^2 \bullet T3^2)}}$$

$$C2 = \frac{T2}{T1 - T2} \bullet C1$$

$$R2 = \frac{T2}{C2}$$

$$C3 = \frac{C1}{10}$$

$$R3 = \frac{T3}{C3}$$

These completely determine the values, except for Rpp. It is not obvious what the function of this is. This is to provide extra current and may be dependent on the transistors used. For starters, try Rpp = 10 KΩ. Choosing Rpp too large will cause the circuit to be unstable and the carrier to dance around the frequency spectrum. Choosing Rpp small will cause excessive current consumption. Note that the high voltage, Vpp is grounded through the resistor Rpp.

The damping factor and natural frequency can be calculated as well:

$$wn = \sqrt{\frac{Kf \bullet Kvco}{N \bullet C1}} \qquad x = \frac{R2 \bullet (C1 + C2)}{2} \bullet \sqrt{\frac{Kf \bullet Kvco}{N \bullet C1}}$$

Conclusion

A design is given here for a high voltage tuner. Using the transistors as opposed to an op amp is done in order to reduce cost and the noise in the filter. By specifying the same parameters as done in a passive filter, all of the components can be determined. This design has been used less in practice and is less intuitive than some of the op amp designs. However, this circuit has been practically implemented. For the extra tinkering, this circuit allows a low cost and low noise solution.

High Voltage PLL DESIGN

USER NEEDS TO ENTER THESE:

$Kvco := 22 \cdot \frac{MHz}{volt}$ Enter the Tuning Constant Here

$K\phi := 5 \cdot mA$ Enter the Phase Detector gain do not divide by 2*π

$Fout := 2250 \cdot MHz$ RF output frequency.

$Fcomp := 1000 \cdot kHz$ Comparison Frequency

$Fc := 10 \cdot kHz$ Enter the True Loop Bandwidth in KHz.

$\phi p := 45 \cdot deg$ Phase margin. Default is 50 degrees.

$ATTEN := 5$ Reference spurious attenuation in dB added by R3 and C3.

$Vpp := 30 \cdot volt$

Enter the value of Vp Here

CALCULATIONS

$$N := \frac{Fout}{Fcomp}$$

$$\omega c := 2 \cdot \pi \cdot Fc$$

$$T3 := \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{2 \cdot \pi \cdot Fcomp}$$

$$T2 := \frac{\frac{1}{\cos(\phi p)} - \tan(\phi p)}{\omega c} - T3$$

$$Rp := \frac{Vp}{30 \cdot volt} \cdot 22 \cdot k\Omega$$

$$T1 := \frac{1}{(\omega c^2 \cdot (T2 + T3))}$$

$$C1 := \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \left[\frac{1 + \omega c^2 \cdot T1^2}{(1 + \omega c^2 \cdot T2^2) \cdot (1 + \omega c^2 \cdot T3^2)} \right]^{\frac{1}{2}}$$

$$C2 := C1 \cdot \frac{T2}{T1 - T2}$$

$$C3 := \frac{C1}{10}$$

$$R2 := \frac{T2}{C2}$$

$$R3 := \frac{T3}{C3}$$

DERIVED QUANTITIES

Parameters	Time Constants	Filter Poles	Filter Zero
$N = 2.25 \cdot 10^3$	$T2 = 6.358 \cdot 10^{-6} \cdot sec$	$\frac{1}{T2} = 1.573 \cdot 10^5 \cdot sec^{-1}$	
	$T3 = 2.34 \cdot 10^{-7} \cdot sec$	$\frac{1}{T3} = 4.273 \cdot 10^6 \cdot sec^{-1}$	
	$T1 = 3.842 \cdot 10^{-5} \cdot sec$		$\frac{1}{T1} = 2.603 \cdot 10^4 \cdot sec^{-1}$

CALCULATED VALUES:

$C1 = 3.005 \cdot 10^{4} \cdot pF$ $\quad C2 = 5.958 \cdot 10^{3} \cdot pF$ $\quad C3 = 3.005 \cdot 10^{3} \cdot pF$

$R2 = 1.067 \cdot k\Omega$ $\quad R3 = 0.078 \cdot k\Omega$ $\quad Rp = 22 \cdot k\Omega$

$K\phi := \frac{K\phi}{2 \cdot \pi}$ $\quad Kvco := 2 \cdot \pi \cdot Kvco$

$T2 := R2 \cdot C2$ $\quad T3 := R3 \cdot C3$

SIMULATION

Generates 5 decades from 10 Hz to 1 MHz

$j := 20 .. 120$

100 points

$f_j := 10^{\frac{j}{20}} \cdot Hz$

$S_j := 2 \cdot \pi \cdot f_j \cdot i$

S = iω

$$OL(S) := \frac{Kvco \cdot K\phi \cdot (1 + S_j \cdot T1)}{(S_j)^2 \cdot N \cdot C1 \cdot (1 + S_j \cdot T2) \cdot (1 + S_j \cdot T3)}$$

$$CL(S) := \frac{N \cdot OL(S)}{1 + OL(S)}$$

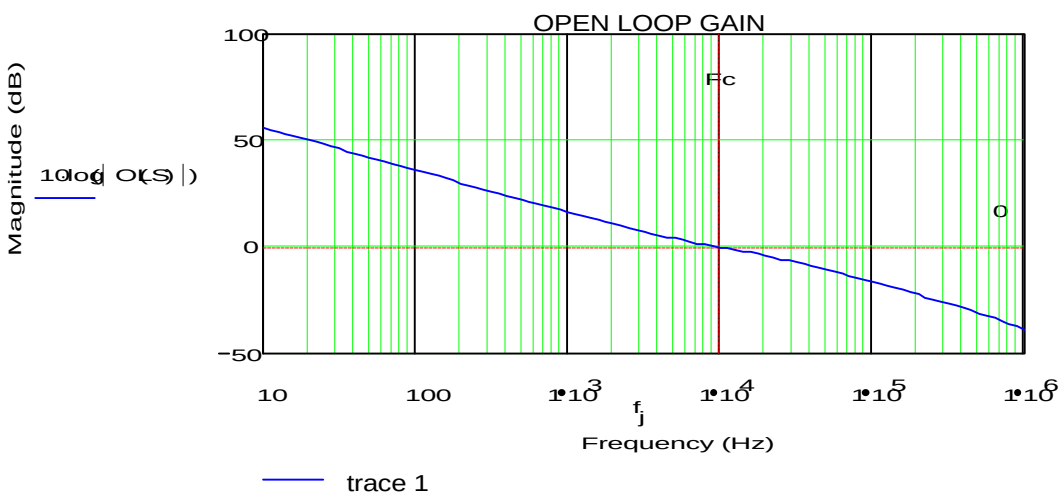
$$PM(S) := 180 - \left| \arg(OL(S)) \cdot \frac{180}{\pi} \right|$$

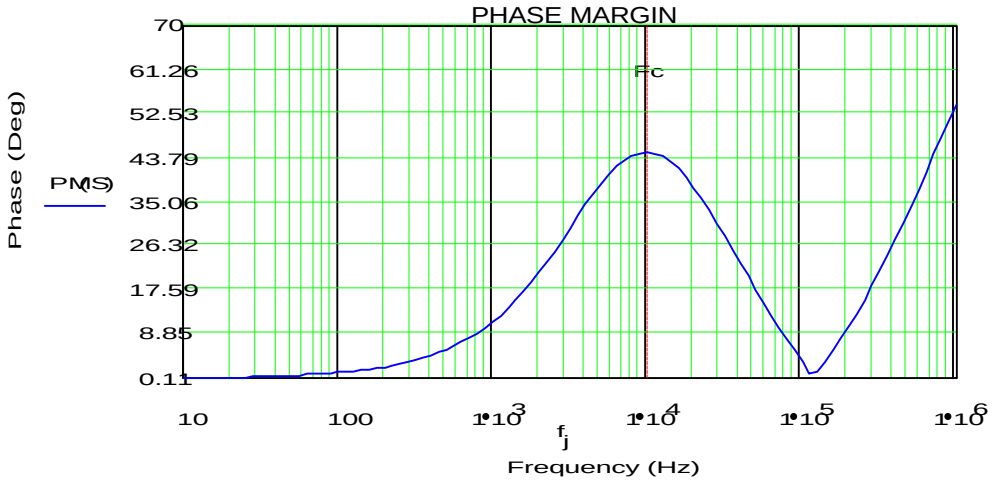
$$\omega n := \sqrt{\frac{K\phi \cdot Kvco}{N \cdot C1}}$$

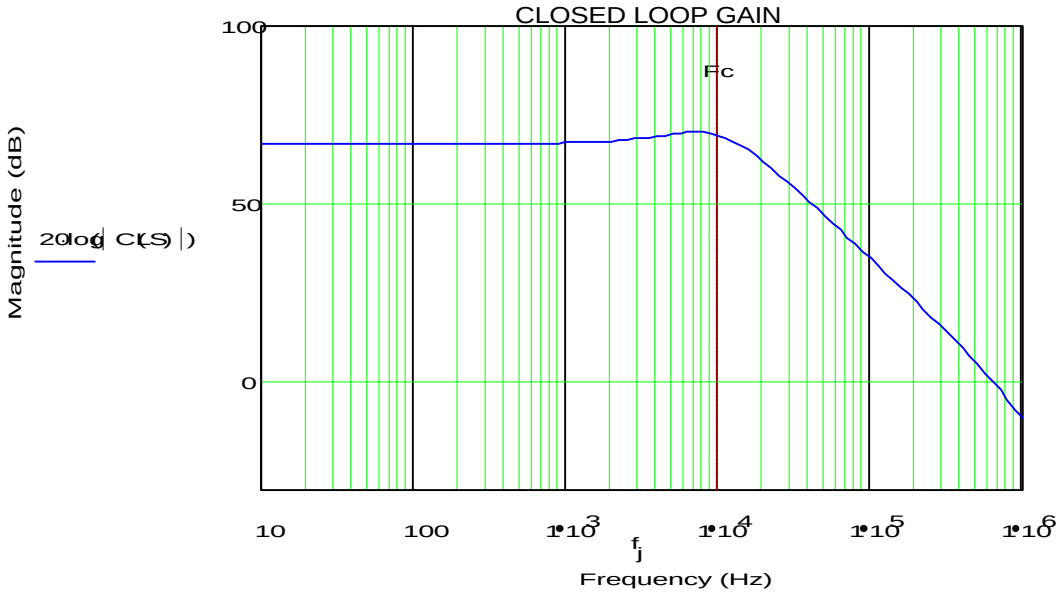
$$\zeta := \frac{R2 \cdot (C1 + C2)}{2} \cdot \omega n$$

Calculated Results

$\omega n = 4.034 \cdot 10^{4} \cdot sec^{-1}$ $\quad \zeta = 0.775$ $\quad Fc = 10 \cdot kHz$




PHASE MARGIN
Phase (Deg)
PM(S)
70
61.26
52.53
43.79
35.06
26.32
17.59
8.85
0.11
Fc
10
100
1·10^3
1·10^4
1·10^5
1·10^6
f_j
Frequency (Hz)


CLOSED LOOP GAIN
Magnitude (dB)
20log(|CL(S)|)
100
50
0
Fc
10
100
1·10^3
1·10^4
1·10^5
1·10^6
f_j
Frequency (Hz)

Supplemental Information

15. Lock Detect Circuit Construction and Analysis

Introduction

In many PLLs, including the LMX233X series from National Semiconductor, there is an analog lock detect pin, which does not put out a logic level signal to indicate whether or not the part is in lock. For this reason, external circuitry is necessary in order to make meaningful sense of this signal. This chapter discusses the design and simulation of such a circuit.

Using the LMX233X FoLD pin for lock detect

One of the possible functions of the FoLD pin is to give an output that can be used in conjunction with external circuitry in order to produce a steady signal that indicates whether or not the PLL is in lock. When the lock detect mode for the pin is selected, the FoLD pin outputs a signal which is high most of the time with narrow pulses which occur at a frequency equal to the reference rate. These pulses represent voltage inputs to the charge pump and are created by taking the OR function of the ϕ_r and the ϕ_p outputs of the PLL.

When the PLL is in the locked state, these pulses are on the order of 25-50 nS in width however this number can vary based on the VCO gain, loop filter transfer equations, phase detector gain, and other factors, although it should be constant for a given application.

When the PLL is not in the locked state, the average width of these pulses changes. The information about the PLL being out of the locked state is in no individual pulse, but rather in the average pulse width as calculated from a collection of pulses. For a ballpark estimate of how much the average width of the pulses will change and a rough idea on how sensitive the circuit is, the average change in the width of the pulses at any given time could be approximated by the difference in the periods of the N counter and the R counter. This result was discussed in a previous chapter concerning the performance of the phase detector. In other words,

$$Tlow - Tloc = \frac{1}{Fcomp} - \frac{N}{Fout} \tag{1}$$

LOCK DETECT CIRCUIT CONSTRUCTION

The basic strategy of the type of lock detect circuit described in this application note is to integrate over some number of reference periods in order to accumulate some DC value which can then be compared to a thresholding value at a comparator. Since the average DC contributions of the pulses are so small relative to the rest of the time, it may be necessary to use unbalanced time constants to maximize sensitivity. The recommended circuit is shown below.

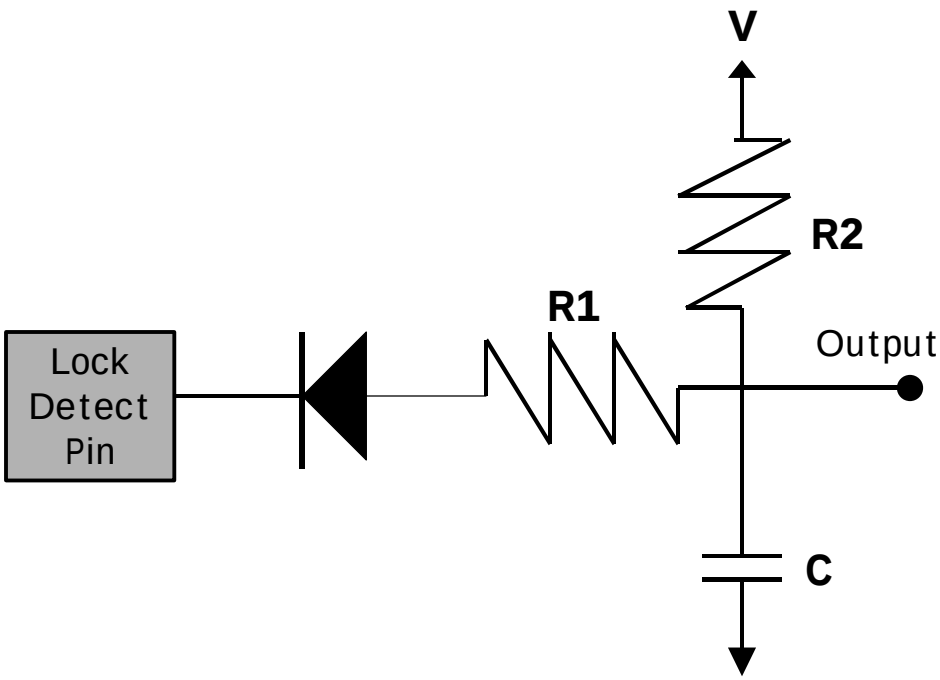


Figure 1 *Lock Detect Circuit*

Theoretical Operation of the Lock Detect Circuit

When the LD pin goes to its low voltage, Vol, then the diode will conduct, and if R2 >> R1 then the following holds:

$$V_{out} = R_1 \bullet C \bullet \frac{\P V_{out}}{\P t} \tag{2}$$

This has a solution of:

$$V_{n+1} = V_L + (V_n - V_L) \bullet b$$

$$\begin{aligned} &where \\ &V_{n+1} = voltage\, at\, the\, end\, of\ the\, low\, pulse \\ &V_n = voltage\, at\, the\, start\, of\ the\, low\, pulse \\ &V_L = V_D + V_{OL} \\ &V_D = voltage\, drop\, accross\, the\, diode \\ &V_{OL} = low\, voltage \\ &T_L = Time\, Duration\, of\ low\, pulse \\ &b = e^{-\frac{T_L}{R1 \bullet C}} \end{aligned} \tag{3}$$

Using a similar reasoning, the same analysis can be done when the LD output goes high:

$$
\begin{aligned}
&V_{n+1} = V + (V_n - V) \bullet a \\
&where \\
&V_{n+1} = voltage\ at\ the\ end\ of\ the\ high\ pulse \\
&V_n = voltage\ at\ the\ start\ of\ the\ high\ pulse \\
&T_H = Time\ Duration\ of\ low\ pulse \\
&a = e^{-\frac{T_H}{R2 \bullet C}}
\end{aligned}
\tag{4}
$$

Applying interative methods, after many cycles, the output of the signal will oscillate between V_{High} and V_{Low} . $V_{high} - V_{low}$ will be called ripple.

$$
\begin{aligned}
V_{High} &= V_L + \frac{(1-a) \bullet (V - V_L)}{1 - a \bullet b} \\
V_{Low} &= V + \frac{(1-b) \bullet (V_L - V)}{1 - a \bullet b}
\end{aligned}
\tag{5}
$$

Lock Detect Circuit Design

For design of the circuit, the following information is needed.

T_{lock} The width of the pulses in the locked condition. This should be around 25 nS for the 4X current mode and 50 nS for the 1X current mode.

T_{switch} The width of the LD pulses that are to be detected.

V_{high} The "trip point". In the unlocked condition, the maximum voltage output would be V_{high}. In the locked condition, the voltage output should be higher

Ripple $V_{high} - V_{low}$. This should be a couple hundred millivolts. Designing for too much ripple can cause a noise circuit, while designing for too little will cause the circuit to take longer to settle to it's final values of Vlow and Vhigh

Using the above expressions for V_{high} and V_{low} , the following equation can be derived.

$$a^2 \bullet A + a \bullet B + C = 0$$

where

$$A = K \bullet (V_L - V_{High})$$

$$B = V - V_{High} - K \bullet V_L + K \bullet V_{High}$$

$$C = V_{High} - V \qquad (6)$$

$$K = \frac{V - V_{low}}{V_{High} - V_{Low}}$$

$$a = \frac{-B + \sqrt{B^2 - 4 \bullet A \bullet C}}{2 \bullet A}$$

$$b = 1 + (a - 1) \bullet K$$

From these, C needs to be specified. Once C is specified, then the other components can be found

$$R1 = \frac{-T_L}{C \bullet \ln(b)}$$

$$R2 = R1 \bullet \frac{\ln a}{\ln b} \bullet \frac{T_H}{T_L} \qquad (7)$$

Voltages	***volts***	**Times**	***nS***	**Design Specification**	***volts***	
Vd	0.7	**T_L**	55	**High Trip Point**	2.1	
Vol	0.5	**T_H**	1600	**Ripple Voltage**	0.1	
V	4.1					
Constants		**Components**	***pF***	**Calculated Values**		
k	2.3333	**Choose C1**	220	**R1**	2.12	*KW*
a	-2.1			**R2**	149.1	*KW*
c	-2			**Low Trip Point**	2	Volts
α	0.9524					
β	0.8889					

Table 1 *Typical Lock Detect Circuit Design*

Note that after the design is done, it is necessary to assure that the lowest voltage in the locked state Vlow (lock) is higher than the highest state attained in the unlocked condition Vhigh(not locked).

Simulation

A simulation of this design is shown below. Note that it is also necessary to include lots of margin for error, since it is very difficult to get an accurate idea of the width of the LD pulses. Furthermore, as shown below, it does take time for the system to settle down to it's final state.

Par.	***Volts***	**Components**			**Times**	***nS***	**Const.**	***Volts***	**Locked Parameters**		
Vd	0.7	C	220	*pF*	T_L	55	α	0.9524	T_{lock}	25	nS
Vol	0.5	R1	2.1	*K W*	T_H	1600	β	0.8888	β_{lock}	0.9478	V
V	2.1	R2	149	*K W*							
Vstart	4.5										

Iter.	**Vhigh**	**Vlow**		**Iter.**	**Vhigh**	**Vlow**		**Locked Parameters**		
0	2.5000	2.3554	*Volts*	**8**	2.2051	2.0933	*Volts*	**Vhigh Final**	2.0996	*Volts*
1	2.4385	2.3007	*Volts*	**9**	2.1889	2.0789	*Volts*	**Vlow Final**	1.9995	*Volts*
2	2.3864	2.2545	*Volts*	**10**	2.1751	2.0667	*Volts*	**Ripple**	0.1001	*Volts*
3	2.3424	2.2153	*Volts*	**11**	2.1635	2.0564	*Volts*	**Vlock**	2.5451	*Volts*
4	2.3051	2.1822	*Volts*	**12**	2.1537	2.0476	*Volts*			
5	2.2735	2.1541	*Volts*	**13**	2.1454	2.0402	*Volts*			
6	2.2468	2.1304	*Volts*	**14**	2.1384	2.0340	*Volts*			
7	2.2242	2.1103	*Volts*	**15**	2.1324	2.0287	*Volts*			

Table 2 *Typical Lock Detect Circuit Simulation*

Conclusion

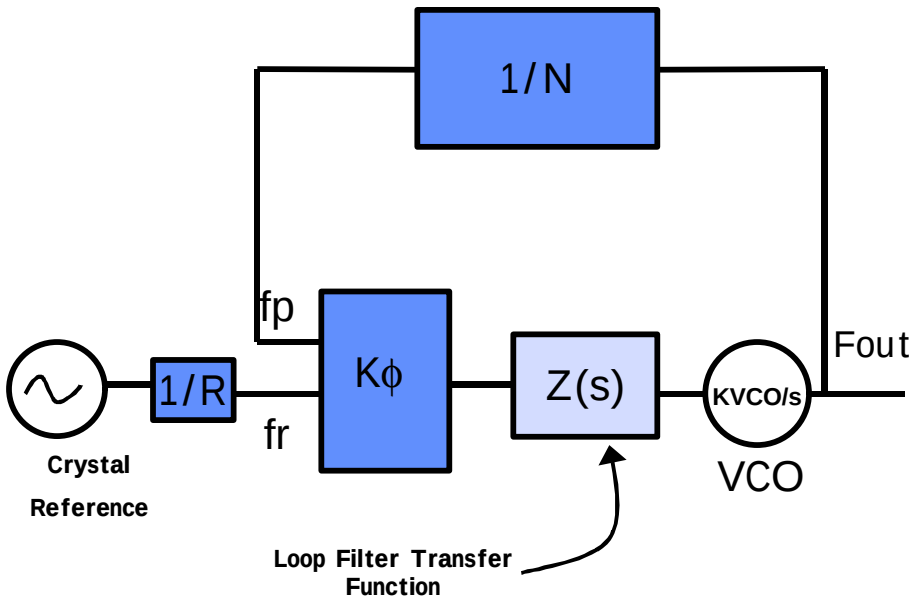
This paper has investigated some of the concepts behind a lock detect circuit design. It is necessary for the designer to have some sort of idea how much the width of the pulses are changing. After this is done the components are given. Note that there is a trade-off between the sensitivity of the circuit and the time it takes the circuit to respond, as seen in the simulation.

Note that some PLLs may come with a digital lock detect feature which makes this circuitry unnecessary. Also, some PLLs may come with an open drain type of output, which would not require the diode.

16. Other PLL Design and Performance Issues

Introduction

This is a collection of small topics not addressed in other sections. Included in this section is the N counter determination, relationship between phase margin and peaking counter sensitivity, and impedance matching.



What N Value Should One Design the Loop Filter For?

For a fixed output frequency, the choice of the N value is fixed, and therefore this is the value to design the loop filter for. However, typically this is not the case and the N counter value changes over a range.

Variation of Loop Bandwidth with N counter Value, VCO Gain, and Charge Pump Gain

Note that there is a factor of 1/s multiplying the VCO gain, which converts the VCO output from voltage to phase. There is also always a factor of 1/s in the transfer function of any passive loop filter discussed in this book. There are also poles and zeros in this transfer function. The poles should be much greater than the loop bandwidth, and therefore really do not have a large contribution at the frequency equal to the loop bandwidth. There is also a zero in the transfer function and this zero does have some contribution near the loop bandwidth, but this contribution usually small relative to the $1/s^2$ term that comes from taking the 1/s from the transfer function and multiplying this by the 1/s from the VCO gain. From this, it can be concluded that the loop bandwidth is roughly inversely proportional to the square root of the N value. It can be also concluded that the loop bandwidth is roughly proportional square root of the VCO gain and also proportional to the square root of the Charge Pump Gain. It may seem at first that disregarding the poles and zeros of the filter seems like a bold assumption, but simulation and actual testing show that it is not that rough of an assumption. To summarize these results:

$$\frac{wc2}{wc1} = \sqrt{\frac{Kf2}{Kf1}} \bullet \sqrt{\frac{Kvco2}{Kvco1}} \bullet \sqrt{\frac{N1}{N2}}$$

N Value to Use for Loop Filer Design

From the above equation, it can be seen that it is roughly true that the loop bandwidth is inversely proportional to the square root of the N value, so it therefore follows that designing the N value for the geometric mean of the minimum and maximum values minimizes the variation of the loop bandwidth of the PLL from the value for which it was designed. In summary, design for:

$$N = \sqrt{N\,min \bullet N\,max}$$

Relationship Between Phase Margin and Peaking in the Filter Response

The phase margin is related to the stability of the system and a higher phase margin implies more stability. This can be seen by looking at the roots of the closed loop transfer function and tracking how negative the real parts of these roots are. The specific details on this are beyond the scope of this text. On the spectrum analyzer, if the phase margin is very low, then the loop filter response will show a peaking. This section explains why.

Recall that the closed loop transfer function is of the form:

$$T(s) = \frac{G(s)}{1 + G(s) \bullet H}$$

Of special interest is at the point where the magnitude of G(s)● H = 1. The frequency that makes this true is the loop bandwidth. Also of interest is the phase. If this phase is 180 degrees, then the transfer function would have an infinite value, and thus the most peaking. If the phase was zero degrees, then there would be a minimal amount of peaking. Phase margin is therefore defined as the amount of margin on the phase which would be 180 degrees minus the phase of G(j● ωc)● H. Zero degrees phase margin is absolute instability, and 180 degrees phase margin is absolute stability. In practice, loop filters with less than 20 degrees phase margin are likely to show instability problems and filters above 80 degrees phase margin have yield components that unrealistic because they are too large, or are negative.

On the Pitfalls of Sensitivity

Sensitivity is a feature of real world PLLs. The N counter will actually miscount if too little or too much power is applied to the high frequency input. There are limits on this power level, and these limits are referred to as the sensitivity. The sensitivity changes as a function of frequency. At the higher frequencies, the curve degrades because the of process limitations, and at the lower frequencies, the curve can also degrade because of problems of the counters making thresholding decisions (the edge rate of the signal is too slow). At the lower frequencies, this limitation can be addressed by running a square wave instead of a sine wave into the high frequency input of the PLL. Sensitivity can also change from part to part, over voltage, or over temperature. When the power level of the high frequency input approaches sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to this limit, or exceeds it, then the PLL loses lock.

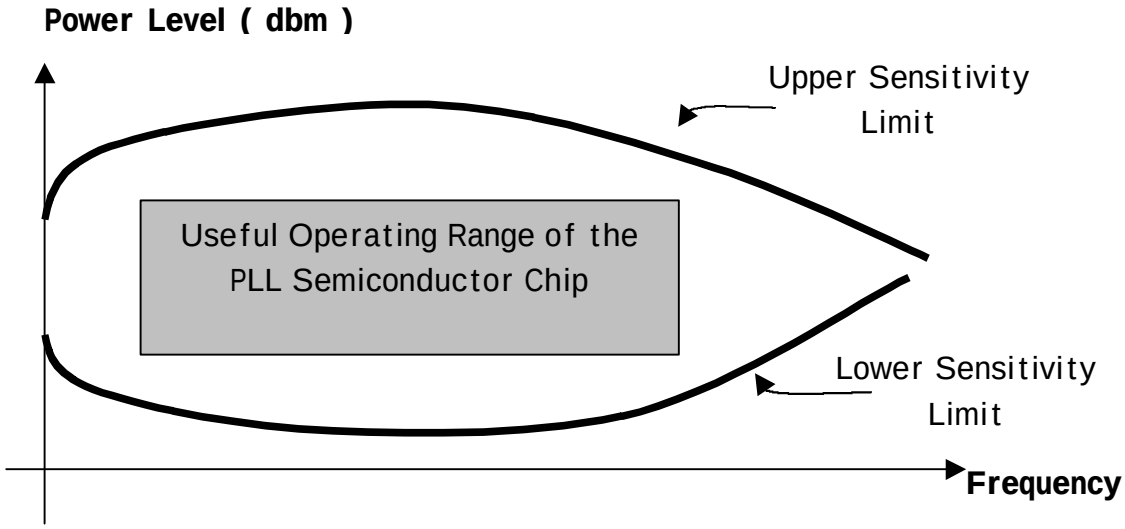


Figure 1 *Typical Sensitivity Curve for a PLL*

The sensitivity curve is usually not flat vs. frequency and it is relevant to consider what this is for the VCO harmonics as well as the fundamental. This can especially be an issue when a part designed for a very high operating frequency is used at a very low operating frequency. Unexpected sensitivity problems can also come into play when there is poor matching to the high frequency input of the PLL.

Although sensitivity issues are most common with the N counter because it usually involves the higher frequency input, these same concepts apply to the R counter as well.

Impedance Matching

This section is not intended to be an overview of impedance matching, but rather is included to alert the reader of impedance matching issues. In most instances, impedance matching is usually not an issue, but it can be in others. Although most test equipment has an input impedance of 50 Ω, this is not typical of most PLLs, and assuming this can give rise to a lot of problems. The input impedance of most PLLs is typically capacitive and also changes as a function of the frequency as well. There are many ways to match this impedance, and one way is to put a series inductance to the high frequency input of the PLL semiconductor ship such that it has a reactance equal to the negative reactance of the PLL at the desired frequency. This method also causes the impedance for the higher VCO harmonics to be poorly matched, which is desirable.

Conclusion and Author's Parting Remarks

This chapter has addressed some of the issues not addressed in other chapters. This book has not discussed everything there is to say about the PLL, but should give the reader a solid foundation which is based on mathematical models and tested data. It was the intention of this book to provide the reader with enough information to deal with both the hows as well as the whys of PLL design. The data in this book was all gathered from various National Semiconductor Synthesizer chips, which include the R counter, N counter, charge pump, and phase-frequency detector.

17. Glossary

ATTEN
The attenuation index, which is intended to give an idea of the spurious attenuation added by the components R3 and C3 in the loop filter.

Charge Pump
Used in conjunction with the phase-frequency detector, this device outputs a current of constant amplitude, but variable polarity and duty cycle. It is usually modeled as a device that outputs a steady current of value equal to the time-averaged value of the output current.

Closed Loop Transfer Function , C(s) (see figure 3)
This is given by $\frac{G(s)}{1+G(s)\bullet H}$, where H= $\frac{1}{N}$ and G(s) is the Open Loop Transfer Function

Comparison Frequency, Fcomp (see figure 1)
The crystal reference frequency divided by R. This is also sometimes called the reference frequency.

Control Voltage , Vtune (see figure 1)
The voltage that controls the frequency output of a VCO.

Crystal Reference, Xtal (see figure 1)
A stable and accurate frequency that is used for a reference.

Damping Factor (ζ) (see figure 5)
For a second order transient response, this determines the shape of the exponential envelope that multiplies the frequency ringing.

Dead Zone
This is a property of the phase frequency detector caused by component delays. Since the components making up the PFD have a non-zero delay time, this causes the phase detector to be insensitive to very small phase errors.

Dead Zone Elimination Circuitry
This circuitry can be added to the phase detector to avoid having it operating in the dead zone. This usually works by causing the charge pump to always come on for some minimum amount of time.

Frequency Jump, Fj (see figure 5)
When discussing the transient response of the PLL, this refers to the frequency difference between the frequency the PLL is initially at, and the final target frequency.

Frequency Synthesizer
This is a PLL which has a high frequency divider (N divider), which can be used to synthesize a wide variety of signals

Locked PLL
A PLL such that the output frequency divided by N is equal to the comparison frequency within acceptable tolerances.

Lock Time **(see figure 5)**
The time it takes for a PLL to switch from an initial frequency to a final frequency for a given frequency jump to within a given tolerance.

Loop Bandwidth , ωc or ωp **(see figures 2,3, and 4)**
The frequency at which the magnitude of the open loop transfer function is equal to 1. ωc is intended to be the true loop bandwidth, while ωp is an mathematical approximation to ωc.

Loop Filter
A low pass filter that takes the output currents of the charge pump and turns them into a voltage, used as the tuning voltage for the VCO. Z(s) is often used to represent the impedance of this function. Although not perfectly accurate, some like to view the loop filter as an integrator.

Modulation Domain Analyzer **(see figure 5)**
A piece of RF equipment that displays the frequency vs. time of an input signal.

Modulation Index , β
This is in reference to a sinusoidally modulated RF signal. The formula is given below, where F(t) stands for the frequency of the signal.

$$F(t) = const. + F_{dev} \bullet cos(w_m \bullet t)$$

$$b = \frac{F_{dev}}{w_m}$$

Natural Frequency , ωn **(see figure 5)**
For a second order transient response, this is the frequency of the ringing of the frequency response.

Open Loop Transfer Function , G(s) **(see figure 2)**
The transfer function which is obtained by taking the product of the VCO Gain, Charge Pump Gain (This includes the Phase Detector Gain) and Loop Filter Impedance divided by N.

$$G(s) = \frac{Kf \bullet Kvco \bullet Z(s)}{N \bullet s}$$

Overshoot **(see figure 5)**
For the second order transient response, this is the amount that the target frequency is initially exceeded before it finally settles in to the proper frequency

Phase Detector, Kϕ **(see figure 1)**
A device that produces an output signal that is proportional to the phase difference of its two inputs.

Phase-Frequency Detector, Kϕ **(see figure 1)**
Very similar to a phase detector, but it also produces an output signal that is proportional to the frequency error as well.

Phased Locked Loop (PLL) **(see figure 1)**
A circuit that uses feedback control to produce an output frequency from a fixed crystal reference frequency. Note that a PLL does not necessarily have an N divider. In the case that it does, it is referred to as a frequency synthesizer, which is the subject of this book.

Phase Margin (ϕp or ϕc)
180 degrees minus phase of the open loop transfer function at the loop bandwidth. The phase margin is usually between 30 and 70 degrees. Lower phase margin designs tend to be less stable and show peaking in the closed loop transfer function. Designs with excessively high phase margin have slower lock times. The formula is given below:

$$fc = 180 - \angle C(j \bullet wc)$$

Phase Noise **(see figure 4)**
This is noise on the output phase of the PLL. Since phase and frequency are related, it is visible on a spectrum analyzer. Within the loop bandwidth, the PLL is the dominant noise source. The metric used is dbc/Hz (decibel relative to the carrier per Hz). This is typically normalized to a 1 Hz bandwidth by subtracting 10*(Resolution Bandwidth) of the spectrum analyzer.

Phase Noise Floor
This is the phase noise minus 20 times the log of the N value. Note that this is generally not a constant because it tends to be dominated by the charge pump, which gets noisier at higher comparison frequencies.

Prescaler
Since the output of the PLL tends to be high frequency, it requires a high frequency process. However, it is not feasible to make the whole PLL chip out of this high frequency process, so only the high frequency part is made this way. This is actually part of the architecture inside of the N divider.
Single Modulus Prescaler
This is a single high frequency divider placed in front of a counter. In this case, N = M*P, where M can be changed and P is fixed. Note that for this type of prescaler, frequency resolution is sacrificed.
Dual Modulus Prescaler **(see diagram 6)**
In order not to sacrifice frequency resolution, a dual modulus prescaler is used. These come in the form P/(P+1). For instance, a 32/33 prescaler has P = 32. At first a fixed prescaler of size P+1 (which is actually a prescaler of size P with a pulse swallow circuit) and uses this for a total of A cycles. This takes a total of A*(P+1) cycles. There is also a B counter that is counting all of the time. Since it started with B counts, the remaining counts would be (B-A). The size P prescaler is then switched in. This takes (B-A)*P counts to finish up the count, at which time, all of the counters are reset, and the process is repeated. Notice that B>=A, in order for proper operation, otherwise the B counter would prematurely reach zero and reset the system. N values that yield B<A are called illegal divide ratios. From this we get the fundamental equations:

$$N = (P+1) \bullet A + P \bullet (B - A) = \quad P \bullet B + A$$

$$B = N \ trunc \ P \quad \left(N \ divided \ by \ P, \ chop \ of \ the \ remaider\right)$$

$$A = N \ mod \ P \quad (\ The \ remainder \ when \ N \ is \ divided \ by \ P \ )$$

B>=A is a requirement for a legal divide ratio.

Note that this prescaler gains the better resolution at the cost of not being able to synthesize all N values.

Triple Modulus and Quad Modulus Prescalers

These use a similar concept as the dual modulus prescaler, except more than two prescalers are used. The advantage of these types of prescalers is that they have less illegal divide ratios.

N Divider **(see figure 1)**

A divider that divides the high frequency (and phase) output by a factor of N.

R Divider **(see figure 1)**

A divider that divides the crystal reference frequency (and phase) by a factor of R.

Reference Spurs

Undesired frequency spikes on the output of the PLL caused by leakage currents and mismatch of the charge pump that FM modulate the VCO tuning voltage.

Resolution Bandwidth , RBW

See definition for Spectrum Analyzer.

Sensitivity

Power limitations to the high frequency input of the PLL chip (from the VCO). At these limits, the counters start miscounting the frequency and do not divide correctly.

Spectrum Analyzer, SA **(see figure 4)**

A piece of RF equipment that displays the power vs. frequency for an input signal. This piece of equipment works by taking a frequency ramp function and mixing it with the input frequency signal. The output of the mixer is filtered with a bandpass filter which has a bandwidth equal to the resolution bandwidth. The narrower the bandwidth of this filter, the less noise that is let through.

Spurious Attenuation **(see figure 3)**

This refers to the degree to which the loop filter attenuates the reference spurs. This can be seen in the closed loop transfer function.

Temperature Compensated Crystal Oscillator (TCXO)

A crystal that is temperature compensated for improved frequency accuracy

Tolerance (tol) **(see figure 5)**

The acceptable frequency error to within which the PLL is considered locked.

Voltage Controlled Oscillator (VCO) **(see figure 1)**

A device that produces an output frequency that is dependent on an input (Control) voltage.

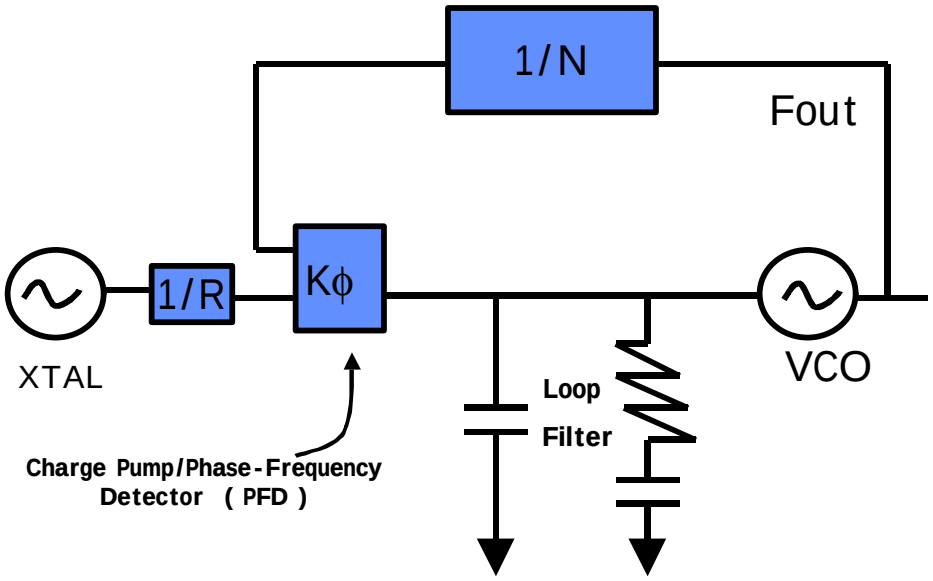


Figure 1 *Basic PLL (Frequency Synthesizer) Diagram*

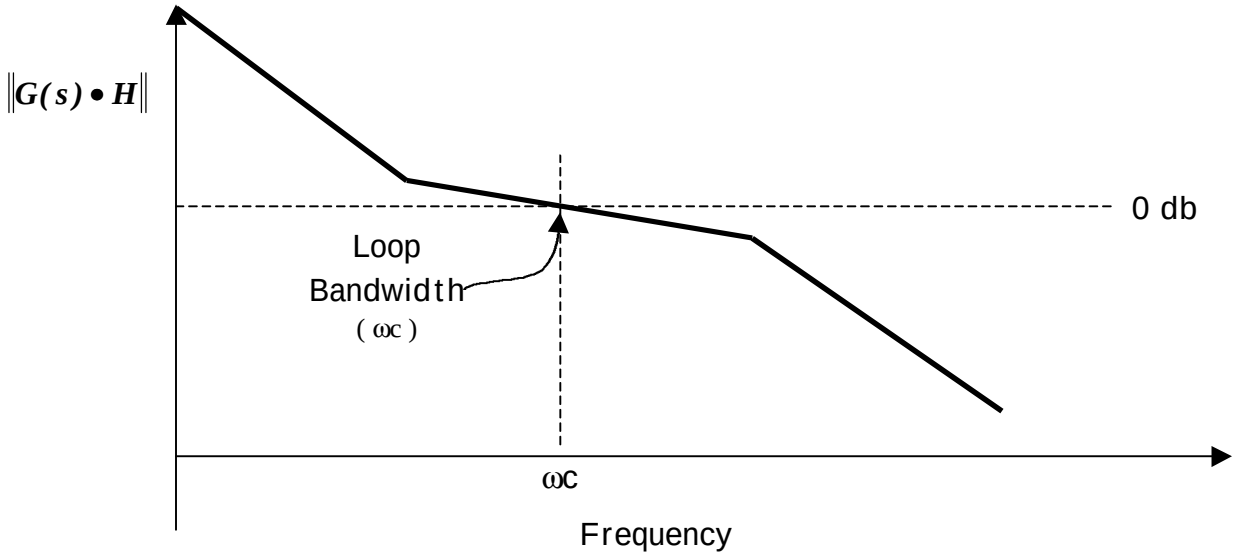


Figure 2 *Open Loop Response of a PLL*

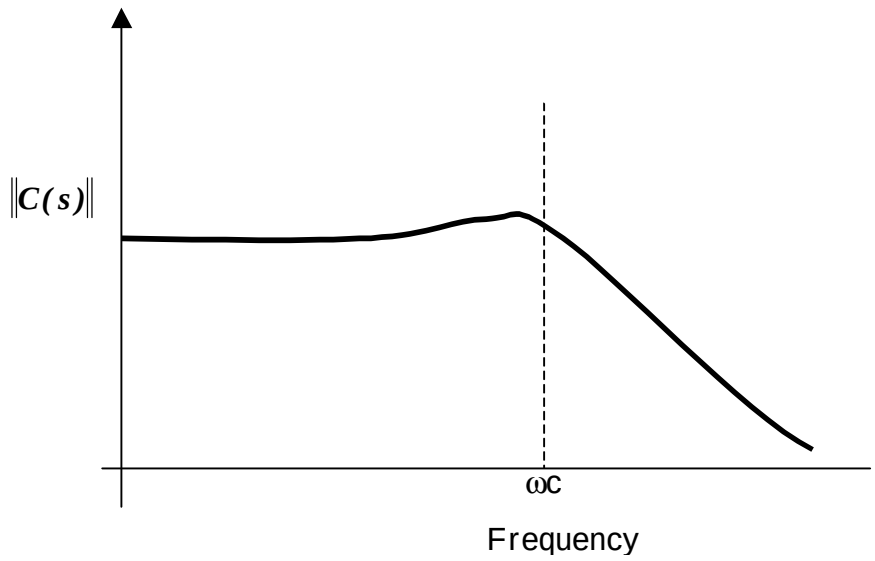


Figure 3 *Typical Closed Loop Transfer Function for a PLL*

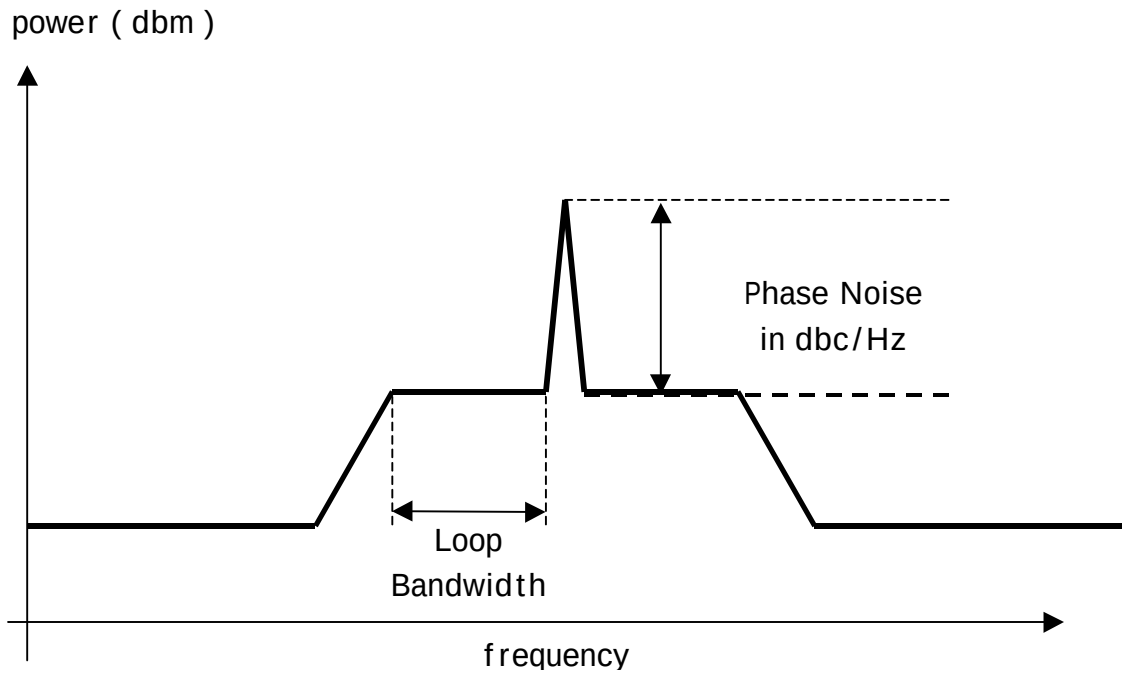


Figure 4 *Typical Phase Noise Spectral Plot for a PLL*

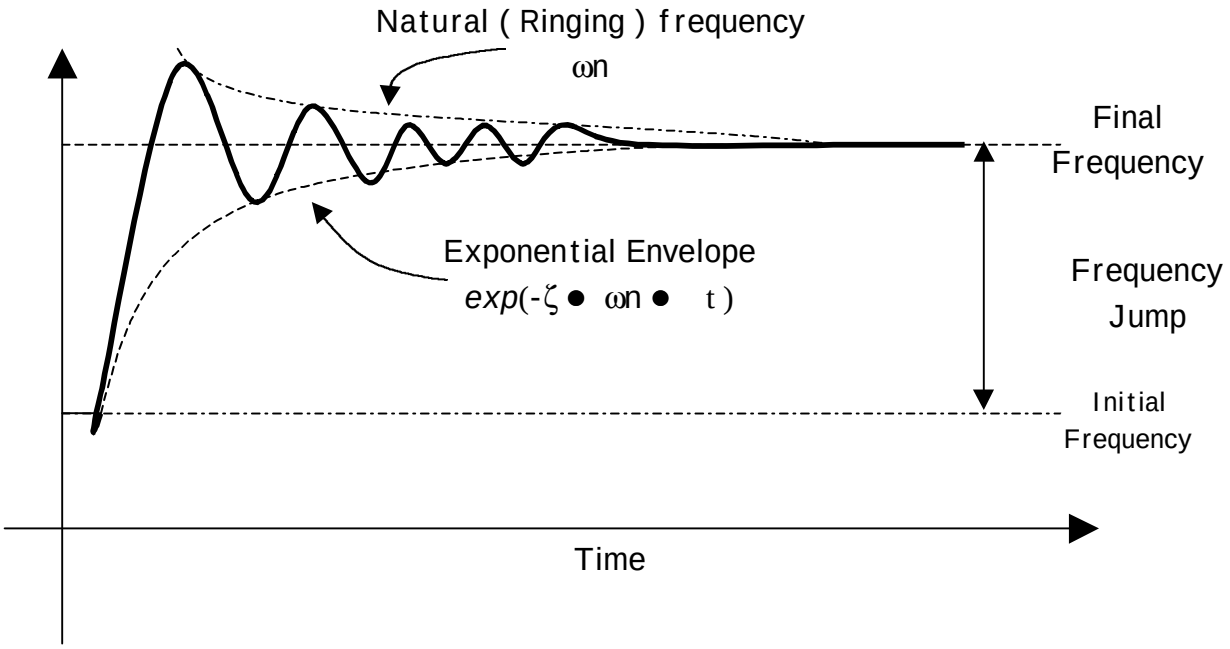


Figure 5 *Typical Transient Response of a PLL*

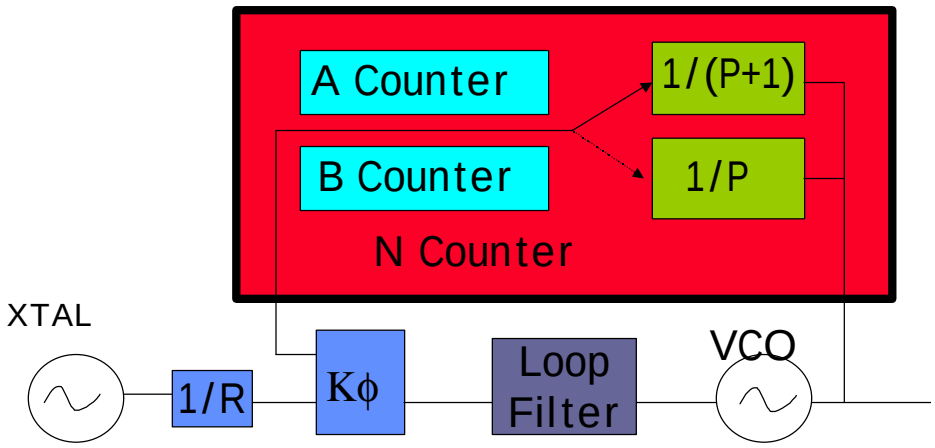


Figure 6 *Dual Modulus Prescaler*