Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs

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Abstract

We fabricated and characterized new ambipolar silicon nanowire (SiNW) FET transistors featuring two independent gate-all-around electrodes and vertically stacked SiNW channels. One gate electrode enables dynamic configuration of the device polarity (*n* or *p*-type), while the other switches *on*/*off* the device. Measurement results on silicon show $I_{on}/I_{off} > 10^6$ and $S \approx 64$mV/dec (70mV/dec) for *p*(*n*)-type operation in the same device. We show that XOR operation is embedded in the device characteristic, and we demonstrate for the first time a fully functional 2-transistor XOR gate.

Introduction

Ambipolar conduction is observable in several nanoscale FET devices (45nm node and below), built using silicon (1,2), carbon nanotubes (3) and graphene (4). Specifically, the trend towards devices with intrinsic channels at the 22nm node and below makes this phenomenon a potential limitation for circuit design. Whereas ambipolarity is often suppressed by processing steps, this feature can be exploited to enhance logic functionality. We fabricate vertically stacked *Double Gate* (DG) *Silicon Nanowire* (SiNW) FETs, featuring two *Gate-All-Around* (GAA) electrodes (Fig. 1). Vertically stacked GAA SiNWs represent a natural evolution of FinFET structures, providing the best geometry for electrostatic control over the channel and consequently superior scalability properties (5,6).

In our device, one gate electrode, the *Control Gate* (CG) acts conventionally by switching *on* and *off* the device. The other electrode, the *Polarity Gate* (PG), acts on the side regions of the channel, in proximity of the *Source/Drain* (S/D) Schottky junctions, switching the device polarity dynamically between *n* and *p*-type (Fig. 4). The applied voltage ranges for the PG and CG are comparable. Digital circuits using these transistors can therefore exploit both gates as logic inputs, enabling the design of compact cells that implement XOR more efficiently than in CMOS (7).

The top-down approach used in this work distinguishes it from previous art (1,3,8) as it enables large-scale fabrication of arrays of vertical stacks of nanowires, without requiring complex transfer procedures of pre-grown nanowires on a final substrate. The fabricated devices show great potential in terms of logic design due to their intrinsic high logic expressive power. Recent works (7,9) demonstrate that logic design using ambipolar DG devices requires fewer resources than conventional CMOS. Moreover, implementation of sea-of-gate architectures with DG SiNW devices (10) can reduce fabrication costs by providing efficient circuit implementations and maintaining a high level of regularity in circuit layouts.

In the following, we present both device fabrication and characterization on silicon and extensive TCAD modeling and simulation.

Device fabrication

The devices are fabricated in a top-down fashion, exploiting a single *Deep Reactive Ion Etching* (DRIE) Bosch process step (11) to form device channels. The channels consist of 350nm long vertical stacks of 4 nanowires on a slightly *p*-doped ($\sim 10^{15}$atoms/cm^{-3}) SOI substrate.

E-beam lithography is used to create 350nm long and 60nm wide HSQ patterns to fabricate the nanowires with a single Bosch DRIE procedure. Gate oxide (~8nm) is then formed by self-limiting oxidation of the nanowires followed by a conformal polysilicon layer deposition. Then the polarity gate is patterned all-around the nanowires after e-beam lithography (Fig. 2(a)). Hence, a second oxidation and polysilicon deposition is performed. The CG structure is self-aligned to the PG (Fig. 2(b)). As a result, three gated regions are obtained, each of 100÷120nm in length and electrically isolated by the CG gate oxidation (about 8nm thick).

After the formation of the gates, silicon nitride spacers are patterned to isolate the structures. A nickel layer is deposited by evaporation and annealing (20'@200°C + 20'@300°C + 20'@400°C) is performed to produce NiSi at the S/D and gate contacts. NiSi is ideal as it features a near midgap workfunc-

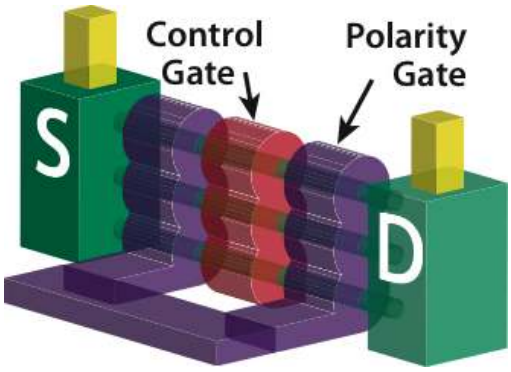

Fig. 1: Conceptual drawing of the SiNWFET. S/D pillars (green) support a vertical stack of nanowires. The nanowires are surrounded by the GAA Polarity Gate (violet) and GAA Control Gate (red).

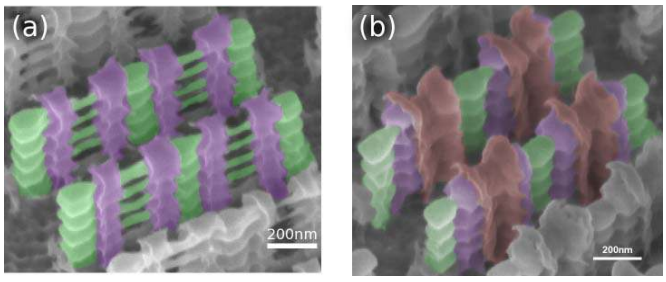

Fig. 2: Tilted SEM views of an array of fabricated devices (a) before creation of the control gates and (b) after addition of the polarity gates. S/D pillars and nanowires (green), PG (violet) and CG (red) are shown.

tion with respect to silicon. Unreacted nickel is removed by selective wet etching in hot piranha solution.
SEM images at different fabrication steps are provided in Fig. 2. In order to produce a more compact layout, in this case devices are coupled together, with the central pillar supporting a nanowire stack on both sides. Fig. 3 shows cross sections of the nanowire stacks surrounded by a polysilicon gate. Nanowire diameters below 20nm are shown.

Device characterization

Polarity control by means of the PG is illustrated in Fig. 4 and Fig. 5. Linear and semi-logarithmic plots of the same device are provided at different PG biases. Fig. 6 presents a conceptual band diagram showing the carriers involved in device operation at different CG and PG biases. A positive PG bias allows electrons to create a current through the device, while low PG bias makes holes become the majority carriers. In Fig. 6, band bending at the S/D contacts is shown for weakly *p*-doped silicon nanowires. Subthreshold slopes of 64mV/dec and 70mV/dec are obtained, respectively, for the *p*-type and *n*-type conduction branches in the same device. Moreover, I_{on}/I_{off} values range from 10^6 to 10^7 respectively for the *p*-type and *n*-type conduction branches still in the same device.
Hence, Schottky contact barrier height extraction is performed on the device of Fig. 4 using the activation energy approach. This approach is still one of the most used, both for its accuracy and for its independence from the electrically active area. In Fig. 7, some of the experimental I_{ds} current measurements at different temperatures are shown. The linear decreasing slope of the Arrhenius plot in Fig. 8, fitted within 5% error in experimental data with a measured ideality factor η=1.84, indicates thermionic emission regime. Near-midgap Schottky ($q\Phi_{Bp}$) barrier height of 0.45eV is observed, confirming that the type of silicide is compatible with the expected NiSi, whose barrier height value on *p*-Si is ~0.4eV. This value is consistent both with literature (12,13) and simulation results, as shown in Fig. 10. In the inset of Fig. 8, the energy-band diagram of metal-*p*-type semiconductor junction at thermal equilibrium is represented, showing the $q\Phi_{Bp}$ barrier.
Compared to previous art (2,3,8), our device shows excellent I_{on}/I_{off} and subthreshold slope characteristics, combined with a high degree of symmetry between the *n* and *p* conduction

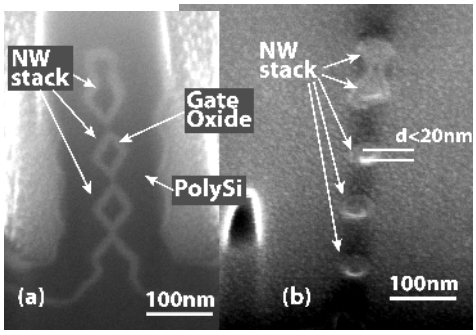

Fig. 3: SEM/FIB cross-sections of fabricated devices, showing (a) the nanowire stack with 10-nm gate oxide and 50nm thick conformal polysilicon GAA structure; and (b) optimized d < 20nm stacked nanowires.

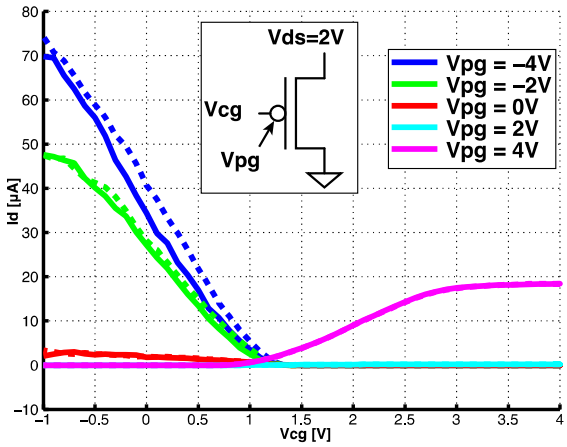

Fig. 4: Linear plot of a measured device. The device connections are shown in the inset. *n* and *p*-type conduction is selected by different Vpg biases. Currents in the *p*-type and *n*-type branch are comparable. Asymmetry is due to the non-perfectly midgap contact workfunction.

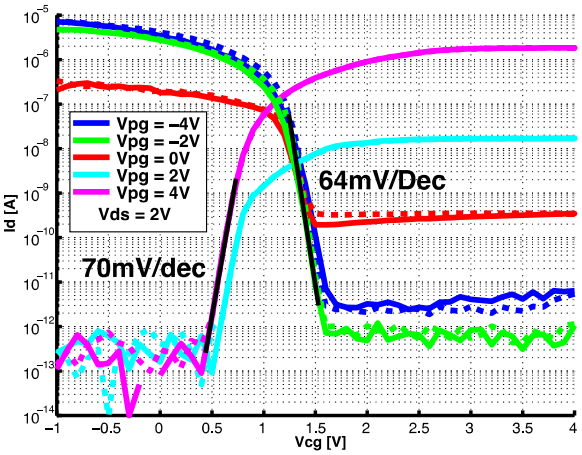

Fig. 5: Logarithmic plot for the same device conditions of Fig. 4. Both *n* and *p*-type device branches show subthreshold slopes S ≤ 70mV/dec. Ion/Ioff ratios of ≈10^7 (≈10^6) are obtained respectively for the *n*-type (*p*-type) conduction branches.

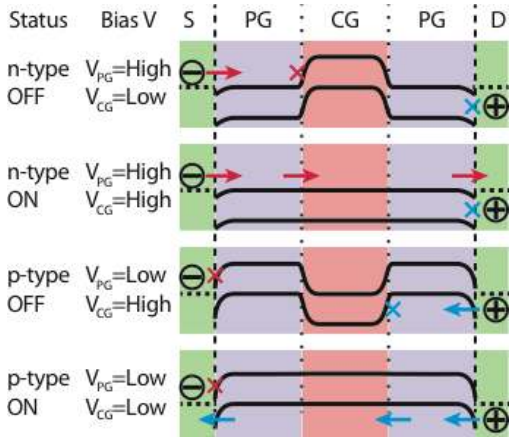

Fig. 6: Conceptual band diagrams for the ambipolar double gate device. Four cases are shown, describing the four combinations of high/low bias for the polarity gate and control gate of the device. Electron paths are shown with red arrows/crosses, hole paths are shown with blue arrows/crosses.

branches. Moreover, the device shows a normally *p*-type *on* state, when $V_{pg} = V_{cg} = 0V$. This is due to the alignment of the S/D metal workfunction to the conduction band of the SiNWs, as shown in the bottom case of Fig. 6, and is achieved using weakly *p*-doped nanowires. As described in the following sections, this feature enables fabrication of cascadable logic gates.

Device simulation

In order to perform predictions in terms of circuit design and device performance, we used a two-step simulation approach. We first built a TCAD model of the fabricated device, fitting this model with experimental results and data from Schottky barrier height extraction. Fig. 10 shows a fitted characteristic of an experimental device. In the second phase, we built an optimized model by scaling dimensions and introducing technological adjustments to the device structure. The optimized structure, including high-κ gate dielectric, metal gates with midgap workfunction and 45nm gate regions, is shown in Fig. 9. Schottky barrier height $q\Phi_{Bp}$ for electrons is fixed at 0.41eV at both source and drain junctions. The I-V characteristics of the optimized device are shown in Fig. 11, obtained with hydrodynamic transport and quantization models. Tunneling masses for electrons and holes are set to $0.19m_0$ and $0.16m_0$ respectively, consistent with theory and measurement fitting.

Logic circuit demonstration and simulation

Exploiting dynamic polarity control, reconfigurable logic gates (9) with high expressive logic capability (7) can be implemented with these devices. In particular, Fig. 12 presents the possible configurations of a logic gate comprising a single transistor in the *pull-down* network (Fig. 12(b)) or its complementary logic equivalents (Fig. 12(c,d)). Fig. 12(e-g) shows how the gate can behave as an inverter (buffer), when the *pull-down* transistor is set as *n*-type (*p*-type). A measured inverter operation is shown in Fig. 13. Finally, the gate can be used as an XOR gate when the PG is biased as a logic input. Note that multi-level static logic synthesis requires PG and CG input biases to be compatible with V_{dd}, i.e., all voltages ranging between 0V and V_{dd}. Fig. 14 shows a measured complementary gate exhibiting this feature. In this case, the output characteristic of the buffer branch is highly degraded; this is due to the presence of the poorly polarized *n*-type FET in the *pull-up* network and the *p*-type FET in the *pull-down* network. In this early measurement, the inverter characteristic does not reach 0V due to the *pull-up* transistor not turning off completely. Nonetheless, control and polarity gate input voltages both range from 0V to $V_{dd} = 1V$, making this gate fully functional for implementing multi-level static logic. Using pairs of transistors with opposite polarities, as shown in Fig. 12(d), will restore the degraded output characteristic of the measurement of Fig. 14.
From the device model described in Fig. 9, we performed simulations, shown in Figs. 15-17, demonstrating a 47GHz ring oscillator and full swing XOR operation using the 4-transistor schematic of Fig. 12(d). In particular, in Fig. 16 we show a simulation of the circuit of Fig. 12(d), which presents full swing in the inverter configuration and good agreement to the measured circuit.

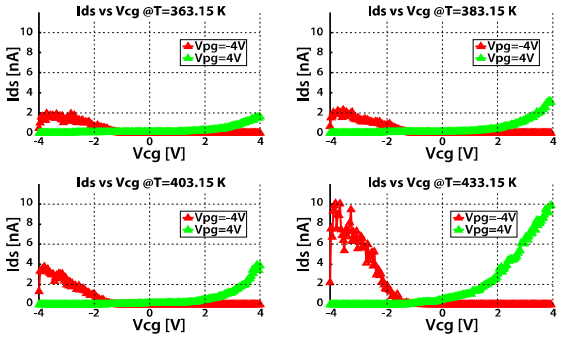

Fig. 7: A selection of the performed measurements at different temperatures, used for Schottky barrier height extraction, at Vds=100mV. Quasi-symmetric device operation is observable.

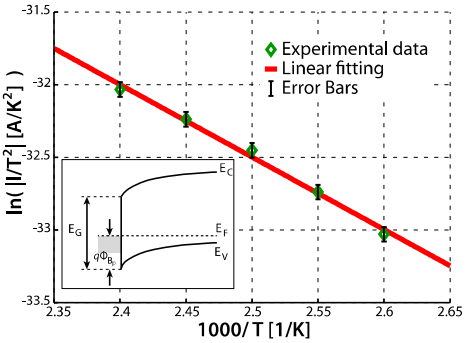

Fig. 8: Arrhenius plot extracted from measurements, some of which are represented in Fig. 10.

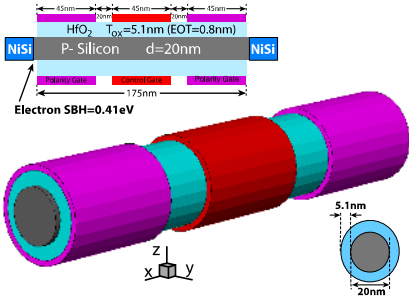

Fig. 9: Structure of the optimized ambipolar Silicon Nanowire device used for simulation with TCAD.

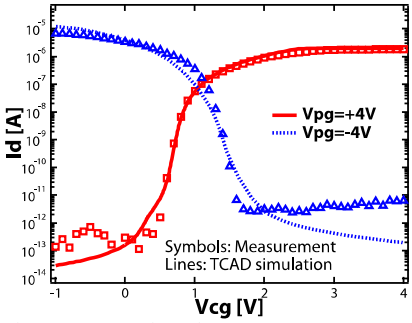

Fig. 10: Comparison between measurement and TCAD simulation by using Synopsys Sentaurus. Good agreement shows the validity and prediction ability of the simulated model and parameters.

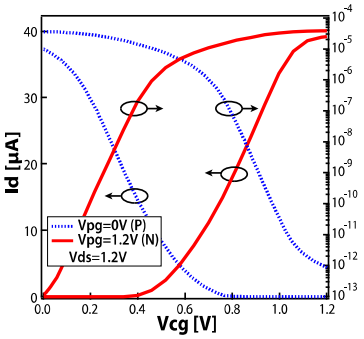

Fig. 11: I-V characteristics of the optimized device predicted by TCAD simulation. Symmetric characteristics for *n* and *p*-type operation are observed at 1.2V.

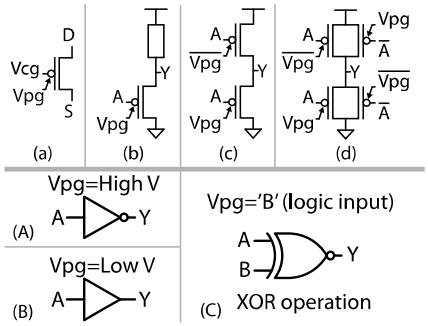

Fig. 12: Logic cell design with DG-SiNWFETs. (a) Circuit symbol for the device. (b) Pseudo-logic gate with a single device in the pull-down network. (c) Complementary design and (d) complementary design with full-swing output. (A) Operation as an inverter, (B) as a buffer and (C) as an XOR gate.

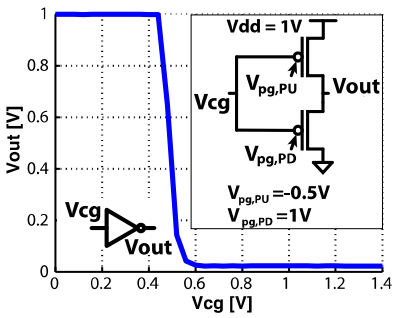

Fig. 13: Measured inverter characteristic obtained by connecting two transistors as shown in the inset. The polarity gates are biased so as to obtain a CMOS-like inverter, with a *p*-type transistor in the *pull-up* network and a *n*-type transistor in the *pull-down* network.

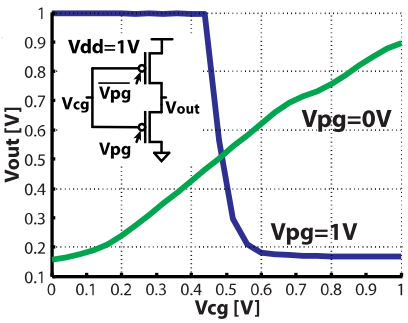

Fig. 14: Output characteristic of a two-transistor complementary XOR logic gate. The PG in this case is used as logic input.

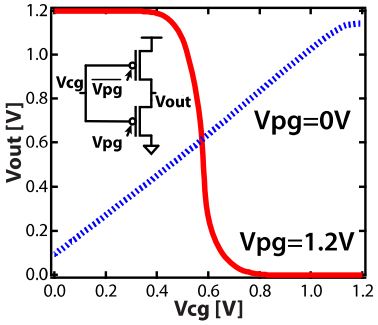

Fig. 15: TCAD simulation of the 2-transistor XOR gate built with optimized devices corresponding to the measurement in Fig. 14.

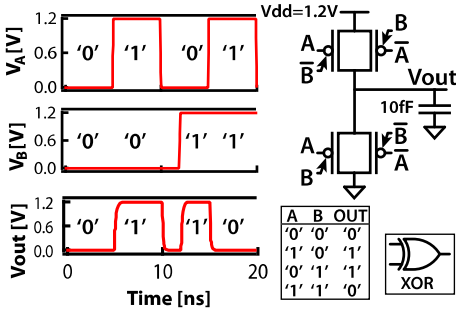

Fig. 16: The four-transistor XOR gate is built and simulated by using a table model for the optimized device based on the data extracted from TCAD simulations.

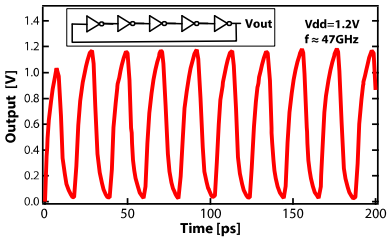

Fig. 17: Transient simulation of a 5-stages ring oscillator. The number of vertically stacked nanowires is 6 per device. 0.3fF load capacitance is included in each stage to explicitly account for parasitics. Frequency reaches 47GHz.

Conclusion

The ability of a single double-gate SiNW FET with in-field polarity control to implement the XOR function enables several applications and advantages in logic circuit design. The top-down stacked SiNW fabrication with GAA electrodes presents a straightforward approach with great potential in terms of scalability, large-scale integration and compatibility with current CMOS fabrication processes. Moreover, the simplicity of the proposed fabrication process opens the possibility to a number of potential technological improvements, which can be implemented to further tune the symmetry and efficiency of the devices. The *p* and *n* branch threshold voltages can be adjusted by engineering of the gate material, of the S/D contact workfunction and doping of the device channel.

Our fabricated devices are the first demonstrated so far to combine remarkable device characteristics with sufficient symmetry and compatible operating voltages to enable complementary multi level logic synthesis and fully exploit the advantages of the efficient DG-SiNWFET XOR implementation.

Acknowledgement

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