Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages

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***Abstract*— Gate-all-around (GAA) silicon nanowires enable an unprecedented electrostatic control on the semiconductor channel that can push device performance with continuous scaling. In modern electronic circuits, the control of the threshold voltage is essential for improving circuit performance and reducing static power consumption. Here, we propose a silicon nanowire transistor with three independent GAA electrodes, demonstrating, within a unique device, a dynamic configurability in terms of both polarity and threshold voltage (V_T). This silicon nanowire transistor is fabricated using a vertically stacked structure with a top-down approach. Unlike conventional threshold voltage modulation techniques, the threshold control of this device is achieved by adapting the control scheme of the potential barriers at the source and drain interfaces and in the channel. Compared to conventional dual-threshold techniques, the proposed device does not tradeoff the leakage reduction at the detriment of the ON-state current, but only through a later turn-ON coming from a higher V_T. This property offers leakage control at a reduction of loss in performance. The measured characteristic demonstrates a threshold voltage difference of ∼0.5 V between low-V_T and high-V_T configurations, while high-V_T configuration reduces the leakage current by two orders of magnitude as compared to low-V_T configuration.**

***Index Terms*— Polarity, Schottky barrier, silicon nanowire, threshold voltage.**

I. Introduction

SILICON devices based on nanowire structures have already shown broad applications in electronics [1], [2], optoelectronics [3], [4], and biochemical sensing [5], [6]. While the device dimensions have been reduced down to the nanometer scale, silicon nanowires enable the ultimate electrostatic control of the semiconductor channel and lead to great opportunities for conceiving electronic devices. Moreover, semiconducting materials with metallic source and drain contacts provide both electron and hole transport in the same device. This property can be exploited in dopant-free transistors, whose polarity can be reconfigured by electrostatically controlling the source and drain Schottky barriers [7]–[14]. Within the family of polarity-controllable devices, double-gate [12] and two-independent-gate structures [13], [14] are promising solutions because of the independent polarity control of each device.

In modern system-on-chips, the threshold voltage and device leakage are key parameters to achieve high performance (HP), while maximizing the energy efficiency. However, threshold voltage and leakage tuning are usually performed by adapting the process parameters during fabrication [15]–[17], thus largely impacting the versatility of circuits based on polarity-controllable devices. Moreover, in these technologies, the leakage reduction is achieved by a V_T increase that results in a delayed turn-ON during switching operation. In the meantime, the ON-state current is also reduced unavoidably. Both of these aspects lead to a significant performance cost.

In this paper, we propose a silicon nanowire field-effect transistor (SiNWFET) with three independent gates. Nickel silicide is chosen as the source/drain contacts. By independently modulating the Schottky barriers at the source and drain regions, as well as the barrier induced in the channel, the proposed device is configurable both in terms of polarity and threshold voltage. The device demonstrates a ∼0.5 V reduction of V_T in low-V_T configuration, which helps to improve circuit speed. Rather than sacrificing the ON-state current, the high-V_T configuration reduces leakage current by two orders of magnitude with respect to low-V_T configuration through suppressing injection of carriers at both Schottky barriers. Thus, the leakage reduction can be performed with a reduced impact on performance because the ON-state current is not degraded in high-V_T configuration. Such a property is not achievable with conventional multi-V_T techniques [15]–[17]. It results in a finer tradeoff between performance and standby power consumption, and helps to meet both constraints in circuit design more easily.

The remaining parts of this paper are organized as follows. In Section II, we introduce the structure and fabrication process of the three-independent-gate SiNWFET. In Section III, we present the operation of the device and electrical characterization. The basic device physics of the dual-V_T characteristics is discussed in Section IV followed by a discussion of circuit design opportunities in Section V. The conclusions are drawn in Section VI.

Manuscript received April 8, 2014; revised June 17, 2014 and July 30, 2014; accepted September 15, 2014. Date of publication October 2, 2014; date of current version October 20, 2014. This work was supported in part by the Research Project under Grant ERC-2009-AdG-246810 and in part by the Swiss National Science Foundation under Grant 200021-122168. The review of this paper was arranged by Editor J. Knoch.

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Digital Object Identifier 10.1109/TED.2014.2359112

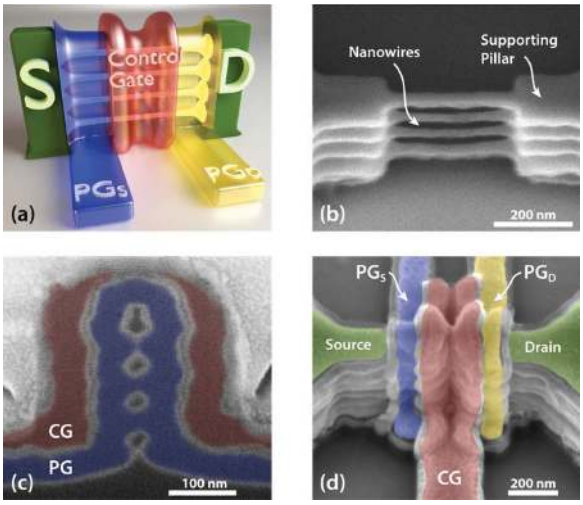


Fig. 1. (a) Conceptual sketch of a SiNWFET with three independent gates. (b) SEM image of vertically stacked nanowires. (c) Cross-sectional SEM image of the SiNWFET at the region where CG and PG are overlapped. (d) SEM image of fabricated SiNWFET.

II. Device Overview and Fabrication Process

The conceptual sketch of the SiNWFET with three independent gates is shown in Fig. 1(a). Four vertically stacked nanowires are confined within the source, and drain pillars. They are surrounded by three-independent-gate structures, named polarity gate (PG) at source (PG_S), control gate (CG) and PG at drain (PG_D). Nickel silicide is used as source/drain material to form Schottky junctions with the silicon channel. In this structure, PG_S and PG_D modulate the Schottky junctions at the source and drain contacts, whereas CG controls the current flow through the silicon nanowire channel.

For the fabrication of the SiNWFET, a lightly p-type doped ($\sim 10^{15}/\text{cm}^{-3}$) silicon-on-insulator substrate with a 340-nm-thick silicon device layer is used. First, the nanowires are defined using electron-beam lithography. The length and diameter of the defined nanowires are 350 and 50 nm, respectively. Then, four vertically stacked nanowires are formed in a top-down fashion, using a single deep reactive ion etching process step [12], [18] [see Fig. 1(b)]. The typical vertical spacing between the nanowires is 40 nm. Following a 15-nm SiO_2 gate dielectric formation, two gate-all-around (GAA) structures with a length of 120 nm are patterned in polycrystalline silicon to form PG_S and PG_D. Then, a second 15-nm gate oxidation is performed and polycrystalline silicon CG is patterned in a self-aligned way. Fig. 1(c) shows the cross-sectional scanning electron microscopy (SEM) image of the silicon nanowire stack and gates. Considering the silicon consumed during oxidation, the resulting nanowires are $\sim$30 nm in diameter. In the current fabrication setup, the thick gate oxide is used to maximize the fabrication yield within an academic clean room facility by guaranteeing the correct connectivity and reduce the risk of gate leakage. Nevertheless, no physical constraints limit gate oxide scaling in this device with state-of-the-art high-κ dielectric stacks directly implementable in the fabrication process. After the formation of the gates, silicon nitride spacers are used to isolate the structures. A 20-nm nickel layer is subsequently deposited with sputtering instead of evaporation used in [12] to perform an *in situ* cleaning and increase the layer uniformity. Then, the nickel layer is annealed to form nickel silicide on source and drain pillars. The silicidation step creates Schottky junctions with the silicon channel. The nickel silicide is also formed on the polycrystalline silicon gates at the same time to reduce the resistance of the gate contacts. By controlling the annealing temperature and duration, Ni_1Si_1 is selected among different phase of nickel silicide. The Ni_1Si_1 phase is preferred because of its near midgap workfunction ($\sim$4.8 eV) and low resistivity [19], [20]. Fig. 1(d) shows the SEM image of the final structure. Note that the device may be more aggressively scaled without any fundamental limitations coming from the device physics. In particular, the GAA channel geometry is best suited for strong suppression of short-channel effects. In addition, the absence of abrupt doping profiles in the channel relaxes constraints on doping levels down to the current nanoscale technology nodes (22 nm and beyond).

III. Operation and Electrical Characterization

Next, we explain the operation of the three-independent-gate SiNWFET. In this device, V_{PGS} and V_{PGD} independently modulate the thickness of the corresponding Schottky barrier. The desired type of carriers is selected to tunnel into the channel through the thin Schottky barrier, and the other type of carriers is blocked by the thick Schottky barriers. The electrostatic polarization is thereby achieved. V_{CG} induces a potential barrier in the inner region of the channel to control the selected carriers flow through the channel. Following the working principle, the transfer characteristics of the fabricated device are measured and shown in Fig. 2. Both n-type and p-type behaviors with different threshold voltages (low-V_T and high-V_T) are observed in the same device.

In all demonstrated characteristics in Fig. 2, the applied voltages at source and drain are set to 0 and 2 V, respectively. According to the measured characteristics, we summarize the operation states of the device under different bias conditions in Fig. 3(a). For the sake of clarity, logic values 0 and 1 are used to show the operation of the device. The ON-states of the device are defined as the states when: 1) $V_{PGS} = V_{PGD} = V_{CG} = 0$ (p-type) and 2) $V_{PGS} = V_{PGD} = V_{CG} = 1$ (n-type).

Low-V_T (LVT) p-FET configuration [LVT curves in Fig. 2(a)] is observed when V_{PGS} and V_{PGD} are set to 0 V. Thus, electrons are blocked at source, and band bending at drain leads to a reduction of the width of the Schottky barrier, i.e., thin Schottky barrier, which enables holes to tunnel from drain into the channel. The CG modulates the barrier in the channel, thereby turning the device ON or OFF as in conventional MOSFETs [21]–[23]. While in the ON-state, the Schottky barrier is thin enough and has a limited impact on the device operation. When V_{CG} is set to 0 V, the barrier for holes along the CG is suppressed. Holes flow through the device easily [curve (1) in Fig. 3(b)]. While setting V_{CG} to 2 V, the potential barrier induced by the CG cuts the current flow and turns the device OFF [curve (2) in Fig. 3(b)].

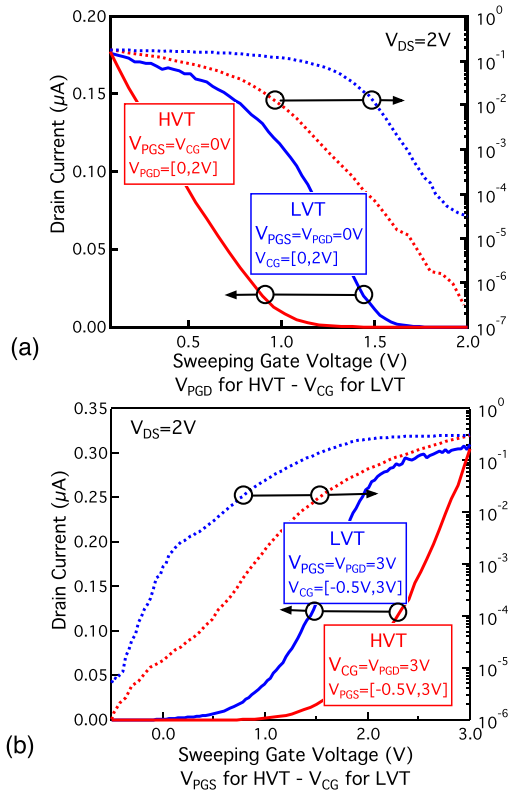


Fig. 2. Measured characteristics of a three-independent-gate SiNWFET. (a) p-type transfer characteristic. (b) n-type transfer characteristic in the same device.

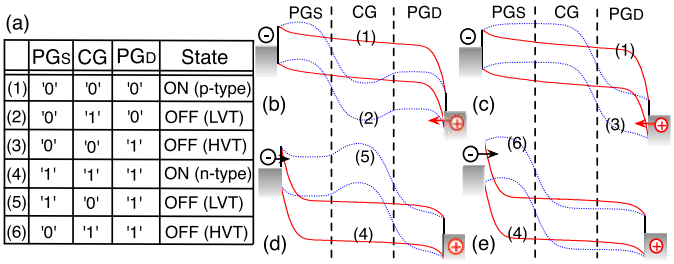


Fig. 3. (a) Operation states of fabricated device under different bias conditions. Note that, two other possible configurations do not yield useful operation states. Band diagrams of corresponding configurations. (b) Low-V_T p-FET. (c) High-V_T p-FET. (d) Low-V_T n-FET. (e) High-V_T n-FET. Numbers: corresponding states in (a).

In contrast, high-V_T (HVT) p-FET configuration [HVT curves in Fig. 2(a)] is obtained when V_{PGS} and V_{CG} are set to 0 V to block the electrons tunneling from source. PG_D modulates the Schottky junction at drain and thereby controls the hole tunneling. By setting V_{PGD} to 0 V, holes can tunnel through the thin barrier and flow through the channel [curve (1) in Fig. 3(c)]. Because this condition is exactly the same as in low-V_T p-FET configuration [state (1) in Fig. 3(a)], the ON-state currents of both high-V_T and low-V_T modes are exactly the same value, regardless of the supply voltage. Although a lower V_T, i.e., earlier turn-ON, is helpful for improving the circuit speed, the high-V_T mode with the same ON-state current will not significantly degrade the circuit performance. This property of the proposed SiNWFET is not achievable in conventional multi-V_T techniques and represents one of the key advantages of our approach. For the OFF-state, V_{PGD} is set to 2 V. The opposite band bending at the Schottky contacts prevents both electron and hole injection into the channel [curve (3) in Fig. 3(c)] and also ensures the whole channel to be unpopulated [13]. This OFF-state current suppression is thereby more effective than in the low-V_T configuration, where holes are induced in the PG_D-controlled region. Therefore, the OFF-state current is reduced by two orders of magnitude as compared to low-V_T configuration, and reaches a leakage floor of 10.5 pA/μm (315 fA) normalized to the nanowire diameter.

Similarly, low-V_T n-FET configuration [LVT curves in Fig. 2(b)] is reached when V_{PGS} and V_{PGD} are set to 3 V. The Schottky barrier at drain blocks holes. At the same time, the Schottky barrier at source is thin enough for electrons tunneling due to a band bending induced by PG_S. CG controls the current flow [Fig. 3(d)] as in the low-V_T p-FET configuration. High-V_T n-FET configuration [HVT curves in Fig. 2(b)] is reached for V_{PGD} and V_{CG} fixed to 3 V that blocks holes tunneling from drain. PG_S controls the Schottky junction at source and consequently turns the device ON or OFF [Fig. 3(e)]. In the same principle as p-FET configurations, the ON-state currents of low-V_T and high-V_T n-FET configurations are the same since they share the same ON-state [state (4) in Fig. 3(a)], and the leakage current is also suppressed in high-V_T configurations.

To summarize the performance of the fabricated device, the ON-state currents of p-FET and n-FET configurations are 177 nA (5.9 μA/μm) and 310 nA (10.3 μA/μm), respectively, which are comparable to recent works on polarity-controllable devices [12], [14]. Extracted at 1-nA drain current [24], the threshold difference in p-FET configurations and in n-FET configurations are 0.48 and 0.86 V, respectively. The OFF-state currents of high-V_T p-FET and n-FET configurations reach 315 fA (10.5 pA/μm) and 1 pA (33.3 pA/μm) compared to 30 pA (1 nA/μm) and 4.6 pA (153.3 pA/μm) in low-V_T configurations. Thus, the total I_{ON}/I_{OFF} ratio for the high-V_T p-FET and n-FET configurations are 6×10^5 and 3×10^5, respectively. Currently, limited by the thick oxide used in fabrication process, low-V_T configurations demonstrate subthreshold slopes of 155 mV/decade (p-FET) and 217 mV/decade (n-FET). However, the performance of the device can be further improved by optimizing the fabrication steps to enhance the electrostatic control, such as reducing the gate oxide thickness.

Regarding scaling issues, high-κ gate dielectric materials and metal gates, together with channel strain techniques can be directly applied to the presented structure. We do not foresee fundamental limitations to size downscaling in terms of drain-induced barrier lowering effect and power consumption compared with conventional MOSFET. Moreover, the proposed device concept may be applied to other materials (e.g., carbon nanotube, graphene, and MoS_2 [8]–[10]), giving the opportunities for continuous scaling down.

IV. Physical Understanding

After showing n-type and p-type operations in both high-V_T and low-V_T configurations, we will discuss the reason of this dual-V_T characteristic.

Let us take the n-FET configurations for example. Band bending induced by a positive voltage on PG_S reduces the thickness of the source Schottky barrier and enhances the tunneling of electrons through the source barrier. This leads to a reduction of the effective barrier height [21]. In low-V_T configuration [Fig. 3(d)], the effective Schottky barriers at the source are fully suppressed by sufficiently positive voltage configured on PG_S. V_{CG} is swept to tune the conduction of the device. Therefore, the current transport is dominated by thermionic emission of electrons over a potential barrier induced by CG [25], particularly

$$I_D = AA^*T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right) \tag{1}$$

where A is the junction area, A^* is the effective Richardson constant, T is the temperature, q is the elementary charge, k_B is the Boltzmann constant, and ϕ_B is the effective barrier height. This barrier height is determined by the electrostatic potential in the CG-controlled region. If we assume that there is no induced charge in the channel under subthreshold operation, the applied voltage on CG directly translates into a reduction of ϕ_B. Therefore

$$\Delta\phi_B = -\Delta V_{CG}. \tag{2}$$

In contrast, in high-V_T configuration [Fig. 3(e)], a sufficiently positive voltage is applied to CG and PG_D to make sure there is no barrier inside the silicon channel. The current is therefore determined by an effective Schottky barrier height at source. A positive voltage on PG_S reduces the thickness of the Schottky barrier at source, and the consequent enhancement of tunneling by V_{PGS} leads to a reduction of ϕ_B. Thus

$$\Delta\phi_B = -\lambda\Delta V_{PGS} \tag{3}$$

where the coefficient λ represents the dependence of the effective barrier height on V_{PGS}. Since the tunneling probability is smaller than 1, λ is also smaller than 1 [21]–[23].

Due to the lower efficiency of tuning the effective barrier height by PG_S than CG, a higher V_{PGS} than V_{CG} is needed to turn ON the device. That results in a higher threshold voltage in this configuration.

Through the above analysis, we can also explain the saturation trend of the drain current with a large positive V_{CG} in low-V_T n-FET configuration [V_{CG} from 2 to 3 V in Fig. 2(b)]. First, when the applied voltage on CG goes above the threshold voltage, electrons are induced in the channel, and the electrostatic potential in the channel gradually saturates [26], [27]. More importantly, when the bended conduction band edge is lower than the Fermi level in the source, the current starts to be dominated by the source injection and cannot be further modulated by CG. Therefore, the current saturates at a large positive V_{CG}.

The above analysis is also applicable for p-FET configurations. Tuning the effective barrier height for holes by PG_D is less efficient than tuning it by CG. Thus, higher voltage on PG_D is required to turn ON the device in high-V_T p-FET configuration. Similar to the n-FET configuration, the current also saturates in low-V_T p-FET configuration [V_{CG} from 0 to 0.7 V in Fig. 2(a)].

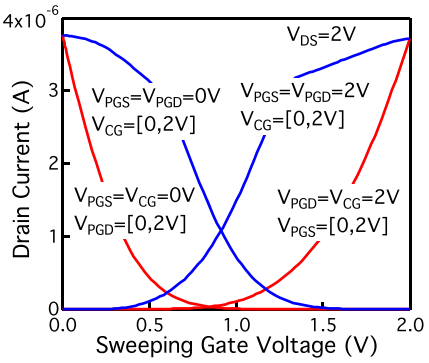


Fig. 4. Simulation results of an optimized three-independent-gate SiNWFET, showing the dual-V_T characteristic and polarity control of the device.

To further prove the dual-V_T characteristics of the proposed transistor and analysis above, and also predict further performance improvement by technological innovations, we simulated a single three-independent-gate SiNWFET using finite-element method with Sentaurus Device [28]. The simulation employs drift-diffusion transport in the silicon channel, whereas thermionic emission and quantum mechanical tunneling with Wentzel–Kramers–Brillouin approximation are used at the junctions. The simulated SiNWFET has the same structure than the fabricated one except that an optimized 2-nm gate oxide and a fine-adjusted Schottky barrier height (0.35 eV for electrons and 0.75 eV for holes) are used. Fig. 4 shows the simulation results. By optimizing the gate oxide, the performance of the device reaches levels of regular advanced MOSFETs. Fine-adjusted Schottky barrier height also gives symmetric n-type and p-type characteristics, which is important to achieve energy-efficient circuits with balanced delay [14]. The simulated device reproduces all the key properties demonstrated in the measured characteristics, including the shared ON-state current but different threshold voltages in dual-V_T configurations, as well as the saturation trend of the ON-state current in low-V_T configurations.

According to the previous analysis, the V_T difference is determined by the efficiency of tuning effective barrier height, i.e., λ in (3). Therefore, we simulated a series of devices with different parameters related to this efficiency, including the oxide thickness (Tox), radius of nanowire (Rnw), tunneling effective mass (m_h*), and Schottky barrier height (SBH_h). The V_T difference of p-FET configurations of different devices is plotted in Fig. 5. The reduction of Tox and Rnw enhances the electrostatic control of the gate, thus resulting in a thinner Schottky barrier at a given gate voltage in high-V_T configurations. Tunneling current is thereby improved and reduces the effective barrier height further [21], implying a larger λ and decreased V_T difference. A smaller effective mass also results in a larger tunneling probability and V_T difference is consequently reduced. The V_T difference is also proportional to the Schottky barrier height. Other than the previous three parameters, a reduction of Schottky barrier height for holes leads to an increase of Schottky barrier height for electrons. Thus, tuning of Schottky barrier height can achieve a tradeoff between V_T differences in n-type configurations and p-type configurations.

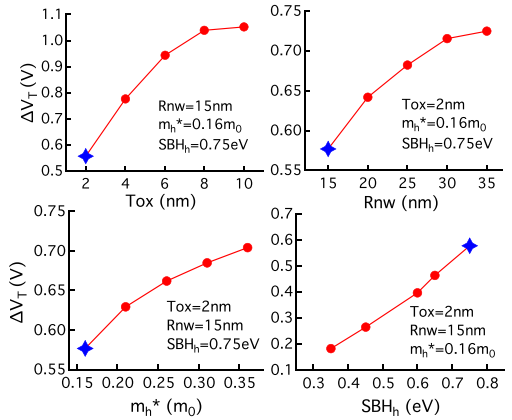


Fig. 5. V_T difference of p-FET configurations in simulated devices. m_0 is the free electron mass. Stars: simulated device in Fig. 4.

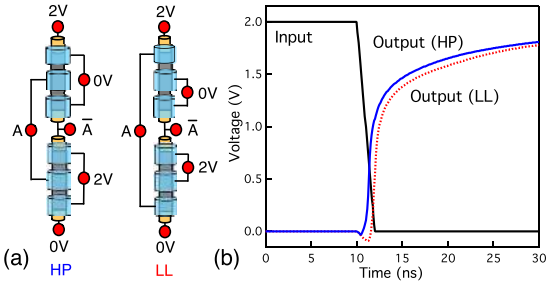


Fig. 6. (a) Different wiring schemes of the inverters with two identical devices presented in Fig. 4. (b) Transient simulation of two inverters for HP and LL applications. The load capacitance is assumed to be the same as input gate capacitance.

V. Circuit Design Opportunities

Recently, design with polarity-controllable devices has been widely investigated. For a complete review on design opportunities compared to CMOS, we refer the interested reader to [29] and [30]. In this section, we show the interest of the dual-V_T device from the perspective of circuit applications.

With the dual-V_T characteristic, circuits can achieve either HP or low leakage (LL) by changing the wiring scheme on the devices. For example, Fig. 6(a) illustrates two inverters for HP and LL applications. According to Fig. 3(a), the HP inverter is obtained by assigning the input signal to the control gates of the two devices, whereas LL inverter is obtained by connecting the input to corresponding polarity gates. Fig. 6(b) gives the transient simulation results of the two inverters. This evaluation takes into account the parasitics, such as the impact of gate capacitances. Because of a low-V_T, the HP inverter demonstrates a 0.8-ns propagation delay as compared to 1.4 ns of LL inverter. In contrast, the LL inverter consumes a leakage power of 8.5×10^{-14} W as compared to 2.8×10^{-13} W of HP inverter. Therefore, by applying this strategy, dual-V_T design is achievable with a single fabrication process for the SiNWFETs. This property increases the configurability of the circuits while reducing the process complexity compared to dual-V_T technologies for conventional CMOS.

In addition to dual-V_T design of conventional logic circuits, the three-independent-gate SiNWFETs also provide

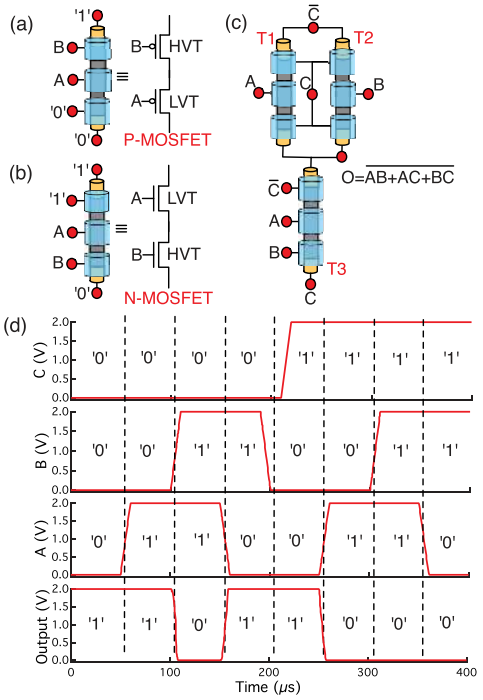


Fig. 7. Three-independent-gate SiNWFET configured as (a) two series p-FETs and (b) two series n-FETs. (c) Implementation of a minority gate with three-independent-gate SiNWFETs. (d) Transient simulation of the minority gate with the device presented in Fig. 4.

opportunities to implement circuits in a novel and compact form. From the operation states listed in Fig. 3(a), we found that by setting PG_S to logic 0, the device is ON only when PG_D and CG are both 0. In this way, we obtain two series p-FETs through inputs from PG_D and CG [Fig. 7(a)]. Alternatively, we obtain two series n-FETs on PG_S and CG by setting PG_D to logic 1 [Fig. 7(b)]. Along with the characteristic of electrostatic polarization, more logic functions can be implemented in a compact form [31], showing the potential applications of the three-independent-gate SiNWFET. Fig. 7(c) shows a minority gate consisting of three devices, excluding the inverter for C. When C is logic 0, the transistors T1 and T2 are programmed as p-type and T3 is programmed as n-type. Thus, the minority gate reduces to a NAND gate. While C is logic 1, it becomes a NOR gate. Fig. 7(d) shows the transient simulation results, validating the functionality in different input conditions. Moreover, the two series FETs in Fig. 7(a) and (b) show different threshold voltages, so that we can optimize both the delay and leakage power consumption at device level.

To further demonstrate the potential of the proposed technology, benchmarking of configurable dual-V_T circuits was presented in [32].

As a future perspective, we can extend the device structure to multiple independent gates. According to the working principle of the device, if we add more gates between the polarity gates PG_S and PG_D, these additional gates only modulate the potential barriers in their controlled regions. Any of these barriers will prevent current flowing through the channel. Therefore, these gates all operate as the CG in the three-independent-gate device. By applying this strategy within the

limit of series silicon resistance, we can obtain multiple series transistors in a single nanowire with a single source/drain contact, which can be used to build dense nanowire circuits [33]. Compared to MOSFETs with doped source/drain and other polarity-controllable devices, the multiple-input nanowire transistor significantly reduces the average number of S/D contacts for each input. It is thus expected to reduce the area cost of circuits [34], [35]. In addition, as there is no internal node between successive equivalent resistors in the nanowire, an improvement of the circuit performance is expected.

VI. Conclusion

We have introduced and demonstrated a silicon nanowire transistor with three independent gates. The uniqueness of the proposed device lays in the high degree of configurability reachable by a unique device. By biasing separately the three independent gates, this device is configured as n-type or p-type transistor in either high-V_T or low-V_T mode. The threshold voltage tuning of this device is achieved by independently modulating the carrier transport at source/drain interface and in the channel. By fully suppressing the Schottky barriers and controlling the potential barrier in the channel, low-V_T configuration with earlier turn-ON, is helpful for improving the circuit speed. In contrast, by efficiently controlling the Schottky barriers at both source and drain, high-V_T configuration achieves a suppression of leakage current by two orders of magnitude without sacrificing the ON-state current, showing advantages over the conventional multi-V_T techniques.

References

[1] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, no. 5545, pp. 1313–1317, 2001.

[2] N. Singh *et al.*, "High-performance fully depleted silicon nanowire (diameter $\leq$5 nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.

[3] B. Tian *et al.*, "Coaxial silicon nanowires as solar cells and nanoelectronic power sources," *Nature*, vol. 449, pp. 885–889, Oct. 2007.

[4] E. Garnett and P. Yang, "Light trapping in silicon nanowire solar cells," *Nano Lett.*, vol. 10, no. 3, pp. 1082–1087, 2010.

[5] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, no. 5533, pp. 1289–1292, 2001.

[6] P. R. Nair and M. A. Alam, "Design considerations of silicon nanowire biosensors," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3400–3408, Dec. 2007.

[7] S.-M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel, "Enhanced channel modulation in dual-gated silicon nanowire transistors," *Nano Lett.*, vol. 5, no. 12, pp. 2519–2523, 2005.

[8] Y.-M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 481–489, Sep. 2005.

[9] N. Harada, K. Yagi, S. Sato, and N. Yokoyama, "A polarity-controllable graphene inverter," *Appl. Phys. Lett.*, vol. 96, no. 1, p. 012102, 2010.

[10] S. Sutar, P. Agnihotri, E. Comfort, T. Taniguchi, K. Watanabe, and J. U. Lee, "Reconfigurable $p-n$ junction diodes and the photovoltaic effect in exfoliated MoS_2 films," *Appl. Phys. Lett.*, vol. 104, no. 12, p. 122104, 2014.

[11] F. Wessely, T. Krauss, and U. Schwalke, "CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors," *Solid-State Electron.*, vol. 70, pp. 33–38, Apr. 2012.

[12] M. De Marchi *et al.*, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *IEEE IEDM Tech. Dig.*, Dec. 2012, pp. 8.4.1–8.4.4.

[13] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Lett.*, vol. 12, no. 1, pp. 119–124, 2012.

[14] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually active silicon nanowire transistors and circuits with equal electron and hole transport," *Nano Lett.*, vol. 13, no. 9, pp. 4176–4181, 2013.

[15] A. Bansal, J.-J. Kim, K. Kim, S. Mukhopadhyay, C.-T. Huang, and K. Roy, "Optimal dual-V_T design in sub-100-nm PD/SOI and double-gate technologies," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1161–1169, May 2008.

[16] O. Weber *et al.*, "Work-function engineering in gate first technology for multi-V_T dual-gate FDSOI CMOS on UTBOX," in *IEEE IEDM Tech. Dig.*, Dec. 2010, pp. 3.4.1–3.4.4.

[17] Y. Jiang *et al.*, "Nanowire FETs for low power CMOS applications featuring novel gate-all-around single metal FUSI gates with dual Φm and V_T tune-ability," in *IEEE IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[18] R. M. Y. Ng, T. Wang, F. Liu, X. Zuo, J. He, and M. Chan, "Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 520–522, May 2009.

[19] Y.-J. Chang and J. L. Erskine, "Diffusion layers and the Schottky barrier height in nickel silicide—Silicon interface," *Phys. Rev. B*, vol. 28, no. 10, pp. 5766–5773, 1983.

[20] Q. T. Zhao, U. Breuer, E. Rije, S. Lenk, and S. Mantl, "Tuning of NiSi/Si Schottky barrier heights by sulfur segregation during Ni silicidation," *Appl. Phys. Lett.*, vol. 86, no. 6, p. 062108, 2005.

[21] J. Appenzeller, M. Radosavljević, J. Knoch, and P. Avouris, "Tunneling versus thermionic emission in one-dimensional semiconductors," *Phys. Rev. Lett.*, vol. 92, no. 4, p. 048301, 2004.

[22] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, and S. De Franceschi, "Multifunctional devices and logic gates with undoped silicon nanowires," *Nano Lett.*, vol. 12, no. 6, pp. 3074–3079, 2012.

[23] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, 2004.

[24] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in *IEDM Tech. Dig.*, Dec. 2000, pp. 719–722.

[25] M. S. Lundstrom and D. A. Antoniadis, "Compact models and the physics of nanoscale FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 225–233, Feb. 2014.

[26] W. Z. Shangguan *et al.*, "Surface-potential solution for generic undoped MOSFETs with two gates," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 169–172, Jan. 2007.

[27] J. Zhang, L. Zhang, J. He, and M. Chan, "A noncharge-sheet channel potential and drain current model for dynamic-depletion silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 107, no. 5, pp. 054507-1–054507-7, Mar. 2010.

[28] Synopsys, Inc. (Jun. 2009). *Sentaurus Device User Guide Version C-2009.06*. [Online]. Available: http://www.synopsys.com

[29] P.-E. Gaillardon, L. G. Amarù, S. Bobba, M. De Marchi, D. Sacchetto, and G. De Micheli, "Nanowire systems: Technology and design," *Philosoph. Trans. Roy. Soc. A, Math., Phys. Eng. Sci.*, vol. 372, p. 20130102, Mar. 2014.

[30] P.-E. Gaillardon, L. Amaru, J. Zhang, and G. De Micheli, "Advanced system on a chip design based on controllable-polarity FETs," in *Proc. Conf. DATE*, Dresden, Germany, Mar. 2014, p. 235.

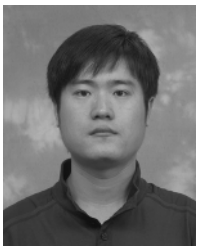
[31] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Elementary aspects for circuit implementation of reconfigurable nanowire transistors," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 141–143, Jan. 2014.

[32] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2851–2861, Oct. 2014.

[33] H. Yan *et al.*, "Programmable nanowire circuits for nanoprocessors," *Nature*, vol. 470, no. 7333, pp. 240–244, 2011.

[34] J. Zhang, P.-E. Gaillardon, and G. De Micheli, "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs," in *Proc. IEEE ISCAS*, May 2013, pp. 2111–2114.

[35] X. Li *et al.*, "Vertically stacked and independently controlled twin-gate MOSFETs on a single Si nanowire," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1492–1494, Nov. 2011.



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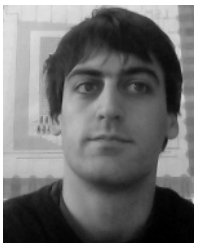

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