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Polarization diversity DPSK demodulator on the silicon-on-insulator platform with simple fabrication

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Abstract: We demonstrate a novel polarization diversity differential phase-shift keying (DPSK) demodulator on the SOI platform, which is fabricated in a single lithography and etching step. The polarization diversity DPSK demodulator is based on a novel polarization splitter and rotator, which consists of a tapered waveguide followed by a 2 × 2 multimode interferometer. A lowest insertion loss of 0.5 dB with low polarization dependent loss of 1.6 dB and low polarization dependent extinction ratio smaller than 3 dB are measured for the polarization diversity circuit. Clear eye-diagrams and a finite power penalty of only 3 dB when the input state of polarization is scrambled are obtained for 40 Gbit/s non return-to-zero DPSK (NRZ-DPSK) demodulation.

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1. Introduction

The differential phase-shift keying (DPSK) format is widely used in optical communication networks due to its better fiber nonlinearity tolerance [1]. Various types of DPSK demodulators, including delay interferometers [2], optical bandpass filters [3], a birefringent fiber loop [4], or a single silicon wire [5] have been demonstrated. Recently, the use of silicon microring resonators (MRRs) has been proposed and demonstrated for ultra-compact DPSK demodulation [6, 7]. The use of such devices as multi-channel wavelength division multiplexing (WDM) non return-to-zero DPSK (NRZ-DPSK) demodulators has also been demonstrated [8]. One of the main practical limitations of the silicon-on-insulator (SOI) technology used to implement these MRRs is its inherent polarization sensitivity. To realize a polarization insensitive NRZ-DPSK demodulator, a polarization diversity (Pol-D) circuit is typically employed [9–11, 17, 18]. There are mainly two methods to realize a Pol-D circuit. One is based on two-dimensional grating couplers, which work on a particular polarization and play the role of a polarization splitter [9–12]. However, this scheme is limited by the insertion loss and bandwidth of the grating coupler. Another method is based on polarization splitter and rotator (PSR) technology [13–18]. Recently a Pol-D circuit for NRZ-DPSK demodulation relying on an asymmetrical coupler-based PSR has been demonstrated [19]. However, the demonstrated polarization dependent extinction ratio (PDER) was still over 15 dB, partly due to a tight fabrication tolerance.

In this paper we demonstrate a Pol-D DPSK demodulator on the SOI platform based on a novel PSR and a single MRR, which are fabricated in a single step of exposure and etching. The PSR is based on a tapered waveguide-based TM_0-TE_1 mode converter followed by a 2×2 multimode interferometer (MMI) [20]. A lowest insertion loss of 0.5 dB with a minimum polarization dependent loss (PDL) of 1.6 dB and a PDER below 3 dB are demonstrated. The Pol-D operation is illustrated in the case of NRZ-DPSK demodulation at 40 Gbit/s. Compared to a standard MRR demodulator without polarization diversity, the use of the proposed Pol-D structure results in a clear eye-diagram and finite power penalty of only 3 dB when the input state of polarization is scrambled.

2. Principle and design of the Pol-D DPSK demodulator

2.1 Polarization splitter and rotator

The principle of NRZ-DPSK demodulation is to use the through transmission of a MRR to convert phase modulation to amplitude-modulation [6]. To achieve a Pol-D MRR-based demodulator, a novel PSR is designed, as shown in Fig. 1(a). The PSR consists of a tapered waveguide connected to a 2×2 MMI through two arms, which introduce an extra phase difference of $\Delta\varphi = \pi/2$, as shown in Fig. 1(a). In case of TE_0 input, the light will directly propagate through the adiabatic taper and be split into two TE_0 beams with the same phase. After the two arms, the two TE_0 beams will have a $\pi/2$ phase difference when injected into the MMI. By properly designing the MMI, light will output from arm 1 on the TE_0 mode, as shown in Fig. 1(b). On the other hand, in case of TM_0 input, the light is converted to the TE_1 mode during the adiabatic tapering [21], and split into two TE_0 beams with π phase difference. After the two arms, the two TE_0 beams will have a $-\pi/2$ phase difference, and light will output the MMI from arm 2 on the TE_0 mode, as indicated in Fig. 1(c). A SOI wafer with top silicon layer of 250 nm is selected for the design. In our design, air is employed as top cladding material to achieve an efficient TM_0-TE_1 polarization conversion [21]. To decrease the tapering length, the TM_0-TE_1 converter is divided into three sections, as shown in Fig. 1(a). The first and third sections (L_1 and L_3) are from a single-mode silicon waveguide ($w_1 = 450$ nm) to $w_2 = 650$ nm, and from $w_3 = 750$ nm to $w_4 = 800$ nm, respectively, with tapering lengths as short as 10 μm. The second section L_2 is from $w_2 = 650$ nm to $w_3 = 750$ nm with tapering length as long as 120 μm in order to achieve a TM_0-TE_1 conversion efficiency higher than 95% [20]. After that, the 800 nm waveguide is split into two arms with widths of 400 nm and connected to the 2×2 MMI through tapering to $w_0 = 700$ nm to improve the fabrication tolerance [22]. With a calculated TE_0 effective index of 2.234 for a 400 nm wide waveguide, the two arms are designed to have a length difference of 173 nm to introduce the required $\pi/2$ phase difference at 1550 nm. The 2×2 MMI is designed to have a width of $w_{MMI} = 2$ μm and length of $L_{MMI} = 13.7$ μm. Thanks to the use of the 2×2 MMI, a wide operation band over 100 nm with large fabrication tolerance of more than 50 nm has been both numerically predicted and experimentally demonstrated [20].
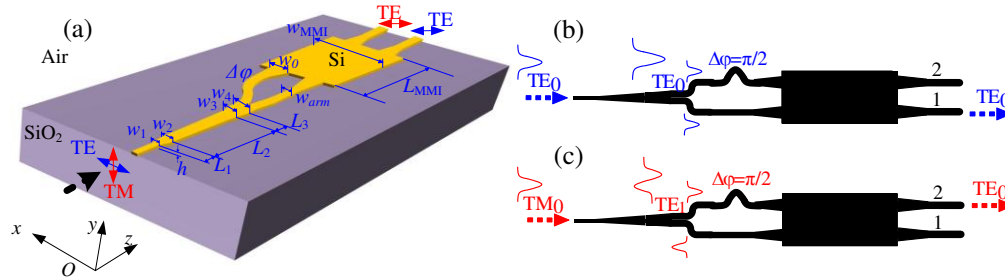

Fig. 1. (a) Structure of the PSR. TE_0 (b) and TM_0 (c) light are input to the PSR, and output from arm 1 and 2, respectively, on the TE_0 mode.

2.2 Polarization diversity NRZ-DPSK demodulator

Based on the PSR, a Pol-D circuit consisting of two identical PSRs and a single MRR is proposed, as shown in Fig. 2. A light field $E_{in} = xE_{TE} + yE_{TM}$ with two orthogonal polarization states (E_{TE} and E_{TM}) is injected into the Pol-D circuit. The first PSR_1 splits the two orthogonal polarization states into two beams of TE light. The two TE lights are then injected into the MRR, which is designed to have two identical coupling regions. With the same through transmission t_{TE} after the MRR, the two TE beams are combined back to two orthogonal polarization states by the second PSR_2, therefore avoiding interference. The output light field

can be expressed as $E_{out} = r_{TE\text{-}TE}r_{TM\text{-}TE}(xE_{TM} + yE_{TE})t_{TE}$, where $r_{TE\text{-}TE}$ and $r_{TM\text{-}TE}$ are the transmission coefficients from the input TE and TM components to the output TE light at port 1 and port 2 of a single PSR, respectively. As a result, the total device exhibits a polarization independent transmission t_{TE}. One point that should be noticed is that the long arms in the input and output PSRs are asymmetrically placed with respect to the MRR plane, which makes the two input orthogonal polarization components propagate along the same path length in the Pol-D circuit, thereby circumventing polarization mode dispersion (PMD). In addition, in the proposed Pol-D demodulator, only the alternate mark inversion (AMI) signal is demodulated. For balanced detection, the demodulated duobinary (DB) signal could be obtained from the signal reflected by the chip provided the facet reflectivity is sufficiently low. Otherwise, two identical microring resonators should be used with each drop and through transmissions combined by a PSR to obtain the demodulated AMI and DB signals, respectively.
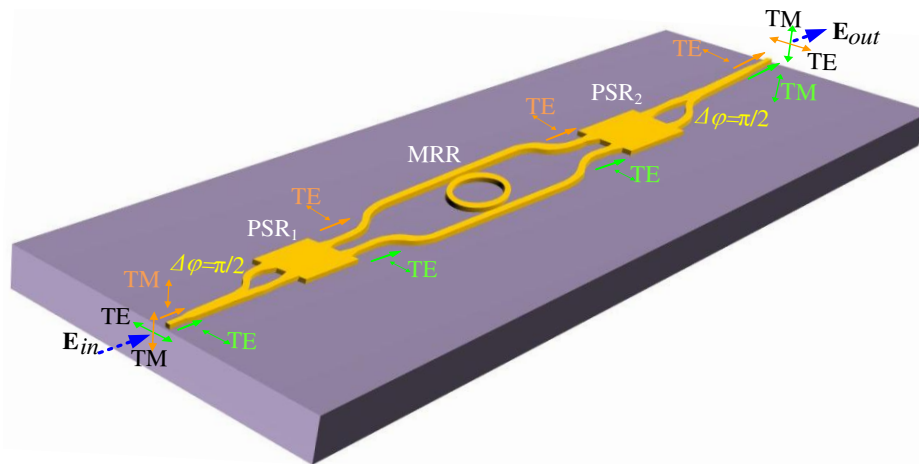

Fig. 2. Pol-D circuit with a single MRR and two identical PSRs.

3. Fabricated device

The proposed Pol-D demodulator was fabricated on a commercial SOI wafer (250 nm top silicon layer, 3 μm buried silicon dioxide) by a single step of E-beam lithography (JEOL JBX-9300FS) and inductively coupled plasma reactive ion etching (STS Advanced Silicon Etcher). Polymer (SU8-2005) waveguides of dimensions 3.5 μm × 3.5 μm covering silicon inverse tapers were fabricated for coupling loss reduction to tapered fibers. Figure 3(a) shows a picture of the fabricated Pol-D device. The racetrack MRR was designed symmetrically with radius of curvature of 9.4 μm, straight section length of 10 μm and coupling gap of 150 nm. A Y-branch with minimum gap of 40 nm between the two arms is introduced as Y splitter in the PSRs, as shown in Fig. 3(b). Other Y splitter designs with ultra-low excess loss [23] could also be utilized to improve the insertion loss of the device. Figure 3(c) illustrates the measured transmission (normalized to a straight waveguide) of the device for 15 random polarization states. The device exhibits similar transmissions with free spectral range (FSR) of 805 GHz and Q value
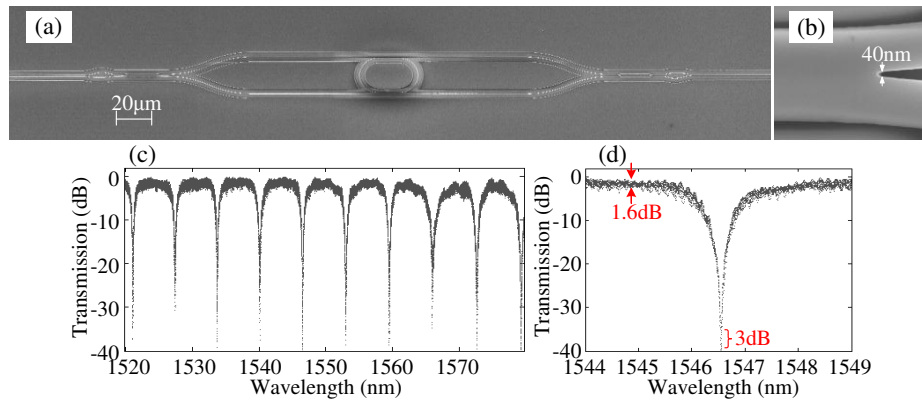
Fig. 3. Scanning electron microscope (SEM) pictures of (a) the Pol-D circuit with a single MRR and (b) detail of the Y splitter of one of the PSRs. (c) Measured transmission of the Pol-D MRR over a 60 nm wavelength range and (d) details of the transmission around the resonance wavelength of 1546.52 nm for 15 randomly chosen input polarization states.

of 1400 regardless of the input polarization. Figure 3(d) shows the details of the transmission around the resonance wavelength of 1546.52 nm. A lowest insertion loss of 0.5 dB is obtained. A low PDL smaller than 1.6 dB, and a high extinction ratio (ER) of 38 dB with PDER better than 3 dB are measured. The total insertion loss of the device is 7 dB, which includes the loss of the Pol-D circuit and the coupling loss of about 3.2 dB between the chip and tapered optical fibers.

4. NRZ-DPSK demodulation with reduced polarization sensitivity

The fabricated Pol-D circuit was then used for NRZ-DPSK demodulation at 40 Gbit/s. Figure 4 shows the experimental setup. Continuous wave (CW) light at 1546.52 nm is modulated in the NRZ-DPSK format in a Mach-Zehnder modulator at 40 Gbit/s with a pseudo-random bit pattern length of $2^{31}-1$, and then amplified by an erbium-doped fiber amplifier (EDFA). A polarization scrambler is introduced before the Pol-D circuit to produce periodically varying arbitrary input polarization states with a low frequency in the range 700 kHz-1 MHz. A polarization controller (PC) is placed before the polarization scrambler to optimize the input state of polarization with respect to residual polarization dependence when the scrambler is turned off. The demodulated AMI signal output from the Pol-D MRR is finally detected in a preamplified receiver.
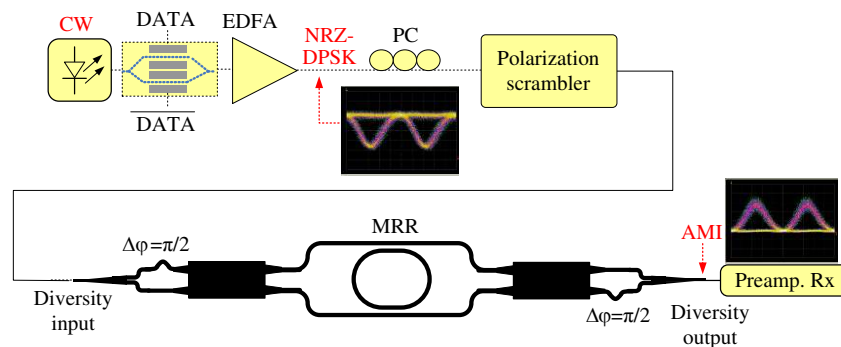

Fig. 4. Experimental setup for Pol-D MRR-based NRZ-DPSK demodulation. The insets show the measured eye-diagrams of the NRZ-DPSK signal, and the demodulated AMI signal obtained at the output of the Pol-D MRR.

Figures 5(a)-5(c) show the demodulation results using the Pol-D MRR with and without polarization scrambler. Clear open eye-diagrams, as shown in Figs. 5(b) and 5(c), are obtained in both cases. Furthermore, a typical AMI spectrum is obtained at the output of the Pol-D circuit, even when the input state of polarization is scrambled. For comparison, a single MRR with the same parameters, but without the Pol-D configuration was also applied for NRZ-DPSK demodulation at the same bit rate. In this case, the demodulated spectrum exhibits the typical features of the AMI format at optimum input polarization, which is no longer the case when the polarization scrambler is applied, as shown in Fig. 5(d). Furthermore, the eye diagram is completely closed when the polarization scrambler is used, as shown in Fig. 5(f), in contrast to the case with optimum polarization illustrated in Fig. 5(e).

Figure 6 shows bit-error-ratio (BER) measurements performed for the signals demodulated by the Pol-D MRR with and without polarization scrambler. A power penalty of 3 dB at a BER of 10^{-9} is found between the signals demodulated with and without (at optimum polarization) the polarization scrambler, which is induced by the residual PDL and PDER. Such residual polarization dependence could be further reduced by increasing the width of the 2×2 MMI to decrease the polarization crosstalk of the PSR [20]. However, error free operation could not be achieved with the polarization scrambler for single MRR demodulation, as can be checked from the closed eye diagram of Fig. 5(f). Consequently our proposed Pol-D scheme is effective at significantly reducing the impact of the polarization dependence of silicon MRRs.
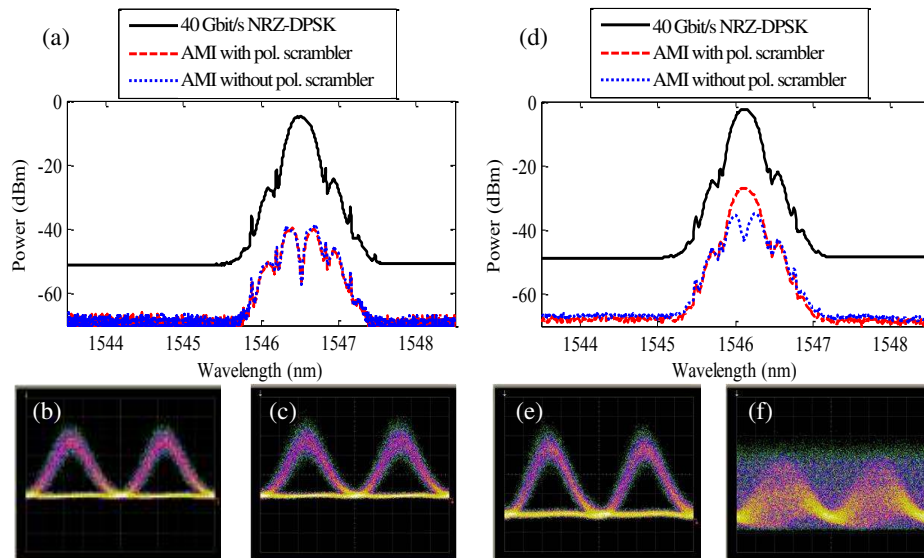

Fig. 5. Measured spectra of the NRZ-DPSK signal, as well as the AMI signals demodulated by the Pol-D MRR (a) and a single MRR (d) with and without polarization scrambling. Measured eye-diagrams of the AMI signal demodulated by the Pol-D MRR without (b) and with (c) polarization scrambling. Measured eye-diagrams of the signal demodulated by a single MRR without (e) and with (f) polarization scrambling.
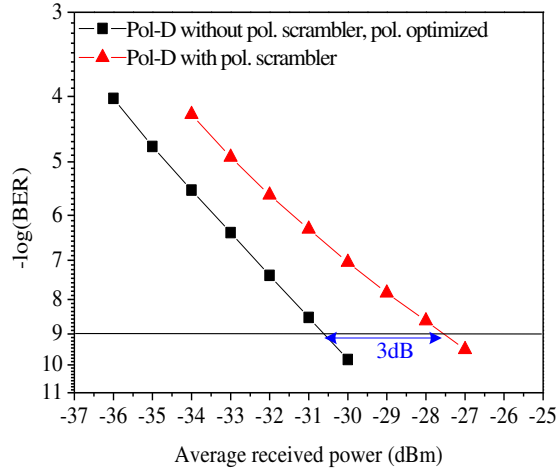
Fig. 6. BER measurements for the AMI signal demodulated by the Pol-D MRR with and without the polarization scrambler.

4. Conclusion

We have reported a simple Pol-D DPSK demodulator on the SOI platform, which is fabricated in a single lithography and etching step. The Pol-D DPSK demodulator shows a lowest insertion loss of 0.5 dB with a low PDL of 1.6 dB and low PDER less than 3 dB. The device is used for NRZ-DPSK demodulation at 40 Gbit/s. System experiments show clear eye-diagrams and only 3 dB power penalty with the proposed Pol-D MRR when the input polarization state is scrambled.