# Polymer Waveguides Enabling Scalable Low-Loss Adiabatic Optical Coupling for Silicon Photonics

Roger Dangel, *Member, IEEE*, Antonio La Porta, *Member, IEEE*, Daniel Jubin, Folkert Horst, Norbert Meier, Marc Seifried, and Bert J. Offrein, *Senior Member, IEEE*

*(Invited Paper)*

***Abstract*—Optically transparent polymer waveguides are employed for interfacing silicon photonics devices to fibers. The highly confined optical mode in the nanophotonic silicon waveguide is transferred to a fiber-matched polymer waveguide through adiabatic optical coupling by tapering the silicon waveguide. The polymer waveguides are either processed onto the silicon photonics wafer or bonded to individual chips. Fibers are interfaced to the polymer waveguides through butt-coupling. We show polarization and wavelength-tolerant fiber-to-chip coupling loss of less than 3.5 dB across the O-band. The polymer waveguide-to-silicon-chip alignment tolerance is 2 $\mu$m for a loss increase of only 1 dB. Reflection losses are well below −45 dB and the scalability to large numbers of channels is demonstrated. These results open a path to broadband and polarization-tolerant optical packaging of silicon photonics devices for ultrahigh bandwidth applications employing wavelength division multiplexing across multiple channels as envisioned for future data-center interconnects.**

***Index Terms*—Optical interconnections, optical waveguides, optical polymers, silicon on insulator technology, optical coupling.**

## I. Introduction

OPTICAL interconnects (OIs) are the enabling technology to sustain the growing performance requirements of both cloud data-center servers and high-performance computers (HPCs) [1], [2]. Compared to electrical interconnects, OIs provide inherent advantages such as a larger bandwidth-distance product, a higher interconnect density, and an improved power efficiency [3].

Integrated CMOS silicon (Si) photonics technology can combine optical and electrical functions on a single chip. Single-mode (SM) Si-photonics chips can be scaled to provide high bandwidth density and can cover the reach of the OIs between and within data-centers [4]. All the Si-photonics functional building blocks required for that purpose have already been demonstrated [5], and coarse wavelength division multiplexing (CWDM) Si-photonics links are commercially available [6]. Nevertheless, OI links based on discrete Si-photonics transceivers suffer from bandwidth-density limitations due to large standardized form-factor housings (e.g., SFP, QSFP) and imply a high assembly cost overhead. To overcome such issues, we suggest a radically different, scalable, and cost-effective integration scheme for Si-photonics chips, as depicted in Fig. 1. Thereby, the Si-photonics chip is co-packaged with the ASIC chip directly on its carrier. SM polymer waveguides (PWGs), designed to realize optical mode matching to SM fibers, are used to couple the optical signals between the Si-photonics chip and SM fibers [7].

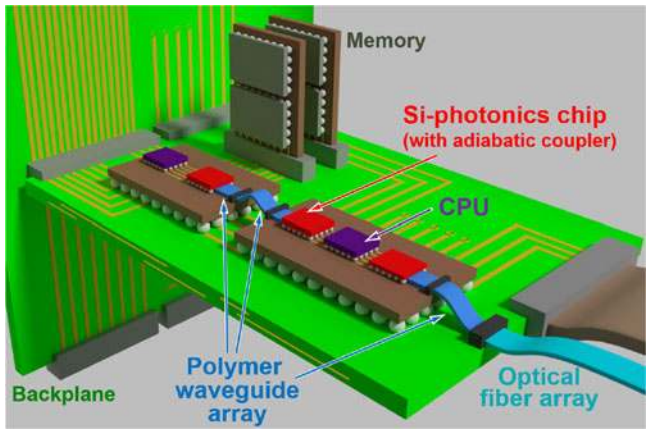


Fig. 1. Tight co-integration of Si-photonics chip and processor on the same carrier substrate enabled by adiabatic optical coupling and polymer waveguides.

Our integration approach is based on adiabatic optical coupling between the Si-waveguides (SiWGs) on the Si- photonics chip and the SM PWGs.

## II. Adiabatic Optical Coupling

In adiabatic optical processes, geometrical changes are sufficiently gradual, such that no energy is transferred from the incoming mode to other modes. This for example means that the fundamental-order mode propagates through the varying structure without transfer of power to any higher-order guided or radiative modes. Adiabatic optical mode transformations have been studied and implemented in the past to determine

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The authors are with the Science and Technology Department, IBM Research–Zurich Laboratory, Rueschlikon 8803, Switzerland. (e-mail: rda@zurich.ibm.com; alp@zurich.ibm.com; dju@zurich.ibm.com; fho@zurich.ibm.com; ynm@zurich.ibm.com; sei@zurich.ibm.com; ofb@zurich.ibm.com).

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the criterion for adiabaticity. Theoretical analysis of adiabatic mode propagation in parabolic-shaped waveguides ('horns') have been carried out [8]. The adiabaticity criterion for the length of a parabolic taper was derived, requiring that the local spreading of the waveguide walls must be slower than the diffraction of the lowest order mode. Operative guidelines for the design of low-loss tapered fiber design were also provided in [9]. Here, a *length-scale* and a *weak power transfer* criterion was derived to compute the minimum taper length required to avoid power transfer from the fundamental order mode to the next, unwanted local mode. Generally, the length-scale of the transition must be much larger than the coupling length between the mode of interest and the closest mode in terms of the propagation constant. For smooth and uniform tapers of length $L$, the adiabaticity criterion can then be expressed by the following formula:

$$L \gg \frac{2\pi}{\beta_0 - \beta_1} \tag{1}$$

where $\beta_0$ and $\beta_1$ are the respective propagation constants of the mode of interest and the closest mode the system could couple to.

Equation (1) indicates that geometrical changes of the structure must be gradual but compared to other approaches, such as directional couplers, does not exhibit a critical length. A consequence is also that adiabatic devices generally are wavelength and polarization-tolerant. The adiabaticity criterion in (1) can be instructively applied to a two-waveguide system in which power is transferred from one waveguide to the other. The adiabatic coupling scheme is for example effectively implemented in III-V-to-Si-photonics hybrid laser integration. Here, the goal is to transfer light between the Si-waveguide and the III-V waveguide. Efficient optical coupling was shown for double-taper structures of the silicon waveguide ends [10], [11].

Adiabatic optical coupling was recently also used for mode-size matching between the sub-micrometer-size SiWG and a standard single-mode fiber for Si-photonics packaging. An adiabatic optical coupling between an array of SiWGs and fiber-matched polymer waveguides (PWGs) was demonstrated experimentally first in [12], followed by other implementations [13]. Subsequently, the fiber array is butt-coupled to the PWGs. Since a scalable I/O interface system for Si-photonics based on the adiabatic coupling of SiWGs and PWGs is the main objective of this paper, a detailed description of this system will be provided in the following section.

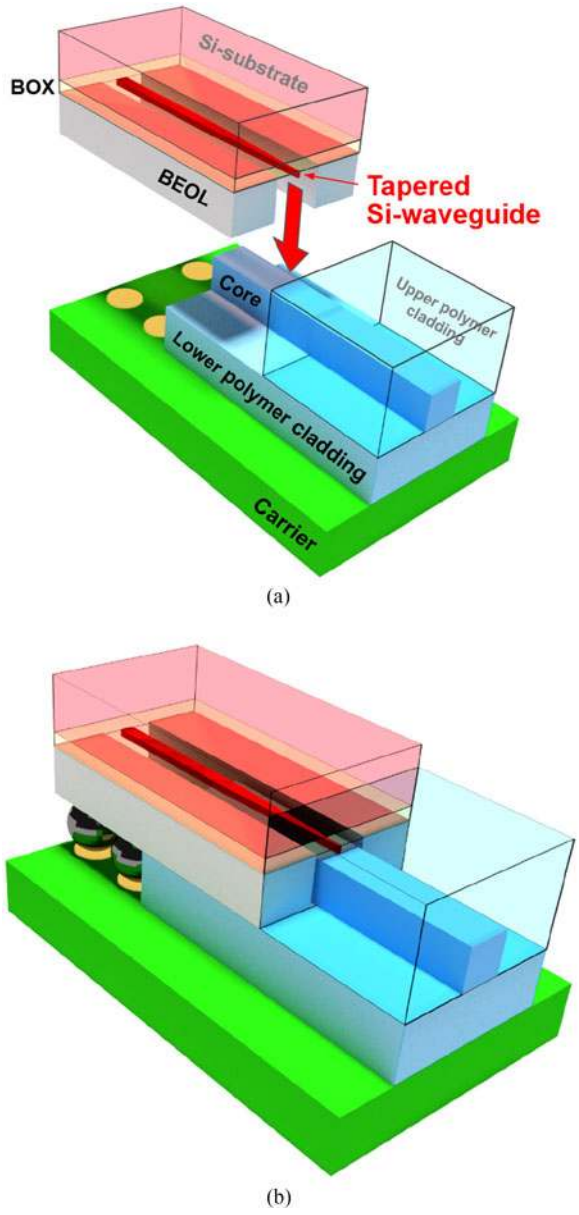


Fig. 2. (a) Flip-chip bonding of Si-photonics chip onto PWG on carrier. Optical coupling as well as electrical contacts can be established in the same flip-chip bonding step. (b) Physical contact between the tapered SiWG and PWG enables low-loss adiabatic optical coupling.

## III. Optical Coupling to Silicon Photonics

### A. Principle of Adiabatic Coupling

To exploit the potential of Si-photonics, the challenge of fiber-to-chip optical coupling needs to be solved as means to interface the Si-photonics chip with the system. Today, mainly grating couplers are applied to convert the highly confined optical mode field of the Si-waveguide to an expanded fiber-matched shape. However, the resonant nature of grating couplers induces strong polarization and wavelength-dependencies. Adiabatic optical coupling from SiWGs to intermediate PWGs is a versatile optical interface to optical fiber arrays with the potential for polarization and wavelength-tolerant operation as well as scalability to large number of optical channels. The physics behind this type of optical coupling is based on the adiabatic transformation of the optical mode from being almost completely confined in the SiWG to being guided in the PWG based on a gradual reduction of the SiWG width. The cores of the SiWGs and PWGs are brought into either direct physical contact or at least in very close proximity to each other. Upon gradually tapering the SiWG, the super-modes (i.e., eigenmodes of the coupled-waveguide system) evolve adiabatically along the coupler. Fig. 2(a) depicts the positioning of the tapered SiWG core on the SM PWG core.

Additional simulations as well as experimental results (see Section VI) show that this approach is tolerant in terms of lateral

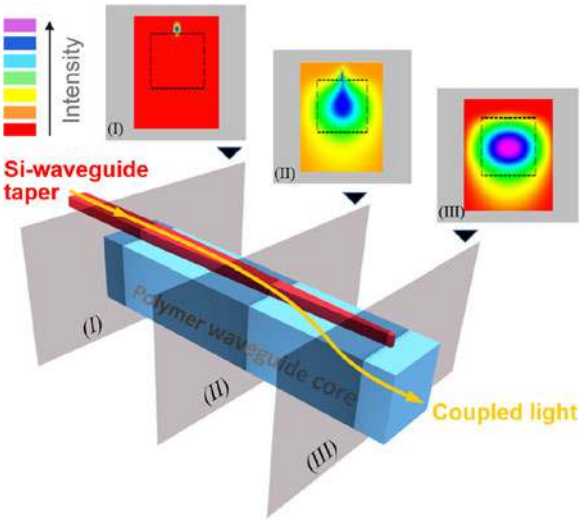


Fig. 3. Optical super-mode evolution in the adiabatic SiWG-to-PWG coupling system. At the onset (left) of the Si-taper, the super-mode is fully confined in the SiWG. At the tip of the Si-taper (right), the light is almost completely localized in the PWG core.

alignment errors and in terms of process variations in dimensions, refractive indices, polarization and wavelength. In contrast to directional coupling, adiabatic optical coupling does not require phase-matching of the SiWG and PWG modes, and their effective refractive indices can be different. The big advantage of adiabatic optical coupling, from an application perspective is the polarization and wavelength tolerant operation. The scalability to a large number of SiWGs and PWGs that can be connected simultaneously in a single bonding step offers assembly and cost advantages and opens opportunities towards applications requiring large channel counts as in future switching and computing systems. Moreover, if the PWGs are deposited on a dedicated interposer or carrier with suitable electrical contact pads, the optical coupling as well as many electrical contacts can in principle be established in the same single flip-chip bonding step, as illustrated in Fig. 2(b).

The schematic in Fig. 3 shows the super-mode field distributions at three waveguides cross-planes (I), (II), (III) and clearly demonstrate the coupling mechanism based on mode transformation: At the input of the taper (I), the super-mode of the coupled silicon-polymer system is completely confined in the SiWG core. In the taper center (II), the super-mode extends over both waveguide cores. And at the output of the taper (III), the super-mode is completely confined in the SM PWG core.

Under the assumptions that (a) the silicon-polymer system exhibits no significant absorptive losses and (b) the taper design fulfills the adiabaticity criterion as described in Chapter II, i.e., the system has no major loss channels, the reciprocity principle between PWG and SiWG applies. In other words, this coupling approach should work from SiWG to PWG as well as from PWG to SiWG.

### *B. Adiabatic Optical Coupling Simulations*

To theoretically determine a suitable design for the envisioned adiabatic coupling system, we performed optical

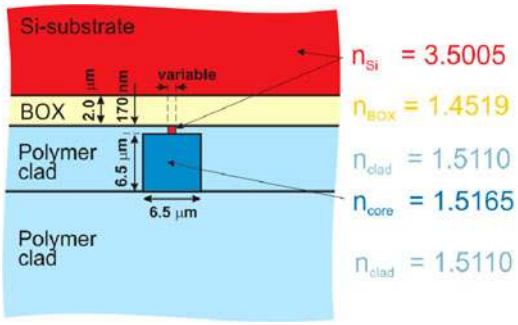


Fig. 4. Cross-sectional schematic of the PWG/SiWG system which was used for adiabatic coupling simulations performed at wavelength $\lambda = 1310$ nm.

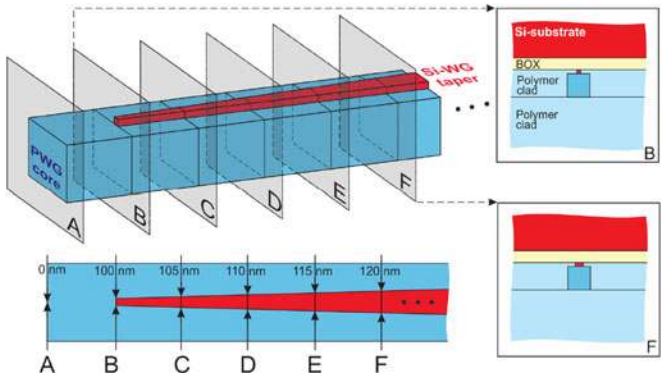


Fig. 5. Schematic illustrating our simulation approach, where the optical overlap of consecutive mode-field distributions was computed for every 5 nm Si-taper width increment.

simulations for a waveguide system as shown in Fig. 4. We used the following parameters: The PWG core has a refractive index of $n_{core} = 1.5165$, with a refractive-index step of $\Delta n = 0.0055$ with respect to the PWG cladding and is designed with a square-shaped cross-section of 6.5 $\mu$m side length. The choice of refractive indices and dimensions is guaranteeing SM operation. The SiWG width is linearly tapered from a 100-nm wide tip to the 350-nm wide standard SiWG, as shown in Fig. 5. In our simulations, the optical system modes for both TE and TM polarization and for wavelength $\lambda = 1310$ nm were calculated using a commercial software (Field Designer by Phoenix) based on the eigenmode expansion method. To derive the shape of the SiWG, we followed the *single-step loss* method for adiabatic mode transformations in waveguide adaptors proposed in [14]. In our case, the overlap between consecutive mode-field distributions was computed for every 5 nm Si-taper width step, as plotted in Fig. 6.

In Fig. 6, the dip of the calculated optical overlap, for TE at 175 nm taper width and for TM at 185 nm, indicates the taper width regime where the corresponding modal field and effective index of the super-mode change the most. It is the taper width regime where the main energy transfer between PWG and SiWG occurs.

### *C. Taper and Coupler Test-Unit Design*

Based on the simulation results for the optical overlaps, we were able to design suitable Si-taper couplers. We had to take

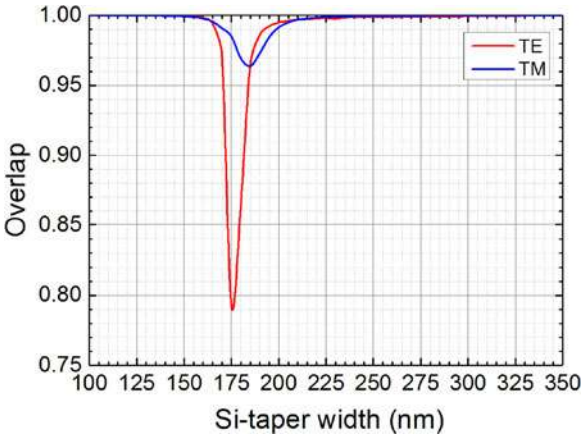


Fig. 6. Simulation results for polarization-dependent optical overlap of consecutive mode-field distributions of the PWG/SiWG system, obtained for wavelength $\lambda = 1310$ nm.

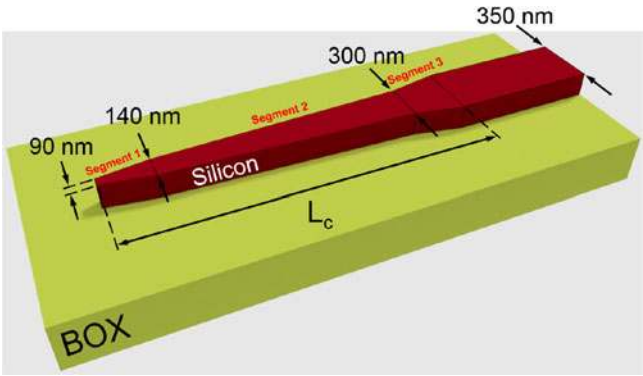


Fig. 7. Schematic of designed adiabatic Si-taper consisting of three linear segments with different width increments and total taper length $L_c$.

into account that for taper-width regions with overlap values $\ll 1$, part of the energy could be transferred to the nearest mode. From the mode-field simulations, we computed the effective index difference $\Delta N_{\text{eff}}$ between the fundamental and the first-order TE super-mode at a Si-taper width of 175 nm to be $\Delta N_{\text{eff}} = 0.00308$, around this region. Applying the adiabaticity criterion reported previously in Eq. (1), we found that the SiWG-taper length L must satisfy $L \gg 425$ $\mu$m. Outside the taper-width region around 175 nm, the overlap change is much smaller, corresponding to a larger difference in the propagation constants of the fundamental and the first-order super-mode. Consequently, we used a three-segment linear taper of total length $L_c$ with the smoothest taper slope for SiWG widths between 140 nm and 300 nm, as shown in Fig. 7.

To determine the optical performance, i.e., the efficiency of a single adiabatic optical coupling process between our designed Si-taper and the corresponding PWG, we designed an S-shaped coupling test-unit, as depicted in Fig. 8. This test-unit consists of a PWG-to-SiWG adiabatic taper coupler, an inverted SiWG-to-PWG adiabatic taper coupler, and an S-shaped connection in between. The S-shaped SiWG connection is used to spatially separate adiabatically coupled light from the light remaining in the initial PWG.

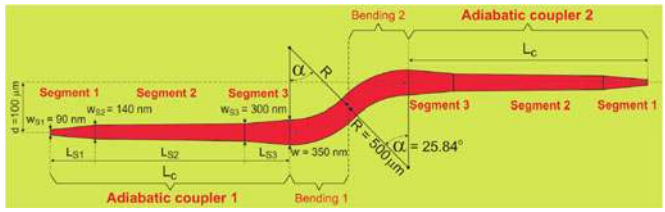


Fig. 8. Layout of S-shaped coupler test-unit with two identical adiabatic taper couplers and 4 PWGs (not shown) to determine coupling efficiency.

The design parameters d, $\alpha$, R, w, $w_{S1}$, $w_{S2}$, and $w_{S3}$ were kept constant in all test units. However, the total taper length $L_c$ was varied from 0.2 mm up to 2.8 mm in increments of 0.2 mm, while the taper segment lengths $L_{S1}$, $L_{S2}$, and $L_{S3}$ were adapted according the relations $L_{S1} = L_{S3}$ and $L_{S2}$: $L_{S1} = 23$ (e.g., $L_c = 1500$ $\mu$m, $L_{S1} = L_{S3} = 60$ $\mu$m, $L_{S2} = 1380$ $\mu$m).

## IV. Single-Mode Polymer Waveguide Technology

In the last few years, we have established a SM PWG technology operating in the O-band (around $\lambda = 1310$ nm) and C-band (around $\lambda = 1550$ nm), extending our existing low-loss MM polymer waveguide technology developed for $\lambda = 850$ nm [15], [7]. The materials of choice are siloxane-based polymers from Dow Corning Corporation (DCC) because of its excellent optical properties and straight-forward processing sequence. It satisfies also a key requirement to be compatible with the system-level integration envisioned in Fig. 2: Thermal stability and compatibility with solder reflow and flip-chip bonding processes. Low absorption at wavelength $\lambda = 1310$ nm and 1550 nm, with a core-cladding refractive-index contrast of $\Delta n \approx 0.005$–$0.008$, provides propagation losses down to less than 0.4 dB/cm at 1310 nm and SM operation of square-shaped waveguides of 6–8 $\mu$m side length. The geometry and the refractive-index contrast were designed to provide low-loss optical coupling to standard SM fibers [7].

Our SM PWG can be processed on different substrates. Examples are large rigid or flexible panels, carrier substrates, and flexible sheets. In the last case, we can further laminate ultra-thin flexible sheets containing SM PWG in or onto another substrate or stack. Additionally, SM PWGs can be processed directly on wafers or on chips. Polymer layer deposition can be performed either by doctor-blading or by spin-coating, depending on the size of the substrate. Both the cladding and the core layers are UV-curable and can be patterned. To this end, a UV-laser direct-writing process or a proximity-mask-lithography is applied, followed by a solvent-based wet-chemical development. Finally, a temperature step cures all layers in the waveguide stack and provides long-term stability. The complete processing sequence is depicted in Fig. 9. As examples, Figs. 10–12 show SM PWGs realized on panel-size (up to 450 mm $\times$ 300 mm), wafer-size, and chip-size substrates.

## V. Implementation of Silicon-to-Polymer-Waveguide Adiabatic Optical Coupling

For the demonstration and detailed analysis of the adiabatic optical coupling concept, we pursued two approaches to

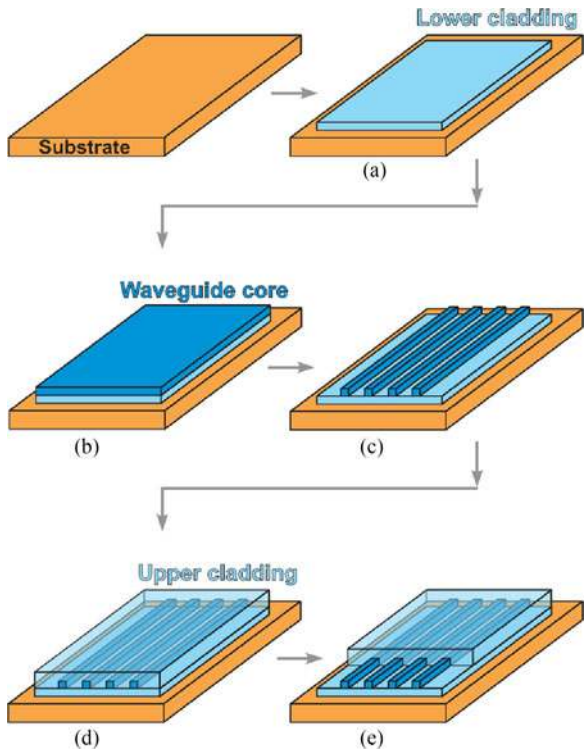


Fig. 9. Schematic illustrating fabrication process of SM PWGs. (a) Deposition of lower cladding followed by UV-flood curing. (b) Deposition of waveguide core layer. (c) Waveguide patterning by UV-laser direct-writing or proximity-mask UV-lithography, followed by solvent-based development. (d) Deposition of upper cladding. (e) UV-flood curing (or optionally, for adiabatic coupling based on flip-chip bonding: UV-patterning and solvent-based development of upper cladding). Finally, thermal curing step.

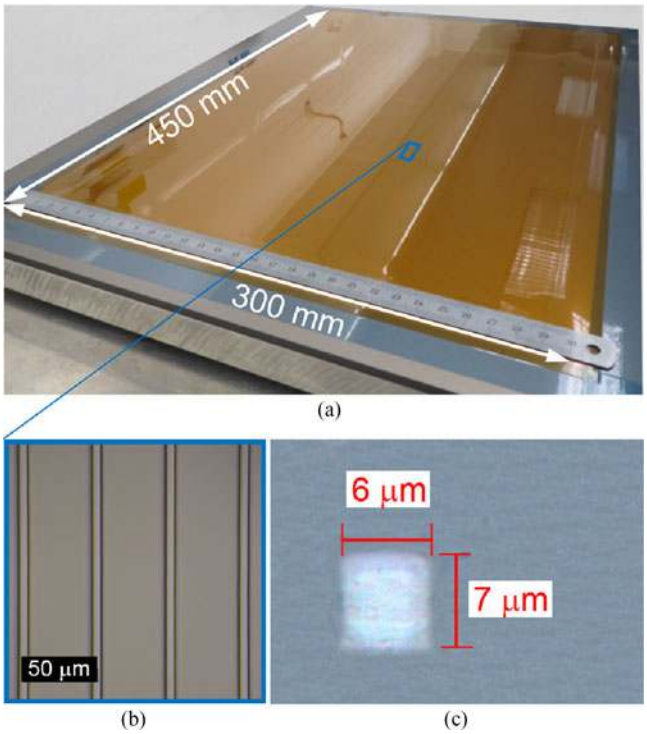


Fig. 10. Panel-size fabrication. (a) Photograph of SM PWGs realized on panel-size flexible substrate, (b) Microscopic blow-up of SM PWG array with 50 $\mu$m waveguide pitch, and (c) corresponding PWG cross-section of 6 $\mu$m $\times$ 7 $\mu$m.

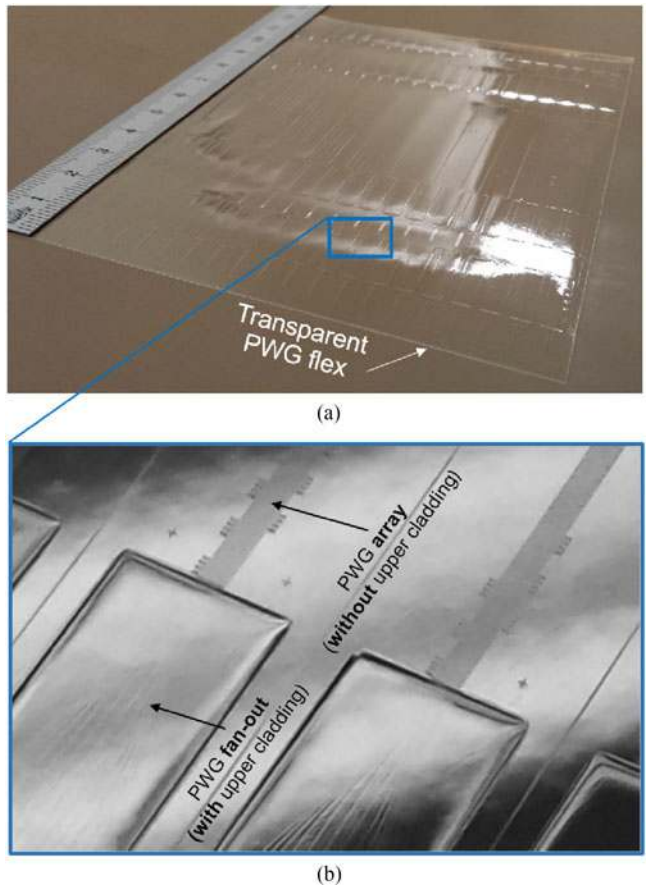


Fig. 11. Wafer-size fabrication. (a) Photograph of SM PWG fan-out structures on wafer-size flexible transparent substrate with (b) locally removed upper cladding required for flip-chip-bonding-based adiabatic optical coupling.

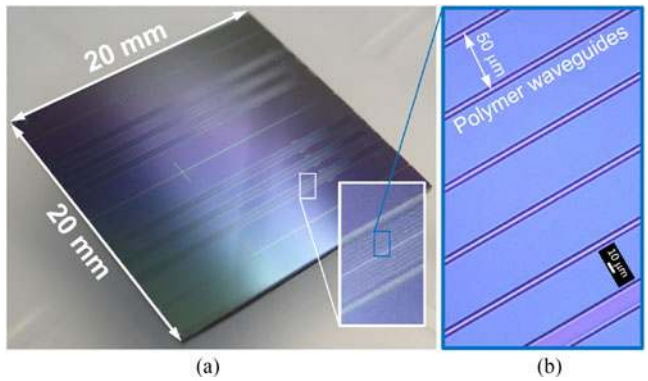


Fig. 12. Chip-size fabrication. (a) Photograph of Si-photonics chip with PWGs directly processed on top for adiabatic optical coupling test-units. (b) Corresponding microscopic blow-up of 50 $\mu$m spaced polymer waveguides.

implement the PWG/SiWG coupling devices: (A) processing the PWGs directly on the Si-photonics chip [16] and (B) assembling the PWG/SiWG system by flip-chip bonding [17]. Because of the easier process steps and the higher accuracy of the PWG-to-SiWG alignment by mask-lithography instead of flip-chip bonding, we started with direct-processing. The direct-processing method acts as a benchmark, providing optimum conditions such as accurate alignment and an ideal polymer-on-

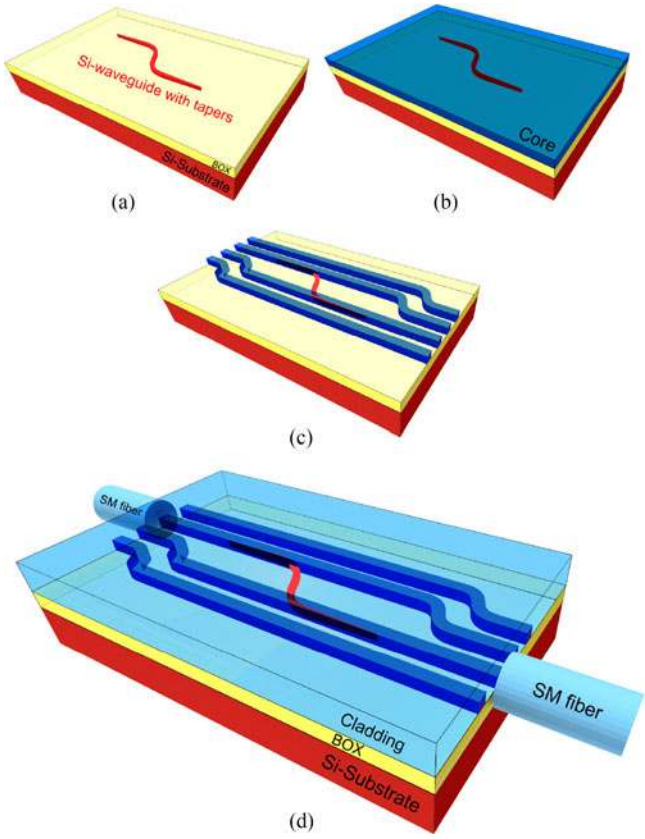


Fig. 13. Processing steps for direct-processing of PWGs on Si-photonics chip. (a) e-beam lithography and dry-etching of Si-photonics chip to obtain S-shaped coupler test-units. (b) Spin-coating of UV-sensitive PWG core layer. (c) UV-mask-exposure and wet-chemical development of PWG cores. (d) Spin-coating of upper cladding and UV-curing followed by final bake.

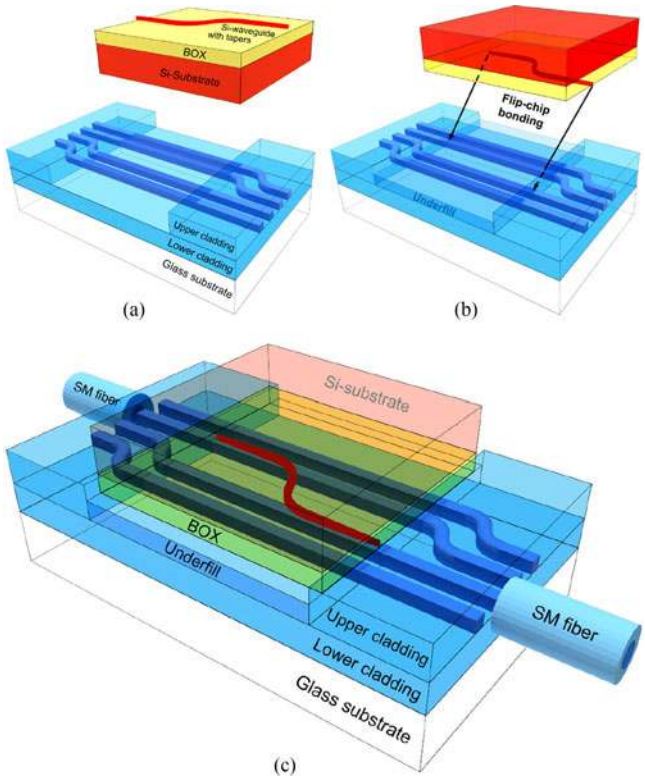


Fig. 14. Processing steps for PWG/SiWG adiabatic coupling system based on flip-chip bonding. (a) Fabricating SiWG with S-shaped coupler test-unit and PWG with opening in the upper cladding. (b) Depositing UV-sensitive optical adhesive in the opening. Flip-chip bonding SiWG chip onto PWG chip. (c) Fixing PWG/SiWG assembly by UV-exposure through glass substrate.

silicon interface. However, our real interest is in exploiting the flip-chip assembly method which is compatible to standard Si-photonics chip processing and packaging.

For the fabrication of the required Si-photonics coupler test-units presented in Section III, we structured 4" SOI wafers having 2-$\mu$m-thick buried oxide (BOX) by means of electron-beam lithography and anisotropic dry-etching. The resulting SiWGs were 350 nm wide outside of the taper regions, while the width along the three-segment Si-tapers varied from 90 nm to the standard width of 350 nm. In terms of SiWG height, we tested 158 nm and 170 nm, respectively. SiWG width and height were chosen to guarantee SM operation at a wavelength $\lambda = 1310$ nm. After the waveguide etching step, the wafers were diced into suitable dies of (a) $20 \times 20$ mm$^2$ size for subsequent direct-processing of PWGs or (b) $10 \times 15$ mm$^2$ size for flip-chip bonding.

### A. Direct-Processing of PWGs on Silicon-Photonics Chip

In the direct-processing approach, the SM PWGs were fabricated according to the process steps illustrated in Fig. 13. A layer of DCC core polymer was spin-coated on the $20 \times 20$ mm$^2$ Si-photonics test dies. The spin-coating speed was chosen to obtain a layer thickness of 6 $\mu$m. To structure the polymer waveguide cores, a proximity-mask UV-lithography was applied followed by a post-exposure bake at 110 °C for 2 min. The polymer core material acts as a negative photoresist, so a mask with openings corresponding to the polymer waveguide cores was precisely aligned to the SiWGs. The opening widths and the UV dose (180 mJ/ cm$^2$) were tuned to obtain a polymer waveguide core width of 6 $\mu$m after a subsequent solvent-based wet-chemical development step. Afterwards, a 20-$\mu$m-thick layer of cladding material was spin-coated over the entire chip and a UV-flood exposure was applied to crosslink the polymer. Finally, the chip was placed on a hot-plate at 200 °C for 1 h to fully cure all layers in the waveguide stack and to provide long-term stability.

### B. Flip-Chip Bonding of Si-Photonics Chip to PWG

In case of the adiabatic coupling approach using flip-chip bonding, SM PWGs with a planar lower cladding of 25 $\mu$m thickness and a partially opened upper cladding with the same thickness were fabricated on a 6" glass wafer. The process steps are depicted in Fig. 14. The upper cladding pattern realized by proximity-mask UV-lithography was designed to have windows with arrays of PWG cores not covered by the upper cladding, thus allowing physical contact between SiWG tapers and PWG cores to enable adiabatic light transfer. After the PWG manufacturing, the glass wafer was singularized with a standard wafer-dicing saw into $25 \times 30$ mm$^2$ dies containing PWG arrays with 50 $\mu$m I/O waveguide pitch. However, instead of using

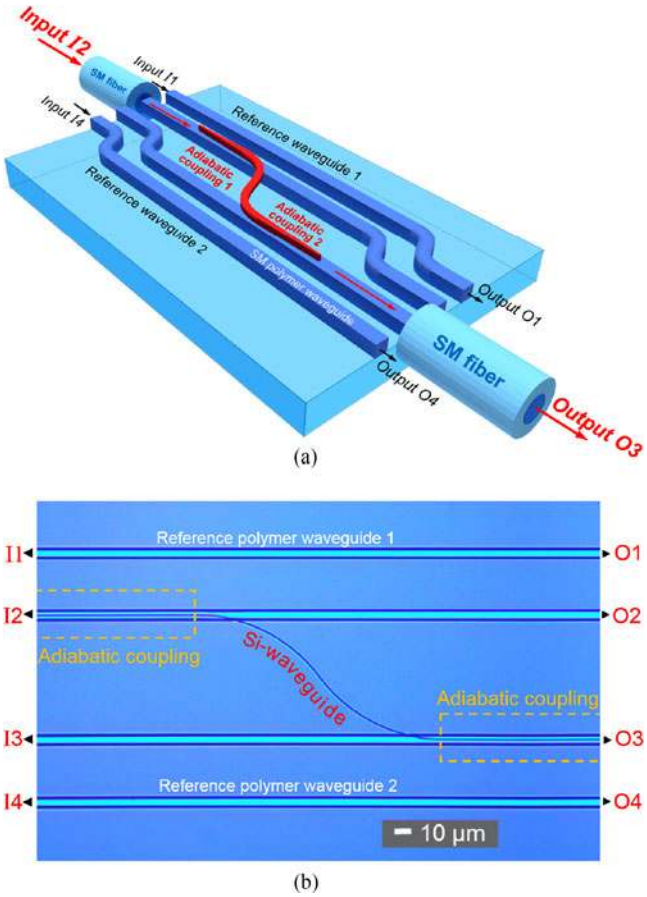


Fig. 15. (a) Scheme depicting experimental configuration to determine optical performance of realized adiabatic coupling systems. (b) Top view micrograph taken through glass substrate of flip-chip-bonded PWG/SiWG assembly shows how accurate the SiWG tapers can be aligned to the corresponding PWGs "I2-O2" and "I3-O3."

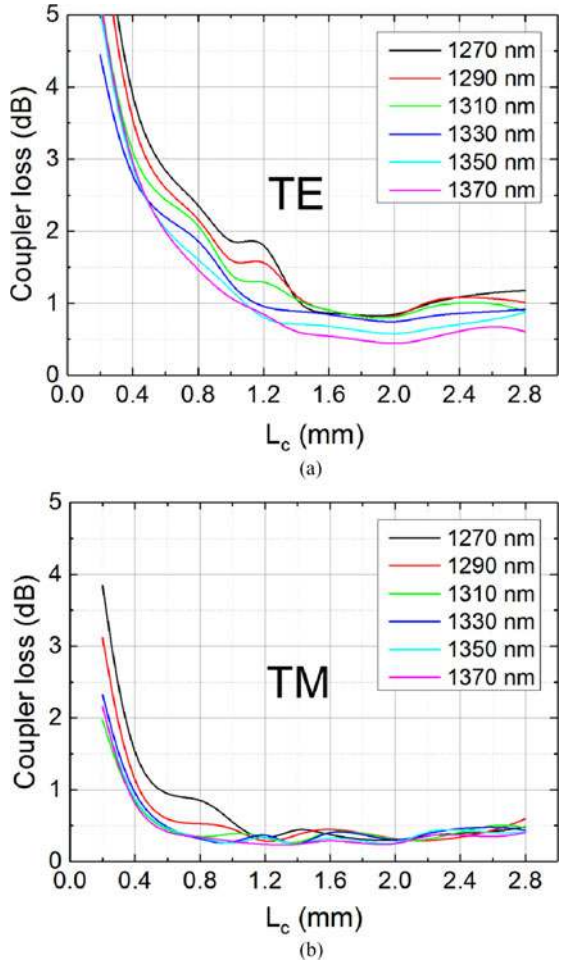


Fig. 16. Coupler loss vs. taper length $L_c$ for PWG/SiWG couplers realized by direct-processing. The measurements were performed for discrete wavelengths in the O-band and for (a) TE-polarization as well as (b) TM-polarization.

a blade and sawing settings for Si-wafers, we used a dedicated blade for glass substrates with very slow feed rate of 1.0 mm/s.

The $10 \times 15$ mm$^2$ Si-photonics dies containing S-shaped test-units were aligned and assembled with a flip-chip bonder to the PWG structure. Between the PWG chip and the SiWG chip a UV-curable adhesive was applied as an optical underfill and UV-exposed through the glass substrate.

## VI. Experimental Results of Adiabatic Coupling

### A. Experimental Configuration and Measurement Principle

For all results in this Section VI, the same experimental configuration, as shown in Fig. 15, and measurement principle could be applied. At the input port I2, on the left, light is coupled from a SM fiber into a first PWG. It is then adiabatically coupled to the SiWG. The SiWG transports the signal to the adjacent PWG through an S-bend. A second adiabatic taper transfers the light to a second PWG where the light is finally coupled out at output port O3 to a second SM fiber. Adjacent reference PWGs "I1-O1" and "I4-O4" with no Si-photonics coupler in between act as references to derive the incremental loss originating from the Si-photonics couplers.

In our measurements, the definition of the adiabatic coupling loss relies on the comparison of the transmitted power through the PWG/SiWG/PWG system with the transmitted power through a bare reference PWG, as depicted in Fig. 15. In this definition, we assume that due to the short SiWG coupler length (few mm) the propagation loss in the PWG/SiWG/PWG system (30 mm long) is approximately the same as in the reference PWG.

To achieve efficient and reproducible butt-coupling between SM fibers and PWGs in our optical measurements, we applied index matching fluid at the input as well as at the output ports. Typical butt-coupling losses were in the order of 0.3 dB.

### B. Coupler Loss Versus Taper-Length and Wavelength

The dependence of the coupler loss on the total taper length $L_c$ and the wavelength was experimentally determined for PWG/SiWG coupler chips which had been realized by direct-processing as well as by flip-chip-bonding.

The results for direct-processing are shown in Fig. 16. The coupler loss was determined for taper lengths $L_c$ ranging from 0.2 to 2.8 mm in 0.2 mm lengths increments. The measurements

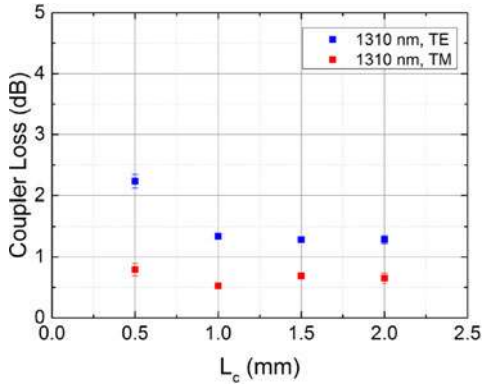


Fig. 17. Coupler-loss vs. taper length $L_c$ for flip-chip-bonded PWG/SiWG couplers. Measurement was done for given wavelength $\lambda = 1310$ nm and for both polarizations.

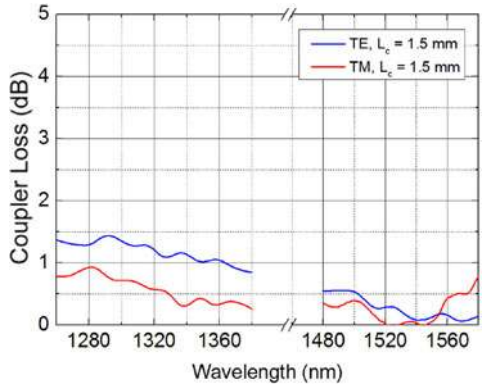


Fig. 18. Coupler loss vs. wavelength $\lambda$ for flip-chip-bonded PWG/SiWG couplers. For given taper length $L_c = 1.5$ mm, coupler loss was measured over entire O-band as well as C-band and for both polarizations.

were performed at discrete wavelengths $\lambda = 1270, 1290, \ldots,$ 1370 nm in the O-band. For taper lengths $L_c$ between 1.6 mm and 2.4 mm, we found that over the entire wavelength range of the O-band the coupler loss is <1.1 dB for TE-polarization and <0.5 dB for TM-polarization, respectively.

In case of the flip-chip-bonded PWG/SiWG coupler assemblies, the taper-length dependence was measured for four different taper lengths $L_c = 0.5$, 1.0, 1.5, and 2.0 mm at the given wavelength $\lambda = 1310$ nm, as shown in Fig. 17. Furthermore, the results of the coupler-loss-versus-wavelength measurement for fixed coupler length $L_c = 1.5$ mm are summarized in Fig. 18.

For taper lengths $Lc \geq 1.0$ mm and $\lambda = 1310$ nm, the coupler loss was found to be <1.4 dB for TE-polarization and <0.6 dB for TM-polarization, respectively. The larger loss of the TE mode can be explained by its more abrupt transition from the PWG to the SiWG upon change of the SiWG width, as shown in Fig. 6. The measurements revealed further, that our coupler design provides a coupler loss of less than 1.5 dB over the entire O-band and even over the entire C-band for both polarizations.

### C. Alignment Tolerance of Adiabatic Coupling Approach

To evaluate the tolerance of the lateral SiWG-to-PWG alignment process, a PWG/SiWG test-unit was designed where the

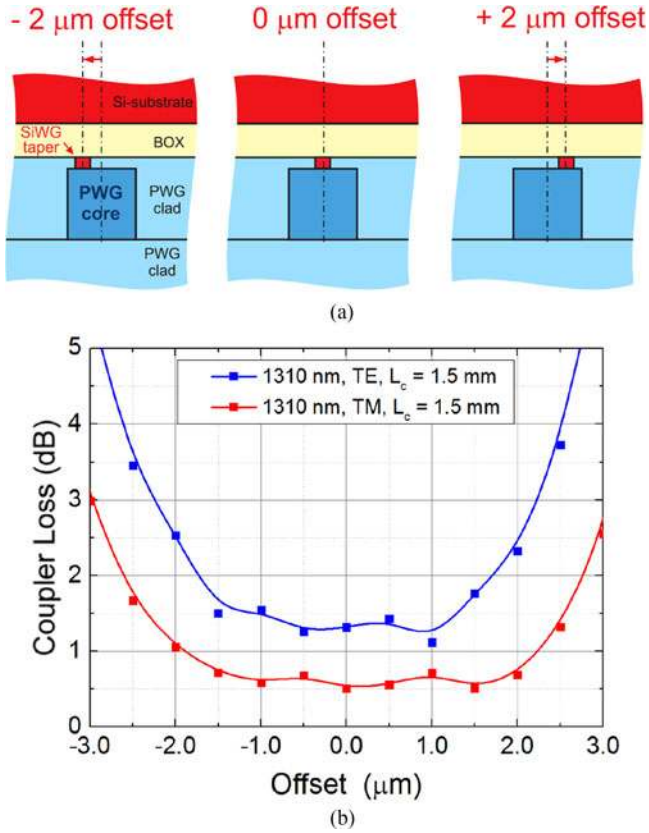


Fig. 19. (a) Cross-sectional schematics of PWG/SiWG flip-chip assembly depicting different alignment offsets between SiWG and PWG. (b) Results of misalignment-tolerance measurements for an adiabatic taper length of $L_c = 1.5$ mm, for given wavelength $\lambda = 1310$ nm, and for both polarizations.

SiWGs and PWGs exhibit on purpose a lateral offset ranging from $-3$ $\mu$m to $+3$ $\mu$m. Our measurements revealed an additional loss of about 1 dB within a lateral misalignment of $\pm 2$ $\mu$m, as shown in Fig. 19.

### D. Insertion Loss Measurements

We also evaluated the overall fiber-to-PWG-to-SiWG loss contribution, i.e., the insertion loss IL per facet (IL/facet). The IL/facet is depicted in Fig. 20 for the O-band and for both polarizations. The IL/facet at $\lambda = 1310$ nm was found to be <3.5 dB for TE-polarization and <3.0 dB for TM-polarization.

All measurements of this section were obtained with PWGs made of a new core polymer test formulation from DCC. Propagation loss measurements based on bare reference PWGs "I1-O1" and "I2-O2" revealed, that this test material had a somewhat increased propagation loss $\Gamma$ of about 1.5 dB/cm. Consequently, the loss contributions for the total connection from the SiWG to the fiber for TE-polarized light are: 1.5 dB adiabatic optical coupler loss +1.5 dB loss over 1 cm of polymer waveguide +0.5 dB polymer waveguide-to-fiber coupling loss. In former experiments with another core polymer formulation from DCC we had already demonstrated a propagation loss $\Gamma \leq 0.4$ dB/cm at $\lambda = 1310$ nm for both polarizations, as presented in Fig. 21. In consequence, we assume that by using this low-loss core

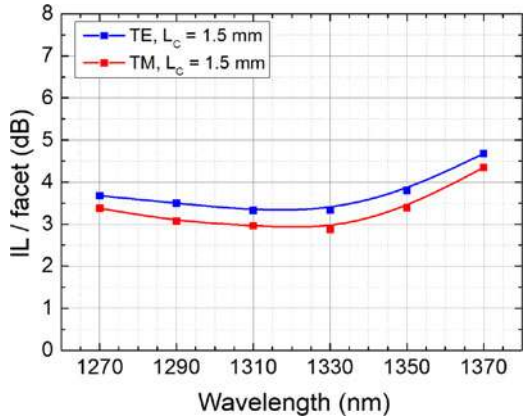


Fig. 20. Insertion loss per facet (IL/facet) vs. wavelength $\lambda$ for flip-chip-bonded PWG/SiWG couplers with given taper length $L_c = 1.5$ mm.

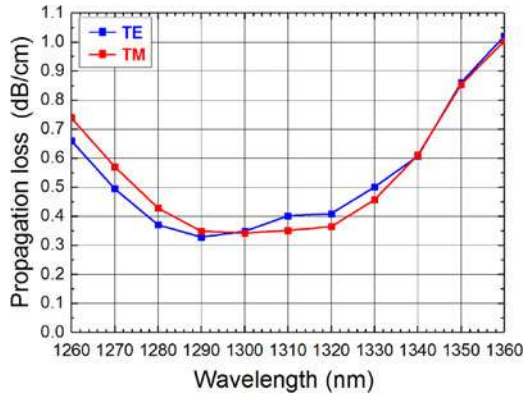


Fig. 21. Results of former propagation loss measurements for SM PWGs based on low-loss core polymer from DCC.

polymer formulation for the PWG/SiWG couplers described, we could reduce the IL/facet values of Fig. 22 by about 1.5 dB.

### *E. Scalability to High Channel Count*

To prove the scalability of our Si-photonics interfacing concept to a high optical channel count, PWG/SiWG chips with a large number of coupler test-units were realized. Fig. 22 shows a dedicated flip-chip bonded PWG/SiWG assembly with 186 optical I/Os, whereof 94 are used for the adiabatic couplers and 92 for the PWG references. The schematic in Fig. 23 illustrates the corresponding PWG/SiWG coupler arrangement exhibiting different total taper lengths $L_c = 0.5$, 1.0, 1.5, 2.0, 2.5, and 3.0 mm.

For a set of loss measurements based on one and the same PWG/SiWG coupler assembly, as shown in Figs. 22 and 23, we performed a statistical analysis of the insertion loss per facet. Overall, 25 PWG/SiWG coupler test-units with 50 optical coupler I/Os were characterized. The results of this statistical IL/facet study are shown in Fig. 24. For $L_c \geq 1.0$ mm and $\lambda = 1310$ nm, an average value <IL/facet> of 3.4 dB for TE-polarization and 2.5 dB for TM-polarization, respectively, was found.

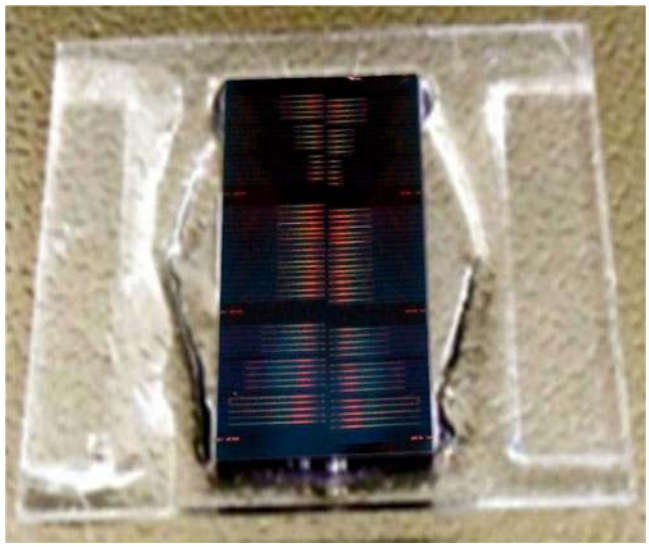

Fig. 22. Photograph of flip-chip-bonded PWG/SiWG assembly. Because the PWG chip lies on top of the SiWG chip, arrays of S-shaped test-units with different total taper lengths $L_c$ are visible through transparent PWG chips.

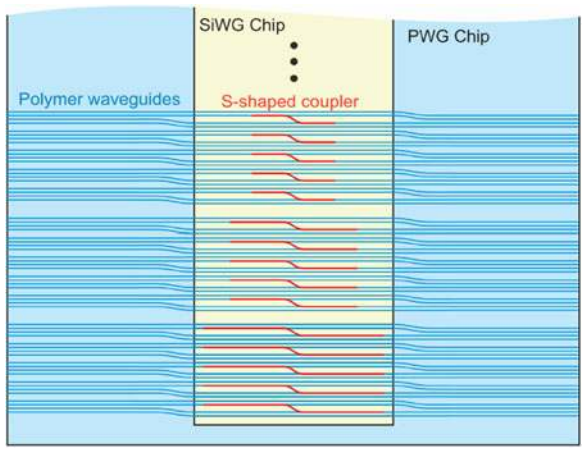


Fig. 23. Schematic of the multiple coupler test-unit design used for large optical I/O count test.

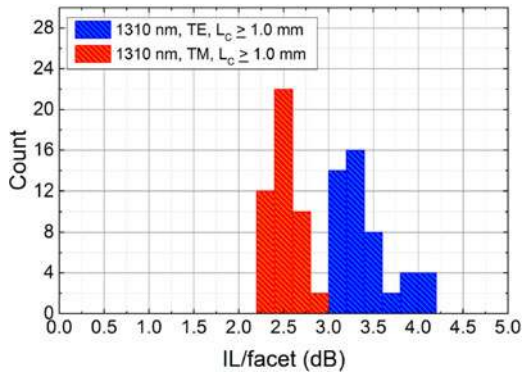


Fig. 24. Polarization-dependent IL/facet occurrences for a total of 50 optical I/Os of couplers with $L_c \geq 1.0$ mm.

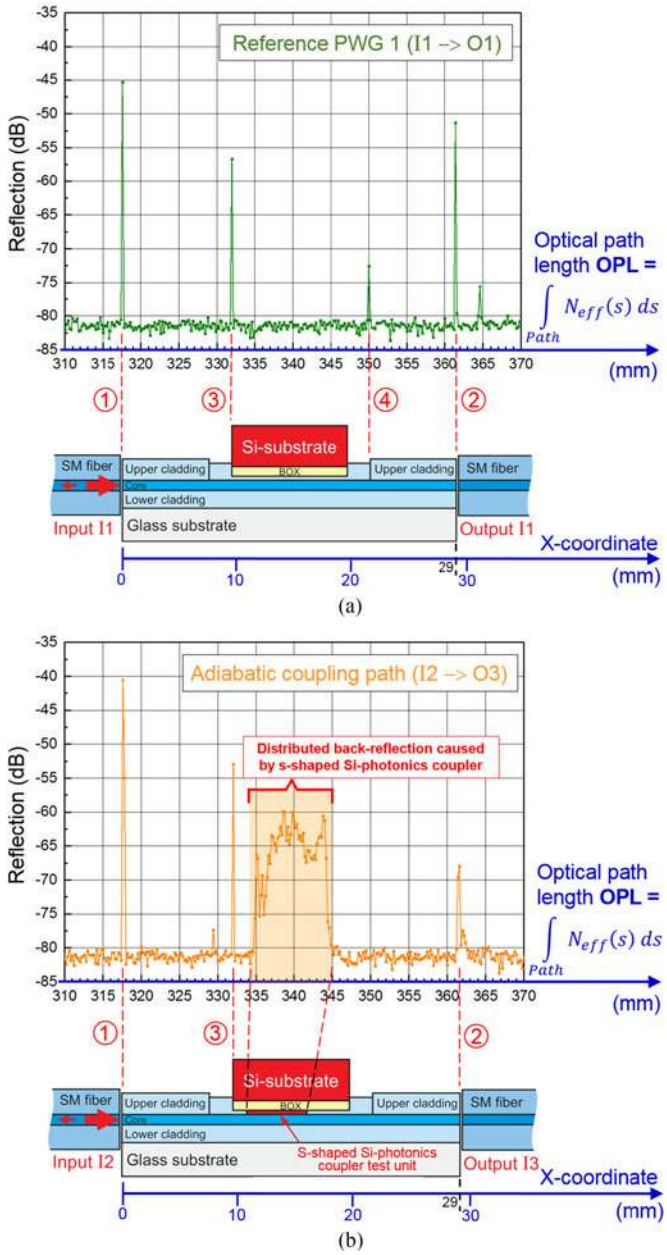


Fig. 25. Reflectometer-measurement results for wavelength $\lambda = 1310$ nm and TE-polarization. (a) Reflection vs. optical path through reference PWG. (b) Reflection vs. optical path (I2 → O3) through S-shaped coupler system with taper length $L_c = 2.5$ mm.

### F. Back-Reflection Measurements

Optical back-reflections in Si-photonics systems can be a serious issue when coupling to a laser source. Therefore, we performed optical reflection measurements at wavelength $\lambda = 1310$ nm for the flip-chip bonded samples. A high-resolution reflectometer was used (HP 8504B). Fig. 25 shows the optical power reflections as a function of the position in the optical path. The reflection peaks were mapped to the actual setup and we resolved the points were the reflections occur in the physical propagation path by comparison with the measured reflections of a reference waveguide next to it. This can be seen in the schematic of the tested system below the measurement plots in Fig. 25 for TE-polarization. The TM-polarization presents lower reflections along the path than TE-polarization, as expected by the smoother TM-modal transition, as shown in Fig. 6. The magnitude of the back-reflections along the optical path is $< -45$ dB for both polarizations and hence represents no issue for connecting these coupling structures to a laser source.

## VII. Conclusion

Adiabatic optical mode-transfer between nanophotonic silicon waveguides and polymer waveguides was demonstrated to be a low-loss and polarization-tolerant fiber-to-silicon photonic-chip coupling method. The broadband capability of this technology provides a path towards larger per channel bandwidth interfacing enabling course wavelength division multiplexed signals to be coupled between a silicon chip and fibers. The scalability to assembling a large number of channels is especially important for large radix switches as a means to flatten the data-center architecture. Furthermore, this technology is compatible with standard flip-chip processes and hence enables the co-packaging of silicon photonics chips on the same carrier substrate as the processor or switch chip. The tight integration of electronics and photonics is an important development to improve power efficiency of data-center interconnects and enable the performance required for future applications.

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**Roger Dangel** received the Diploma degree in physics and the Ph.D. degree in natural sciences from the Swiss Federal Institute of Technology (ETHZ), Zurich, Switzerland, in 1991 and 1997, respectively.

From 1998 to 2000, he was with the Swiss Center for Electronics and Microtechnology, Switzerland. In 2000, he joined the IBM Research – Zurich Laboratory as a Research Staff Member of the Photonics Group. Since 2002, he worked in the field of optical interconnects. His main focus was the development of a single-mode and multimode optical polymer waveguide technology to be used for electro-optical printed circuit boards and the silicon photonics packaging and integration. Just recently, the Photonics Group was changed into the new Neuromorphic Devices and Systems Group, where he is now also involved in the development of hardware for neuromorphic systems.

**Antonio La Porta** received the Master's degree in electrical engineering from Unversita' di Catania, Catania, Italy, in 2003, and the Ph.D. degree in electronics and communications engineering from Politecnico di Torino, Turin, Italy, in 2008.

From 2008, he worked with the R&D department of Linkra (Compel Group), where he was responsible for the design of high-speed electro-optical transceivers exploiting novel modulation formats. Since 2010, he has been a Research Staff Member at IBM Research–Zurich Laboratory, Rueschlikon, Switzerland, where he was involved in the silicon photonics packaging and integration. He is currently focusing on neuromorphic hardware and architectures.

**Daniel Jubin** received the engineering degree in optronics from the Ecole Nationale Supérieur des Sciences Appliquées et de Technologie in Lannion, Lannion, France, in 1993.

Until 1997 he worked for a spin-off with the Swiss Federal Institute of Technology of Zurich, developing all solid-state lasers for ultrashort pulse generation. He then joined JDS-Uniphase, where he participated in developing high power pump laser-diodes for erbium-doped fiber amplifiers. In 2001, he joined the IBM Research – Zurich Laboratory, Rueschlikon, Switzerland, where he contributed to silicon oxynitride waveguide efforts. He then moved to the Micro- and Nanofabrication team, later to the Photonics Group working on the polymer waveguide connectorization and on silicon photonics. He is currently focusing on neuromorphic hardware.

**Folkert Horst** received the M.S. degree in applied physics and the Ph.D. degree in electronics engineering from the University of Twente, Enschede, The Netherlands, in 1992 and 1997, respectively.

In 2000, he joined the IBM Research–Zurich Laboratory, Rueschlikon, Switzerland and became a Research Staff Member. His research interests include integrated optic components for data communication and sensing and analog hardware for neuromorphic data processing.

**Norbert Meier** was born in Uster, Zürich, Switzerland, in 1973. He received the Engineer FH degree in data analysis and process design from the Zurich University of Applied Sciences, Winterthur, Switzerland, in 2004 and the M.S. degree in micro- and nanotechnology from the University of Applied Science in Vorarlberg (FHV), Dornbirn, Austria, in 2006.

**Marc Seifried** received the B.Sc. and M.Sc. degrees in physics from the Technical University Berlin, Berlin, Germany, in 2010 and 2014, respectively. He is currently working toward the Ph.D. degree at IBM Research–Zurich Laboratory, Rueschlikon, Switzerland, on electro-optical integration of III-V lasers on silicon photonics.

In 2014, he joined the IBM Research–Zurich Laboratory. His main research interests include design and processing/fabrication.

**Bert Offrein** (SM'12) received the Ph.D. degree in nonlinear integrated optics from the University of Twente, Enschede, The Netherlands, in 1994.

He then joined IBM Research–Zurich Laboratory, Rueschlikon, Switzerland, and contributed to establishing and commercializing adaptive integrated optical technology for DWDM networks. From 2004 to 2016, he was managing the Photonics Group, addressing optical interconnects for computing systems. Since 2016, he has been leading the Neuromorphic Devices and Systems Group, addressing cognitive hardware for accelerating neural network learning. He is a principal research staff member at IBM Research and has coauthored more than 150 publications and is also the co-inventor of more than 35 patents