

Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuits

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ABSTRACT

DC testing of parametric faults in non-linear analog circuits based on polynomial approximation of the functionality of fault free circuit is presented. Classification of circuit under test (CUT) is based on comparison of estimates of polynomial coefficients with those of the fault free circuit. The method needs very little augmentation of circuit to make it testable as only output parameters are used for classification. Possible fault diagnosis using the proposed method in conjunction with sensitivity of polynomial coefficients is also presented.

Categories and Subject Descriptors

B.7.3 [Hardware]: Integrated Circuits—*Reliability and Testing*[Test generation]; B.8.1 [Hardware]: Performance and Reliability—*Reliability, Testing, and Fault-Tolerance*

General Terms

Experimentation, Reliability, Theory

Keywords

DC test; Parametric faults; Non-linear circuit test; Curve fitting; Polynomial

1. INTRODUCTION

Analog circuits can be primarily classified into two types, namely *linear* and *non-linear* circuits. Linear circuits in general obey the superposition principle. Typically linear circuits are exclusively made up of passive elements. Main examples include LC, RC filters and attenuators. Linear circuit testing for parametric faults making use of Linear Time Invariance (LTI) property of these circuits is available in literature. The prominent ones being the transfer function coefficient estimates based test [1] and signal flow graph based test [2]. On the other hand non-linear circuits

do not obey the superposition principle and consist of combination of passive and active devices. As one would expect, large number of electronic circuits like active elliptic filters, mixers, logarithmic amplifiers, etc., are non-linear. Further, tests which use the LTI properties of CUT cannot be used for non-linear circuits. In this paper, we will address testing of non-linear circuits at DC for parametric faults in circuit components.

Non-linear circuit testing has been studied and different methods have been proposed for finding parametric faults [3, 4, 5, 6, 7, 8, 9, 10]. Prominent among them in the industry is the I_{DDQ} based testing where current from the supply rail is monitored and sizable deviation from its quiescent value is reported. However this requires augmentation of the CUT. For example, in the simplest case a regulator supplying power to any sizable circuit has to be augmented with a current sensing resistor and an ADC (for digital output) and then there is subsequent analysis to be performed on sensed current. Further I_{DDQ} is suitable only for catastrophic faults as the current drawn from the supply is distinguishable only when there is some “big enough” fault so as to change the current drawn from the supply from its quiescent value to a region where it is distinguishable. For example with resistor R_2 being open in Figure 1, the current drawn from supply can change by 50% of its quiescent value. Such faults can typically be found by monitoring I_{DDQ} using a current sensor. However parametric deviations say lesser than 10% from its nominal value cannot be observed using this scheme, specially so in the deep submicron era where the leakage currents can be comparable with defect induced current [11]. It is therefore interesting to develop a method to detect parametric faults while DC testing with lesser circuit augmentation.

To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in complexity of the sensing circuit. However, we would also want only little augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting requirements the method intended should have some way of “seeing through” the circuit with only the outputs and inputs at its disposal. References [1, 12] have accomplished this sort of a strategy for linear circuits in a different context as described next.

Savir and Guo describe a method [1] based on transfer function description of CUT. The transfer function, $H(s)$,

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of the CUT is expressed as in (1):

$$H(s) = \frac{\sum_{i=0}^M a_i s^i}{\sum_{i=0}^N b_i s^i} \quad (M < N) \quad (1)$$

Here, a_i and b_i are referred to as transfer function coefficients (TFCs). The CUT is subjected to frequency rich input signals and the output at these frequencies is observed. With these input-output pairs they estimate the TFCs of CUT. These coefficients are now compared with the ideal circuit TFCs, which are known a priori. The CUT is classified faulty if any of the estimated coefficients are beyond the tolerable range. This method necessarily needs the CUT to be linear, as transfer functions are possible only for LTI systems.

To extend the above idea to more general non-linear circuits we adopt a strategy where we expand the function of the circuit as a polynomial by the Taylor's series expansion about the input voltage $v_{in} = 0$ as follows:

$$v_{out} = f(v_{in}) = f(0) + \frac{f'(0)}{1!}v_{in} + \frac{f''(0)}{2!}v_{in}^2 + \frac{f'''(0)}{3!}v_{in}^3 + \dots + \frac{f^{(n)}(0)}{n!}v_{in}^n + \dots \quad (2)$$

where $f(x)$ is a real function x . Ignoring the higher order terms in (2), we can expand v_{out} up to the n^{th} power of v_{in} , which gives us the approximation in (3):

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \dots + a_n v_{in}^n \quad (3)$$

where $a_0, a_1, a_2, \dots, a_n$ are all real-valued functions of circuit parameters $p_k \forall k$. Further assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha \ll 1$. This means that every parameter p_i is allowed to vary within the range $p_{k,nom}(1 - \alpha) < p_k < p_{k,nom}(1 + \alpha) \forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k . Whenever one or more of the coefficient values slip outside its individual hypercube we get a different set of coefficients that reflects a detectable fault. Therefore, equation (4) describes a hypercube for all parameters that correspond to either good machine values or undetectable parameter faults [1, 4, 10]:

$$a_{i,\min} < a_i < a_{i,\max} \quad \forall a_i, \quad 0 \leq i \leq n \quad (4)$$

This paper is organized as follows. Section 2 deals with the analysis of the nature of coefficients resulting from polynomial expansion of function $f(v_{in})$ and notions of detectable fault sizes of parameters. In Section 3 we describe the problem at hand and discuss the proposed solution with an example. In Section 4 we generalize the solution to an arbitrarily large circuit. Section 5 presents the simulation results for some standard circuits. Section 6 outlines the method of fault diagnosis using the said method and we conclude in Section 7.

2. PRELIMINARIES

The coefficients $a_i \forall 0 \leq i \leq n$ are in general non-linear functions of circuit parameters $p_k \forall k$. The rationale in using these coefficients as metrics in classifying CUT as faulty or fault free is based on the premise of dependence of coefficients on circuit parameters.

2.1 Analysis of Polynomial Coefficients

Theorem 1. If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.

Lemma 1. If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i , then a_i can take its limit values anywhere inside the hypercube enclosing the parameters.

By Theorem 1 and Lemma 1 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 2. In polynomial expansion of Non-Linear Analog circuit there exists at least one coefficient that is a monotonic function of all the circuit parameters.

In conclusion, from Lemma 1 and Theorem 2, circuit parameter deviations have a bearing on coefficients and the monotonically varying coefficients can be used to detect parametric faults of the circuit parameters.

2.2 Some Definitions

Definition 1: A minimum size detectable fault, MSDF ρ , of a parameter is defined as the minimum fractional deviation of the circuit parameter from its nominal value for it to be detectable with all other parameters held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF) accordingly.

Definition 2: A nearly minimum size detectable fault, or NMSDF ρ^* , of a parameter is defined as some fractional deviation of the circuit parameter from its nominal value, with all the other parameters being held at their nominal values, that is close to its MSDF with an infinitesimally small error, ϵ . Thus,

$$\epsilon = |\rho - \rho^*| \quad \epsilon \ll 1 \quad (5)$$

NMSDF also has notions of upside and downside as in case of MSDF. In (5), ϵ can be perceived as a coefficient of uncertainty about the MSDF of a parameter. If ψ is the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{v_0, v_1, \dots, v_n \mid v_0 \in A_0, v_1 \in A_1, \dots, v_n \in A_n\} \\ \forall_k \quad p_{k,nom}(1 - \alpha) < p_k < p_{k,nom}(1 + \alpha)$$

then by definitions 1 and 2, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside the set ψ will result in a detectable fault.

3. PROBLEM AND APPROACH

We shall first illustrate with an example the calculation of limits of the polynomial coefficients for a simple circuit using MOS transistors. We shall follow this up with MSDF values for the circuit parameters.

Example 1. Two stage amplifier Consider the cascaded amplifier shown in Figure 1. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial equation as in (6).

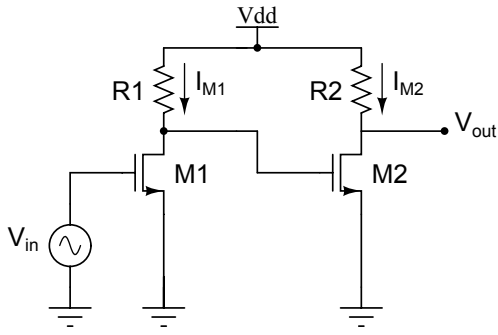


Figure 1: Cascaded amplifier.

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 \quad (6)$$

Where the constants a_0, a_1, a_2, a_3 are defined symbolically in (6) for M1 and M2 operating in saturation region. Nominal values of $V_{DD}=1.2V$, $V_T=400mV$, $(\frac{W}{L})_1 = \frac{1}{2}(\frac{W}{L})_2 = 20$, and $K = 100\mu A/V^2$ are substituted to get coefficients in terms of parameters R_1 and R_2 as stated in (8).

$$a_0 = V_{DD} - R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} (V_{DD} - V_T)^2 + \\ R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^4 - \\ 2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2 \end{array} \right\}$$

$$a_1 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} 4R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^3 \\ + 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 V_T \end{array} \right\}$$

$$a_2 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 \\ - 6R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^2 \end{array} \right\}$$

$$a_3 = 4V_T K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

$$a_4 = -K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2 \quad (7)$$

$$a_0 = 1.2 - R_2 \left(\begin{array}{l} 2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_1^2 \\ - 5.12 \times 10^{-4} R_1 \end{array} \right)$$

$$a_1 = 4.096 \times 10^{-9} R_1^2 R_2 + 5.12 \times 10^{-6} R_1 R_2$$

$$a_2 = 1.28 \times 10^{-5} R_1 R_2 - 1.536 \times 10^{-8} R_1^2 R_2 \quad (8)$$

$$a_3 = 2.56 \times 10^{-8} R_1^2 R_2$$

$$a_4 = 1.6 \times 10^{-8} R_1^2 R_2$$

To find the limit values of the coefficient a_0 we assume the parameters R_1 and R_2 deviate by a fraction x and y from their nominal values respectively. To maximize a_0 we have the objective function as given by (9) subject to constraints in (10). Note that here we have set out to find MSDF of R_1 . Similar approach can be used to find the MSDF of R_2 .

Table 1: MSDF for cascaded amplifier of Figure 1 with $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

$$1.2 - R_{2,nom}(1+y) \left\{ \begin{array}{l} 2.56 \times 10^{-3} + \\ 1.024 \times 10^{-7} R_{1,nom}^2 (1+x)^2 \\ - 5.12 \times 10^{-4} R_{1,nom} (1+x) \end{array} \right\} \quad (9)$$

$$4.096 \times 10^{-9} R_{1,nom}^2 (1+x)^2 R_{2,nom} (1+y) + 5.12 \times 10^{-6} R_{1,nom} (1+x) R_{2,nom} (1+y) = 4.096 \times 10^{-9} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} + 5.12 \times 10^{-6} R_{1,nom} (1+\rho) R_{2,nom} \quad (10)$$

$$1.28 \times 10^{-5} R_{1,nom} (1+x) R_{2,nom} (1+y) - 1.536 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom} (1+y) = 1.28 \times 10^{-5} R_{1,nom} (1+\rho) R_{2,nom} - 1.536 \times 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} \quad (11)$$

$$2.56 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom} (1+y) = 2.56 \times 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} \quad (12)$$

$$1.6 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom} (1+y) = 1.6 \times 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} \quad (13)$$

$$-\alpha \leq x, y \leq \alpha \quad (14)$$

The extreme values for x and y on solving the set of equations in (9-13) we have $x = -\alpha$ and $y = -\alpha$, this gives us the MSDF value for R_2, ρ in (14).

$$\rho = (1 - \alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \quad (15)$$

Table 1 gives the MSDF for R_1 and R_2 based on above calculation.

4. GENERALIZATION

In general, calculation as above cannot be done for arbitrarily large circuits. Such circuits are handled by obtaining a nominal numeric polynomial expansion of the desired circuit. This is done by sweeping the input voltage across all possible values and noting the corresponding output voltages. Now, the output voltage is plotted against the input voltage. A polynomial is fit to this curve and the coefficients of this polynomial are taken to be the nominal coefficients of the desired polynomial. The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced ϵ apart. Polynomials coefficients are obtained for each of these simulations. The maximum and minimum values of coefficient in this search are taken as the limit value on that coefficient. Once the limit values on all coefficients have been determined the CUT is subjected to DC sweep at the input. Its response to the DC sweep is curve fitted to a polynomial of order same as the fault free circuit. If there are any coefficients that lay outside the limit values

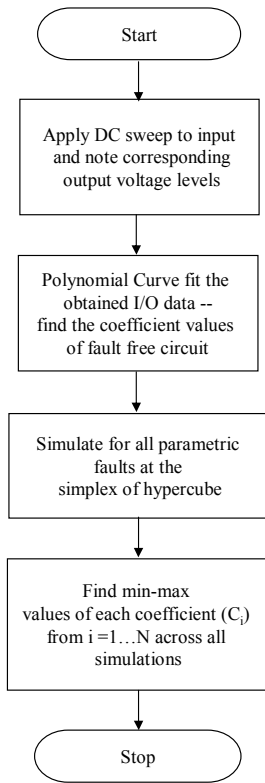


Figure 2: Flow chart showing fault simulation process and bounding of coefficients.

of corresponding coefficients of the fault free circuit, we can conclude the CUT is faulty with a high probability that is inversely proportional to coefficient of uncertainty ϵ . The converse is also true. Flow chart in Figure 2 summarizes the process of numerically finding the polynomial and finding the bounds on coefficients. Flow chart in Figure 3 outlines the procedure to test CUT using the polynomial coefficient method. The bounds on coefficients of fault free circuit are found a priori as shown in flowchart of Figure 2.

5. SIMULATION RESULTS

We subjected an elliptic filter shown in Figure 4 to polynomial coefficient based test. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [13]. Figure 5 shows the computed response and the following estimated polynomial obtained by curve fitting:

$$v_{out} = 4.5341 - 3.498v_{in} - 2.5487v_{in}^2 + 2.1309v_{in}^3 - 0.50514v_{in}^4 + 0.039463v_{in}^5 \quad (16)$$

The combinations of parameter values leading to limits on the coefficients are as shown in Tables 2 and 3. Some of the circuit parameters are not shown in the table because they do not appear in any of the coefficients and are kept at their nominal values. Further, results on pass/fail detectability of some injected faults in tabulated in Table 4.

6. FAULT DIAGNOSIS

Fault diagnosis using sensitivity of output to circuit parameters has been investigated [14]. We have extended this

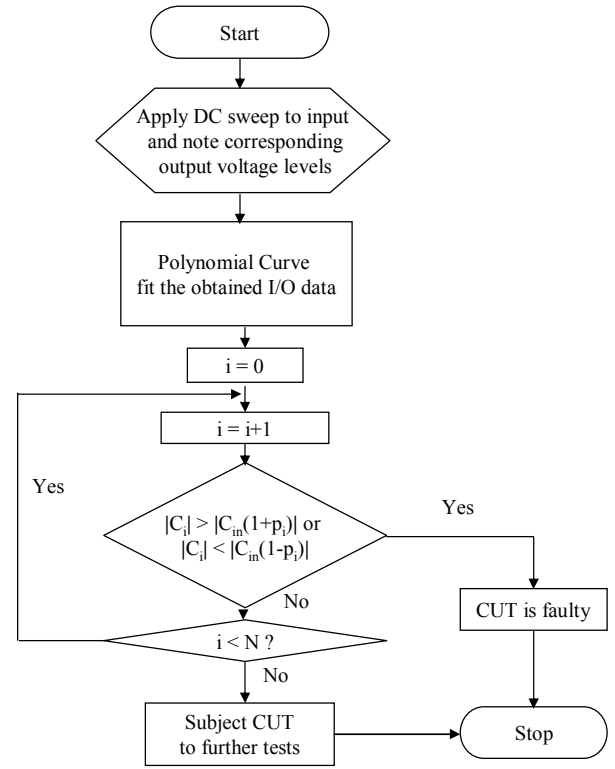


Figure 3: Flow chart of test procedure for CUT.

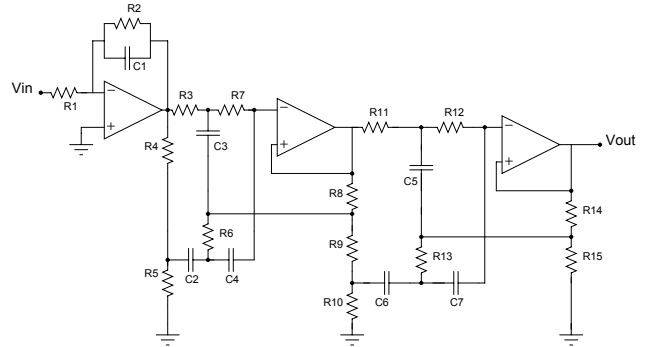


Figure 4: Elliptic filter.

approach of diagnosis exploiting the sensitivity of polynomial coefficients to circuit parameters. The advantage of this approach is improved fault diagnosis without circuit augmentation. Sensitivity of i^{th} coefficient C_i to k^{th} parameter p_k is represented by $S_{P_k}^{C_i}$ and is expressed as,

$$S_{P_k}^{C_i} = \frac{p_k}{C_i} \frac{\partial C_i}{\partial p_k} \quad (17)$$

Figure 6 shows a possible scenario.

6.1 Computation of Sensitivities

Numerical computation of sensitivities given by (17) is accomplished by introducing fractional drifts ($= \alpha$) in each component ($p_k \forall k$); simulating the circuit and measuring the fractional drift in each coefficient of the polynomial resulting from curve fitting operation. This way the numerical

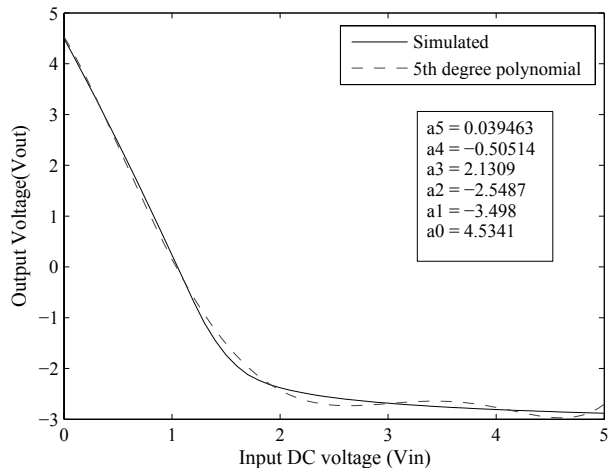


Figure 5: DC response of elliptic filter with curve fitting polynomial.

Table 2: Parameter combinations leading to maximum values of coefficients with $\alpha = 0.05$.

Circuit Parameter (Ω)	a_0	a_1	a_2	a_3	a_4	a_5
R ₁ = 19.6k	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k
R ₂ = 196k	186k	205k	186k	186k	186k	205k
R ₃ = 147k	139k	154k	154k	154k	139k	154k
R ₄ = 1k	950	1010	1010	1010	1010	1010
R ₅ = 71.5	70	80	80	70	80	70
R ₆ = 37.4k	37.4k	37.4k	37.4k	37.4k	37.4k	37.4k
R ₇ = 154k	161k	161k	146k	161k	146k	146k
R ₁₁ = 110k	115k	115k	104k	115k	104k	104k
R ₁₂ = 110k	104k	115k	104k	104k	104k	104k

sensitivities are computed and a dictionary is maintained for sensitivities. The order of complexity in computation of sensitivities is linear in the number of circuit parameters (N), i.e., $O(N)$.

6.2 Diagnosing Parametric Faults

Restricting to single parametric faults, we find the descending order of sensitivities of all coefficients to parameters, depending on the coefficients that have exceeded their limit values. The parameter with highest sensitivity is said to be at fault with a probability $P(\delta p_k | \delta C_i)$, which can be interpreted as the confidence in diagnosing the fault:

$$P(\delta p_k | \delta C_i) = \frac{S_{P_k}^i \delta p_k}{\delta C_i} \quad (18)$$

where δp_k is the suspected drift in parameter p_k and δC_i is the measured drift in coefficient. Single parametric faults in the elliptic filter of Figure 4 were diagnosable with up to 95% confidence level. The results are tabulated in Table 5 for several injected single parametric faults.

Table 3: Parameter combinations leading to minimum values of coefficients with $\alpha = 0.05$.

Circuit Parameter (Ω)	a_0	a_1	a_2	a_3	a_4	a_5
R ₁ = 19.6k	20.5k	18.6k	18.6k	20.5k	20.5k	20.5k
R ₂ = 196k	205k	186k	205k	205k	205k	186k
R ₃ = 147k	150k	139k	139k	146k	154k	139k
R ₄ = 1k	1010	950	950	950	950	950
R ₅ = 71.5	80	70	70	80	70	80
R ₆ = 37.4k	39.2k	39.2k	39.2k	39.2k	35.5k	39.2k
R ₇ = 154k	146k	146k	161k	146k	161k	161k
R ₁₁ = 110k	104k	104k	115k	104k	115k	115k
R ₁₂ = 110k	115k	104k	115k	115k	115k	115k

Table 4: Results for some injected faults.

Circuit Parameter	Out of bound coefficients	Fault detected?
R ₁ down 25%	$a_0 - a_4$	Yes
R ₂ down 15%	a_2, a_5	Yes
R ₃ up 10%	a_1, a_2, a_3	Yes
R ₄ down 25%	$a_0 - a_4$	Yes
R ₅ up 15%	a_0, a_4	Yes
R ₇ up 10%	a_1, a_2	Yes
R ₁₁ up 10%	a_4, a_5	Yes
R ₁₂ down 10%	a_4, a_5	Yes

7. CONCLUSION

A new approach for testing non-linear circuits based on polynomial expansion of the circuit has been proposed. The minimum size detectable faults of some of the parameters in circuits are as low as 10% which implies impressive fault coverage. The method has been extended to sensitivity based fault diagnosis with probabilistic confidence levels in parameter drifts. The method of polynomial expansion at DC, as described here, may not detect certain types of faults, such as, parametric faults of a capacitor. To overcome that deficiency, in our ongoing work, we are generalizing this technique to multiple frequencies.

Table 5: Parametric fault diagnosis with 95% confidence level.

Fault Injected	Coefficient status	Diagnosed fault sites
R ₁ down 25%	$a_0 - a_4$	R ₁ or R ₄
R ₂ down 15%	a_2, a_5	R ₂
R ₃ up 10%	a_1, a_2, a_3	R ₃
R ₄ down 25%	$a_0 - a_4$	R ₁ or R ₄
R ₅ up 15%	a_0, a_4	R ₅
R ₇ up 10%	a_1, a_2	R ₇
R ₁₁ up 10%	a_4, a_5	R ₁₁ or R ₁₂
R ₁₂ down 10%	a_4, a_5	R ₁₁ or R ₁₂

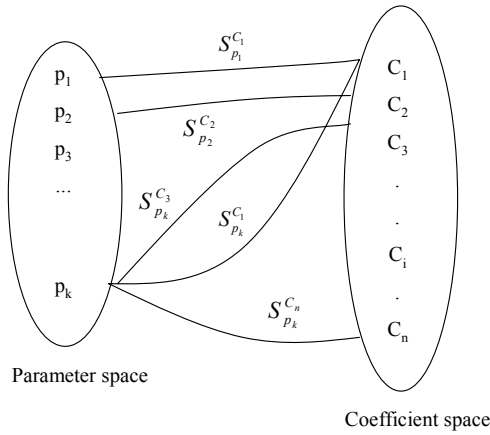


Figure 6: Mapping showing a possible relation between various parameters and coefficients.

8. REFERENCES

- [1] Z. Guo and J. Savir, "Analog Circuit Test Using Transfer Function Coefficient Estimates," in *Proc. Int. Test Conf.*, pp. 1155–1163, Oct. 2003.
- [2] R. Ramadoss and M. L. Bushnell, "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," in *Proc. 9th Int. Conf. on VLSI Design*, pp. 242–248, Jan. 1996.
- [3] A. Abderrahman, E. Cerny, and B. Kaminska, "Optimization Based Multifrequency Test Generation for Analog Circuits," *Journal of Electronic Testing: Theory and Applications*, vol. 9, pp. 59–73, Mar 1996.
- [4] S. Chakravarty and P. J. Thadikaran, *Introduction to IDDQ Testing*. Kluwer Academic Publishers, 1997.
- [5] S. Cherubal and A. Chatterjee, "Test Generation Based Diagnosis of Device Parameters for Analog Circuits," in *Proc. Design, Automation and Test in Europe Conf.*, pp. 596–602, 2001.
- [6] G. Devarayanadug and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," in *Proc. Int. Conf. on Computer-Aided Design*, pp. 44–47, Nov. 1994.
- [7] S. L. Farchy, E. D. Gadzheva, L. H. Raykovska, and T. G. Kouyoumdjiev, "Nullator-Norator Approach to Analogue Circuit Diagnosis Using General-Purpose Analysis Programmes," *Int. Journal of Circuit Theory and Applications*, vol. 23, pp. 571–585, Dec. 1995.
- [8] R. K. Gulati and C. F. Hawkins, *IDDQ Testing of VLSI Circuits*. Kluwer Academic Publishers, 1993.
- [9] W. L. Lindermeir, H. E. Graeb, and K. J. Antreich, "Analog Testing by Characteristic Observation Inference," *IEEE Trans. Comp. Aided Design*, vol. 23, pp. 1353–1368, June 1999.
- [10] R. Rajsuman, *IDDQ Testing for CMOS VLSI*. Artech House, 1995.
- [11] J. Figueras, "Possibilities and Limitations of IDDQ Testing in Submicron CMOS," in *Proc. Innovative Systems in Silicon Conf.*, pp. 174–185, Oct. 1997.
- [12] V. Panic, D. Milovanovic, P. Petkovic, and V. Litovski, "Fault Location in Passive Analog RC Circuits by measuring Impulse Response," in *Proc. 20th Int. Conf. on Microelectronics*, pp. 12–14, Sept. 1995.

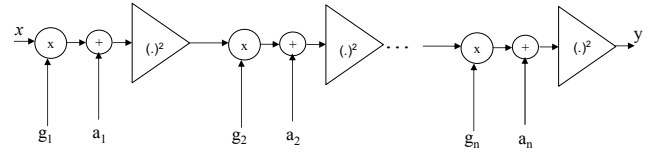


Figure 7: A system model for a non-linear circuit.

- [13] R. Kondagunturi, E. Bradley, K. Maggard, and C. Stroud, "Benchmark Circuits for Analog and Mixed-Signal Testing," in *Proc. 20th Int. Conf. on Microelectronics*, pp. 217–220, Mar. 1999.
- [14] M. Slamani and B. Kaminska, "Analog Circuit Fault Diagnosis Based on Sensitivity Computation and Functional Testing," *IEEE Design & Test of Computers*, vol. 19, no. 1, pp. 30–39, 1992.

APPENDIX

Theorem 1. If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.

PROOF. Let a_i be a function of three parameters say x , y and z . Let a_i reach its maximum value for (x_0, y_0, z_0) . Further let $x_0, y_0 \neq \alpha$. Now if we can show that the maximum value of the coefficient a_i occurs at the $z_0 = \alpha$ we have proved the theorem. From definition of monotonic dependence of a_i on circuit parameters, it follows that $a_i(x_0, y_0, \alpha) \geq a_i(x_0, y_0, z_0)$, $\forall z_0 \leq \alpha$. Because the maximum value taken by z is α , it follows that $z_0 = \alpha$. With similar arguments we can show that the minimum value for the coefficient occurs when $z_0 = -\alpha$. Hence, the statement of theorem follows. \square

Theorem 2. In polynomial expansion of a non-linear analog circuit there exists at least one coefficient that is a monotonic function of all of the circuit parameters.

PROOF. Consider the block diagram in Figure 7, which models an $2n^{\text{th}}$ order non-linear analog circuit. It has an input x and an output y . Constants $a_1 \dots a_n$ are added at the input of each stage. The coefficient corresponding to input x raised to the $2n^{\text{th}}$ power is given by G , as follows:

$$G = \prod_{i=1}^n g_i^{2^i} \quad (19)$$

where $g_i \forall i = 1 \dots n$ are the monotonic gains of individual stages in the cascaded blocks. As the product of two or more monotonic functions is also monotonic we have G to be a monotonic function. G constitutes the coefficient of the n^{th} power of x in this expansion, as it lies in the main signal flow path from input to output. Thus, it is proved that there is at least one monotonically varying coefficient in a polynomial expansion of a Non-Linear analog circuit. Further, in general the coefficient of $2n^{\text{th}}$ power of such a polynomial expansion is monotonic. \square