Polysilicon Gate Enhancement of the Random Dopant Induced Threshold Voltage Fluctuations in Sub-100 nm MOSFET's with Ultrathin Gate Oxide

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***Abstract*—In this paper, we investigate various aspects of the polysilicon gate influence on the random dopant induced threshold voltage fluctuations in sub-100 nm MOSFET's with ultrathin gate oxides. The study is done by using an efficient statistical three-dimensional (3-D) "atomistic" simulation technique described elsewhere [1]. MOSFET's with uniform channel doping and with low doped epitaxial channels have been investigated. The simulations reveal that even in devices with a single crystal gate the gate depletion and the random dopants in it are responsible for a substantial fraction of the threshold voltage fluctuations when the gate oxide is scaled to thickness in the range of 1–2 nm. Simulation experiments have been used in order to separate the enhancement in the threshold voltage fluctuations due to an effective increase in the oxide thickness associated with the gate depletion from the direct influence of the random dopants in the gate depletion layer. The results of the experiments show that the both factors contribute to the enhancement of the threshold voltage fluctuations, but the effective increase in the oxide thickness has a dominant effect in the investigated range of devices. Simulations illustrating the effect of the polysilicon grain boundaries on the threshold voltage variation are also presented.**

***Index Terms*—Doping, fluctuations, MOSFET, semiconductor device simulation, silicon devices, threshold.**

I. Introduction

THE gate oxide thickness has been reduced continuously with the scaling of the channel length for each new generation of MOSFET's [1]. It already approaches the few atomic layers limit in deep submicron devices [2], [3]. The use of a polysilicon gate in combination with such thin gate oxides introduces some problems. The polysilicon depletion effect [4], [5], for example, leads to a pronounced loss of inversion charge. This loss is complementary to the charge losses due to inversion layer quantization [6], [7]. The associated reduction of transconductance and drive current have a detrimental effect on the device [8] and circuit [9] performance. For oxide thicknesses and channel doping levels typical for sub-100 nm MOSFET's, the polysilicon depletion effect starts to dominate the inversion charge losses [10], [11]. In addition to this the granularity of the polysilicon gate can be responsible for a substantial mismatch in the parameters of deep submicron CMOS transistors [12].

Another detrimental effect associated with the polysilicon gate, not yet addressed in the literature, is an enhancement of the random dopant induced MOSFET parameters fluctuation even in devices with a single crystal gate. Fluctuations in the threshold voltage associated with the random number and position of discrete dopants in the MOSFET channel have been predicted in the early seventies [13], [14] and confirmed now experimentally for a wide range of devices [15]–[17]. The polysilicon gate depletion which increases the effective gate-oxide thickness, and introduces additional random dopant charge on the side of the gate oxide opposite to the channel, will enhance the threshold voltage fluctuations, particularly in MOSFET's with ultrathin gate oxide. However, to the best of our knowledge, these effects has not been taken into account in the published analytical models [15], [18]–[20] and numerical [20]–[24] simulation studies of random dopant induced MOSFET threshold voltage fluctuations.

In this paper, for the first time we investigate the effect of the gate random dopants and depletion on the random dopant induced threshold voltage fluctuations in sub-100 nm MOSFET's with ultrathin gate oxides and polysilicon gates. Most of the simulation were conducted for devices with a single crystal gate, but results illustrating the effect of the polysilicon grain boundaries are also presented. The study is carried out using an efficient three-dimensional (3-D) "atomistic" simulation technique [25], which in this case takes into account the discrete random dopant distribution not only in the MOSFET channel but also in the polysilicon gate. Large samples of devices with microscopically different distributions of dopants in the channel and in the gate are used to build a statistically reliable picture of the investigated effects.

The structure of the simulated single crystal gate MOSFET's together with a brief description of the simulation procedures are given in Section II. The major results highlighting the effect of the single crystal gate on the random dopant induced threshold voltage fluctuations in conventional MOSFET's with uniform channel doping and in devices with low doped epitaxial channels are presented in Section III. The analysis in Section IV makes an attempt to disentangle the contribution of the gate depletion and the random dopant charge in the gate to the enhancement of the threshold voltage fluctuations. Simulation results illustrating one aspect of the threshold voltage variation associated with the polysilicon gate grain boundaries are presented in Section V.

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II. Devices and Simulation Procedure

Most of the simulations in this paper are focused on n-channel MOSFET's with single crystal n^+-silicon gate, gate length 60 nm and gate width 50 nm. A junction depth $x_j = 7$ nm with 5 nm lateral sub-diffusion results in an effective channel length $L_{\text{eff}} = 50$ nm for all simulated devices. Both devices with uniform channel doping, and with low doped epitaxial layer, introduced in the channel region to reduce the threshold voltage fluctuations, have been investigated. The doping concentration in the channel or behind the epitaxial layer in most of the simulated devices is $N_A = 5 \times 10^{18}$ cm^{-3}. The oxide thickness t_{ox} varies from 1 to 4 nm. The above choice of MOSFET parameters allows for a direct comparison with previously published atomistic simulation results [24], [26] in which the effects associated with the polysilicon gate have been completely neglected.

We investigate the random dopant induced threshold voltage fluctuations by using an efficient statistical 'atomistic' simulation approach described in more details elsewhere [25]. A typical 'atomistic' simulation domain for a MOSFET with a single crystal gate is illustrated in Fig. 1. The gate is flipped open like the cover of a book to give an impression of the random distribution of dopants at its interface with the gate oxide. An uniform grid with typical grid spacing $h = 0.5$ nm is used to discretize both the silicon substrate and the silicon gate and to resolve the effects associated with individual dopants. The "atomistic" regions in the channel and in the gate are outlined in the figure. The average number of dopants in these regions are calculated by multiplying the volumes by the corresponding doping concentrations. The actual number of dopants in each "atomistic" region is chosen randomly from a Poisson distribution with a mean equal to the corresponding average dopant numbers. The position of each dopant is chosen randomly, and a doping concentration $1/h^3$ is assigned to the nearest grid node. The potential is fixed to the built-in junction potential at the source and drain contacts. At the top surface of the n^+-silicon gate the potential is fixed to the applied gate voltage corrected by the difference between the workfunctions in the continuously doped region of the gate and the continuously doped portion of the p-type substrate. The normal derivative of the potential is set to zero at all other boundaries of the solution domain.

The simulations, carried out at low drain voltage, are based on a single 3-D solution of the nonlinear Poisson equation. At low drain voltage the current is calculated from the channel resistance obtained by solving a simplified current continuity equation in a drift approximation only (see [25]). A standard current criterion $10^{-8} W_{\text{eff}}/L_{\text{eff}}$ [A] is used for determining the threshold voltage. The threshold voltage standard deviation σV_T is extracted from the simulation of samples containing 200 MOSFET's with microscopically different distributions of dopants. The corresponding relative standard deviation of the extracted σV_T is 5% for all results presented in this paper.

Fig. 1 also illustrates the potential distribution at the both gate oxide interfaces for a typical for this study MOSFET with oxide thickness $t_{\text{ox}} = 3$ nm. The gate voltage V_G is equal to the threshold voltage $V_T = 0.723$ V of this particular device. The doping concentrations in the channel region and in the n^+-silicon gate are $N_A = 5 \times 10^{18}$ cm^{-3} and $N_D = 5 \times 10^{19}$ cm^{-3},

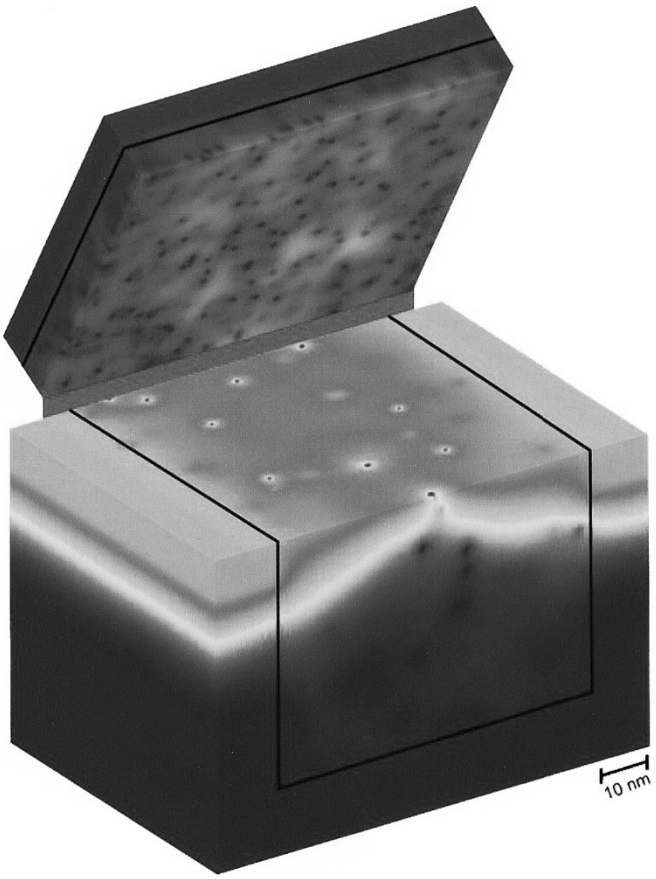

Fig. 1. Typical "atomistic" simulation domain for a MOSFET with a single crystal silicon gate, channel doping concentration $N_A = 5 \times 10^{18}$ cm^{-3}, gate doping concentration $N_D = 5 \times 10^{19}$ cm^{-3}, $L_{\text{eff}} = W_{\text{eff}} = 50$ nm, $x_j = 7$ nm, and $t_{\text{ox}} = 3$ nm The potential distribution corresponds to $V_G = V_T = 0.723$ V.

respectively. This corresponds to approximately 5.8 nm average separation between the acceptors in the channel and 2.7 nm average separation between donors in the gate. The influence of individual acceptors and donors on the surface potential at the both gate oxide interfaces interfaces is clearly visible. The radius of this influence is approximately 2–3 nm. The polysilicon depletion is noticeable at the visible surrounding sides of the gate. The random dopants result in variation in the width of the channel and gate depletion layers. Clustering of dopants at the gate interface result also in a longer range (5–10 nm) potential variations.

It is important to point out that although all simulations were carried out for n-channel MOSFET's with n^+-silicon gate the obtained results for σV_T are valid also for p-channel MOSFET's with p^+-silicon gate, since the electrostatic in the both cases works in the same way.

III. Simulation Results

A. MOSFET's with Uniform Doping in the Channel

The dependence of the threshold voltage standard deviation σV_T on the oxide thickness for a MOSFET with single crystal n^+-silicon gate is compared in Fig. 2 with previously published results for an analogous device with a metal gate [24]. Both

MOSFET's have uniform channel doping $N_A = 5\times10^{18}$ cm^{-3} and $L_{\rm eff} = W_{\rm eff} = 50$ nm. The doping concentration in the gate is $N_D = 1 \times 10^{20}$ cm^{-3}. The term "metal gate" is used in this paper, to indicate that in the simulations a Dirichlet boundary condition was applied at the gate electrode keeping constant the value of the potential on top of the gate insulator in the whole gate area. This is despite the fact that the fixed value of the potential was eventually adjusted to take into account the workfunction of the actual polysilicon gate. To the best of our knowledge all numerical simulation studies of random dopant induced threshold voltage fluctuations published up to now fall to this metal gate boundary condition category, and do not take into account the depletion and the random dopants in the polysilicon gate. We would like also to point out that the change of the gate workfunction in such metal gate simulations changes the value of the threshold voltage but do not affect the value of σV_T.

For the metal gate MOSFET's in Fig. 2 σV_T scales linearly to zero with the corresponding scaling of $t_{\rm ox}$ within the accuracy of the statistical estimation. This is in agreement with most of the available analytical models for σV_T. For example the classical expression for σV_T in [18] can be presented in the form

$$\sigma V_T = C t_{\rm ox}, \quad \text{where } C = \frac{q}{\varepsilon_{\rm ox}}\sqrt{\frac{N_A W_d}{4 L_{\rm eff} W_{\rm eff}}} \tag{1}$$

where q is the electron charge, $\varepsilon_{\rm ox}$ is the dielectric constants of the gate oxide, and W_d is the width of the channel depletion layer. In more recent publications, corrections were introduced in C, for example a multiplicative factor of $2/\sqrt{3}$ in [19], but the general form of (1) remains unchanged. It has to be pointed out that the values of C extracted from our previous "atomistic'" simulations of sub-100 nm MOSFET's [24], [26] are larger than the predictions of the analytical models mentioned above. The values of σV_T corresponding to the silicon gate MOSFET's with different thickness of the gate oxide in Fig. 2 are shifted up almost parallel by approximately 10 mV in respect to the metal gate results and can be approximate by the expression

$$\sigma V_T = C(t_{\rm ox} + \Delta), \tag{2}$$

which will be analyzed further in Section IV.

The displacement Δ depends on the doping concentration in the gate and is responsible for a substantial portion of the threshold voltage fluctuations in devices with ultrathin gate oxides. The gate doping concentration dependence of σV_T is plotted in Fig. 3 for two MOSFET's with gate oxide thickness 1 nm and 2 nm, respectively, and with the same dimensions and channel doping concentrations as the devices in Fig. 2. The relative increase of the threshold voltage fluctuations compared to the metal gate simulations, is illustrated in the same figure. The effect of the silicon gate increases rapidly when the gate doping concentration falls bellow 1×10^{20} cm^{-3}. There is a general agreement that the minimum thickness of the gate oxide, restricted primarily by the total on chip gate leakage current, will be between 1 and 2 nm. Since the dependence of the σV_T on $t_{\rm ox}$ is linear it is easy to interpolate the results presented in Fig. 3 for any oxide thickness in this range. For an oxide thickness of 1.5 nm for example the contribution to the threshold voltage fluctuations varies from approximately 17% at gate doping 5×10^{20} cm^{-3} to approximately 60% at

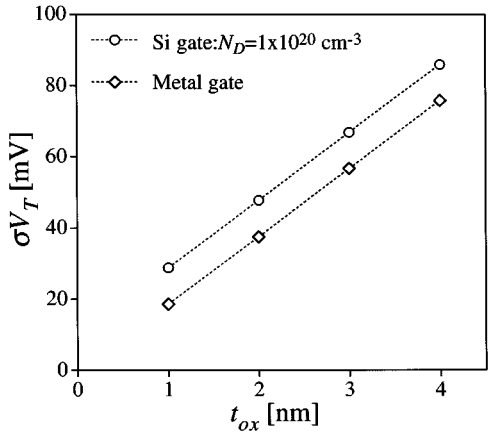

Fig. 2. Dependence of the threshold voltage standard deviation σV_T on the oxide thickness $t_{\rm ox}$ for single crystal silicon gate and metal gate MOSFET's with $L_{\rm eff} = W_{\rm eff} = 50$ nm, $x_j = 7$ nm, $t_{\rm ox} = 3$ nm, and $N_A = 5 \times 10^{18}$ cm^{-3}. The gate doping concentration is $N_D = 1 \times 10^{20}$ cm^{-3}.

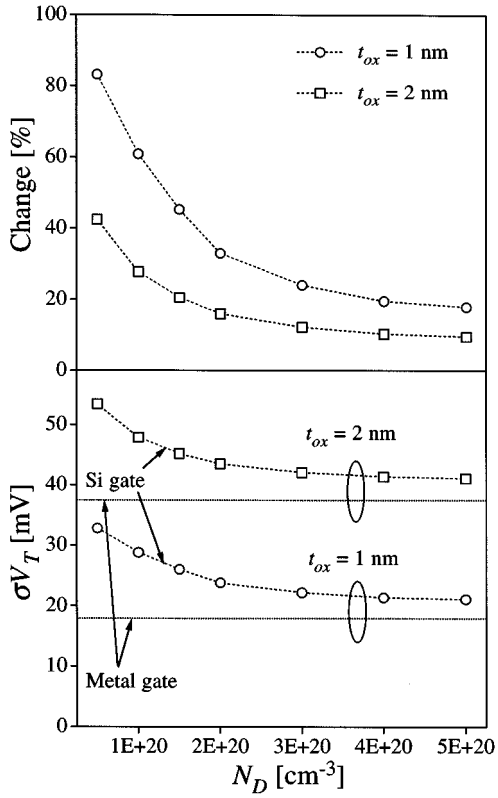

Fig. 3. Dependence of the threshold voltage standard deviation σV_T on the gate doping concentration N_D for MOSFET's with different gate oxide thickness $t_{\rm ox}$. The change in σV_T in respect to analogous metal gate devices is also plotted. All other MOSFET parameters are the same as in Fig. 2.

gate doping 5×10^{19} cm^{-3}. The high end of the gate doping is typical for n-channel MOSFET's with n$^+$-polysilicon gates while the low end is representative for p-channel MOSFET's with p$^+$-polysilicon gates.

The dependence of σV_T on the doping concentration in the channel N_A is plotted in Fig. 4 for an n$^+$-silicon and for metal gate MOSFET's with two oxide thicknesses 1 nm and 2 nm, respectively. The rest of the device dimensions are again the same as in Fig. 2 and the gate doping concentration is $N_D = 5\times10^{19}$

cm^{-3}. The reduction in the channel doping concentration reduces the influence of the gate. This can be explained in the following way. The reduction in the channel doping concentration reduces the width of the depletion layer in the gate at threshold and hence the effective increase in the oxide thickness. The reduction in the gate depletion width increases also the screening of the random dopants in the gate depletion layer by the free carrier behind it and hence reduces their influence on the surface potential fluctuation in the channel. Nevertheless, even for substrate doping $N_A = 1 \times 10^{18}$ cm^{-3} the enhancement of the random dopant induced threshold voltage fluctuations remains between 25% and 45%.

B. MOSFET's with Low Doped Epitaxial Channel

An efficient approach to reduce the random dopant induced threshold voltage fluctuations without a drastic change in the MOSFET architecture is the introduction of a low doped epitaxial layer in the channel region [10], [19], [20], [26]. Here we investigate the effect of the single crystal silicon gate on σV_T in such devices.

Fig. 5 compares the oxide thickness dependence of the threshold voltage standard deviation σV_T for epitaxial channel MOSFET's with n$^+$-silicon and with metal gates. Both devices have a 10 nm epitaxial layer with doping concentration $N_A^e = 1 \times 10^{15}$ cm^{-3}, uniform doping $N_A^b = 5 \times 10^{18}$ cm^{-3} behind it, and dimensions $L_{\text{eff}} = W_{\text{eff}} = 50$ nm. The doping concentration in the silicon gate is $N_D = 1 \times 10^{20}$ cm^{-3}. The results are qualitatively similar to the results for uniformly doped MOSFET's presented in Fig. 2 but with reduction in the magnitude of the threshold voltage fluctuations typical for epitaxial devices [26]. Again, in the metal gate MOSFET's the fluctuations scale to zero with the corresponding scaling to zero of the oxide thickness. σV_T in the silicon gate MOSFET's is shifted up by almost constant values the the whole range of investigated oxide thicknesses.

The gate doping concentration dependence of σV_T is plotted in Fig. 6 for two epitaxial channel MOSFET's with gate oxide thickness 1 nm and 2 nm respectively, and with the same dimensions and channel doping concentrations as the devices in Fig. 5. Similarly to Fig. 3, the relative increase of the threshold voltage fluctuations compared to the metal gate simulations, is illustrated in the same figure. It has to be pointed out that practically over the whole range of investigated gate doping concentrations the percentage increase of the threshold voltage fluctuations in the epitaxial channel MOSFET's is smaller than the corresponding increase in the devices with uniform channel doping.

IV. Analysis

Here we return to the devices with uniform channel doping from the first part of the previous section in order to analyze the factors which are responsible for the enhancement of the threshold voltage fluctuations associated with the single crystal silicon gate. Using simulation experiments we will separate the contribution of the effective increase in the oxide thickness due to the gate depletion from the direct contribution of the random dopants in the gate depletion layer.

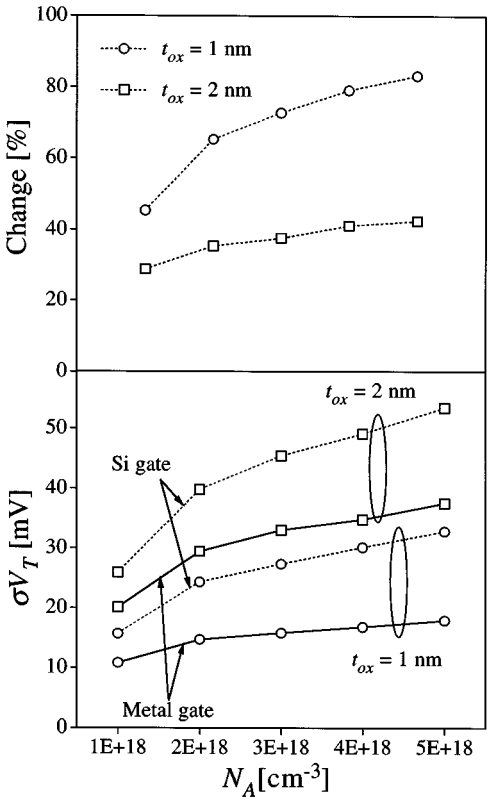

Fig. 4. Dependence of the threshold voltage standard deviation σV_T on the channel doping concentration N_A for single crystal silicon gate MOSFET's with different gate oxide thickness. The change in σV_T in respect to analogous metal gate devices is also plotted. The devices have $L_{\text{eff}} = W_{\text{eff}} = 50$ nm, and $x_j = 7$ nm. The gate doping concentration is $N_D = 1 \times 10^{20}$ cm^{-3}.

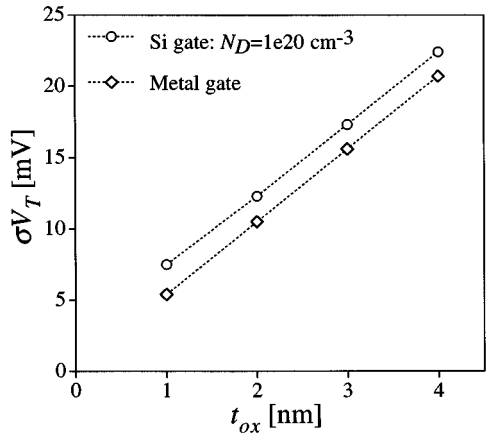

Fig. 5. Dependence of the threshold voltage standard deviation σV_T on the oxide thickness t_{ox} for single crystal silicon gate and metal gate MOSFET's with low doped epitaxial channels. Both devices have a 10 nm epitaxial layer with doping concentration $N_A^e = 1 \times 10^{15}$ cm^{-3}, and uniform doping $N_A^b = 5 \times 10^{18}$ cm^{-3} behind it. The dimensions are $L_{\text{eff}} = W_{\text{eff}} = 50$ nm and $x_j = 7$ nm. The doping concentration in the gate is $N_D = 1 \times 10^{20}$ cm^{-3}.

The parallel shift of σV_T in Fig. 2 for MOSFET's with a silicon gate suggests that the effective increase in the oxide thickness plays an important role in the enhancement of the threshold voltage fluctuations. Indeed the width of the gate depletion layer d_{pT} at threshold voltage does not depend on the thickness of the

gate oxide. Bearing this in mind the oxide thickness in (1) can be corrected by the equivalent gate depletion width leading to

$$\sigma V_T = C\left(t_{\rm ox} + \frac{\varepsilon_{\rm ox}}{\varepsilon_s} d_{pT}\right) \tag{3}$$

where ε_s is the dielectric constants of the silicon. The surface potential ψ_{pT} in the silicon gate at threshold can be determined by equating the depletion layer charges in the channel $\sqrt{2q\varepsilon_s N_A(2\phi_b)}$, where ϕ_b is the Fermi potential in the silicon substrate, to the depletion layer charge in the gate $\sqrt{2q\varepsilon_s N_D \psi_{pT}}$, which leads to $\psi_{pT} = 2\phi_b N_A/N_D$. The corresponding gate depletion width d_{pT} is given by

$$d_{pT} = \sqrt{\frac{4\varepsilon_S \phi_b N_A}{qN_D^2}}. \tag{4}$$

Equation (3) is similar in form to (2) but the value of the oxide thickness correction $\varepsilon_{\rm ox} d_{pT}/\varepsilon_s$ in it is smaller than the shift Δ in Fig. 2 extracted from the "atomistic" simulations.

The role of the gate depletion has been investigated separately from the effects associated with the random dopants in the gate by conducting simulation experiments in which the "atomistic" doping in the gate has been replaced with a continuous doping. The increase in the threshold voltage standard deviation associated with the silicon gate $\sigma V_{T(\rm poly)} - \sigma V_{T(\rm metal)}$, is compared in Fig. 7 for "atomistic" and continuous gate doping simulations. The increase corresponding to "atomistic" doping is extracted from the simulation results shown in Fig. 2. The increase in σV_T obtained from the continuous gate doping simulations is smaller for equivalent MOSFET's than the increase observed in the "atomistic" doping simulations. This is a clear indication that the gate depletion and the associated increase in the effective oxide thickness cannot solely explain the silicon gate enhancement of the random dopant induced threshold voltage fluctuations.

The increase in σV_T obtained from (3) is also plotted in Fig. 7 with the value of C extracted from the metal gate results presented in Fig. 2. The analytical results, which take into account solely the effective increase in the oxide thickness associated with the gate depletion, are in qualitative agreement with the corresponding continuous gate doping numerical simulations. We believe that the quantitative difference between the analytical and numerical results comes from the fact that carriers within a Debye screening length behind the depletion layer are involved in the screening of the random dopant charge in the channel region. Good quantitative agreement was obtained by modifying (3) to

$$\sigma V_T = C\left(t_{\rm ox} + \frac{\varepsilon_{\rm ox}}{\varepsilon_s}(d_{pT} + 0.5L_D)\right) \tag{6}$$

where L_D is the extrinsic Debye length.

In order to investigate separately the effect of the random dopants in the gate depletion layer on σV_T a second simulation experiment was conducted in which a continuous doping is used in the channel region and random dopants are placed only in the gate "atomistic" region. The MOSFET's in this experiment have the same dimensions and channel doping concentration as the devices in Fig. 7. Fig. 8 illustrates the dependence of σV_T on the oxide thickness $t_{\rm ox}$ for various doping concentrations in the gate. The results prove that the random dopants in the gate alone induce threshold voltage fluctuations. The corresponding values

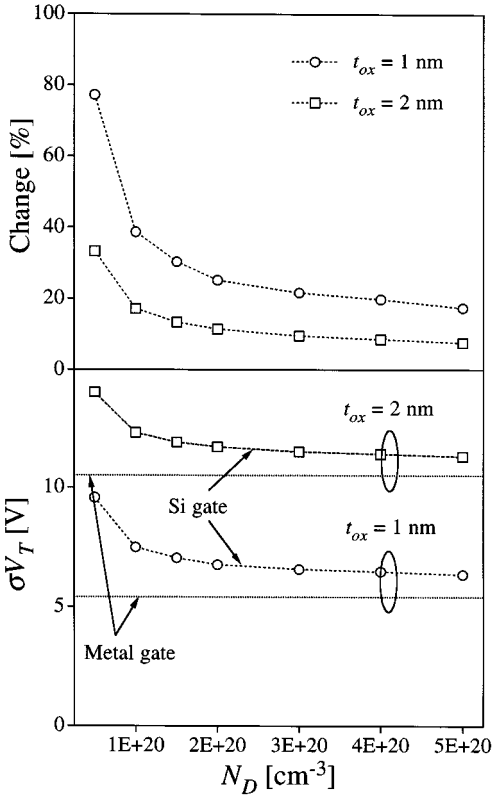

Fig. 6. Dependence of the threshold voltage standard deviation σV_T on the gate doping concentration N_D for MOSFET's with low doped epitaxial channels and two different oxide thicknesses. The change in σV_T in respect to analogous metal gate devices is also plotted. All other MOSFET parameters are the same as in Fig. 5.

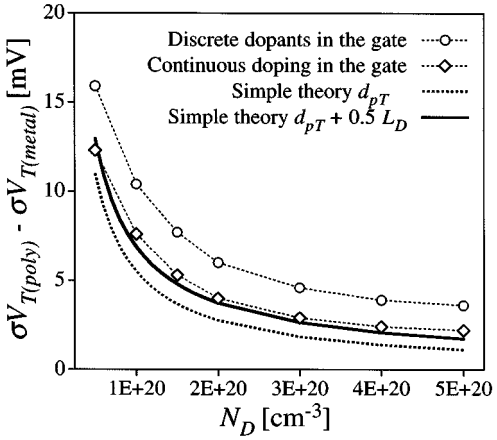

Fig. 7. Increase in the threshold voltage standard deviation associated with the single crystal silicon gate gate $\sigma V_{T(\rm poly)} - \sigma V_{T(\rm metal)}$ as a function of the gate doping concentration N_D. Comparison of simulations with "atomistic" and continuous gate doping of MOSFET's with $L_{\rm eff} = W_{\rm eff} = 50$ nm, $x_j = 7$ nm, $t_{\rm ox} = 2$ nm and $N_A = 5 \times 10^{18}$ cm^{-3}.

of σV_T decrease with the increase in the gate doping concentration. We believe that this is associated with the screening of the random dopant charge in the very thin gate depletion layer from free electrons behind it. With the increase of the doping concentration the gate depletion layer becomes thinner which leads to a more efficient screening of the random charge in it.

It is also important to note that for the range of $t_{\rm ox}$ from 1 nm to 4 nm presented in Fig. 8 σV_T is practically independent of

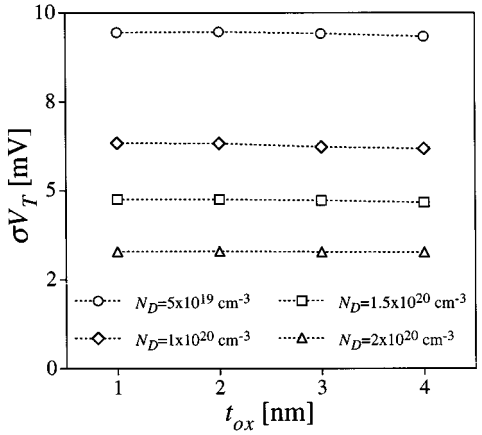

Fig. 8. Dependence of the threshold voltage standard deviation σV_T on the oxide thickness t_{ox} for MOSFET's with different "atomistic" doping in the single crystal silicon gate, continuous doping in the channel $N_A = 5 \times 10^{18}$ cm^{-3}, $L_{\text{eff}} = W_{\text{eff}} = 50$ nm, and $x_j = 7$ nm.

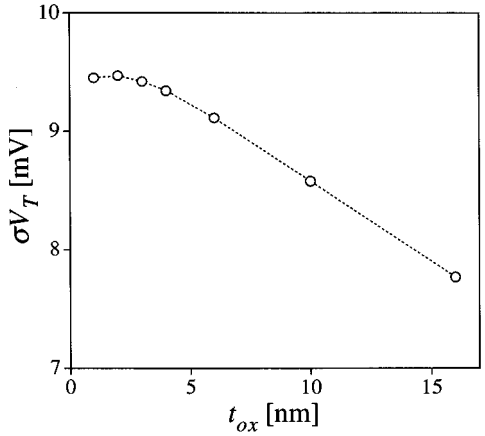

Fig. 9. Dependence of the threshold voltage standard deviation σV_T on the oxide thickness t_{ox} for MOSFET's with "atomistic" doping in the single crystal silicon gate $N_D = 1 \times 10^{20}$ cm^{-3} and continuous doping in the channel $N_A = 5 \times 10^{18}$ cm^{-3} $L_{\text{eff}} = W_{\text{eff}} = 50$ nm, $x_j = 7$ nm.

the oxide thickness. This is in agreement with the parallel shift of σV_T in Fig. 2 associated with the silicon gate and allows us to conclude that both the increase in the effective oxide thickness and the random dopants in the gate depletion region contribute to the magnitude Δ of this shift. However for the range of investigated devices the first of the two factors have a more pronounced effect.

The independence of the threshold voltage fluctuations on the thickness of the gate oxide, observed in Fig. 8, suggests that the fluctuations are associated not with individual dopants but most probably with dopant clustering in the gate. The influence of individual dopants in the gate on the surface potential in the channel rapidly decrease with the increase of the oxide thickness from 1 to 4 nm. At the same time the influence of the cluster regions will start to fade away only when the thickness of the gate oxide becomes comparable to the characteristic size of the clusters. In order to prove this hypothesis we extend the oxide thickness range to 15 nm in the simulation of one of the MOSFET from Fig. 8 with gate doping concentration $N_D = 5 \times 10^{19}$ cm^{-3}. The corresponding dependence of σV_T on the oxide thickness is plotted in Fig. 9 showing a plateau for oxide thicknesses below 4 nm and a linear reduction in the fluctuations for thicknesses above 5 nm. This is in agreement with the visually estimated size of the dopant clusters at the gate-Si/SiO_2 interface which for the MOSFET shown on Fig. 1 is in the range of 5 to 10 nm.

V. The Effect of the Grain Boundaries

As mentioned in the introduction, the grain structure of the polysilicon itself and particularly the effects associated with the grain boundaries introduce also mismatch in the threshold voltage of deep submicron MOSFET's [12]. The enhanced diffusion and segregation along the grain boundaries lead to a nonuniform polysilicon doping which may be complemented by a local penetration of dopants in the channel region. The large number of trapping states at the grain boundaries may result in a boundary potential pinning [27]. In the same time the number of grains, their areal distribution and the total length of grain boundaries varies in a transistor with given

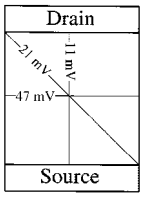

Fig. 10 Shift in the threshold for different positions of a single grain boundary in the gate region of a polysilicon gate MOSFET's compared to a similar MOSFET with a single crystal silicon gate. The both transistors $L_{\text{eff}} = W_{\text{eff}} = 50$ nm, $x_j = 7$ nm, $t_{\text{ox}} = 2$ nm, and $N_A = 5 \times 10^{18}$ cm^{-3}. The gate doping concentration is $N_D = 2 \times 10^{20}$ cm^{-3}.

dimensions. All these factors, which may affect the threshold voltage mismatch, depend strongly on the concrete fabrication conditions. Due to a lack of systematic knowledge and data in the literature it is difficult to incorporate consistently most of them in detailed numerical simulations. Therefore in this section we present simulation experiments which illustrate only one aspect of the influence of the polysilicon grain boundaries on the threshold voltage mismatch.

We investigate the effect of the position of only one polysilicon gate grain boundary in the channel region of a typical 50×50 nm MOSFET described in Section II of this paper with oxide thickness 2 nm and continuous doping concentration in the channel and in the polysilicon gate. We assume that the doping distribution in the two grains separated by the grain boundary is uniform and equal to $N_D = 5 \times 10^{20}$ cm^{-3}. We assume also that the surface potential is pinned at the grain boundary by monoenergetic acceptor type trapping states 0.5 eV bellow the conducting band edge. The results obtained in the simulations are illustrated in Fig. 10. A single grain boundary passing through the middle of the channel and parallel to the source and the drain results in the largest threshold voltage shift of 47 mV compared to a single crystal gate device. This shift, which is of the same order of magnitude as the random dopant induced standard deviation of the threshold voltage in a similar devices with a single crystal gate, illustrates the importance of the grain boundaries effects which should be studied in more details in the future.

VI. Conclusion

Apart form various effects associated with the polysilicon grain boundaries, the gate depletion region and the random dopants in it are important factors enhancing the mismatch in deep submicron CMOS transistors. Compared to metal gate devices even a single crystal silicon gate may cause a significant increase in the random dopant induced threshold voltage fluctuations in sub-100 nm MOSFET's with gate oxides ranging from 1 to 4 nm and uniform channel doping. The enhancement of σV_T increases with the reduction of the gate doping concentration.

The above effects are present also in fluctuation resistant MOSFET's with low doped epitaxial channel. However not only the absolute values of σV_T but also the relative enhancement of the threshold voltage fluctuations, associated with the gate depletion and random dopants, are smaller in the epitaxial channel MOSFET's compared to the devices with uniform channel doping.

Simulation experiments clearly indicate that the effective increase of the oxide thickness associated with the gate depletion, and the influence of the random discrete dopants in the gate depletion layer on the surface potential fluctuation in the MOSFET channel, both contribute to the polysilicon gate enhancement of the threshold voltage fluctuations. However, for the range of devices investigated in this paper, the effective increase in the oxide thickness has a more pronounced effect.

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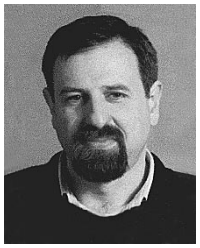

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