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Research Article

Poole–Frenkel Emission Saturation and Its Effects on Time-to-Failure in Ta-Ta_2O_5-MnO_2 Capacitors

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I-V characterization of Ta-Ta_2O_5-MnO_2 capacitors was investigated at different temperatures, and Poole–Frenkel (PF) emission saturation was experimentally observed. Under the saturation voltage, the *I-V* curves at different temperature converged, and the temperature dependency was vanished. Above the saturation voltage, the leakage current was decreasing as the temperature increased. In order to evaluate the effects of saturation voltages (V_S) on time-to-failure (TTF) of the capacitors, V_S were first determined at +2°C and +25°C, then voltage accelerating tests were conducted at 85°C under 1.6 times of rated voltage. The distribution of V_S and TTF of the samples were plotted and compared. It was shown that samples with lower saturation voltage failed earlier in the distribution of time-dependent dielectric breakdown. Comparing conventional methods for evaluating the quality of tantalum capacitors by measuring the leakage current at elevated temperature, the nondestructive measurement of saturation voltage at +2°C and +25°C may provide a novel and practicing approach tool to screening out capacitors with defected Ta_2O_5 layers.

1. Introduction

Because of its wide applications in electronics sciences, tantalum pentoxide (Ta_2O_5) has been extensively investigated both experimentally and theoretically over the past decades [1]. Due to its promising properties as a dielectric layer, Ta_2O_5 can be employed for anodic dielectric film in electrolyte capacitors, storage capacitors in DRAMs, and gate oxides in field effect transistors. Among these electronics devices, chip tantalum capacitors are the most important applications for Ta_2O_5. As dielectric layers, the properties of tantalum oxide films affected the leakage current, time-dependent dielectric breakdown (TDDB) behaviors, temperature stability, and other characteristics of tantalum capacitors. For capacitor applications, the most desirable property of the electrical insulator is its ability to not conduct an electrical current.

Because tantalum capacitors can be considered as a metal-insulator-semiconductor (MIS) structure [2], or referred as metal-oxide-semiconductor (MOS) structure (in this case, the Ta-Ta_2O_5-MnO_2 system), based on MIS theory, it provides a powerful tool to investigate the conduction mechanism. In order to improve the quality and reliability of tantalum capacitors, evaluation methods are needed based on the assessment of defects in the insulating layer. Basically, electrode-limited conduction and bulk-limited conduction are the two types of conduction mechanisms in dielectric films. Bulk-limited conduction mechanism depends on the electrical properties of the Ta_2O_5 itself, including the trap level, the trap density, the carrier mobility, and the density of states in the conduction band. Current transport through the MIS structure has been reported in many papers [3, 4]. Based on the physical mechanism, electron transport through the tantalum capacitor in normal mode (with the tantalum electrode positive) follows the PF and Schottky mechanisms [5, 6].

For the quality and reliability of tantalum capacitors can be affected by PF conduction mechanism, it is necessary to characterize the PF emission and its effect on time-dependent dielectric breakdown in tantalum capacitors. PF

conduction of $Ta-Ta_2O_5-MnO_2$ capacitors was investigated using *I-V* characterization technique at different temperature. The PF emission saturation predicted theoretically by Ongaro and Pillonnet [7] was experimentally observed in tantalum capacitors. Based on the technique developed by Harrel and Frey [8], the saturation voltages were measured. The concept of PF saturation leakage was also proposed in this paper. In order to evaluate the effect of PF saturation on time-to-failure in tantalum capacitors, voltage accelerating test were conducted.

2. PF Emission Saturation

The classical PF effect is the thermal emission of charge carriers from Coulombic (i.e., charged) traps in the bulk of a dielectric, enhanced by the applied electric field [9]. PF emission involves a mechanism that is similar to Schottky emission; namely, the thermal excitation of electrons may emit from traps into the conduction band of the dielectric [10]. Therefore, PF emission is sometimes called the internal Schottky emission. Considering an electron in a trapping center, the Coulomb potential energy of the electron can be reduced by the application of an electric field across the dielectric film. Driving by the electric field, the barrier height on one side of the trap can be reduced, thereby increasing the probability of the electron being thermally exited out of the trap into the conduction band of the dielectric. This process is illustrated in Figure 1, where a Coulombic potential well is shown in the presence of an electric field.

In Figure 1, $q\Phi$ is the ionization potential, which is the amount of energy required for the trapped electron to escape from the trapping center without electric field applied. $\beta\sqrt{E}$ is the amount of the trap barrier height reduced by the applied electric field. The schematic energy band diagram of PF emission is shown in Figure 2.

For a Coulombic attractive potential between electrons and traps, the current density due to the PF emission is

$$J = q\mu N_C E \cdot \exp\left[-\frac{q\phi - \beta\sqrt{E}}{kT}\right], \quad (1)$$

where J is the current density, μ is the electronic drift mobility, N_c is the density of states in the conduction band, $q\Phi$ (=Φ) is the trap energy level, T is the absolute temperature, q is the electronic charge, E is the electric field across the dielectric, k is the Boltzmann's constant, and β, the PF constant, which is given by Hill [11] as

$$\beta = \sqrt{\frac{q^3}{\pi\varepsilon_r\varepsilon_0}}, \quad (2)$$

where ε_0 is the permittivity in vacuum and ε_r is the optical dielectric constant.

Because PF emission is caused by thermal activation under an electric field, this conduction mechanism is often observed at high temperature and high electric field. Zednicek et al. reported that the dominant conduction mechanism through Ta_2O_5 is the PF emission at high temperature and high electric field [12].

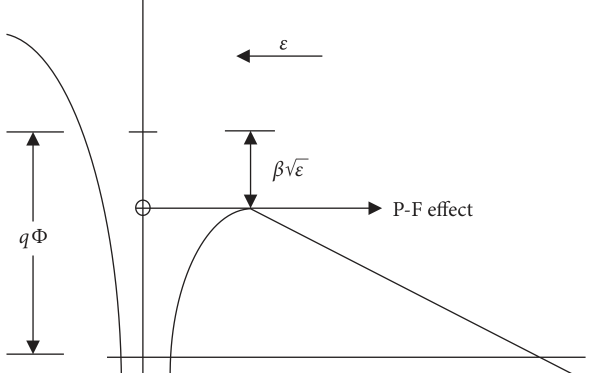

Figure 1: Coulombic potential well in the presence of an electric field illustrating the PF effect [8].

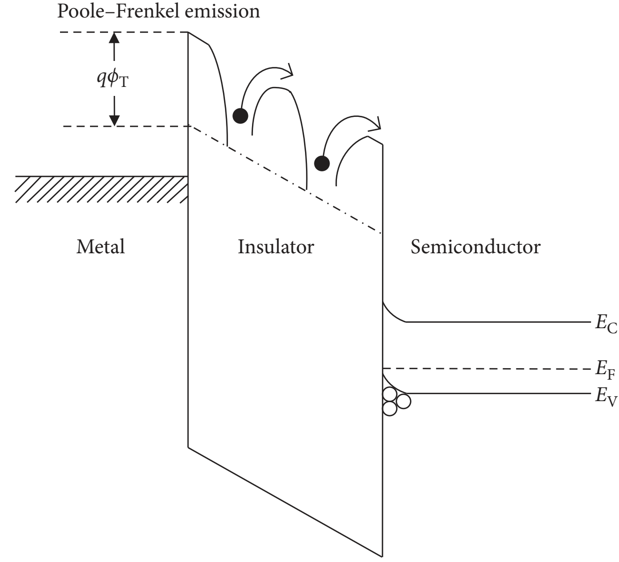

Figure 2: Energy band diagram of PF emission.

As the field increases, the potential barrier decreases on the right side of the trap, making it easier for the electron to vacate the trap by thermal emission and enter the quasi-conduction band of the dielectric. When the field reached a certain point that makes

$$q\phi_T = \beta\sqrt{E}. \quad (3)$$

From equation (1), we see that the temperature-dependent term is unity, and there is therefore no variation with temperature. Under this condition, the trap barrier height is reduced to the ground state of the trap, and all of the traps will be ionized. The condition described by equation (3) is defined as the saturation of the PF emission and was first predicted and observed by Ongaro and Pillonnet, etc. [7, 8, 13]. Thus, the voltage at which the curves converged is the PF saturation voltage or V_S.

Under PF saturation condition, where $q\phi = \beta\sqrt{E}$, then equation (1) can be written as

$$J = q\mu N_C E_s, \quad (4)$$

where E_S is the saturation electric field, and rewriting equation (4) as a current, which is given by

$$I = \frac{q\mu A N_C V_S}{d}, \tag{5}$$

where A is the area of current injection and d is the thickness of the dielectric.

Thus, the saturation current (I_S) can be defined by equation (5). As described by equation (5), at PF saturation voltage, for a given capacitor sample, the area and the thickness are constants; thus, the leakage current is directly proportional to N_c—the density of states in the conduction band of Ta_2O_5 film.

Mathematically, the general behavior of the curves can be understood based on equation (1). At low voltage, $q\phi > \beta\sqrt{E}$, the argument in the exponential is negative and results in an increase in current with temperature. At saturation voltage, $q\phi = \beta\sqrt{E}$, the temperature variation term is unity, and the current is independent of temperature. Past saturation, $q\phi < \beta\sqrt{E}$, the argument in the exponential is positive and results in an decrease in current with temperature [8].

The physical explanation of different voltage ranges is gained from an understanding of the PF mechanism as illustrated in Figure 1 and described earlier. At lower voltage, PF emission is the thermal ionization of trapped electrons, enhanced by the applied electric field. So, at a certain field, it can be expected that the higher of the temperature, the more of electrons to escape from the traps. At saturation, all of the electrons are detrapped, and the Coulombic traps have no effect on them. Therefore, the temperature makes no contribution to detrapping. When voltage is greater than V_s, the PF model becomes invalid. In this case, the leakage current is dependent on the scattering of electrons by thermal lattice vibrations and the scattering by lattice defects or impurities. The higher the temperature, the more intensively its atoms oscillate about their equilibrium position and the lower the free electrons in conduction band of the dielectric move. It means electrons will be scattered more frequently and results in an increase of resistivity. Thus, the leakage current of the dielectric decreases with temperature after the saturation voltage.

Based on the theory, Harrel and Frey developed a technique that makes the measurement and determination of saturation voltage an easily way in practice [8]. First, the saturation voltage of tantalum capacitors can be experimentally determined by measuring the I-V curves at different temperature. Secondly, the ionization potential can be extracted from the measurement and the use of equation (3). Using this technique, it is possible to find some correlations between the V_s and TTF in tantalum capacitors.

3. Experimental

The conventional chip tantalum capacitors were used in this study. Tantalum powders with specific charge per volume are pressed with tantalum wires into rectangular pellets. The pellets are then sintered in vacuum at high temperature for 30 min. After sintering, the tantalum anodes are anodized in a dilute aqueous solution. After formation of the dielectrics, the cathode electrode is produced by pyrolysis of manganese nitrate into manganese dioxide. The anode riser wire is welded onto the anode lead frame, and the cathode lead termination is adhesive to the silvered cathode layer. The unit is then molded into an epoxy-based encapsulant. All samples were marked before measurement and testing. Thus, the capacitor consists from metallic tantalum as anode electrode, insulating layer made from anodic Ta_2O_5 as dielectric, and semiconductor MnO_2 as counterelectrode and is referred as to Metal-Insulator-Semiconductor device or MIS device.

For observation of the PF saturation, the I-V characteristics for the capacitors were measured in the range of −65°C to +85°C by using a Keithley 2400 Source Meter. In order to be more universal, samples with lower voltage and larger capacitance with a value of 10 V 220 μF, median voltage and capacitance with a value of 35 V 22 μF, and higher voltage and lower capacitance with a value of 63 V 10 μF were measured.

In TDDB testing, capacitors with typical value of 35 V 22 μF was chosen for further study. In order to remove the potential influence of freezing water vapor in the test chamber, and for engineering practice, the measurements were conducted at +2°C and +25°C. The saturation voltages (V_s) and currents at V_s (refer as to saturation currents, or I_s) were recorded, respectively.

After I-V characterization, voltage accelerating tests were conducted at 85°C under 1.6xVr for 100,000 seconds. Each capacitor was connected with a fast-blow fuse in series and monitored during testing. The failure criterion was a catastrophic short or a scintillation event (considered as a blown fuse). Individual failure time was recorded by a monitoring system. The distributions of TTF, V_S, and I_S were plotted and compared.

4. Results and Discussion

4.1. Experimental Observation of PF Saturation in Tantalum Capacitors. I-V curves of three type capacitors with values of 35 V 22 μF, 10 V 220 μF, and 63 V 10 μF at −65°C, +25°C, and +85°C are measured as depicted in Figures 3–5, respectively.

PF emission saturation was observed from experimental for chip tantalum capacitors with typical value 35 V 22 μF as depicted in Figure 3. Similar phenomena were also observed in samples with lower voltage and larger capacitance for 10 V 220 μF and samples with higher voltage and lower capacitance for 63 V 10 μF, as shown in Figures 4 and 5. In Figure 3, the I-V curve at −65°C converges with the curve at +25°C around 30 V and with the curve at +85°C near 35 V. There are two converged points in the sample. There are no converged points with the curves between 2°C and 85°C for both 10 V 220 μF and 63 V 10 μF, as shown in Figures 4 and 5. Theoretically, the three curves converged at a single saturation voltage. The inconformity with the PF model as described can be explained as follows.

For a real tantalum capacitor with porous anode, the conduction mechanisms of leakage current are complicated.

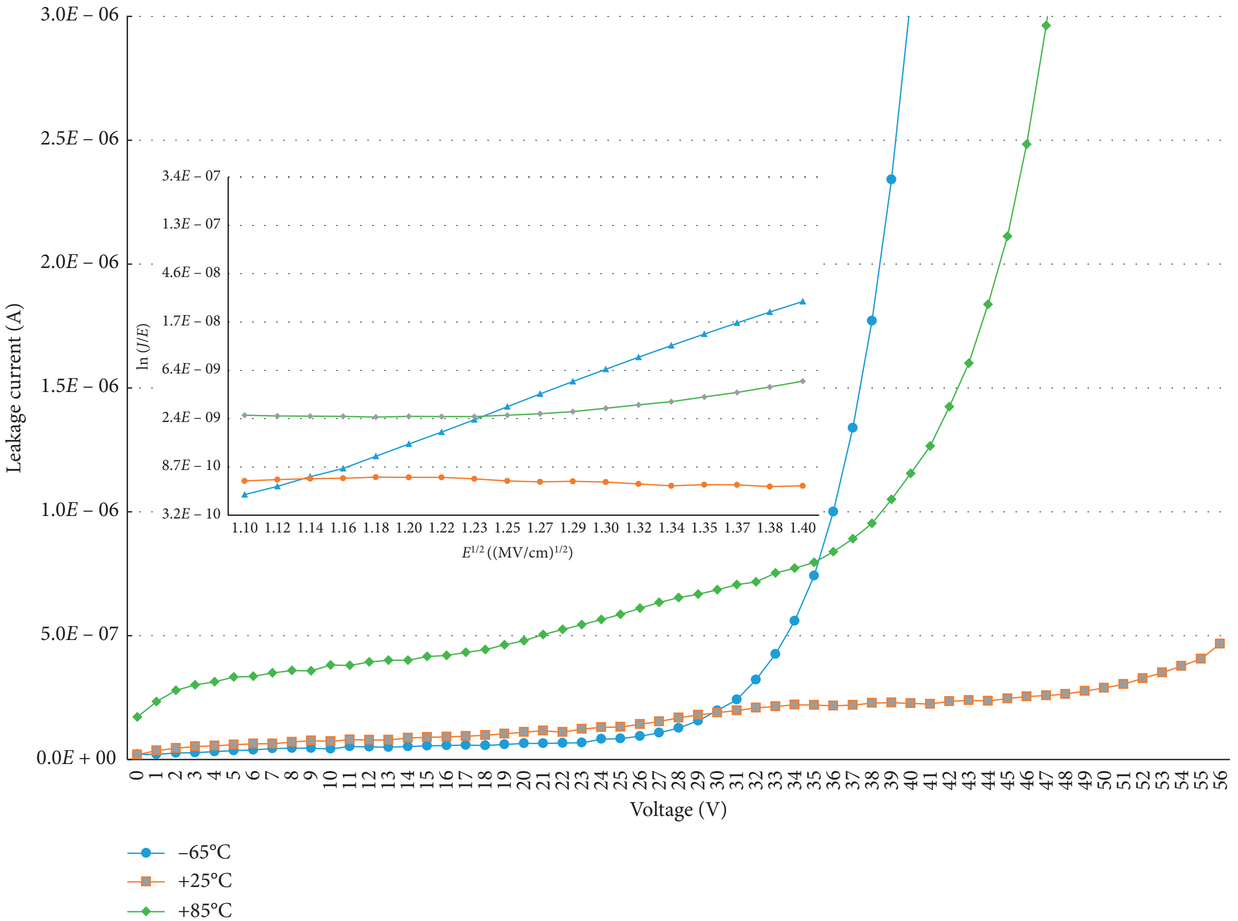

Figure 3: PF emission saturation observed in 35 V 22 μF chip tantalum capacitors. The I-V curve at −65°C converges with the curve at +25°C around 30 V and with the curve at +85°C near 35 V.

Tantalum capacitor is a typical device with metal-insulator-semiconductor (MIS) structure in which metal consists from tantalum, insulator layer Ta_2O_5, and semiconductor MnO_2. In a MIS capacitor, besides PF conduction, the leakage current may be consisting of Ohmic conduction, ionic conduction, Schottky emission, and tunneling effect. Except for tunneling effect, Ohmic conduction, ionic conduction, and Schottky emission are temperature-sensitive mechanism as summarized in Table 1 [4].

As illustrated in Figures 3–5, at low voltage below rated voltage, the current is linearly proportional to the voltage, and it is assumed that the conduction mechanism of capacitors with MnO_2 electrodes is mainly dominated by Ohmic conduction. Around the rated voltage, the PF plots ($\ln J/E - E^{1/2}$) are linear. It means that the conduction is mainly contributed by PF emission, and the leakage current is increased with temperature. As the voltage increased, tunneling effects may prevail the conduction process. Described by equations in Table 1, we expect an increase in leakage currents originated from these mechanisms as temperature increased. At elevated temperature, the delta of leakage currents caused by these temperature-sensitive processes are greater than the value increased by PF conduction above the range of saturation voltage at low temperature. Thus, we are not expected to observe the converged point between curves at −65°C and at +85°C, as shown in Figures 4 and 5. In order to reduce the influence from other conduction mechanisms, higher temperature ranges such as +85°C are not suggested for the measurement of PF saturation voltage. For removing the potential influence of freezing water vapor in the test chamber, +2°C was chosen as the lower measurement temperature. Based on the ideas, additional measurements were conducted at 2°C and 10°C as illustrating in Figure 6 for 35 V 22 μF.

As illustrated in Figure 6(a), the I-V curve at 2°C converges with the curve at +25 near 56 V, but there is no single converged point with the curve at +10°C but a crossover around 53 V. As the interval of temperature decreased, the converged points among the three curves get closer. However, there is still no single converged point among the curves, and there is no observable converged point between the I-V curve at 2°C and at +10°C but a crossover around 53 V. For practice, it is reasonable to set +2°C and +25°C as the two test points to determine the saturation voltage of tantalum capacitors and to further evaluate the effect of PF saturation on time-to-failure in tantalum capacitors. In Figure 6(b), at lower

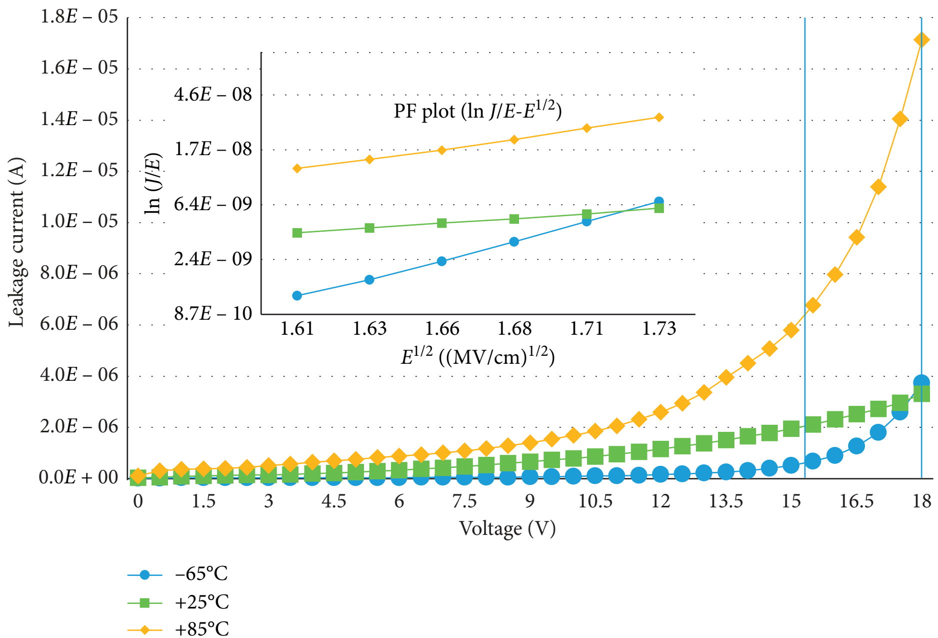

Figure 4: PF emission saturation observed in 10 V 220 μF chip tantalum capacitors. The I-V curve at −65°C converges with the curve at +25°C around 17 V. There is no converged point with the curve of 85°C.

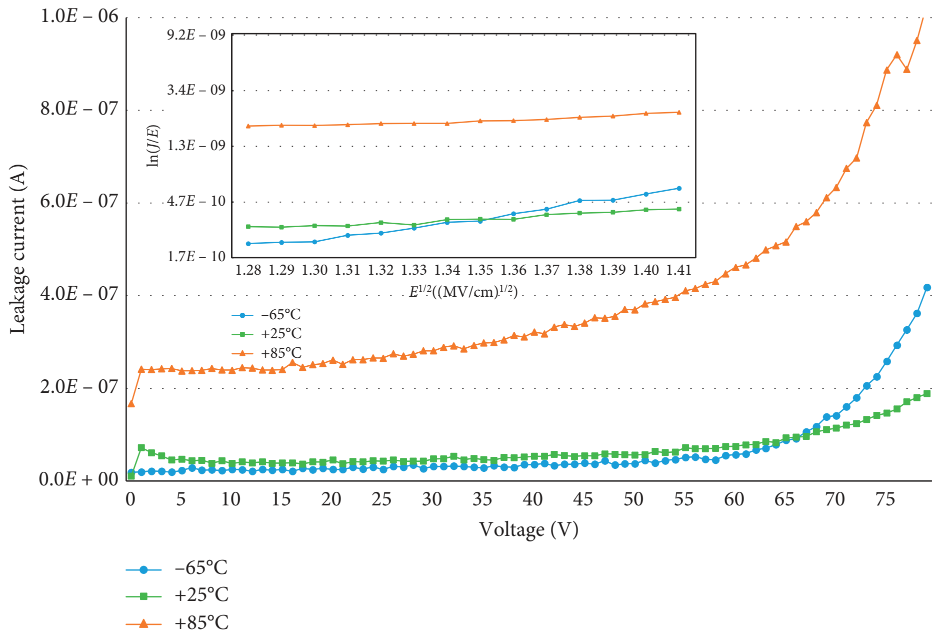

Figure 5: PF emission saturation observed in 63 V 10 μF chip tantalum capacitors. The I-V curve at −65°C converges with the curve at +25°C near 65 V. There is no converged point with the curve of 85°C.

field (below 2.13 MV/cm), the PF plots are nonlinear, where it is assumed that the conduction mechanism is not PF dominated. As the field increasing, the PF plots are becoming linear. As seen in Figure 6(b), in the high field region, PF plot at 2°C is more linear than the plot at 25°C; it means the other conduction mechanisms are involved as temperature increased, which resulted in the bendings of the PF plots at higher temperatures. According to a study made by Teverovsky previously [14], PF effect is the dominant conduction mechanism around the range of room temperature; this is another reason for choosing +2°C and +25°C as the measurement conditions.

4.2. Effects of the PF Saturation on Time-To-Failure in Tantalum Capacitors. The observed effects of PF saturation on time-to-failure of tantalum capacitors with typical value of 35 V 22 μF were characterized and tested as shown in Table 2.

Table 1: Basic conduction process

Process	Voltage and temperature dependence
Tunneling	$\propto V^2 \exp(-(b/V))$
Schottky emission	$\propto T^2 \exp[q(a\sqrt{V} - \Phi_B)/kT]$
Ohmic	$\propto V \exp(-(c/T))$
Ionic conduction	$\propto (V/T)\exp(-d'/T)$

(*Note.* V is the voltage applied, T is the temperature, Φ_B is the Schottky barrier height, and a, b, c, and d' are constants.)

The saturation voltages and leakage currents were measured at 2°C and 25°C, and TTF recorded during voltage accelerating test at 56 V (1.6xVr) and 85°C for 96 hours, respectively.

Based on the data measured in Table 2, time-to-failure of failed samples are sorted in ascending order as depicted in Figure 7, and the corresponding saturation voltage and saturation current curves of failed samples are illustrated in Figures 8 and 9, respectively.

First, by looking into details on the curves for TTF and V_s, we see that samples with low saturation voltages failed earlier during the voltage accelerating test as shown in Figures 7 and 8. It means that the higher the saturation voltage, the longer the life of the capacitor will be. Thus, time-to-failure of the capacitors is directly related to the saturation voltages.

For further investigating the effect of PF saturation on time-to-failure of tantalum capacitors, let us rewrite equation (3) as saturation voltage, V_s, as

$$V_S = d\beta^{-2}(q\phi)^2, \tag{6}$$

where d is the thickness of the dielectric. As described by equation (6), V_s is proportional to the exponential of ionization potential energy $q\phi$; thus, the lower the saturation voltage, the smaller the amount of energy required for a trapped electron to escape from the trapping center. Because the ionization potential energy is directly related to the properties of defects in the dielectric film, it is important to further analyze the formation of these defects in tantalum capacitors.

In a Ta-Ta_2O_5-MnO_2 capacitor, the tantalum pentoxide layer is formed by electrochemical process of anodization. The pellets of tantalum are dipped into a weak solution of phosphoric acid, at an elevated temperature, for example 65°C, and the voltage and current are controlled to form the pentoxide layer. Tantalum is valve metal, and the amorphous pentoxide grown is able to form a uniform, closely coupled layer over the tantalum surface. During the formation process, it is inevitable to incorporate defects into the dielectric layer. First, the commonly metallic impurities such as Ni, Fe, Cr in the tantalum powders are the main sources of defects in the dielectric. Carbon and oxygen also affect the conformity of the tantalum pentoxide layer. Furthermore, electrolyte-derived species in the acid solution may also incorporated into the film during the anodization process. These impurities may become the Coulombic centers in the dielectric layer. Different impurities may create different defect energy levels in the diagram band. These defective energy levels can affect the ionization potential. In tantalum capacitors, these defects are also as refer to oxygen vacancies.

In Ta_2O_5, TDDB has been demonstrated for solid tantalum capacitors [15, 16] and studied using MIM and MIS structures for DRAM applications [17–19]. Failures of tantalum capacitors at steady-state conditions can be considered as a result of field and temperature-accelerated degradation of the electrical strength of the Ta_2O_5 dielectric, or as a time-dependent dielectric breakdown, TDDB [20].

At the beginning of the voltage applied to the MIS capacitor, current transports through the Ta_2O_5 layer is limited by the barrier at the interface between Ta_2O_5-MnO_2. The emission of electrons from the surface of MnO_2 into the conduction band of Ta_2O_5 is considered as thermionic process, or the Schottky effect. Because the emission is controlled by the barrier height at the interface between the electrode and the dielectric, the Schottky effect is an electrode limited process.

Over the time, electric field in Ta_2O_5 assists in the release of electrons from the traps, suggesting that electrons are hopping from one trap to the other with low mobility. Meanwhile, under the voltage stress, oxygen vacancies and other positive charged traps in the bulk of Ta_2O_5 are migrated toward the cathode, which lowering the barrier height at the interface between the insulating layer and the semiconductor electrode. When the Schottky barrier is lowered enough, the electrons are more easily emitted and a transition from electrode-limited conduction to bulk-limited conduction occurs.

Previous study by Teverovsky [16] shows that the degradation of leakage currents of tantalum capacitors is caused the migration of oxygen vacancies to the cathodes, lowering the Schottky barrier at the MnO_2-Ta_2O_5 interface. After sufficient time, the oxygen vacancies arriving at the cathode side will accumulate as a sheet of positive charge, and increased band bending occurs in the dielectric as a result. This may result in a decrease of the effective thickness of Ta_2O_5 layers. The leakage mechanism then changes from the PF to the Fowler–Nordheim mechanism, and the leakage current will increase further with time [21] and resulted in a final dielectric breakdown. Based on the above assumption, the concentration of oxygen vacancies and other defect-related traps may contribute to the degradation process of leakage currents and dielectric breakdown in tantalum capacitors.

Furthermore, if we look more in-depth into the curves of TTF and I_s, we see that samples with lower saturation currents failed earlier during the voltage accelerating test as shown in Figure 9. It seems that this phenomenon is contrary to common sense from basic conduction process.

According to the model developed by Lloyd and coworkers [22], the rate of defect generation is proportional to the product of the injected electron current and the probability that when the inelastic scattering event occurs, the electron has more energy than the threshold energy for defect generation. Assuming the nature of the defects caused by the energetic electron, the latter can be written as

$$P(\lambda > \lambda_t) = \exp\left(-\frac{\lambda_t}{\mu}\right). \tag{7}$$

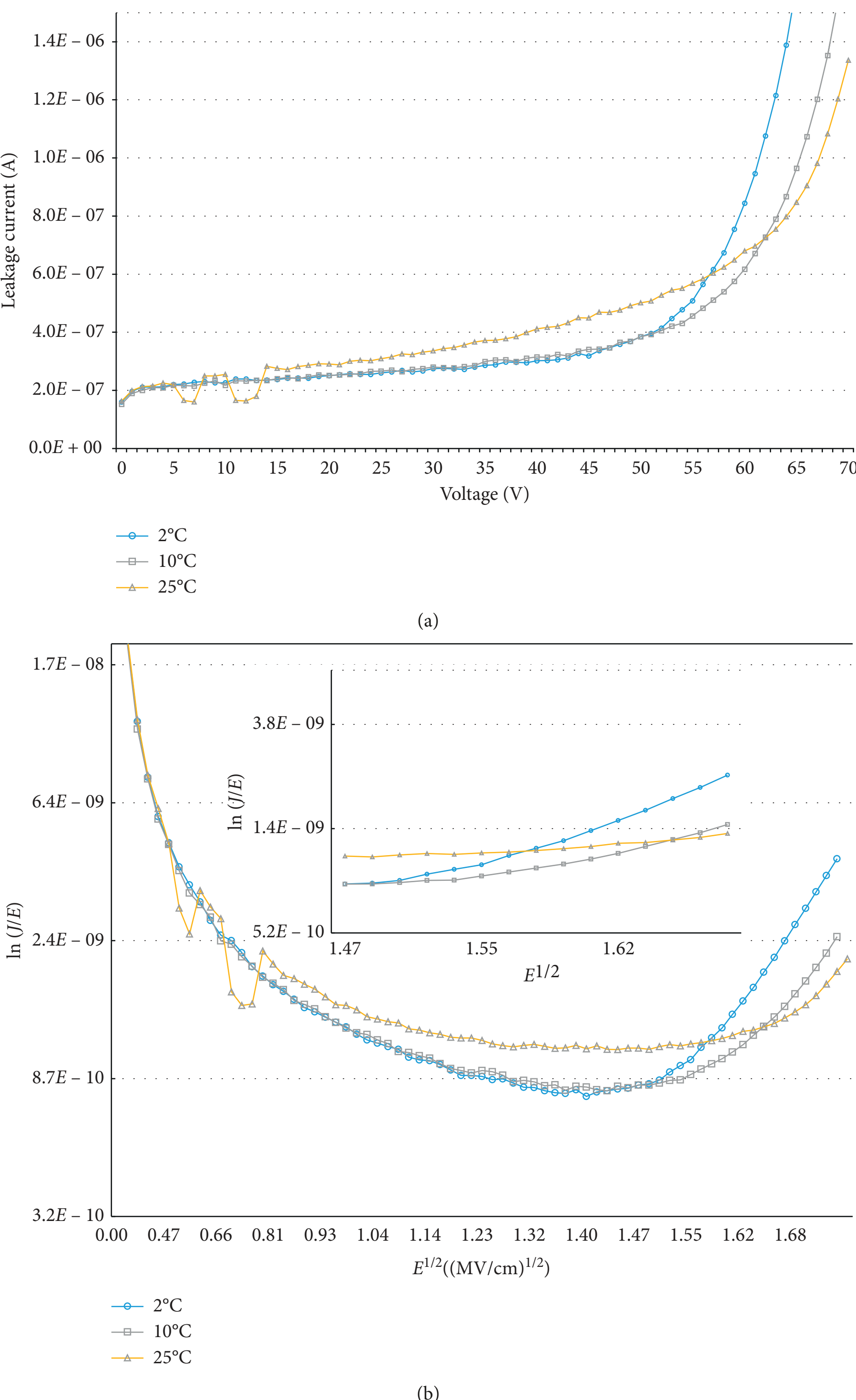

Figure 6: PF emission saturation observed in 35 V 22 μF chip tantalum capacitors at temperature range within 25°C. (a) I-V plots and (b) PF plots ($\ln J/E - E^{1/2}$).

Table 2: Saturation voltages (V_s), leakage currents (I_s), and TTF of failed samples.

Sample ID	V_s (V)	I_s (μA)	TTF (s)
A	44	0.423	6370
B	50	1.27	19795
C	54	1.05	25165
D	60	3.78	64954
E	48	0.578	10707

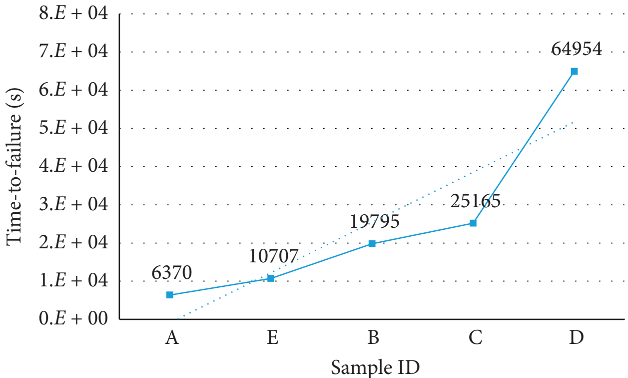

Figure 7: Time-to-failure of failed samples in ascending order for 35 V 22 μF chip tantalum capacitors after 1.6xVr at 85°C for 100,000 s.

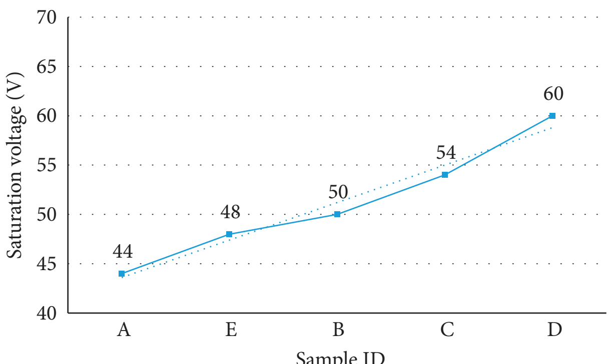

Figure 8: PF emission saturation voltages of failed samples as sorted by time-to-failure in ascending order for 35 V 22 μF chip tantalum capacitors after 1.6xVr at 85°C for 100,000 s.

In equation (7), λ is the electron path length; λ_t is the path length needed to acquire the threshold energy E_t, and μ is the mean free path of the electron in the dielectric. Using the relationship $\lambda_t = E_t/qE$,

$$P(\lambda > \lambda_t) = \exp\left(-\frac{E_t}{\mu qE}\right). \quad (8)$$

If it takes just one single event to cause failure, then the probability of failure as a function of time will be simply the production of current density and equation (8). For PF conduction, the probability of failure as a function of time at constant temperature will simply be

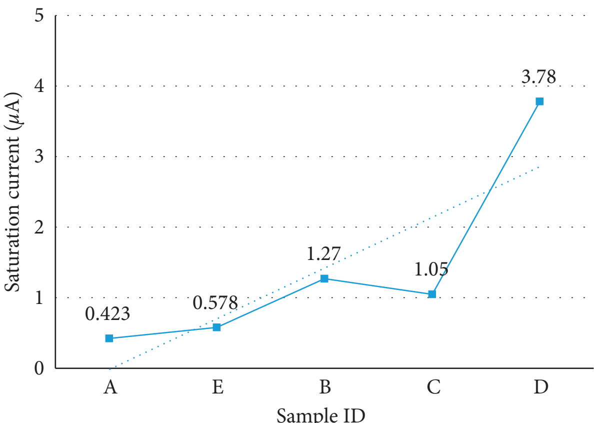

Figure 9: PF emission saturation currents of failed samples as sorted by time-to-failure in ascending order for 35 V 22 μF chip tantalum capacitors after 1.6xVr at 85°C for 100,000 s.

$$P(E,t) = \mathrm{JP}(E)t = \mathrm{AE}\exp\left(\gamma\sqrt{E} - \frac{E_t}{\mu qE}\right)t, \quad (9)$$

where A and γ are the parameters related to the PF conduction, $A = q\mu N_C$, $\gamma = -(q\phi - \beta\sqrt{E})/(kT\sqrt{E})$. It is assumed the accumulation of defects up to some threshold number N_f will result in dielectric failure at time TTF. Thus, N_f can be obtained by integrating equation (9) from $t = 0$ to $t = \mathrm{TTF}$:

$$N_f = \int_0^{\mathrm{TTF}} \mathrm{AE}\exp\left(\gamma\sqrt{E} - \frac{E_t}{\mu qE}\right)\mathrm{d}t + N_0. \quad (10)$$

The time to dielectric failure is predicted by the following equation [21]:

$$\mathrm{TTF} = \frac{(N_f - N_0)}{\mathrm{AE}}\exp\left(-\gamma\sqrt{E} + \frac{E_t}{\mu qE}\right). \quad (11)$$

The $\sqrt{E}$ dependence in equation (11) is due to the PF injection mechanism, whereas the $1/E$ dependence within the exponential function arises from the exponential probability distribution function in equation (7).

As described in equation (11), at a given electric field E, for given number of preexisting defects, the greater the threshold number defects N_f, the longer the time-to-fail (TTF) for the dielectric. On the other hand, in a MIS capacitor, in general, the current is increasing with voltage. Thus, it is reasonable that the higher the saturation voltage, the larger the saturation current, and the longer the time for these capacitors to fail. As seen from Figure 9, in the order of microampere range, because the differences between samples are small and may be affected by measuring conditions, it is suggested that we should take the saturation voltage as a benchmark rather than saturation current while evaluating the effects of PF saturation on the TDDB behaviors of tantalum capacitors.

5. Conclusions

PF conduction of Ta_2O_5 film in Ta-Ta_2O_5-MnO_2 capacitors was investigated using *I-V* characterization technique. *I-V*-T curves were measured from −65°C to +85°C, and the PF emission saturation was experimentally observed. At low voltage, $q\phi > \beta\sqrt{E}$, an increase in current with temperature was observed. At saturation voltage, $q\phi = \beta\sqrt{E}$, the current is independent of temperature. Past saturation, $q\phi < \beta\sqrt{E}$, the argument in the exponential is positive and results in an decrease in current with temperature. A physical explanation was also suggested for the PF saturation and post-saturation. It is supposed that the current decreasing is due to scattering, and this is not predicted in the either the classical or modern model [7]. By measuring the saturation voltages and currents at temperature of +2°C and +25°C, effect of PF saturation on time-to-failure was further investigated through voltage accelerated test. It shows that the higher saturation voltages, the longer the time capacitors to fail. It means that properties such as defect energy level of traps in the dielectric have profound influences on time-to-failure of the dielectric. Comparing conventional methods for evaluating the quality of tantalum capacitors by measuring the leakage current at elevated temperature such as +85°C and +125°C, the nondestructive measurements of saturation voltages at +2°C and room temperature (+25°C) may provide a novel and effective way to screening out capacitors with defected Ta_2O_5 layers in engineering practice.

Data Availability

The data used to support the findings of this study are included within the article and can be accessed without any restrictions.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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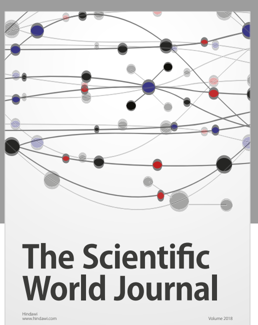

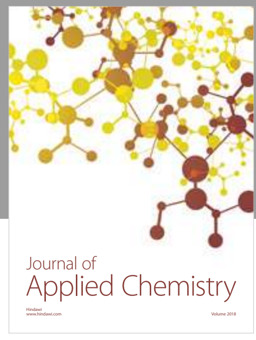

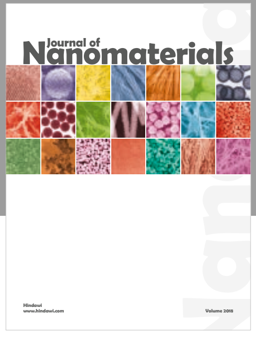

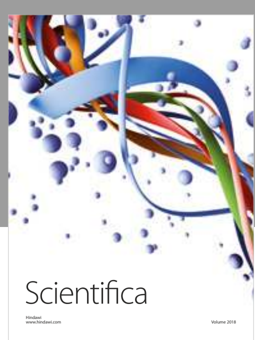

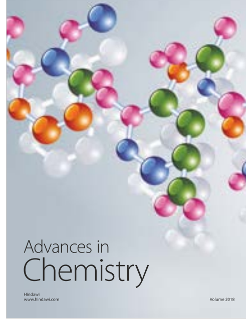

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