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Porous silicon as a sacrificial material

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Abstract. Porous silicon is emerging in micromachining technology as an excellent material for use as a sacrificial layer. This is largely due to the ease of fabrication and freedom of design it allows. The rate of pore formation is heavily dependent upon the doping type and concentration of the silicon, allowing patterned porous silicon formation through selective doping of the substrate. Etch-rates above 10 mm min^{-1} have been reported for highly doped material. Silicon that has been made porous can be quickly and easily removed in a dilute hydroxide solution, as low as 1%. Porous silicon technology offers the unique ability to fabricate free-standing structures in single-crystal silicon with separation distances from the substrate ranging from a few microns to over one hundred microns. A review of the development of porous silicon for micromachining applications is given.

1. Introduction

The high mechanical quality of single-crystal silicon has led to a wide range of mechanical sensors. The first devices were fabricated using bulk micromachining from the backside. In bulk micromachining, a masking layer is patterned on the back of the wafer and the unmasked areas of bulk silicon are removed in an anisotropic wet chemical etch such as KOH. The etching can be stopped via time stop, p+ etch-stop or electrochemical etch-stop. Bulk micromachining allows free-standing structures to be constructed of single-crystalline silicon and results in a planar surface on the front side of the wafer. There are, however, several disadvantages to this process. Since KOH stops etching on $\langle 111 \rangle$ planes, it has an etching slope of 54.74°, limiting the potential packaging density of the structures [1]. The required double-sided lithography adds to process complexity, and the time it takes to etch through the entire thickness of a wafer (up to eight hours, depending on etch conditions and wafer thickness) adds to processing time. Another disadvantage of KOH etching is that it is incompatible with standard CMOS processing due to wafer contamination with alkali metal ions, and therefore needs to be applied as a post processing step. This problem can however be alleviated using alternative non-contaminating etchants such as TMAH [2]. A further limitation on packing density is its severe underetching of a mask at convex corners resulting in the need for large corner compensation structures [3] .

The problems associated with KOH etching are eliminated by surface micromachining, in which thin film processing is performed on top of a sacrificial material layer which is then removed in an isotropic wet chemical etch, leaving the materials deposited on top of it as free-standing structures. However, thermal silicon dioxide (SiO_2) and chemically deposited (CVD) SiO_2 and doped silicate glasses (PSG, BSG, BPSG), which are the materials most commonly used as sacrificial layers, are limited in thickness to a few microns. This limits the separation between free-standing structures and the substrate to a distance which is not large enough for many micromachining and microsensor applications [4]. Another disadvantage of surface micromachining is that the resulting free-standing structures can be made only of materials that are deposited on top of the bulk silicon, such as polycrystalline silicon or silicon nitride, and not of single crystal silicon. Topographical problems are also encountered due to non-planarity of thermally grown and CVD sacrificial layers. Surface micromachining does, however, offer several advantages, including high packing density and electronics process compatibility [5].

Many of these disadvantages can be avoided by using porous silicon as a sacrificial etching layer. The formation of pores in silicon results from selective electrochemical etching in hydrofluoric acid (HF). The resulting surface discoloration was first discovered by Uhlir [6] in 1956 and Turner [7] in 1958 who suggested that this was a thin film deposited on the surface. In 1972 Theunissen reported that the colouration was due to pore formation in the silicon [8]. Electrochemical etch-stop using the electropolishing of n+ silicon and stopping on a n-type epitaxial layer was applied by Esashi *et al* to the manufacture of pressure sensors [9]. This process was similar to the electrochemical etch stop in KOH.

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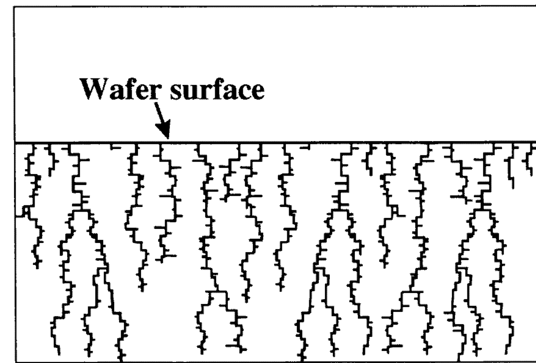
Porous silicon technology combines the advantages of both bulk and surface micromachining. The sacrificial layer is formed in the silicon substrate and can be processed from the front side. Porous silicon membranes have been formed using the full thickness of the wafer [10] and channels 100 μm deep have been formed in the silicon substrate using a porous sacrificial layer [4]. Furthermore, sacrificial porous silicon is a material that makes it possible to manufacture free-standing structures of high mechanical and electrical quality [11] since the mechanical structures may be constructed from single-crystal silicon. Sacrificial layer formation can be patterned both by selective substrate doping, as porous silicon formation is highly selective with respect to different dopant types and concentrations [12,13], and by masking of the substrate [4]. Porous silicon provides a planar sacrificial surface and is formed much more quickly than thermally grown or chemically deposited sacrificial layers. It can also be oxidized to form thick sacrificial oxide layers [13], thick oxide layers for thermal isolation [14] or for SOI applications [15], or used directly as a sacrificial layer [11]. The large surface area of porous silicon yields a high etch rate, which is desirable for a sacrificial layer. Porous silicon is rapidly etched in dilute hydroxide solutions at room temperature. Using porous silicon as a sacrificial layer also greatly reduces processing time and complexity, as well as device area, over bulk micromachining. Sacrificial porous silicon has also been used to increase the air gap in surface micromachining. After forming n-doped polysilicon structures on an oxide sacrificial layer the underlying p-type substrate was made porous. The resulting surface micromachined structures were 30 μm above the bulk [16].

The formation of porous silicon is an isotropic process, so devices may lie in any direction relative to the crystal orientation and structures have very well-defined geometries since etch stops obtained by differential doping offer excellent selectivity [12,13]. Depending on the etching conditions, both n- and p-type material can be selectively etched, although the resulting pore structure is quite different as shown in figure 1 [17]. Finally, this technology is fully compatible with standard CMOS processes if a non-alkali solution such as photoresist remover is used to remove the porous silicon [4].



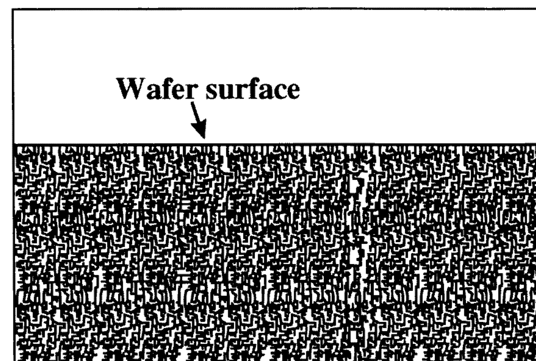


Figure 1. Structure of porous silicon in (a) n-type material and (b) p-type material [17].

2. Porous silicon formation

Porous silicon is formed by the anodic electrochemical etching of monocrystalline silicon in hydrofluoric (HF) acid (figure 2). Porous silicon can also be formed using chemical etching [18], but this has a much slower formation rate. Though silicon is not attacked by HF alone, application of an anodic bias moves the positive charge carriers (holes) to the Si surface where they weaken the Si–Si bonds, allowing them to be attacked by F^- ions. When suitable etch parameters (HF concentration and current density) are used, pores are formed in the substrate [19]. The terms ‘anodic etching’ and ‘anodization’ are used to describe pore formation because the semiconductor acts as the anode in the electrochemical reaction in which silicon atoms are separated from the crystal. Ethanol is often added to the HF solution to reduce its surface tension, thereby allowing the H_2 gas formed during the reaction to escape, preventing it from sticking to the etching surface and improving the homogeneity of the resulting porous layer [20]. There are several theories for the exact nature of the pore formation in the literature [21–24]. All agree on the need for holes

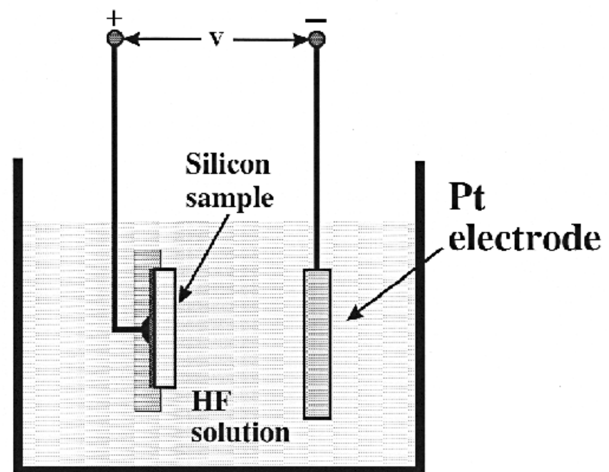


Figure 2. Anodic etching for formation of porous silicon in HF solution.

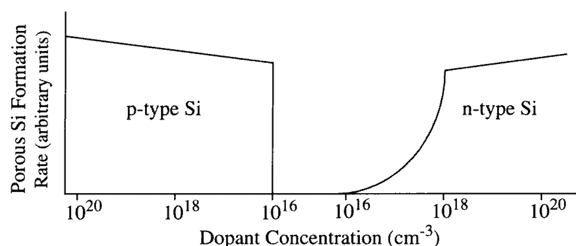


Figure 3. Rates of pore formation in p-type and n-type silicon as a function of dopant concentration with no light generation. P-type silicon becomes porous at any doping level, while n-type silicon becomes porous only when it is doped highly enough to allow for significant interface tunneling (taken from Eijkel *et al* [12]).

in this process, but there is less agreement on the reaction at the tip of the pore.

The formation mechanism of porous silicon is a charge exchange between the semiconductor surface and the electrolytic HF solution. The Si–HF interface acts as a Schottky contact and the charge exchange mechanism is dependent upon the dopant type of the silicon. In p-type material, holes are readily available at the Si–HF interface. In the case of low to moderately doped n-type silicon, holes may be generated by light. For n+ material tunneling of electrons away from the interface facilitates the etching [25]. In the absence of light generation, significant pore formation in n- type substrates occurs only at doping levels above approximately 10^{18} cm^{-3}, when the space charge region is narrow enough to allow tunneling. The relative rates of pore formation in n-type and p-type silicon of different dopant concentrations are shown in figure 3 [12]. In this case the current density was 0.1 A cm^{-2} and the HF concentration 5%. This effect is shown in figure 4. This structure was formed using a n-type diffusion mask. The p-type susbtrate has been etched under the n-type region as expected. An additional etch has occurred at the surface of the n-type diffusion. In this layer the doping concentration was sufficiently high for porous formation to occur. This effect was used by Esashi *et al* [9] to achieve an n-type etch-stop on an n+ substrate. Stopping at a p–n junction was also reported by Gupta *et al* [26].

There are several parameters which define the etch rate, or rate of porous silicon formation. The most important are dopant type and concentration, HF concentration, and applied current density [19]. Since pore growth is believed to be controlled by the diffusion of holes from the silicon crystal to the Si–HF interface for p-type material [21], and the tunneling of electrons from the Si–HF interface to the crystal for heavily doped p- and n-type material [22], factors that affect the rate of these transfers therefore control the etch rate. Etch rate increases with current density, since a higher current density provides an increase in the number of charge carriers, and thereby the rate of charge exchange across the interface. The increase in substrate voltage also facilitates charge exchanges by lowering the energy barrier in p-type silicon and lowering the conduction band in the bulk of n-type silicon (figure 5). Etch rate increases with dopant concentration for both n-type and p-type silicon,

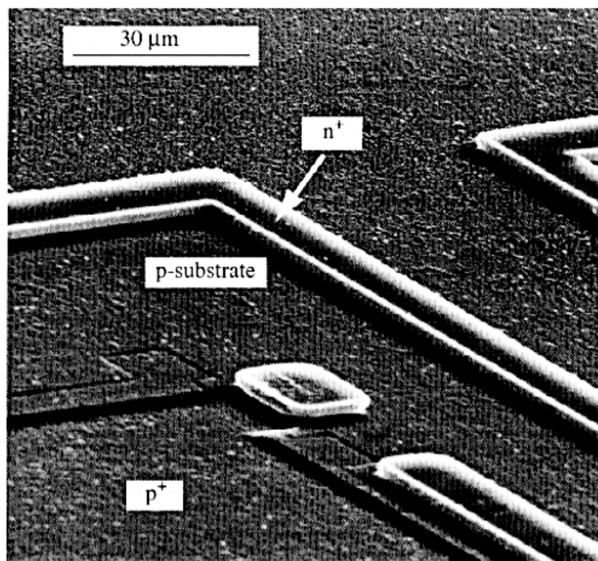


Figure 4. SEM photograph showing the selective nature of porous silicon formation.

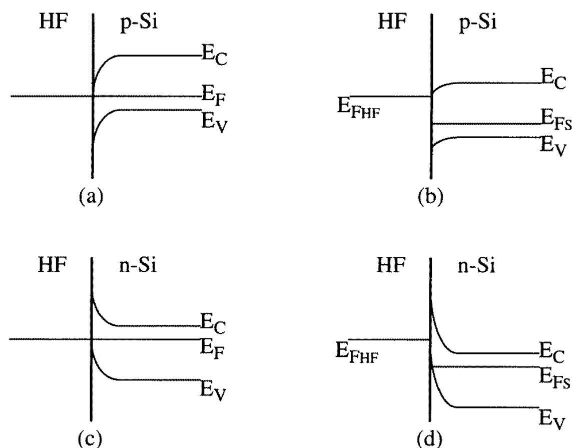


Figure 5. Energy band models of silicon in HF solution: (a) p-type silicon at zero bias, (b) p-type silicon positively biased, (c) n-type silicon at zero bias and (d) n-type silicon positively biased.

because the decreased resistivity as a result of increased doping enhances current flow. The rate differential as a function of dopant concentration is much greater for n-type than for p-type substrates due to the low probability of tunneling at low doping levels. An increase in HF concentration has been found to result in a drop in porosity [27], probably due to the H^+ ions effectively passivating the surface [28]. Higher HF concentration has also been found to result in an increase in pore formation rate [29].

More recently alternative etchants for porous formation have been investigated. One of these etchants, based on ammonium fluoride and acetic acid has the distinct advantage of having an extremely low etch-rate for alumiunium [30].

Lateral pore formation rates as a function of current density and two different HF concentrations (20% and 40%), for p and p+ doped silicon is shown in figure

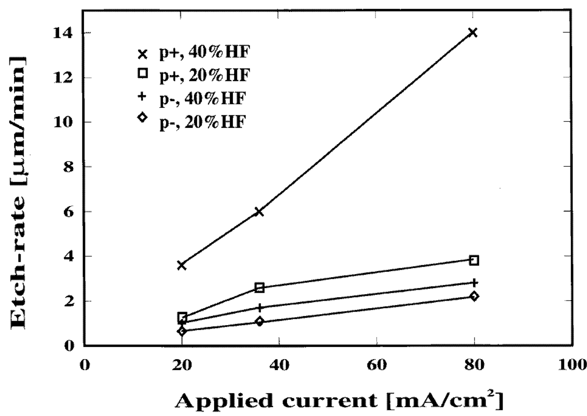


Figure 6. Etch rate as a function of applied current for p and p+ type material.

6. The effect of HF concentration is less pronounced for the low doped material, which agrees with the results of Steiner *et al* [4]. Data on pore formation rate as a function of current density, HF concentration and doping, may be used to make predictions regarding the selectivity of different etch recipes, or combinations of particular current densities and HF concentrations, for different types of silicon. The greatest differences in pore formation rates between differently doped types of silicon, when measured on separate uniformly doped substrates, occur when both a high current density and a high HF concentration are used in anodic etching.

The etching of each type of material is dependent upon several factors. By adjusting the etching parameters selective pore formation can be achieved [31]. Such a technique has been applied to selective pore formation in p+ silicon [32]. In this case buried p+ layers, under a n- type epitaxial layer, were made porous to enable the formation of a buried oxide. Care should be taken when using this technique to minimize the thermal processing in order to prevent out-diffusion and auto-doping of the epitaxial layer.

The relative pore formation rates in the different dopant types of silicon found on the same samples were very different from those found on separate uniformly doped samples. This was because different amounts of current flow through different regions in a non-uniform doping pattern. When n-type and p-type silicon are side by side, a diode voltage exists across the junction, causing the current to stay on one side of the junction and that material to become porous much more quickly than the material on the other side of the junction. As a result, even though pore formation rates in n+ silicon were found to be higher than those in p- and p+ silicon on uniformly doped samples, n+ rings act as an etch stop to pore formation in p- and p+ material. When pore formation in lightly p-doped areas reaches p+ silicon, on the other hand, the rate of formation increases dramatically, as there is no diode voltage across the junction and current flow increases in the low resistivity p+ material. The 40% HF/80 mA cm^{-2} recipe has been found to provide the best pore formation selectivity at dopant junctions [2]. The effect of the p–n junction can also be enhanced by the application of illumination [33]. Short circuiting the p–n junction without illumination results in selective etching of the p-type layer results, whereas reverse biasing of the p–n junction and illumination (650 mW cm^{-2}) results in selective etching of the n-type layer. Using high currents selective electropolishing at the rate of 10 μm min^{-1} was achieved. For lower currents porous silicon was selectively formed at rates of up to 0.6 μm min^{-1}. This porous layer was later removed by chemical etching. The direct generation of a photo current via a p–n junction has also been used to achieve selective porous formation [34]. For surface devices (upper 4 μm of the wafer) the photogeneration alone was sufficient and no external bias was required. In the same paper deep porous etching was also performed and in this case an additional bias was required. The effect of illumination on the etch rate of n-type material in HF has been applied to laser induced etching [35]. For example the etch rate of 0.25–0.35 Ω-cm n-type silicon was increased in 38.8wt% HF to 1.25 μm min^{-1} for a light intensity of about 2200 W cm^{-2}.

3. Use as a sacrificial layer

3.1. Sacrificial techniques

Once silicon has been made porous, it can be removed in diluted hydroxide solutions (KOH, NaOH, NH_4OH, etc) and, because of its high surface area, dissolves very quickly even at room temperature [13,36]. KOH concentrations as low as 1%, at room temperature have been used to remove porous silicon layers [37]. Care must be taken to keep the etch rate slow enough so that the reaction does not become violent, causing delicate microstructures to be destroyed by bubbles. Porous silicon can also be removed by photoresist remover if this is more compatible with a specific process [4].

Anodic etching provides an additional sacrificial technique known as electropolishing. For a solution of any given HF concentration, there is a critical current density above which electropolishing, rather than porous silicon formation, takes place under conditions of anodization. Electropolishing uniformly removes portions of the crystal rather than etching channels into a substrate that remains otherwise intact. Unlike porous material formation, the etch rate of electropolishing is mostly independent of the doping type of silicon being etched, making it much less selective and therefore less desirable as an etching technique. The amount of material etched must be controlled by carefully timing the anodization, since dopant junctions do not necessarily provide an etch stop for electropolishing as they do for pore formation. The critical electropolishing current density increases linearly with HF concentration, so pore formation is favored by high current densities and low HF concentrations [38].

Lateral and vertical microaccelerometers can be fabricated using a n-epitaxial layer and buried n+ and p+ layers on a p-type substrate or simply directly on the p-type substrate. Because of the high doping levels of the buried regions, they become porous during anodic etching, while the lightly doped epitaxial silicon and substrate provide etch stops. The porous silicon is removed in KOH following

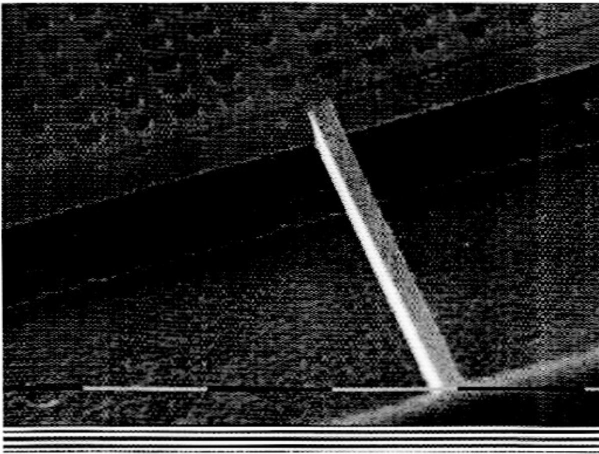


Figure 7. SEM photograph on an under-etched epitaxial layer.

anodization, leaving free-standing n-epitaxial structures. In the case of pore formation directly on the p-type substrate, selectivity over the n-epi is also achieved. Even in illuminated conditions the current passes from the p-type windows to the platinum electrode and thus the epitaxial layer is not etched. An SEM photograph of an under-etched epitaxial layer is shown in figure 7.

3.2. Fabrication techniques

Porous silicon formation follows the lines of current flow and therefore the masking can have a significant influence on the shape of the porous layer. Pore formation begins in the unmasked silicon regions, and the rate and time of the etch must be precisely controlled to obtain the necessary depth and lateral dimensions of porous material. Figure 8 shows four masking configurations [39]. In the first, figure 8(a), an insulating mask is used in conjunction with n-type material. The result is a thin layer of underetching directly under the mask due to an excess of holes in that region. For a p-type substrate, shown in figure 8(b), where holes are plentiful, deeper pore formation is found at the edge of the mask and therefore this is due to a higher current density in this region. Any film that will not be etched by the HF during anodization, including silicon nitride, amorphous silicon carbide (a semi-insulating material), photoresist and the noble metals, can be used as a masking layer [39]. Photoresist can be used alone to mask pore formation only if the HF solution is relatively weak (25% or less) and the anodization time required is less than approximately ten minutes [39]. Stronger solutions or longer etching times result in the photoresist being attacked by the HF. Regardless of the masking layer and anodization time, however, photoresist may be left on during anodic etching to provide an extra layer of masking protection against pore formation. For short anodization times, n-doped polycrystalline silicon over a thin layer of SiO_2 can also be used as the masking layer and constructional material, as it is made resistant to pore formation by the combination of a protective photoresist layer, insulation from the substrate, and the reverse biased HF-polysilicon junction [4,39]. Alternatively silicon nitride may be used as both a masking and a mechanical layer. When a conducting mask is used, as shown in figure 8(c), there is no such current concentration at the edge of the mask and therefore a simple underetching is found. A similar structure is found for a n-type diffusion mask is used as shown in figure 8(d). This technique, like the epitaxial silicon technique, has the advantage of the resulting structures being constructed of monocrystalline silicon. Here, however, it is the low doped areas that are made porous and subsequently dissolved, and the free-standing structures are limited in thickness to the depth of the implant [39].

Anodization is performed to make the sacrificial material porous. If selective doping has been used to pattern the porous silicon formation, the junctions act as highly effective etch stops [13]. Otherwise, the lack of a physical or chemical etch stop requires that the pore formation rate and time be precisely controlled in order to obtain a reproducible sacrificial layer thickness. To allow current flow during anodization through doped buried layers, openings must be etched through the epi to expose the buried layers to HF solution [11]. Anodization must take place for a long enough time so that free-standing structures are completely undercut by the lateral progression of pore formation, and the full desired thickness of the sacrificial layer is reached by the vertical progression of the etching. Complete undercutting of large deposited film structures, especially those whose underlying silicon is not heavily doped, is facilitated by etching small openings across the entire structure to act as access holes for the anodization current.

Normal processing, including film deposition, lithography and etching, can be performed on top of porous silicon as it would be on solid bulk silicon [4]. All processing must be performed before the porous silicon is removed, as the structures are too easily damaged without the support of the sacrificial layer. Any material used must be able to withstand the solution used for porous silicon removal.

Finally, the porous silicon is removed in a hydroxide solution or photoresist remover, leaving the materials on top of it free standing. Porous silicon removal is complete in a matter of a few minutes, but as the etching selectivity between porous and non-porous silicon is extremely high, leaving the sample in solution longer than necessary will not cause significant overetching [17, 39].

4. Applications in micromachining

4.1. Accelerometers

In lateral capacitive accelerometers that have been fabricated using porous silicon technology and an n-epitaxial silicon layer, capacitance is measured between free-standing epitaxial beams and fixed epitaxial fingers [11]. A lateral view of such an accelerometer is given in figure 9. The beams are patterned by dry etching through the epitaxial layer, and are freed from the substrate by forming and subsequently dissolving porous silicon in portions of the substrate. The capacitance is highly controllable since it is determined by lithography and

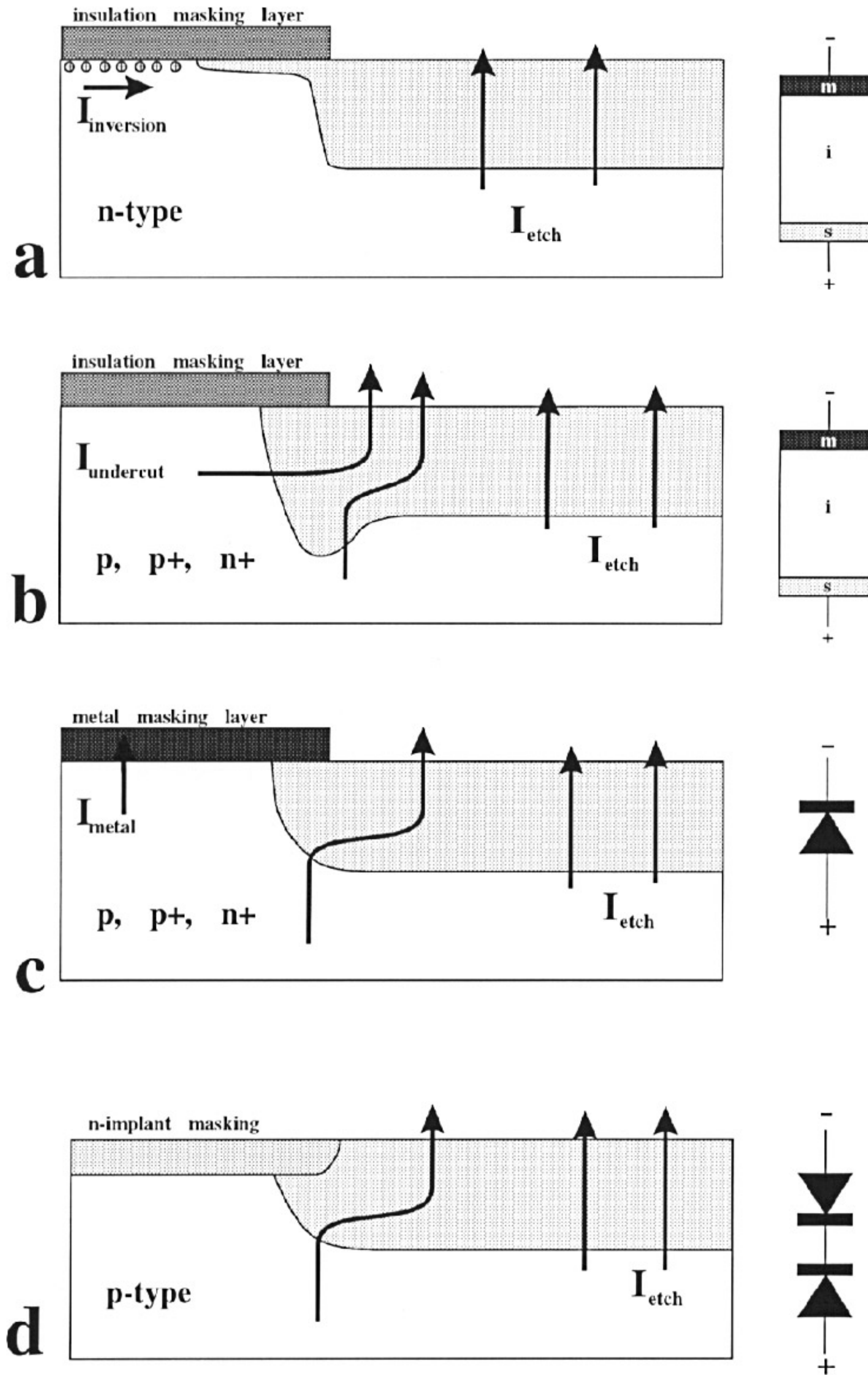


Figure 8. Four porous silicon formation patterns using a mask: (a) n-type material with an insulating mask, (b) p-type or heavily doped n-type material with an insulating mask, (c) a conducting mask and (d) patterned n- type doping in a p-type substrate (taken from [39]).

dry etching. In the time that it takes pore formation to completely undercut the beams, the vertical cross section of porous silicon formed is several microns thick. The resulting large separation between the beams and the substrate upon porous silicon removal helps to minimize parasitic capacitance in the devices. This large separation distance, as well as the roughness of the surface after porous silicon removal, also helps to reduce sticking between beams and the substrate.

Fabrication begins with the growth of a lightly doped n-epitaxial layer over a p-type substrate (figure 10(a)). Next, a layer of LPCVD nitride and a layer of PECVD oxide are deposited, and the oxide is patterned using a dry etch to serve as a mask for plasma etching the nitride and epi layers. Openings are etched through the epi down to the substrate in patterns defining the shape of

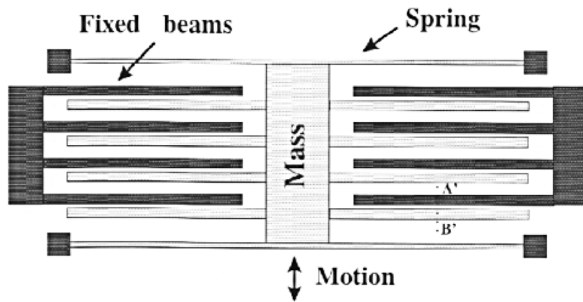


Figure 9. Planar view of a lateral accelerometer.

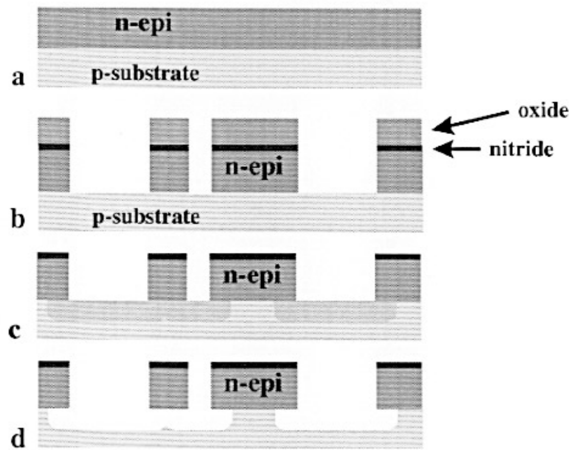


Figure 10. Processing sequence for fabricating the accelerometer shown in figure 9 (cross section A'B') (a) starting material n-type epi on a p-type substrate, (b) etching through the n-type epi to reveal the substrate, (c) formation of buried porous layer and (d) removal of porous layer to form the free-standing structure.

the accelerometer (figure 10(b)). The devices are then anodically etched, making the buried layers underneath the beams porous as shown in figure 10(c). Finally, the porous silicon is removed in KOH, releasing the beams from the substrate (figure 10(d)). An example of a lateral accelerometer fabricated using this process is given in figure 11. Vertical accelerometers may also be fabricated using this technology, with the substrate forming one plate of the capacitor and a free-standing epitaxial silicon mass supported by beams forming the other plate. This type of device, however, offers less controllability of the capacitance, since the plate separation distance cannot be controlled as well using porous silicon formation as it can be using dry etching.

This technique makes use of the epitaxial layer growth method used with porous silicon etching to fabricate free-standing structures. It provides the advantage of devices that are small in size, yet large in mass and capacitance because the capacitor plates are as thick as the full thickness of the epi layer. Both lateral and vertical accelerometers may be fabricated on the same wafer, and the devices have excellent mechanical and electrical properties due to their construction in monocrystalline silicon.

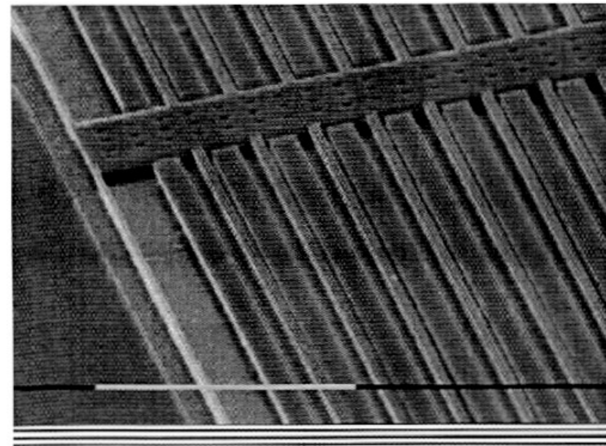


Figure 11. SEM photograph of a lateral accelerometer fabricated using the sacrificial porous technique (taken from [11]).

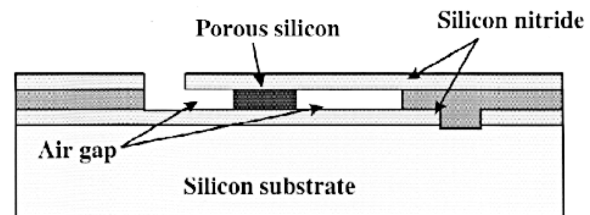


Figure 12. Sealed cavity structure fabricated by lateral porous formation of a polysilicon layer (taken from Anderson *et al* [40]).

4.2. Sealed cavity devices

One important difference in the sacrificial porous silicon technique compared to wet chemical etching is that the pores grow from the tips of the pores and therefore changes in the etch parameters will only effect the new porous regions and not those already formed. This feature has been used to form cavities by Anderson *et al* [40]. In this case the mechanical layer was silicon nitride and the sacrificial layer polysilicon. The resulting structure is shown in figure 12. This structure was fabricated in three-steps. The first step, using 5% HF and a 5 V dynamic hydrogen electrode (DHE), removed the first part of the cavity. This was followed by a high HF concentration step (49% HF) at 0 V DHE, which formed the porous plug. Finally 10% HF at 5 V DHE was used to form the inner cavity.

4.3. Channel devices

Polysilicon bridges constructed using porous silicon as a sacrificial layer have been fabricated for various sensor applications. Porous silicon formation and removal releases the bridges, forming flow channels beneath them (figure 13). Bridges constructed of thin films have small cross sections that allow small time constants and very high speed sensing. This type of structure can be used in fabricating devices such as flow sensors, vacuum sensors, hot-wire anemometers and gas sensors [36,37].

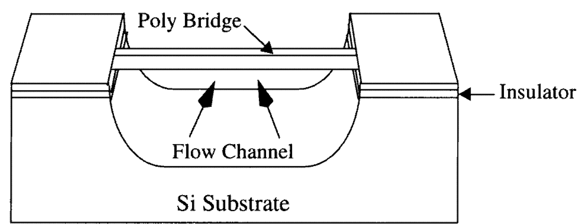


Figure 13. An example of a polysilicon bridge that could be used as a flow or other type of sensor. The flow channel beneath the bridge is formed by making part of the substrate porous, then removing the porous material in a hydroxide solution (taken from [39]).

A thin-film bolometer, consisting of a thin metal resistor on top of a silicon carbide membrane, has also been fabricated using porous silicon as the sacrificial material [36]. The large separation between the membrane and the substrate that is possible using this technique allows for high device sensitivity and thermal isolation. The larger the separation distance, the higher the thermal resistivity between the membrane and the substrate, resulting in reduced parasitic heat transfer and increased thermal sensitivity [36,37].

4.4. Deep hole etching

A further application for porous silicon is the formation of deep vertical holes in AN n-type silicon wafer [42]. This process uses a seed formed in the surface. A small square etched in KOH, for example, will give a starting point for the pore formation. Vertical holes through the whole wafer have been achieved using this method.

5. Conclusions

Porous silicon has many potential applications in micromachining technologies as a sacrificial material. It makes possible the formation of free-standing structures constructed of monocrystalline silicon, and offers several important advantages over bulk and surface micromachining. It is CMOS compatible, planar and easily fabricated. Both thick and thin sacrificial layers may be formed, permitting separations ranging from a few microns to over one hundred microns between free-standing structures and the substrate. The high selectivity of porous silicon formation between differently doped types of silicon makes selective sacrificial etching possible through patterned doping. Fabrication of lateral and vertical accelerometers, as well as several other types of microsensors using porous silicon as a sacrificial layer, has demonstrated the benefits of this material for use in micromachining.

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