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Positive charge trapping phenomenon in n-channel thin-film transistors with amorphous alumina gate insulators

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In this work, we investigate the charge trapping behavior in $InGaZnO_4$ (IGZO) thin-film transistors with amorphous Al_2O_3 (alumina) gate insulators. For thicknesses ≤ 10 nm, we observe a positive charge generation at intrinsic defects inside the Al_2O_3, which is initiated by quantum-mechanical tunneling of electrons from the semiconductor through the Al_2O_3 layer. Consequently, the drain current shows a counter-clockwise hysteresis. Furthermore, the de-trapping through resonant tunneling causes a drastic subthreshold swing reduction. We report a minimum value of 19 mV/dec at room temperature, which is far below the fundamental limit of standard field-effect transistors. Additionally, we study the thickness dependence for Al_2O_3 layers with thicknesses of 5, 10, and 20 nm. The comparison of two different gate metals shows an enhanced tunneling current and an enhanced positive charge generation for Cu compared to Cr. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4972475]

I. INTRODUCTION

In the last 60 years, silicon metal-oxide-semiconductor (MOS) field-effect transistors (FETs) have been employed as the main workhorse of the electronics industry. Traditionally, gate insulator/semiconductor interface traps and bulk insulator charges in MOSFETs have mainly played a role while testing the device reliability under high-electric field stress. In this context, the subthreshold swing (SS) increase as well as the threshold voltage (V_{Th}) shift have been used as tools to investigate the charge trapping mechanisms.[1,2]

Charge trapping has been utilized for information storage in the field of floating gate memory technology[3] (i.e., flash[4]). In such devices, the charge is stored on a floating metal layer by tunneling of channel carriers through a thin SiO_2 barrier at high electric fields. Ideally, all charge carriers are transferred back and forth between the semiconductor and the floating gate. However, defect generation and charge trapping in the thin SiO_2 tunnel layer have been observed, which caused reliability issues.[5] Thus, the physics of charge generation in SiO_2 has been intensively investigated.[6–8]

In 2007, high-k dielectrics have entered the silicon electronics industry with the aim to reduce the power dissipation in MOSFETs.[9] In the meantime, they have gained popularity for high mobility semiconductors such as Ge and III–V,[10] oxide semiconductors,[11] and organic semiconductors.[12] Nevertheless, their larger ionic bonding character compared to SiO_2 results in an increased number of interface and intrinsic defects, especially oxygen vacancies (V_O),[13] which are highly susceptible to charge trapping.[14] Particularly in flexible electronics, defects in high-k dielectrics have to be carefully considered due to the low temperature process requirement of most substrates,[15] which can result in larger intrinsic defect concentrations.

In this work, we investigate the charge trapping effects in flexible $InGaZnO_4$ (IGZO[16]) top-gate thin-film transistors (TFTs) based on thin Al_2O_3 (alumina) gate insulator layers deposited by low temperature atomic-layer deposition (ALD). For 20 nm thick Al_2O_3, we observe a typical interface charge trapping behavior[17–21] with a clock-wise hysteresis of the drain current I_D and a SS degradation. When the Al_2O_3 thickness is scaled down to 5 nm, channel carriers can tunnel into the gate electrode leading to a positive charge generation inside the gate insulator and counter-clockwise hysteresis of I_D. Moreover, the de-trapping of these charges reduces the SS below the conventional FET limit of 60 mV/dec at room temperature.[21,22] Since the trapping/de-trapping is reversible upon cycling, we assume that the intrinsic defect states in the low-temperature, amorphous Al_2O_3 are responsible for the observed behavior. We find that charge trapping and de-trapping is increased for devices with Cu gate metals compared to Cr gate metals, which we attribute to the larger work function of the former.

II. EXPERIMENTAL DETAILS

A. Fabrication

The TFTs were fabricated on a flexible free-standing 50 μm thick polyimide foil. The device schematic and the process flow are depicted in Fig. 1(a). The inset on the top right shows an optical micrograph of a TFT and the inset on the bottom right shows a photograph of a fully processed substrate. The fabrication process was performed as follows: First, the substrates were cleaned in acetone and 2-propanol by sonication in an ultrasonic bath for 5 min. Afterwards the substrate was annealed in an air oven at 200 °C for 24 h. Before the definition of the active layers, a 50 nm thick SiN_X passivation layer was deposited on both sides of the substrate by plasma-enhanced chemical vapor deposition at 150 °C.

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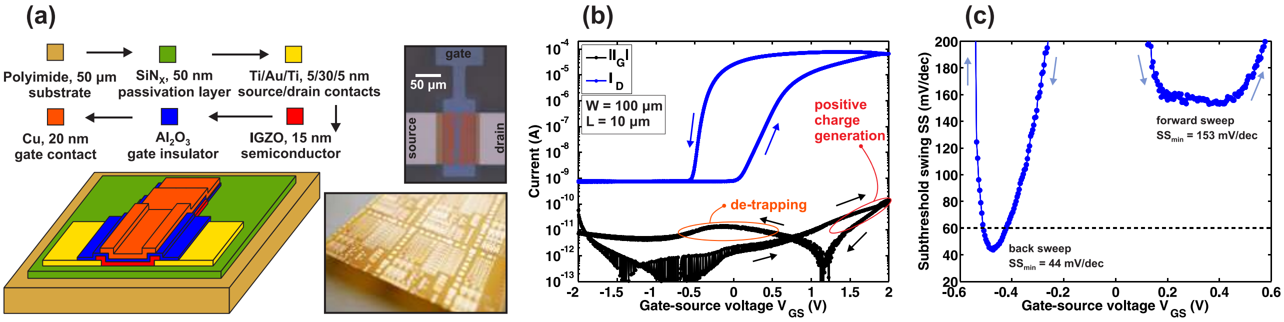

FIG. 1. Characteristics of a Cu/Al_2O_3/$InGaZnO_4$ thin-film transistor with an Al_2O_3 thickness of 5 nm. (a) Device schematic and fabrication flow. The top-right inset shows a microscope image and on the bottom-right a photograph of the fully processed flexible thin-film transistors is displayed. (b) Transfer characteristic with drain current I_D and absolute gate current $|I_G|$. The drain-source voltage is constant at 100 mV. (c) Subthreshold swing SS of the characteristic shown in (b).

The first functional layer was Ti/Au/Ti (5/30/5 nm) which served as source/drain contacts. It was electron-beam evaporated and structured by optical lithography and lift-off. Then, a UV-ozone cleaning for 1 min was performed in order to remove any organic residues. The 15 nm thick semiconductor was RF magnetron sputtered at room temperature from an $InGaZnO_4$ target and structured by optical lithography and wet chemical etching. The Al_2O_3 gate insulators with different thicknesses were deposited by thermal atomic-layer deposition at 150 °C. Contact holes were defined by optical lithography and wet chemically etched. Finally, a 20 nm thick Cu or Cr layer was electron-beam evaporated (substrate rotating at an angle of 30°). The layer was structured thereafter by optical lithography and wet chemical etching to define the top gate contacts.

B. Electrical characterization

All electrical measurements were performed on a probe station at ambient conditions with a semiconductor device analyzer (Agilent technologies, B1500A). The TFT transfer characteristics were acquired in the linear transistor operation regime at a drain-source voltage $V_{DS} = 100$ mV. For the display and calculation of the SS, the moving average with a series of $n = 5$ data points was applied. To reliably measure the gate bias stress (Section III B), the maximum gate-source electric field E_{GS} for pre-bias stress transfer characteristics was set to 1 MV/cm. This resulted in an initial I_D hysteresis below 100 mV. Each gate bias stress test was performed on virgin devices. The gate bias stress was applied for 10 s at a constant V_{DS} of 100 mV.

III. RESULTS AND DISCUSSION

In the beginning of this section, the positive charge generation and subsequent de-trapping in the Cu gate TFTs with a 5 nm thick Al_2O_3 is displayed and explained. Afterwards, the charge trapping behavior in Cu gate TFTs with different Al_2O_3 thicknesses is investigated. Subsequently, the Cu and Cr gate metals for 5 nm thick Al_2O_3 thick TFTs are compared. Finally, the device stability of Cu gate TFTs with 5 nm thick Al_2O_3 is analyzed.

A. Thin-film transistors with 5 nm thick alumina gate insulators and Cu gate electrodes

The transfer characteristic of Cu gate TFTs with 5 nm thick Al_2O_3 gate insulators is displayed in Fig. 1(b). The I_D shows a counter-clockwise hysteresis which indicates the trapping of positive charges at positive gate-source voltages V_{GS}. The tunneling of electrons through the Al_2O_3 gate insulator at positive V_{GS} is visible in the gate current I_G. Similar positive charge generation close to the anode in the presence of electron tunneling has previously been reported in MOS structures.[7,8] During the V_{GS} back sweep, the positive charges are neutralized by electrons from the gate. The occurrence of a broad I_G peak in the range of $V_{GS} = \pm 0.5$ V indicates that the de-trapping happens through resonant tunneling.[23–26] The charge generation mainly occurs when the semiconductor is in accumulation, whereas the de-trapping happens simultaneously with the TFT switching transition. This effect is visualized by the SS with a minimum value of 153 mV/dec in the V_{GS} forward sweep, which then reduces to a minimum value of 44 mV/dec in the V_{GS} back sweep because of simultaneous de-trapping. Thus, the back sweep SS overcomes the fundamental limit of standard FETs at room temperature.[21,22] Here, the SS acts as a measure for the de-trapping behavior. The SS decrease indicates an electron movement into the gate insulator during the V_{GS} back sweep. This movement is opposite to the commonly reported SS increase from charge trapping where the electrons are trapped in the V_{GS} forward sweep and released in the V_{GS} back sweep.[18,19]

To identify the main contributors for the defect formation, the device morphology, alumina composition, and defect energy distribution are examined. The device stack is studied by scanning-electron microscopy (SEM) and the composition of the Al_2O_3 gate insulator is analyzed by Rutherford backscattering spectrometry (RBS) and helium elastic recoil detection (He-ERD). The defect energy distribution and the Al_2O_3 bandgap are analyzed by optical absorption measurements.

The device cross-section is displayed in Fig. 2(a). The gate/source overlap and TFT channel area are indicated, and the layers exhibit a homogeneous coverage of the device topography. Fig. 2(b) summarizes the results of RBS and He-ERD. The O/Al ratio of 1.52 confirms the desired stoichiometry of Al_2O_3. About 7% of hydrogen (H/O ratio) has

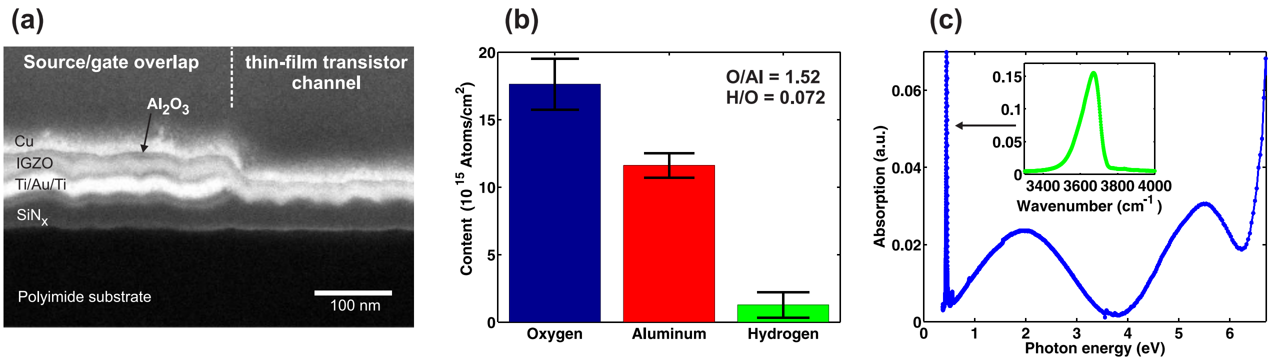

FIG. 2. Structural and elemental analysis (a) Cross-section scanning-electron micrograph of a Cu/Al_2O_3/$InGaZnO_4$ thin-film transistor with an Al_2O_3 thickness of 5 nm. (b) Elemental analysis of the 5 nm thick Al_2O_3 layer. Rutherford backscattering spectrometry (RBS) is used for aluminum and oxygen, and helium elastic recoil detection (He-ERD) is used for hydrogen. (c) Optical absorption spectrum of a 100 nm thick Al_2O_3 layer.

been detected within the film, which agrees with the previous reports on Al_2O_3 thin films deposited by the atomic-layer deposition at 150 °C.[27] A large defect density inside the Al_2O_3 thin-film can be deduced from the significant H-concentration. Fig. 2(c) displays the optical absorption spectrum of a 100 nm thick Al_2O_3 layer deposited on a quartz substrate. The substrate influence has been eliminated by measuring beforehand an uncoated quartz reference. The overall absorption magnitude is low which is expected for a wide-bandgap insulator material. The large peak at 0.45 eV is magnified in the inset, where the corresponding wavenumbers are displayed. The peak can be related to Al-OH stretching vibrations.[28] From the rise in absorption at $\geq$6.4 eV, we estimated the bandgap of Al_2O_3 to be 6.4–6.5 eV assuming a direct transition.[29,30] Additionally, two broad defect-related peaks at 5.5 eV and 1.9 eV can be discerned. Both could be related to electron capturing and electron release of negatively charged V_O, respectively. These absorption energies agree with simulated transition levels of V_O in amorphous alumina.[31]

B. Characteristics of alumina gate insulators with thicknesses from 5 nm to 20 nm

In the following, the influence of the alumina gate insulator thickness for TFTs with Cu gate electrodes is evaluated. For that, the tunneling currents (I_G) through Al_2O_3 are compared, and the possible charge carrier transport mechanisms are discussed.

In recent literature, various tunneling mechanisms for Al_2O_3 thin-films have been considered. Among those are, e.g., space-charge controlled field-emission,[32,33] Poole-Frenkel conduction[34,35] and multi-phonon trap ionization.[36] First, the forward conduction mechanism (Fig. 3) is analyzed. In Fig. 3(a), the forward tunneling currents for different Al_2O_3 thicknesses are compared. The differences between the tunneling currents after normalization on the electric field lead to the conclusion that classic band-to-band tunneling like Fowler-Nordheim tunneling cannot be the dominant conduction process.[37]

The space-charge controlled field-emission model has been studied for different Al_2O_3 thicknesses[32] and different ALD temperatures.[33] It has been found that the model significantly underestimates the current transport at low electric fields for layers <7 nm and thin-films deposited at an ALD temperature $\leq$150 °C. Thus, we exclude the space-charge controlled field-emission from our considerations. Consequently, the enhanced tunneling currents at low $E_{GS} < 3$ MV/cm indicate a trap-assisted tunneling mechanism through the Al_2O_3 insulators with thicknesses $\leq$10 nm.[32–34,38] The temperature dependence (from 25 to 46 °C) of the forward tunneling current for 5 nm thick Al_2O_3 is displayed in the Arrhenius plot in the inset of Fig. 3(a). In Fig. 3(b), the forward tunneling current is shown in a Poole-Frenkel plot. The mismatch for different Al_2O_3 thicknesses clearly shows that Poole-Frenkel emission, although it accounts for temperature dependence,

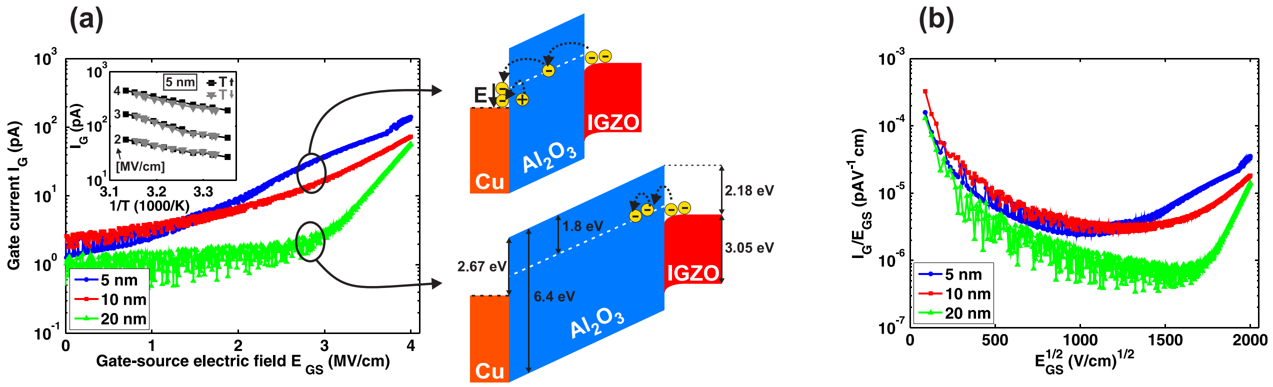

FIG. 3. Forward gate current I_G of Cu gate thin-film transistors with different Al_2O_3 gate insulator thicknesses. (a) Log-scale forward sweep I_G. The inset shows the temperature dependence of the forward I_G for 5 nm thick Al_2O_3. The band diagrams[31,36,41–43] on the right schematically show the generation of positive charges at defects for 5 and 10 nm, and the electron trapping in defect states for 20 nm. (b) Poole-Frenkel plot.

cannot be the governing mechanism in the E_{GS} -range of interest. Consequently, the strong temperature dependence as well as the increased low-E_{GS} current for thinner layers let us conclude that, although the other tunnel mechanisms may contribute, multi-phonon trap ionization[36,39,40] is the dominant current transport process in Al_2O_3 layers with thicknesses $\leq$10 nm.

The band diagram for the studied material system is constructed based on Cu,[41] Al_2O_3,[36,42] and IGZO[43] from literature (see Fig. 3(a) on the right). The obtained band offset values are indicated in the sketch on the bottom-right. The displayed defect level (dashed line) shows the neutral-to-negative (0/−) V_O transition.[31] The band diagram on the top-right depicts the energy release of electrons upon entrance into the Cu gate metal[44,45] and positive charge generation. Traditionally, the positive charge generation has been attributed to impact ionization.[7,8] This effect is caused by tunnel electrons and previously an energy release of $\geq$2 eV has been found to be sufficient to release electrons from intrinsic trap states located inside the band gap of insulating materials.[46] Due to the broad defect energy distribution in amorphous alumina,[47] even smaller energies may excite bound electrons from deep defect levels and thus promote their release into the gate electrode. A second possible cause of the positive charge generation may be local heating[45] which then could allow for further multi-phonon ionization processes[48] to take place at the Cu/Al_2O_3 interface.

The tunneling current for $Al_2O_3 = 20$ nm is negligible up to 3 MV/cm, which indicates that the trap-assisted tunnel current is strongly suppressed when scaling up the insulator thickness. Due to the existence of trap states throughout the insulator, electron trapping is expected for traps, which are in tunnel distance to the IGZO semiconductor. For 20 nm thick Al_2O_3, these trapped electrons cannot be injected into the gate electrode due to their relatively large distance, and hence they are temporarily stored on defect levels in the gate insulator (Fig. 3(a), sketch on the bottom-right). This results in an effective negative charge density close to the semiconductor/insulator interface, which is typically observed in IGZO TFTs.[49,50]

Fig. 4 indicates the back sweep I_G peaks, which occur for Al_2O_3 thicknesses $\leq$10 nm. This observation leads to the conclusion that the forward tunneling current activates the charge trapping, and thus the positive charges are generated when scaling down the Al_2O_3 thickness $\leq$10 nm. Instead, when the trap-assisted forward tunneling current is suppressed ($Al_2O_3 = 20$ nm), there is no negative I_G peak visible. The peaks indicate resonant tunneling into the positively charged trap states[23–26] (see sketch on the right of Fig. 4). The temperature dependent measurements (see inset, top-right) show that at $\geq$42 °C, a second defect level can be ionized. We identified dangling bonds of aluminum atoms as well as the positively charged V_O as possible defect types responsible for the positive charge and resonant tunneling peaks.[31,51]

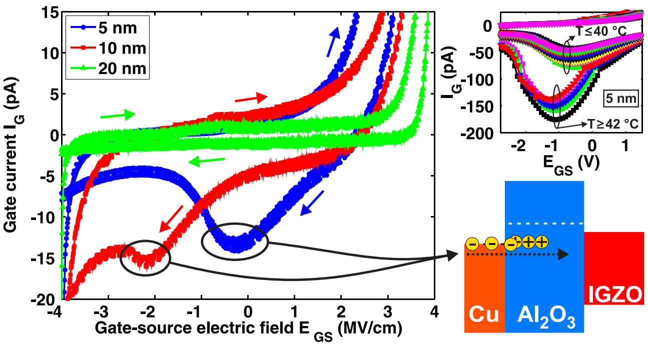

FIG. 4. Linear-scale gate current I_G: the back sweep I_G shows negative peaks for 5 nm and 10 nm thick Al_2O_3. The inset (top-right) shows the temperature dependence of the back sweep I_G peaks for 5 nm thick Al_2O_3. The band diagram[31,36,41–43] (bottom-right) schematically shows resonant tunneling of electrons from the gate electrode into positively charged defect states.

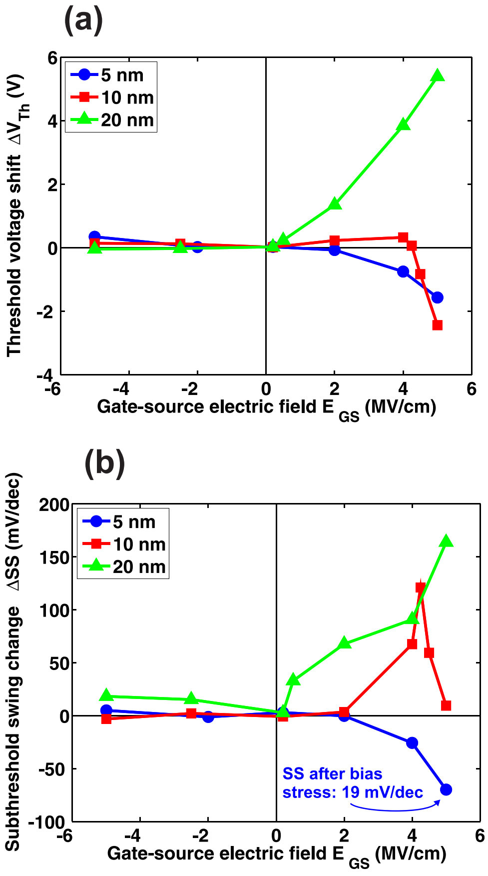

FIG. 5. Changes of Cu gate thin-film transistor parameters after gate bias stress measurements for different Al_2O_3 gate insulator thicknesses. (a) Threshold voltage shift ΔV_{Th}. (b) Subthreshold swing change ΔSS.

The TFTs with different Al_2O_3 thicknesses have been tested in gate bias stress measurements. The resulting threshold voltage shift ΔV_{Th} and subthreshold swing change ΔSS are displayed in Figs. 5(a) and 5(b), respectively. While TFTs with a 20 nm thick Al_2O_3 show negative charge trapping accompanied by a SS increase, the TFTs with a 5 nm thick Al_2O_3 exclusively show positive charge trapping and a SS decrease. For 10 nm thick Al_2O_3, there is a transition between the two mechanisms at $E_{GS} = 4$ MV/cm. For 5 nm thick Al_2O_3, the strongest gate bias stress condition of 5 MV/cm results in a ΔSS of 70 mV/dec leading to a minimum SS of 19 mV/dec for the measurement after bias stress.

C. Comparison of Cu and Cr gate electrodes for TFTs with 5 nm thick alumina gate insulators

In Fig. 6(a), the minimum SS for Cr and Cu gate metals is displayed. For both gate electrodes, the SS decreases with

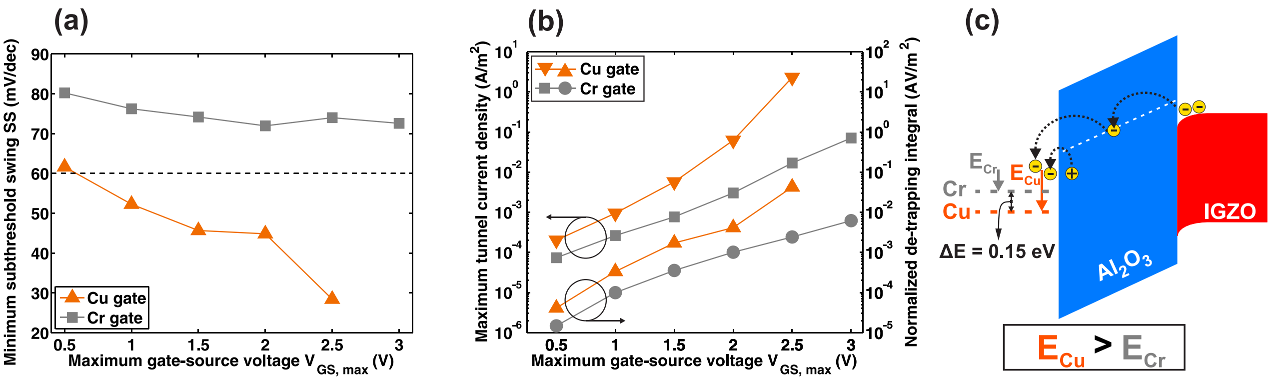

FIG. 6. Comparison of Cu and Cr gate electrodes in thin-film transistors (TFTs) with 5 nm thick Al_2O_3. (a) Minimum subthreshold swing for different maximum gate-source voltages $V_{GS,\ max}$. (b) Maximum forward tunnel current density and normalized de-trapping integral for the negative gate current peaks. (c) Band diagram[31,36,41–43] schematically indicating the difference of the two gate materials at the same voltage drop across the insulator. The energy release of tunnel electrons is larger for a Cu gate electrode compared to Cr.

an increasing maximum gate-source voltage $V_{GS,\ max}$ which is related to a larger charge generation at higher E_{GS}. However, the change is more significant for Cu gates. As shown previously, the forward I_G is strongly related to the positive charge generation (see Sec. III B). Here, the integral of the negative back sweep I_G over V_{GS} is taken as a relative measure for the amount of de-trapped positive charge. In Fig. 6(b), the forward tunneling current density and the normalized de-trapping integral for the Cr and Cu gate electrodes are compared. From both quantities, it can be deduced that the positive charge generation is strongly enhanced for Cu gate metals compared to Cr. The results can be related to the work functions of both materials. The Cu work function is ∼4.65 eV, and the Cr work function is ∼4.5 eV.[41] Hence, the energy released by tunnel electrons and the probability to charge a defect is higher for Cu compared to Cr. This effect is schematically depicted in Fig. 6(c). Nevertheless, it has to be noted that an additional chemical interaction between the electrode material and Al_2O_3 cannot be excluded.

D. Device stability

The device stability for TFTs with a 5 nm thick Al_2O_3 gate insulator and Cu gate electrode has been investigated. In Fig. 7(a), the I_G for different $V_{GS,\ max}$ is shown. At $V_{GS,\ max} = \pm 2.5$ V, the positive I_G hysteresis is reversed compared to smaller $V_{GS,\ max}$ (see arrows at positive V_{GS}). A clockwise positive I_G hysteresis indicates an overall capacitive device behavior whereas a counter-clockwise positive I_G hysteresis followed by an I_G crossing has been found in resistive switching applications where the defects form a conductive filament through the insulator.[52–54] Interestingly, the center of the trap charge distribution (negative peak of I_G) shifts to negative V_{GS} when $V_{GS,\ max}$ is increased, which could be due to a greater depth of charges inside the gate insulator or a change in the dominant energy level of the charged trap states. In Fig. 7(b), the convergence of the back sweep SS during 100 V_{GS} sweeps is displayed. There are minor instabilities at $V_{GS,\ max} = \pm 2.5$ V, however, the devices recover during cycling with the majority of minimum SS values around 27 mV/dec. The stability upon cycling gives another indication that the material is not degraded by defect generation and in contrast the defect charging is performed on previously described intrinsic defect states.[55,56]

IV. CONCLUSIONS

We reported a tunneling activated charge trapping phenomenon which significantly alters the device behavior of our IGZO TFTs. The main difference from usual charge trapping observations is the polarity of the trap charge inside the gate insulator. Usually, channel carriers are trapped. However, in this case, the tunneling of channel

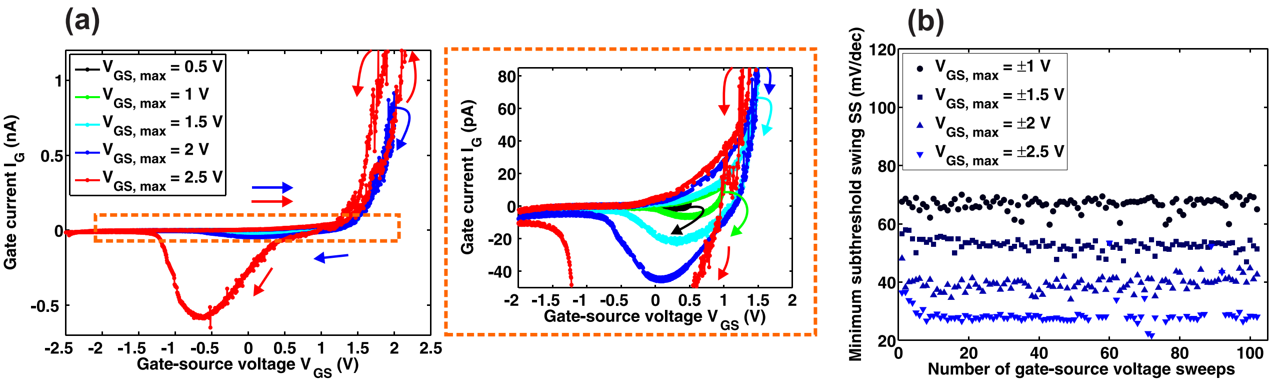

FIG. 7. Thin-film transistor device stability. (a) Gate current I_G as a function of the maximum gate-source voltage $V_{GS,\ max}$. The arrows indicate the I_G hysteresis direction. The magnified area shows the negative I_G peaks at $V_{GS,\ max} \leq 2$ V (b) Minimum subthreshold swing of the V_{GS} back sweep for 100 cycles at different $V_{GS,\ max}$.

carriers activates the charge trapping of the opposite sign. This mechanism leads to two main observations: (1) a change in the I_D hysteresis direction and (2) a reduction of the SS of the I_D back sweep even below the fundamental limit of 60 mV/dec. We find that the charge generation is mainly activated at a V_{GS} above the transistor switching transition. Thus, the effect on the SS in forward sweep direction is small. In contrast, the de-trapping by resonant tunneling into localized defect states on deep energy levels significantly impacts the SS with a remarkable reduction down to minimum values of 19 mV/dec at room temperature. This leads to the conclusion that resonant tunneling may be a mechanism, which could be exploited in alternative device technologies targeting the reduction of operating voltage for low power consumption. On the other hand, the observed hysteresis characteristic could be investigated for low-power memory applications. That our device may be suitable for such application is supported by the fact that the charge trapping/de-trapping is stable upon cycling and does not cause a permanent breakdown from oxide degradation. Furthermore, the device fabrication process flow is compatible with the standard technology and requires less layers than flash technology where another floating gate has to be implemented within the gate stack.

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