Positive-Feedback-Based Active Anti-Islanding Schemes for Inverter-Based Distributed Generators: Basic Principle, Design Guideline and Performance Analysis

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***Abstract*—The positive-feedback-based anti-islanding schemes invented by the authors are highly effective in preventing islanding without causing any degradation in power quality. This paper presents the basic principles of these schemes and their design guidelines. Moreover, their performance is investigated for inverter-based distributed generators (DGs). The parametric study reveals the factors significantly influencing the performance of these schemes. The simulation results demonstrate the effectiveness of these schemes.**

***Index Terms*—Basic principles, design guidelines, inverter-based distributed generators (DGs), performance analysis, positive-feedback anti-islanding (AI).**

NOMENCLATURE

d_d, d_q	Direct-axis and quadrature-axis duty ratio of pulsewidth modulation (PWM).
$G_d(s)/G_q(s)$	Voltage/frequency open-loop gain without voltage/frequency anti-islanding (AI) compensator.
$H_d(s)/H_q(s)$	Transfer function of voltage/frequency AI compensator.
i_{abc}	Three-phase currents of distributed generator (DG).
i_d, i_q	Direct-axis and quadrature-axis current of DG.
i_{d_ai}, i_{q_ai}	Small direct-axis and quadrature-axis variations used to disturb current references.
$i_{d\mathrm{grid}}$, $i_{q\mathrm{grid}}$	Direct-axis and quadrature-axis grid current.
$i_{d\mathrm{ref}}$, $i_{q\mathrm{ref}}$	Direct-axis and quadrature-axis reference current of DG.
K, T_w, and T_1	Gain, corner-time constant, and time constant of the AI compensator, respectively.
K_p, K_i	Gain and time constant of current regulator.
K_{pll}, T_{pll}	Gain and time constant of phase-lock loop (PLL).
L_f	Filter inductance of DG.
P_e	Active power output of DG.
Q_f	Quality factor of the *RLC* load (evaluated at the line frequency 60 Hz).
R, L, and C	Load resistance, inductance, and capacitance, , respectively.
R_e, L_e	Grid resistance and inductance.
$T_d(s)/T_q(s)$	Voltage/frequency open-loop gain with voltage/frequency AI compensator.
u_{abc}	Three-phase voltages of DG.
u_d, u_q	Direct-axis and quadrature-axis voltage of DG.
u_d^∞, u_q^∞	Direct-axis and quadrature-axis voltage of infinite bus.
V_g	DC voltage of DG.
V^∞	Voltage magnitude of infinite bus.
α	Phase angle of infinite bus.
ω^*	Frequency output of PLL.
θ^*	Phase-angle output of PLL.

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I. INTRODUCTION

THE PHENOMENON of islanding in the presence of DGs requires considerable attention because of its potential to result in an unsafe operating condition of the system. Almost all utilities require that, in case of an island formation in the presence of DG, generators should disconnect themselves from the grid as soon as possible. IEEE Standard 1547 has stipulated a maximum delay of 2 s for the detection of an island, and established the need for proper coordination of any autoreclosing scheme with the AI protection [1]. While the past decade saw the introduction of many new concepts, several outstanding issues remain, especially with regard to reliable and economical AI for inverter-based DGs.

Depending on whether there is interaction with power systems or not, the schemes proposed to detect an island sustained

by inverter-based DGs can be basically divided into two categories: passive and active [2]–[4], [10]–[13], [16]. A good summary of island-detection techniques can be found in [16]. The main drawback to the passive schemes is that they cannot effectively differentiate between the loss of the grid and other nonislanding transients. The most basic and universal means of detecting islanding passively is to establish an under/over frequency and under/over voltage window within which a DG can operate. When a DG is islanded from the utility system because of a fault or other abnormal condition, the frequency or voltage will quickly move outside the operating window, if there is a significant difference between loads and the local generation level. However, there is a possibility that the system voltage and frequency can be maintained within the specified limits following loss of the grid in cases where the load and generator are closely matched. Therefore, special means are required to detect the loss of the grid.

The most widely used active methods include active frequency drift (AFD) and slide-mode frequency shift (SMS). The basic idea behind the AFD method is to introduce a small increase or decrease in the current frequency of the inverter. Any deviation in the voltage frequency, measured at the terminal, indicates the occurrence of an islanding event. However, the AFD method fails when the load phase angle matches the phase offset, which is generated by perturbing the frequency. The SMS method applies a similar strategy as AFD. In this method, the starting angle of the inverter current is altered so that any isolation of DG would lead to a measurable frequency deviation in the island. However, this method is ineffective when the load phase angle is equal to the starting angle.

Active schemes are more effective and robust than the passive ones, but most existing active schemes have the disadvantages of high cost and the degradation of power quality [13], [16]. Recently, schemes based on a positive-feedback concept have been proposed by the authors to detect islanding [5], [14], [15]. The basic mechanism is to disturb a smooth transition at the moment of islanding so that large transients in the voltage/frequency can be generated to trigger the voltage/frequency relay. This is achieved by a positive-feedback loop, which is referred to as active AI compensation. This idea has inspired other researchers to study the performance of these schemes for multiple inverter-based DGs [18], [19]. This paper is built on the earlier studies [5], [14], and [15], and aims to outline the basic principles of these schemes, present the design guidelines, and investigate their characteristics.This paper is organized as follows. Dynamic models of inter-based DG are presented in Section III. The basic principles and the design guidelines of these schemes are discussed in Sections IV and V, respectively. The performances of these schemes for a single inverter-based DG and multiple inverter-based DGs are evaluated in Sections VI and VII. The summary is given in Section VIII.

II. Dynamic Models of Inverter-Based DG

A simple block diagram of a typical inverter-based DG is shown in Fig. 1. The main components of the DG include a three-phase inverter, a current regulator and an active AI compensator

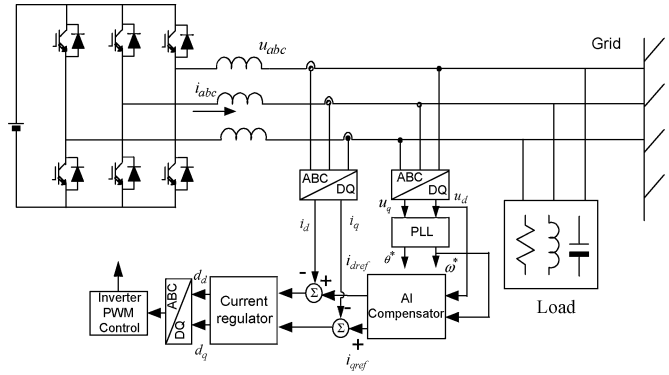

Fig. 1. Switch model of an inverter-based DG.

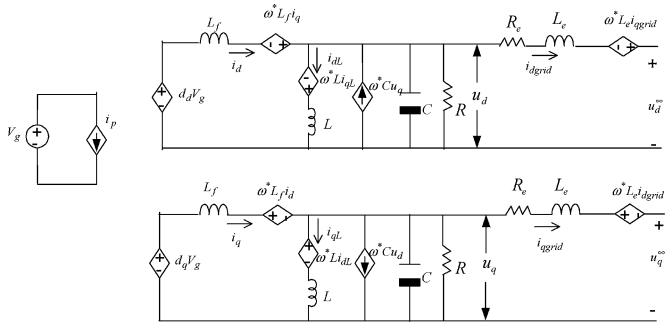

Fig. 2. Averaged large-signal model of an inverter-based DG in DQ coordinates.

(if in use). The DG has been connected to a utility through a three-phase inverter, which is commonly based on a voltage source inverter and operated to achieve objectives such as power flow regulation or power factor optimization by regulating the currents into the grid. To simplify the discussion, the energy source in the DG is represented by a constant voltage source to decouple the dynamics between the primary energy source and power system.

By assuming that the output currents i_{abc} and the voltages u_{abc} are continuous (and with negligible ripple), the averaged large-signal model of an inverter-based DG in stationary coordinates (see Fig. 1) was obtained after a moving average operator has been applied to each switching branch in the three-phase inverter. Furthermore, this model can be transformed into the DQ coordinates, as shown in Fig. 2 [6]–[9]. The O channel equivalent circuit has been omitted, since three-phase balance is assumed[1] Fig. 3 shows the current regulator of the DG implemented in the DQ representation. A three-phase PLL has been used to extract the frequency and phasor information from the three-phase terminal voltages. A detailed discussion on the operation of PLL can be found in [10]. The sensed three-phase currents have been transformed into the DQ coordinates as i_d and i_q and compared with the references $i_{d\mathrm{ref}}$ and $i_{q\mathrm{ref}}$. The error signals of the current then drive a proportional-integer compensator to produce the switch patterns for the PWM, d_d and d_q.

[1]When the three-phase system is not balanced, the O-channel equivalent circuit should be included. Analysis needs to be performed carefully to ensure the robustness of the proposed schemed under unbalanced situations.

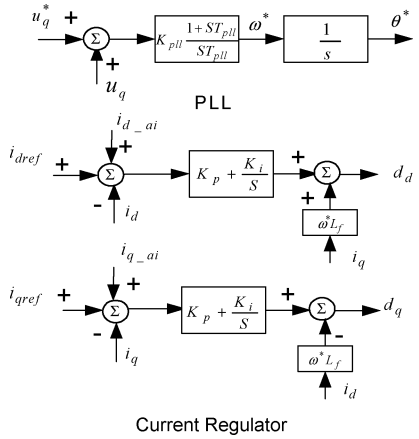

Fig. 3. Current regulator of an inverter-based DG in DQ coordinates without the AI compensators.

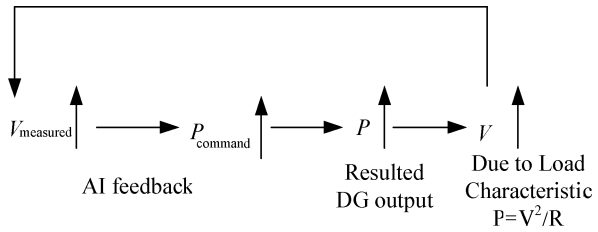

Fig. 4. Illustration of voltage (magnitude) positive feedback.

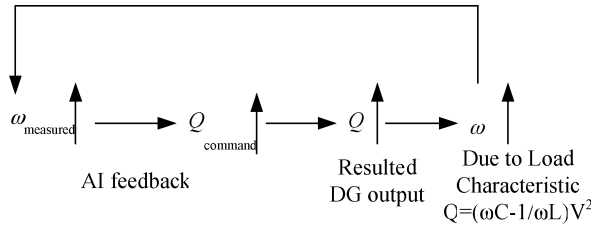

Fig. 5. Illustration of frequency positive feedback.

The disturbances i_{d_ai} and i_{q_ai}, which are generated from the active AI compensators, are the small variations used to disturb the current references $i_{d\mathrm{ref}}$ and $i_{q\mathrm{ref}}$, respectively. Therefore, the combination of the equivalent circuit (see Fig. 2) and the current regulator (see Fig. 3) constitutes a complete dynamic model of an inverter-based DG.

If the representation of the DG unit is modeled in the DQ frame, its steady states prior to the disturbance are dc quantities. After linearization has been applied to the dynamic model of the DG around these steady states, the small-signal model of the inverter-based DG was obtained. For the purpose of discussion, the voltage open-loop gain without the compensator $G_d(s)$ is defined as the transfer function from $\hat{i}_{d\_ai}$ to $\hat{u}_d$

$$G_d(s) = \frac{\hat{u}_d}{\hat{i}_{d\_ai}} \tag{1}$$

and the frequency open-loop gain without the compensator $G_q(s)$ is defined as the transfer function from $\hat{i}_{q\_ai}$ to $\hat{\omega}^*$

$$G_q(s) = \frac{\hat{\omega}^*}{\hat{i}_{q\_ai}} \tag{2}$$

where $\wedge$ denotes the small disturbance around the steady states.

III. Basic Principles

Two positive-feedback mechanisms can be established. One is voltage (magnitude) feedback; the other is frequency (of the voltage) feedback. An *RLC* load, as defined in Standards, is assumed. The relationships between the *RLC* load active/reactive power and the voltage/frequency are

$$P = \frac{V^2}{R} \tag{3}$$

$$Q = V^2(\omega C - 1/\omega L) \tag{4}$$

where R, L, and C denote the resistance, inductance, and capacitance of *RLC* load, respectively.

For voltage feedback, the mechanism is described as shown in Fig. 4. When the inverter-sensed output voltage is increasing, the AI feedback will command the inverter active power output to be increased. Due to the load characteristic in (3), the voltage will keep increasing in order to balance the active power. The increased voltage will further drive the inverter active power up due to the AI feedback. As a result, the voltage will be eventually out of the nominal ranges so that the islanding can be detected. Similar but opposite destabilization occurs when the sensed voltage is decreasing initially.

For frequency feedback, the mechanism is described in Fig. 5. When the inverter-sensed frequency is increasing, the AI feedback will command the inverter reactive power output to be increased. Due to the load characteristic in (4), the frequency will keep increasing in order to balance the reactive power. The increased frequency will further drive the inverter reactive power up due to the AI feedback. As a result, the frequency will be eventually out of the nominal ranges so that the islanding can be detected. A mirror image response, with similar destabilization, occurs when the sensed frequency is decreasing initially.

IV. Design Guidelines

Positive feedback can be implemented in two different ways for inverter-based DGs to prevent islanding, denoted as the voltage and frequency AI scheme, respectively [5], [14]. The structures of these AI schemes are shown in Fig. 6. The frequency AI compensator $H_q(s)$ takes the variations in the frequency $\hat{\omega}^*$ to generate the output i_{q_ai}, which disturbs the quadrature-axis current reference to the DG $\hat{i}_{q\mathrm{ref}}$. The voltage AI compensator $H_d(s)$ uses the variation in the voltage magnitude $\hat{u}_d$ to obtain the output i_{d_ai}, which changes the direct-axis current reference of the DG $\hat{i}_{d\mathrm{ref}}$.

Both schemes destabilize the isolated DG units by using the positive-feedback compensators [5], [14], [15]. Instability caused by the positive feedback, giving rise to large transients in the voltage or frequency in an island, will disrupt the islanding operation regardless of the gap between the local load and generation. However, the positive feedback has detrimen-

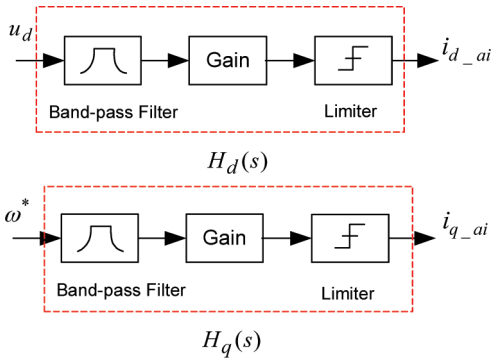

Fig. 6. Block diagram of the active AI compensators for inverter-based DGs.

tal effects on the normal operation of power systems. To limit these adverse impacts, a sufficient stability margin must be ensured when the grid is connected by selecting the appropriate positive-feedback compensator for the voltage and frequency AI schemes. A positive-feedback compensator may have the form [14], [15]

$$H(s) = K\frac{sT_w}{(1+sT_w)(1+sT_0)}. \tag{5}$$

It consists of a washout filter, gain, and first-order filter. The critical settings include the following.

1) The corner frequency of the washout filter $1/T_w$.
2) The gain *K*.
3) The corner frequency of the low-pass filter $1/T_0$.

Within the compensator, the signal washout block serves as a high-pass filter, with a time constant T_w to allow signals with frequency higher than $1/T_w$ to pass unchanged. A signal with frequency lower than $1/T_w$, especially a dc signal, will be attenuated by the washout filter. This is to minimize the impact of the positive-feedback loop on the steady-state regulation. The selection of gain *K* is a compromise between a high gain to ensure fast islanding detection and a low gain to prevent adverse impact, particularly stability impact, on the DG normal operations under the grid-connected conditions [14], [15]. The gain selection should leave gain margins of at least 5 dB. For the purpose of discussion, the voltage open-loop gain for inverter-based DGs with the voltage AI compensator is defined as follows:

$$T_d(s) = G_d(s)H_d(s) \tag{6}$$

and similarly, the frequency open-loop gain with the frequency AI compensator is defined as follows:

$$T_q(s) = G_q(s)H_q(s). \tag{7}$$

V. Performance Evaluation for a Single Inverter-Based DG Unit

The voltage/frequency open-loop gains $T_d(s)$ and $T_q(s)$ can be utilized to evaluate the performance of these AI schemes. In this section, the analysis is conducted under a simplified scenario, where one sole DG unit is embedded in the island. The parameters of the DG and the local load are given in Appendix A. Before islanding, the DG operates at a steady state. The DG's real-power output and the local load are closely matched, and the DG only exports the active power to the utility ($i_{q\text{ref}} = 0$). Islanding is caused by the tripping of the utility breaker without any involvement of faults.

The AI compensators must be designed under the worst case conditions, which can be identified by studying the impact of the various load conditions on the open-loop gains [16]. Following this procedure, the AI compensators are chosen as follows:

$$H_d(s) = \frac{0.318s}{(1+0.159s)(1+0.0159s)} \tag{8}$$

$$H_q(s) = \frac{1.272s}{(1+0.159s)(1+0.0159s)}. \tag{9}$$

After the compensators have been selected, the impact of the different factors over the performance of these AI schemes is examined in the following three sections.

A. Power Level

The Bode plots of the open-loop gains under different levels of the power output are shown in Fig. 7 in which the active power output of the DG [which matches the real power to a static local load ($Q_f = 1.8$)] is varied from 30% to 90%. Under the islanding condition, the magnitude of both the voltage and frequency open-loop gain has been increased by the positive feedback, resulting in a peak value greater than 0 dB, while the associated phase is lagging more than 0° (due to space limitation, the phase angle of Bode plots is omitted in Figs. 7–9). This insufficient phase margin will drive the islanded DG unstable.

The peak value of the voltage/frequency open-loop gain decreases as the DG increases its output power, which means that the effectiveness of these AI schemes is adversely impacted by the high-power output of the DG. It is also shown that under the grid-connected situation, the peak value of the voltage and frequency open-loop gain is much less than 0 dB. Therefore, the DG is stable when the utility is connected so that any nonislanding disturbance will be attenuated and diminished eventually.

B. Quality Factor

The quality factor of a *RLC* load is defined as the ratio of the reactive power stored in the load inductor or capacitor to real power consumed by the resistant load. For a load with fixed active power, the different quality factors imply varying reactive power of the load. Usually, a load with the quality factor of 2.5 is considered an extreme case for the islanding study [1], [15]. The voltage and frequency open-loop gains with the different quality factors, $Q_f = 0.0$ and $Q_f = 1.8$, are compared with each other in Fig. 8. It is shown that, for the islanded inverter-based DG, the peak magnitude of the open-loop gains for both voltage and frequency AI schemes decreases a little with the increasing quality factor.

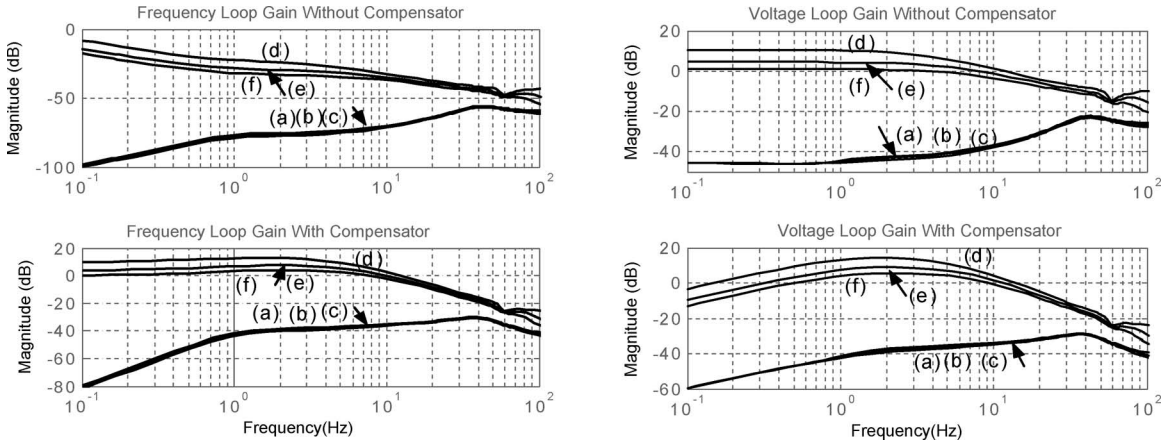

Fig. 7. Open-loop gains with the varying power output ($Q_f = 1.8$). (a)–(c) Grid-connected $P_e = 30\%$, $P_e = 60\%$, and $P_e = 90\%$. (d)–(f) Grid-disconnected $P_e = 30\%$, $P_e = 60\%$, and $P_e = 90\%$).

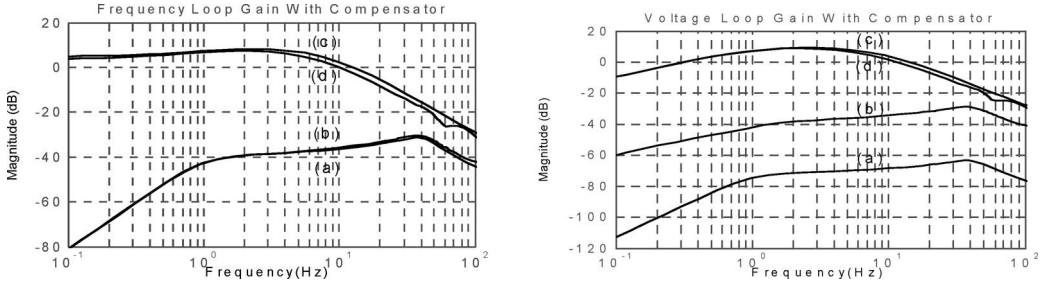

Fig. 8. Open-loop gains with different quality factor (*RLC* load and P = 1.0 p.u.) ((a) (b) Grid-connected $Q_f = 0.0$ and $Q_f = 1.8$ (c)(d) Grid-disconnected $Q_f = 0.0$ and $Q_f = 1.8$).

C. Grid Impedance

The compensated voltage and frequency open-loop gains have been evaluated for grid impedances varying from 5% to 60% (on a base of the DG power rating), as shown in Fig. 9. The compensated voltage/frequency open-loop gains increase with the grid impedance. As the grid impedance increases as high as 0.3 per unit (p.u.), the open-loop gains for both the voltage AI scheme and the frequency AI scheme have about 10 dB gain margin. Due to this, a tradeoff in selecting the gain of the compensator has to be made to avoid the devastating effect on the normal operation of power systems when the grid impedance is high.

Therefore, in an island where only one inverter-based DG unit is present, the effectiveness of the frequency and voltage AI schemes will be negatively affected by either the high grid impedance or the high output power of the DG, while the effect of the quality factor of *RLC* load is negligible.

VI. Performance Evaluation for Multiple Inverter-Based DG Units

To evaluate the performance of the AI schemes for a multiple inverter-based DG system, seven cases with different conditions, which are defined in Table I, have been investigated. In these investigations, the grid was disconnected at $t = 1.0$ s. The DG is operating at its full power output, and the quality factor for the *RLC* load is 1.8. Fig. 10 shows the maximum singular value (MSV) of the open-looped multiple DG system generated from MATLAB under these different scenarios with the different AI compensators as specified in Table I[2]. The corresponding time-domain simulation results obtained from PSCAD are shown in Fig. 11.

A baseline case for inverter-based DGs without any positive feedback, denoted as case 1, is simulated in Fig. 11. The variations in the frequency and the terminal voltage are very small, which necessitates the positive-feedback-based means to detect islanding. The same situation has been simulated except that the voltage/frequency AI scheme is enabled. In cases 2 and 3, the voltage AI scheme and frequency AI scheme is enabled simultaneously but either voltage or frequency scheme was applied to only one DG unit. The peak value of the new voltage/frequency open-loop gain is less than 0 dB at the full power output of the DG, which causes the positive feedback to fail. This is also consistent with the time-domain simulation results in Fig. 11. In cases 4 and 5, the peak value of MSVs of the island is still greater than 0 dB, which indicates that the schemes are effective in preventing islanding for the multiple-DG units. This has also been verified by the time-domain simulation shown in Fig. 11.

The simulation results clearly show that only when all of DGs can perturb their P_{command} (or Q_{command}) simultaneously, the

[2]The peak value of the MSV evaluated under the open-looped condition is an indication of the stability of the multiple-input and multiple-output dynamical system [17]. The close-looped system is stable when the peak value of MSV of the open-looped dynamical system is less than 0 dB.

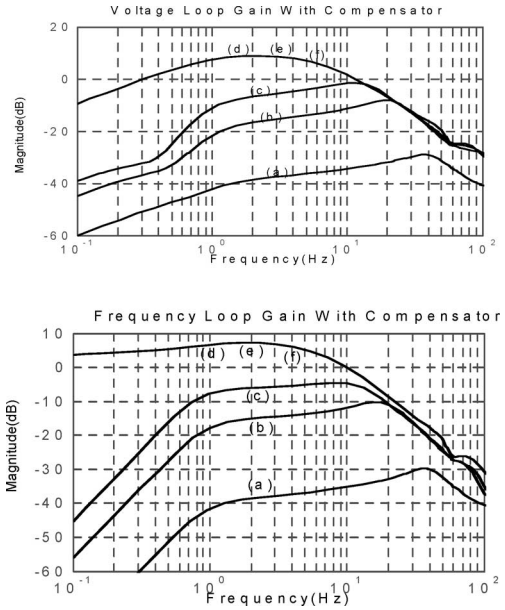

Fig. 9. Compensated loop gain with varying grid impedances for the inverter-based DG (static *RLC* load $Q_f = 1.8$). (a)-(c) Grid-connected $R_e = 0.5\%$, $L_e = 5\%$; $R_e = 3\%$, $L_e = 30\%$; $R_e = 6\%$, $L_e = 60\%$. (d)–(f) Grid-disconnected $R_e = 0.5\%$, $L_e = 5\%$; $R_e = 3\%$, $L_e = 30\%$; $R_e = 6\%$, $L_e = 60\%$.

TABLE I
DIFFERENT SCENARIO FOR MULTIPLE DG UNITS

	DG_1		DG_2		Power Line	
	Voltage AI Scheme	Frequency AI Scheme	Voltage AI Scheme	Frequency AI Scheme	Resistance (p.u.)	Inductance (p.u.)
case 1					0.0	0.0
case 2	Enabled	Enabled			0.0	0.0
case 3	Enabled			Enabled	0.0	0.0
case 4	Enabled		Enabled		0.0	0.0
case 5		Enabled		Enabled	0.0	0.0
case 6	Enabled		Enabled		0.0	0.2
case 7		Enabled		Enabled	0.0	0.2

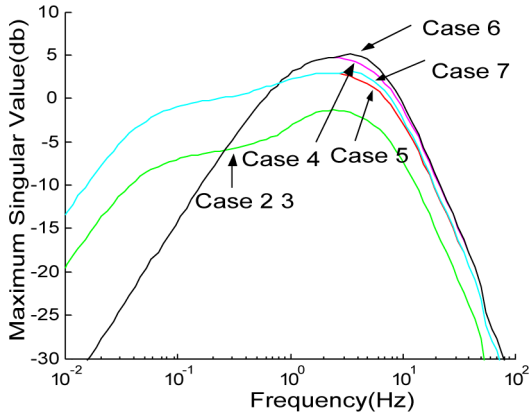

Fig. 10. MSV for the multiple DG systems under the scenario depicted in Table I.

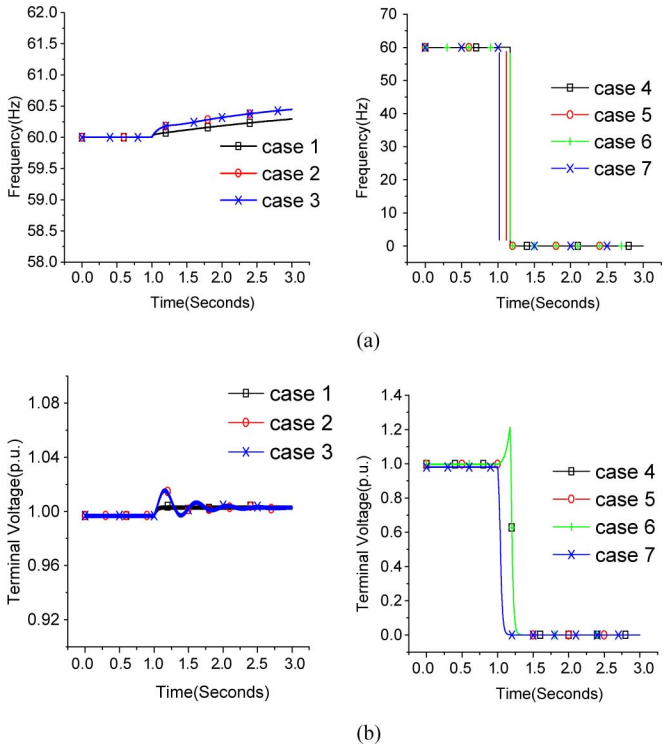

Fig. 11. Time-domain simulation results in PSCAD for the interconnection of two inverter-based DG systems. (a) Frequency (Hz) in response to the islanding at $t = 1.0$ s. (b) Terminal voltage (p.u.) in response to the islanding at $t = 1.0$ s.

positive-feedback-based AI scheme will be effective in preventing islanding.

It is also shown in cases 6–7 that the line impedance between two DG units only causes a slight change in the MSVs of the island. This indicates that the time impedance is not an important factor influencing the effectiveness of the positive-feedback-based AI schemes for the inverter-based DGs.

VII. SUMMARY

In this paper, the basic principles and the design guidelines of positive-feedback-based AI schemes have been provided, and their performance has been evaluated for inverter-based DGs. The evidence demonstrated by the time-domain simulation and analytical results clearly shows that these methods are reliable, robust to other nonislanding disturbances, and effective in the presence of a high penetration of DG units. The major contributions in this paper can be summarized in the following.

1) The positive-feedback-based AI schemes for inverter-based DGs have been proposed, and the basic principles are provided. These AI schemes are superior to others because they can discriminate between the islanding event and other nonislanding disturbances.
2) High grid impedance and high output power constitute the worst case scenarios to be considered when these positive-feedback-based AI schemes are designed for a single-DG island. The interactions between multiple inverter-based DGs in the island may have a negative impact over the performance of these schemes. To circumvent this effect, the best strategy is to equip each DG unit with the same

AI scheme (either the voltage AI scheme or the frequency AI scheme).

3) The design guidelines of these schemes are provided, which include three steps as follows.

Step 1: Identify the voltage/frequency open-loop gains $T_d(s)$ and $T_q(s)$, under the worst case conditions (high grid impedance or high output power of the DG or multiple DGs).

Step 2: Determine the corner frequency of the washout filter $1/T_w$, the gain *K,* and the corner frequency of the low-pass filter $1/T_0$ so that sufficient stability margin is ensured when the grid is connected, and the peak value of the closed-loop gain is greater than 0 dB, while the associated phase is lagging more than 0° when the DG is isolated.

Step 3: Evaluate the performance of the voltage/frequency AI schemes with time-domain simulations.

APPENDIX

A. Inverter-Based DG Parameters

Current Regulator	K_p =0.25
	K_i =100
Three-phase PLL	K_{pll} =0.0822
	T_{pll} =0.2581
Voltage AI Compensator	Gain K =2
	Corner Time Constant T_w =0.1592
	Time constant T_1 =0.0159
Frequency AI Compensator	Gain K =80
	Corner Time Constant T_w =0.1592
	Time Constant T_1 =0.0159
System Parameters	Output filter L_f =2.5 *mH*
	Constant Voltage Source V_g =500 *V*
	Grid resistor R_e = 0.012 Ω
	Grid inductor L_e = 0.3056 *mH*
Load Parameters (100 % of Load)	R =1.536 Ω
	L =2.26354 *mH*
	C =3108.295e3 μF

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