IEEE Transactions on Nuclear Science, Vol. NS-34, No. 6, December 1987

POST-IRRADIATION EFFECTS IN FIELD-OXIDE ISOLATION STRUCTURES*

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Abstract

We have studied experimentally the time dependence of leakage currents in six CMOS (complementary metal-oxide semiconductor) processes using LOCOS (local oxidation of silicon) isolation structures. These six process lines represent six different U.S. semiconductor companies. In their radiation response, these processes range from very hard to very soft. In the softer processes, the radiation-induced leakage currents are due to the turning on of a leakage path either under the thick field-oxide or along the transistor edge (bird's beak) region. In the hardest process, the field-oxide did not turn on, and the leakage was entirely due to subthreshold current in the gate region. These different mechanisms have qualitatively different time dependences, which we describe and discuss. We also discuss the implications of our results for hardness assurance testing.

Introduction

In recent years most researchers have come to recognize that metal-oxide semiconductor (MOS) structures have a complex time-dependent response to ionizing radiation. The "total dose response" of a circuit depends on bias, temperature, and dose rate or annealing time, in addition to total dose. These other factors may be critical in determining whether a circuit performs well in a given operational environment. For this reason, many researchers have been studying the time-dependent response of MOS structures--either to understand the individual processes involved or to determine how they all fit together.

Another factor motivating this study is the question of how to test complex integrated circuits. The use of test chips is obviously necessary to determine the mechanisms which cause functional failure, but how does one correlate test chip results with the radiation response of a large circuit? Many of the previous studies have concentrated on the threshold voltage shift of the individual transistors, using either edgeless or guardbanded transistors or transistors with hardened field oxides to suppress leakage currents. While the threshold voltage shift under irradiation is an important parameter and an easy one to measure, a circuit can and frequently does fail even though all the transistors are still working. If, for example, in a 64K static RAM, each cell contains one n-channel transistor biased off which has 10^{-7} A leakage current, the total power supply current is 6.4 mA. Even if the circuit is still functional, many systems have a power budget which cannot support this load. On the other hand, if this leakage current recovers by, let us say, a factor 10, the system might also recover. There is relatively little data in the literature on the time dependence of radiation induced leakage currents, and most of it concerns gate-oxide subthreshold current in a hardened process.[1]

There have been a few basic studies[2-4] of the response of thick field-oxide capacitors. Also Sexton et al. have examined the correlation between transistor response and circuit response.[5] In that study, they found that the power-supply current correlated very well with the leakage current of the n-channel transistors (see Fig. 1b of reference 5). Several authors[6-11] have reported that thinning the gate oxide produces harder gate oxides. Since the historic trend in the semiconductor industry has been and is still toward thinner oxides, one would expect gate-oxide response to be relatively less important in future technologies. For this reason, the field-oxide response will be increasingly important in future technologies.

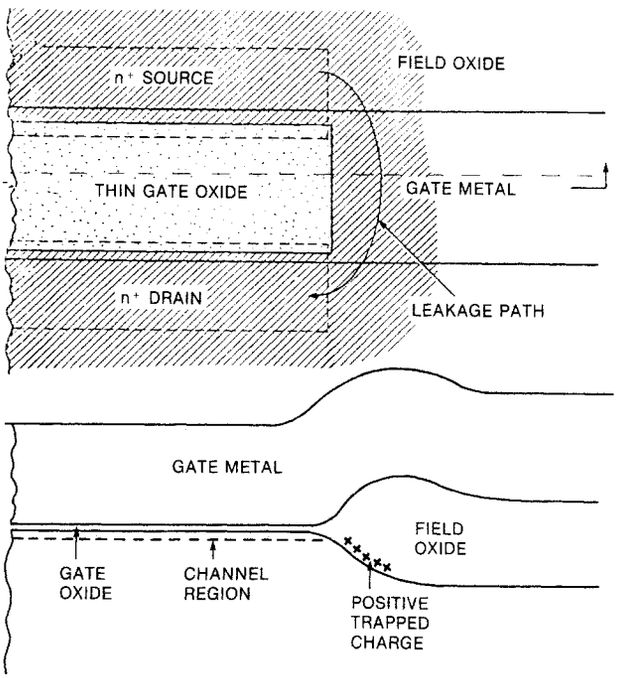

Fig. 1. Schematic illustration of the LOCOS field oxide isolation structure. Possible leakage paths are: (1) under the thick, uniform field oxide; (2) under the edge (bird's beak) oxide; (3) under the thin gate oxide.

In this study, we have examined six CMOS processes using LOCOS isolation from six different manufacturers. The basic LOCOS structure is illustrated in Fig. 1a and 1b. Fig. 1a shows the top view of a transistor surrounded by a thick field oxide. If one cuts along the dashed line in Fig. 1a, the cross section is shown in Fig. 1b. We have considered three leakage paths in our discussion. Of the five unhardened processes, all five showed significant leakage current at relatively low doses (kilorads to tens of kilorads). In two of these cases, the response of the field-oxide transistors (FOXFETs) tracked the response of the parasitic leakage transistor, suggesting that effects in the thick field oxide controlled the device response. In the other three cases, the parasitic characteristic was different from the FOXFET response, suggesting that effects in the transitional edge (bird's-beak) region controlled the overall device response. (It is also possible that the FOXFET structures were processed differently than the real isolation structures.) In all five cases where we observed significant leakage current, the I-V characteristic of the parasitic transistor showed a very strong time dependence. The recovery process seems to be a thermally activated detrapping of holes with a characteristic time at room temperature of about 10^6 s. This process is qualitatively different from what has previously been reported in thick field oxides or

* Supported by the Defense Nuclear Agency TREE Program

thin gate oxides. Previously, many authors have described annealing of gate-oxide radiation damage with approximately a logarithmic time dependence.[12-15] This t-dependence can be explained in terms of a tunneling model. We observe a similar ln t annealing of thick field-oxide test transistors on some of these samples, suggesting that the same kind of tunneling process causes the recovery observed there. However, for the parasitic transistor controlling leakage, a qualitatively different process is observed. In two cases, the thick field oxide shows this behavior, but in three other cases it may be limited to the bird's-beak edge region. Tunneling may play a role in the annealing in this process, but is not the rate controlling step. We emphasize that since we have observed this annealing in five out of five processes, we believe it to be generally true in LOCOS processes. We will present data showing the recovery of the parasitic electrical characteristics, and also data showing the recovery of leakage current with time in these devices.

For the hardened process, the process has been modified to harden the field oxide and edge. The only leakage current we observed is subthreshold current in the gate region. We examined this process for two reasons. First, to determine if the field oxide depended on a large interface-state buildup to achieve its hardness. In fact, the interface-state buildup is relatively small, and the field-oxide hardness arises from the fact that the hole trapping saturates. Second, if any leakage current did occur, we wanted to find a scheme for making predictions. Since subthreshold leakage in the gate region does occur, and the threshold voltage is "well behaved," we discuss how to make predictions for leakage currents at other times and other dose rates.

Experimental Procedure

Irradiations were performed on six different bulk CMOS processes with LOCOS isolation (each process came from a different vendor). In each case, the test vehicle was an n-channel field-oxide-region transistor, along with an n-channel FET in the normal gate-oxide region. In some cases, a p-channel FET was put in series with the n-channel gate-oxide FET in an inverter configuration. However, the p-channel shifts were small in all cases, and little recovery was observed. For this reason, we did not perform the p-channel tests in all cases. The irradiations were performed with an ARACOR 10-keV x-ray source. Dosimetry was performed with a silicon p-i-n diode. The diode readings in rad(Si) were corrected to rad(SiO_2) by dividing by 1.8. The dose numbers presented in this paper are for a gate-oxide device. The actual dose in the bird's-beak region is somewhat less than the gate-oxide dose. The correction factors for a 10-keV source depend upon knowing the oxide field during irradiation and the oxide thickness, parameters not easily determined in this transition region.

Both the irradiations and the subsequent anneals were done with gates biased both high (+5 V) and low (0 V); the other terminals were grounded. The drain-current versus gate-voltage curves used to analyze the effects of the irradiations were measured with an HP 4145B semiconductor parameter analyzer. The data were then downloaded to an HP1000 mainframe computer for analysis. Currents between 0.1 pA and 1 mA were measured. Measurements were made between doses of radiation, and then about every half decade of time (in seconds) following the last irradiation out to 3 x 10^6 s.

Results and Discussion

In Fig. 2, we illustrate the basic effects which we will discuss. We show the pre-irradiation I-V characteristic for an n-channel gate oxide transistor. After some dose, this characteristic is shifted some distance to the left. Also shown is the pre-irradiation I-V characteristic of a parasitic field oxide or edge region transistor. For this parasitic device, the initial threshold voltage is set much higher than for the gate oxide transistor to prevent the leakage path from turning on. But because the field oxide is much thicker than the gate oxide, the shift of the I-V characteristic from radiation exposure is much larger than for the gate oxide. In Fig. 2, we show the parasitic I-V characteristic moving past the gate oxide characteristic. When this happens, the actual I-V characteristic of the transistor will resemble the combined response curve in Fig. 2. This curve is representative of the response we observed in all five of our unhardened processes.

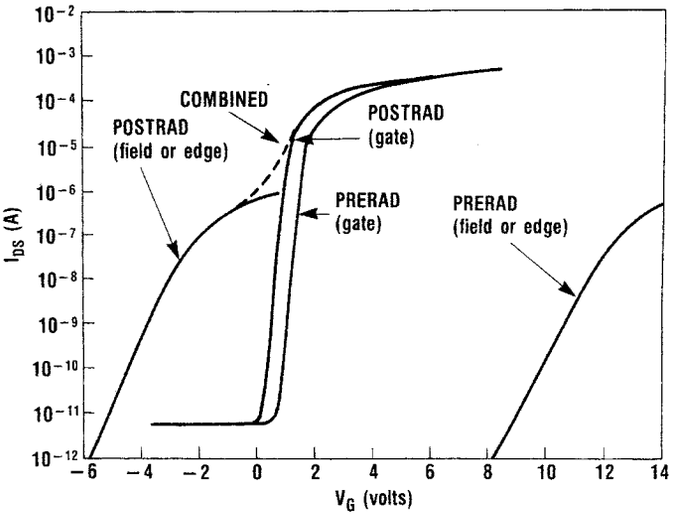

Fig. 2. Schematic illustration of the I-V characteristic of an n-channel gate oxide transistor and the parasitic leakage transistor before and after irradiation. The parasitic device shows a much larger threshold shift under irradiation because the oxide is thicker. After irradiation, the parasitic leakage dominates the response of the gate oxide transistor.

For these devices, the inversion point current corresponding to the surface potential $\psi_s = 2\phi_B$ is about 10^{-7}A. For a transistor with no parasitic leakage, the inversion point shift is reasonably close to the threshold voltage as determined by conventional methods. In the following discussion, we plot the voltage corresponding to 10^{-7}A as the apparent threshold voltage shift. However, this apparent threshold shift is dominated by the response of the parasitic leakage path, and is much larger in most cases than the actual threshold voltage shift of the transistor itself.

In Fig. 3, we show typical raw data for a soft oxide which we have labelled Process A. In this case, a soft sample was irradiated to a dose of 20 krad at a dose rate of 10 rad/s. Both n- and p-channel transistors were irradiated in an inverter configuration with V_G = 5 V. The preradiation curve is shown, and the curve after a dose of 5 krad is displaced slightly to the left, but not distorted at all. In addition, the 0-V leakage current has not increased at all from the preradiation value. After 10 krad, the threshold voltage has shifted only a little more, but the edge has started to turn on and the subthreshold current has started to increase. The V_G = 0 leakage current has increased by about two orders of magnitude, from less than 10^{-10} A to almost 10^{-8} A. After 20 krad, the parasitic leakage transistor seems to be fully on, and the leakage current at V_G = 0 has increased to several μA. The apparent threshold voltage has shifted to about -2.5 V. However, the actual threshold voltage shift in the gate region is much

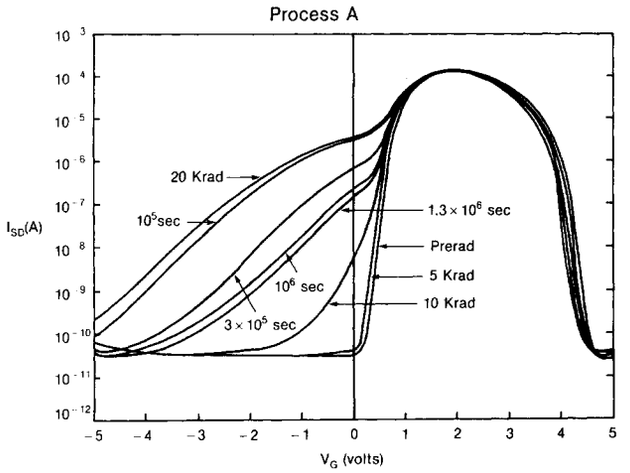

Fig. 3. Raw data for an n-channel and a p-channel transistor connected as an inverter. Data taken during irradiation is indicated by dose (5, 10 and 20 krad) and annealing curves are indicated by annealing time (10^5, $3x10^5$, 10^6, and $1.3x10^6$s). Dose rate is 10 rads(SiO_2)/s.

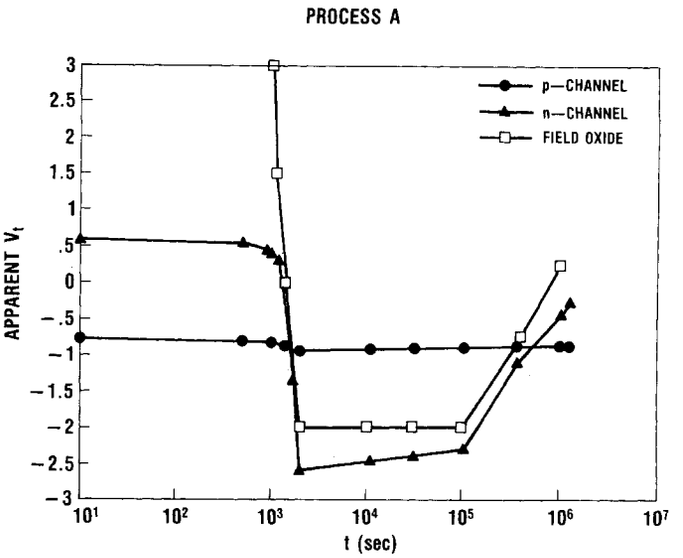

Fig. 4. For the sample illustrated in Fig. 3, apparent threshold shift is plotted as a function of time for n- and p-channel gate oxide FETs and for an n-channel FOXFET. Dose is 20 krads(SiO_2) delivered at 10 rads(SiO_2)/s.

smaller. At low doses before edge effects become apparent, the threshold voltage shift in the gate region is 0.013 V/krad or 0.260 V at 20 krad.

In Fig. 3, we also show four curves illustrating the time dependent annealing of the damage to the field-oxide. These curves were taken after 10^5, 3 x 10^5, 10^6, and 1.3 x 10^6 s respectively. The apparent threshold voltage recovers about 2 V in 1.3 x 10^6 s. This recovery is primarily due to the annealing of fixed charge rather than interface-state buildup, because the subthreshold slope changes very little. (Also, we note that the slope of the subthreshold I-V curve will generally be a function of the oxide thickness. The fact that the slope of the subthreshold I-V curve does not change much during annealing indicates that the active region controlling the response is in the thick (but uniform) field oxide, rather than the edge region, where the oxide thickness changes rapidly.) In addition, the recovery does not show a ln t dependence (the time dependence of the recovery is shown more clearly in Fig. 4). Along with the recovery of the apparent threshold voltage, the leakage current at V_{GS} = 0 is reduced by about a factor 30 after 1.3 x 10^6 s. (This recovery will be shown more clearly later--see Fig. 6.)

In Fig. 4, we plot the apparent threshold voltage for n- and p-channel transistors for Process A, and also the threshold voltage for an n-channel field-oxide transistor. For this irradiation, the dose was 20 krad, delivered in 2000 s--that is, at 10 rad(SiO_2)/s. For this process, we show the p-channel curve for comparison, but all the important changes occur on the n-channel devices. For this reason, we discuss primarily the n-channel results. The n-channel gate-oxide transistor threshold shows a small negative shift at 1000 s (10 krad), but shifts very rapidly negative between 1000 and 2000 s. The field-oxide threshold voltage it tracks the n-channel gate-oxide threshold very closely. Both go negative at the same time; the maximum negative value of the shift is 2 to 2.5 V for both; both show little or no recovery for the first 10^5 s after irradiation; and both show rapid recovery between 10^5 and 10^6 s. This result indicates that the response of the n-channel gate-oxide transistor is really controlled by the field-oxide isolation structure around it. (For this process, the n-channel MOSFET response tracks the response of the thick FOXFET, suggesting that the thick field oxide controls the leakage current response. However, in Fig. 5, we show an example where the parasitic leakage response is clearly different than the thick field oxide response.)

The time dependence of the n-channel transistor shown in Fig. 4 is qualitatively different from what has been reported previously. Many authors have reported a ln t dependence for the recovery of transistor threshold voltages. A ln t dependence is consistent with a tunneling model. Recently we presented measurements and analyses pointing out that small deviations from ln t annealing can be accounted for in a tunneling model if the spatial distribution of traps is not uniform.[14] Basically, one can think of a tunneling front moving into the oxide with a logarithmic velocity. Because of the exponential nature of the tunneling process, there is a depth at a given time beyond which almost all the traps are still filled and up to which the traps are mostly emptied. The rate at which this front moves depends on the barrier height, but we estimated it at about 0.2 nm/decade. If the spatial density of traps is nonuniform, but varying only slightly in 0.2 nm, deviations from simple ln t behavior that we and others have observed could be accounted for. However, trying to force the results in Fig. 3 into this model would require all the traps to be located in 0.2 nm (less than half a monolayer), several monolayers from the interface--clearly an unreasonable result.

A more reasonable explanation for the results in Fig. 4 is that the recovery is due to a thermally activated detrapping process with a characteristic time on the order of 10^6 s. For the five unhardened processes we have tested for this study, all five parasitic leakage devices show the same qualitative recovery illustrated in Figs. 3 and 4. That is, there is a characteristic time for the recovery, which is about 10^6 s. Before 10^5 s virtually no recovery occurs; after 10^6 s the apparent threshold voltage has recovered almost completely. However, the response of the field-oxide FET does not always track the response of the edge region. For the five processes, the field-oxide FET recovery has a logarithmic recovery characteristic of tunneling in three cases (B, C, E). For processes A and D, on the other hand, the field-oxide FET has the same qualitative time dependence to its recovery that we observe in the apparent threshold voltage of the n-channel MOSFET. In the edge region the oxide thickness, the initial threshold voltage, and doping profiles are all

changing rapidly with position. In addition, fringing fields probably play a large role, and the edge region is probably more highly strained than other parts of a MOS structure. For these reasons, it is not too surprising that a recovery mechanism qualitatively different from that observed in either the gate oxide or the thick field oxide away from the edge seems to control the response of the edge region. However, in two cases the field oxide FET seems to be different, too.

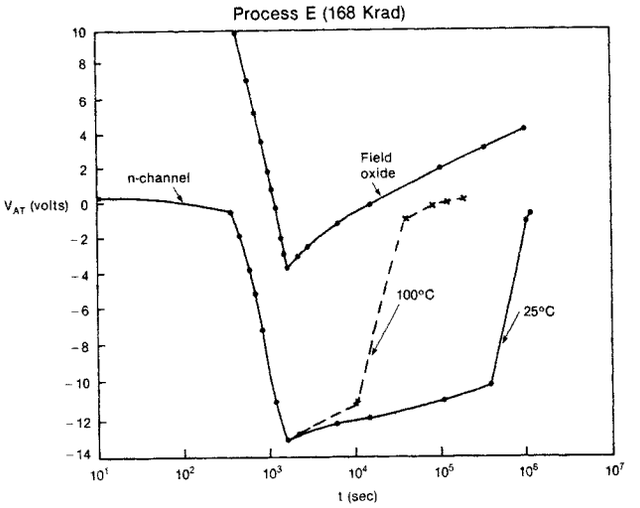

Fig. 5. Apparent threshold shift for n-channel gate oxide FET exposed to 168 krad(SiO_2) at 100 rads (SiO_2)/s, annealed at 25°C and 100°C. Also shown is the response of a field oxide transistor receiving the same exposure and annealed at 25°C. Note that the annealing of the parasitic leakage device does not have the same qualitative time dependence as the FOXFET.

In Fig. 5, we show experimental results for process E. The FOXFET seems to recover logarithmically, but the apparent threshold voltage for the n-channel MOSFET has a characteristic recovery time at room temperature of about 10^6 s. Also included in Fig. 5 are the results of an annealing experiment conducted at elevated temperature, 100°C. The recovery occurs earlier, between 1 and a few times 10^4 s, but the curve is roughly parallel to the room temperature curve. From this result we estimate an activation energy for process E of about 0.42 eV. (So far we have performed high-temperature anneals only for one other process (A) and obtained an activation energy of 0.58 eV for it. We conclude that although all five processes have a qualitatively similar thermally activated annealing process, the different processes are characterized by a range of activation energies.)

In Fig. 6, we plot the recovery of the apparent n-channel threshold voltage shift for all five unhardened processes we have tested. We plot $\ln(-\Delta V_T)$ on a linear time scale from zero to 1.4×10^6 s. For a detrapping process controlled by random thermal excitations, the recovery will be an exponential function of time--a straight line on a plot like Fig. 6. All five processes show a straight line recovery, at least until most of the charge is removed. The fact that annealing of charge along the parasitic leakage path is exponential with time rather than logarithmic in time is clearly a new result, and it can have important implications for the way parts are tested. However, the parasitic threshold voltage in the field oxide has an impact on circuit performance only in that it affects the leakage current.

In Fig. 7, we present leakage current data for processes A and E as a function of time. These results are for the n-channel transistors with $V_G = 0$,

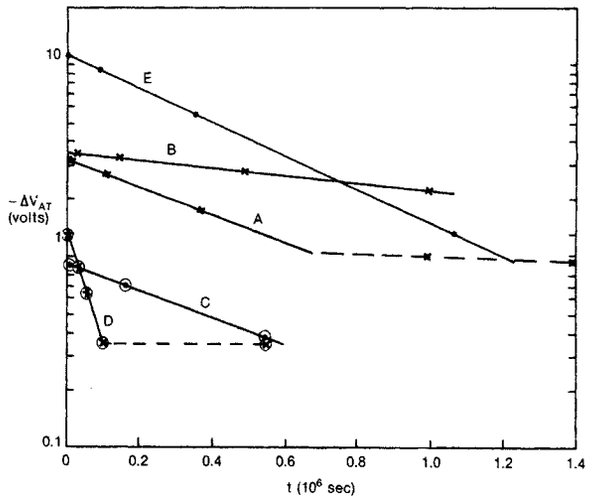

Fig. 6. Apparent threshold voltage recovery for all five unhardened processes plotted on a linear time scale. If annealing is caused by random thermal excitations, the threshold recovery will follow a straight line in this plot.

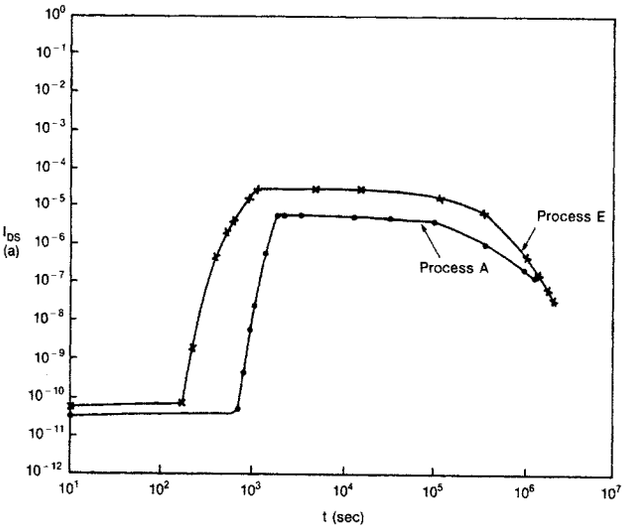

Fig. 7. Time dependence of leakage currents for two unhardened processes. Recovery occurs with a characteristic time of about 10^6s, similar to the threshold voltage recovery time.

and are for the same devices whose responses are shown in Figs. 3 and 5. The preradiation leakage current starts to increase after some dose, and increases until the end of the radiation exposure. After irradiation, the $V_G = 0$ current remains roughly constant until about 10^5 s, and then it starts to drop. For process A, the reduction in current at $V_G = 0$ is about a factor of 30. For process E, the improvement in leakage current with annealing is about three orders of magnitude. For process E, the bird's-beak damage is now essentially completely gone, and the remaining leakage current is due to subthreshold current in the gate region--a different mechanism. For process A, there is still some damage to the parasitic device. We conclude that the annealing of the parasitic device can significantly affect the leakage current and, therefore, the power requirements of a circuit. However, we feel obliged to point out that such is not always the case. If the apparent threshold voltage shift due to the bird's beak is large enough, the current at $V_G = 0$ V will saturate. Then, even if the apparent threshold voltage recovers significantly, the current at $V_G = 0$ V may not change much. We have observed three examples of this kind of

response (processes B, C, D), although we will not show them here.

These results have a number of implications for the testing of unhardened parts. First, functional failure of a circuit will sometimes be due to excessive leakage current rather than true ΔV_T in the gate region. If test chips for very-large-scale-integration (VLSI) processes are used for parametric testing, one will obviously have to look for all the possible failure mechanisms. Second, a typical Co^{60} test lasting 10^3 or 10^4 s is a much more severe test than, say, a space environment. If damage to the parasitic leakage device anneals in 10^6 s, one might hope that in an environment where the dose is delivered in a period much longer than 10^6 s, the device would never turn on. In such an environment, even a soft part could do very well. However, as we have shown in Fig. 7a and 7b, the current at 0 V may not change much even when the edge region threshold voltage changes significantly. Although one might hope that a soft part would be good enough for a given environment, a fairly realistic test must be done to be sure. Third, none of these processes show any signficant interface-state buildup at the doses to which we have tested. For this reason, one can ignore the possibility of a late time rebound failure for these processes. That is, by testing to a realistic dose and letting the sample anneal for about 10^6 s, one can at least be sure that if the part recovers, it will stay recovered.

Besides testing unhardened processes, we have also tested one hardened process. For this process (F), we did not observe any field-oxide leakage of any kind in any test we performed. The only leakage current was subthreshold leakage in the gate region. We discuss the response of the field oxide and the gate separately for this process.

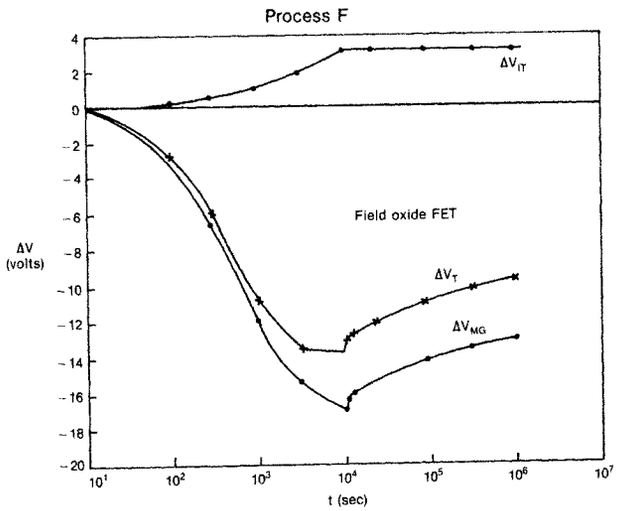

Fig. 8. Threshold voltage shift for a hardened field oxide, resolved into fixed charge and interface trapped charge components. Saturation of fixed charge trapping is what makes this oxide hard. Interface state charge contribution is relatively small. Total dose is 1 Mrad(SiO_2) delivered in 10^4s.

Initially, we wanted to test this process to ensure that the manufacturer was not relying on a large interface-state buildup to achieve a hardened field oxide. In Fig. 8, we show results which indicate that, in fact, the interface-state buildup is rather small at this dose. The sample was exposed to 1 Mrad (SiO_2) in 10^4 s, and we have used the midgap charge separation technique [16-17] to resolve the threshold shift into components. The hardness of this field oxide is a consequence of the fact that the hole trapping (midgap shift) saturates fairly strongly. In Fig. 8, 90% of the maximum midgap shift is observed after 30% of the dose has been delivered. We believe this result is due to field modification rather than to filling of all the available traps. The threshold voltage shift is about 14 V, much greater than the 5 V applied bias. Also, ΔV_{IT} is only about 15% of ΔV_{MG} at the end of the radiation exposure (10^4s). In this field oxide, we conclude that subtle process changes are unlikely to degrade the hardness. The changes in internal fields which cause the changes in hole trapping do not depend on processing. Also, the interface state density would be more likely to increase than decrease, which improves the response of a field oxide.

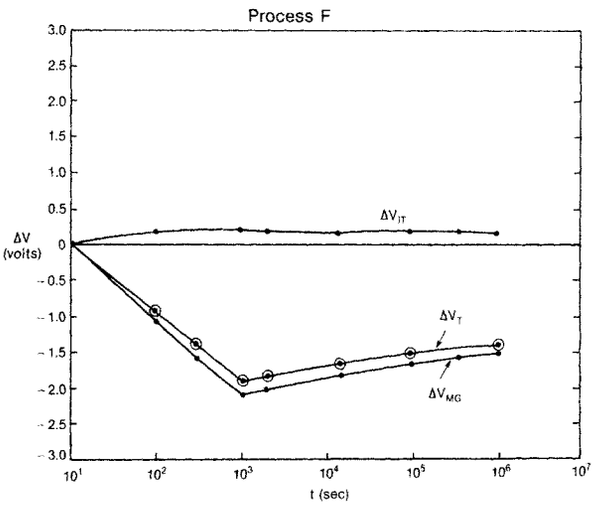

Fig.9. For a hardened n-channel gate oxide transistor, threshold voltage shift is resolved into interface state charge and oxide fixed charge components. For this process, interface trapped charge makes a very small contribution to the threshold voltage shift. Dose is 1 Mrad (SiO_2) delivered in 1000s.

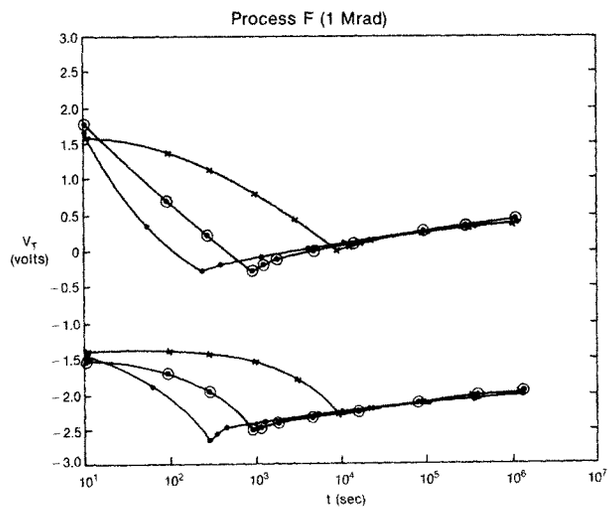

Fig. 10. Threshold voltage shifts for hardened n- and p-channel transistors irradiated to 1 Mrad(SiO_2) at three different dose rates. At late times, all the curves fall together, and are nearly linear with ln t.

In Fig. 9, we show results for an n-channel MOSFET (process F) exposed to 1 Mrad(SiO_2) in 10^3 s. The main point here is that the voltage shift due to interface states is extremely small, and can be neglected for practical purposes, at least at this dose. The shift due to hole trapping (midgap shift) is large enough that significant subthreshold leakage current occurs in the gate region. Since this leakage current is controlled by the gate threshold voltage which is controlled in turn by hole trapping, making

predictions about post irradiation response is relatively easy, especially at lower dose rates.

In Fig. 10, we show threshold voltage shifts for n- and p-channel MOSFETs (from process F) exposed to 1 Mrad (SiO_2) at three different dose rates. After the end of the longest exposure, all three samples have almost exactly the same threshold shift, and they are clearly following the same recovery curve. The recovery is very close to a simple ln t anneal. Clearly, one can extrapolate this recovery curve out to 10^7 or 10^8 s with good accuracy. We point out, however, that even though the recovery curve in Fig. 10 is well-behaved and predictable, one cannot use a simple linear systems theory (LST) approach because the response is nonlinear with dose. That is, the hole trapping is saturating--the response per unit dose depends on the previous dose. This effect is obscured here because all three exposures ended at the same total dose. For this reason, one must use a modified LST treatment to make predictions as a function of dose.

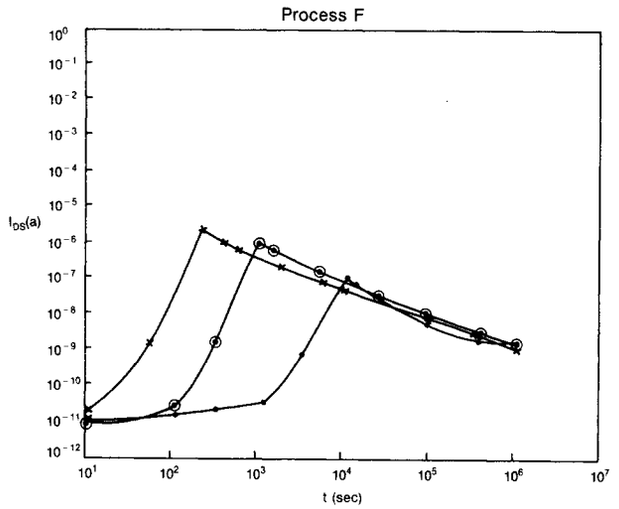

Fig. 11. Time dependence of subthreshold gate oxide leakage current for the same samples as Fig. 10. Roughly linear dependence of leakage current with time arises because ΔV_T is logarithmic with time, and because current is an exponential function of V_T.

In Fig. 11, we show the n-channel leakage current for the same devices discussed in Fig. 10. The leakage current increases to a maximum value at the end of the exposure (1 Mrad(SiO_2)), then it recovers linearly with time. The basic linear recovery is a consequence of two things. First, the threshold voltage is a logarithmic function of time. Second, the subthreshold current is an exponential function of the threshold voltage. The linear response of the current follows from taking the exponential of a log function. Clearly one can extend the annealing curve in Fig. 11 to later times. Also, if the same dose were delivered at a lower dose rate, one could estimate the leakage current at the end of the exposure. Predictions are relatively simple when the data are well behaved.

Conclusions

We have examined the time dependent leakage currents in five unhardened processes and one hardened process, and we have discussed the mechanisms controlling the leakage currents. For the unhardened processes, oxide trapped charge in the field oxide or edge region controls leakage current. Most of this charge is removed by a thermally activated process (exponential time dependence), with a characteristic time of about 10^6 s at room temperature. This process is qualitatively different from the logarithmic tunneling process observed in thin gate oxides and (often) in thick field oxides on the same chips. After a short laboratory irradiation, some processes will show orders of magnitude improvement in leakage current after about 10^6 s, but others will not. Some of these processes may perform well in a low dose rate environment, but it is difficult to predict which ones without some fairly realistic testing.

For the hardened process, the field-oxide hardness does not depend on interface states. The gate-oxide radiation response is almost entirely due to fixed charge trapping. In this process, the only leakage current is subthreshold current in the gate region. This leakage current decreases linearly with time after irradiation, making it easy to predict from simple tests.

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