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# Post-Correction of Pipelined Analog-Digital Converters based on Input Dependent Integral Nonlinearity Modeling

Samer Medawar, Peter Händel, Niclas Björsell, Magnus Jansson

Abstract—The integral nonlinearity (INL) is used for the post-correction of analog-digital converters (ADCs). An inputfrequency-dependent INL-model is developed for the postcorrection. The model consists of a static term that is dependent on the ADC output code and a dynamic term that has an additional dependence on the input frequency. The concept of ADC digital output post-correction by INL is first introduced. The INL model is subtracted from the digital output for postcorrection. The static compensation part is made by adjacent sets of gains and offsets, where each set corrects a range of output codes. The dynamic information, i.e., the frequency dependence of the INL dynamic component is used to construct a set of filter blocks that performs ADC compensation in the time domain. The compensation scheme is applied to measured data of two ADCs of the same type (Analog Devices AD9430). Performance improvements in terms of spurious-free dynamic range (SFDR), signal-to-noise and distortion ratio (SINAD), intermodulation distortion (IMD) and noise are obtained. The dynamic compensation part, due to its frequency dependence, can be generalized; hence, a post-correction block model can be used for compensating multiple ADCs of the same type.

*Index Terms*— Radio frequency systems, analog-digital conversion, integral nonlinearity, dynamic modeling, post-correction.

# I. INTRODUCTION

Error correction is a crucial task in a wireless digital communication system. Correction schemes are present in all layers of the open system interconnection (OSI) model. In this work, we consider errors caused by the hardware, or, more specifically, errors induced by the analog-digital converter (ADC). ADCs are ubiquitous in the receiver chains of communications systems, and faster devices with higher resolution are always in demand.

Modern communication system receivers consist mainly of an antenna at the radio frequency (RF) front-end followed by a preselection RF filter, a low-noise amplifier plus a frequency down-converting stage prior to the in-phase and quadraturephase branches. Each branch has an ADC at its periphery, which feeds data to the digital signal processing (DSP) blocks. Because contemporary and future telecommunications systems enjoy a substantial increase in data rate relative to the data rates of earlier systems, the digital signal processing is now

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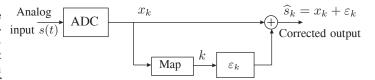


Fig. 1. Static ADC post-correction employing a look-up-table approach.

performed at a higher rate and covers a wider bandwidth. The ADC performance is crucial due to its position at the input of the DSP block. Thus, a potential error or distortion generated by the ADC propagates over the processing scheme, adding to the channel, DSP processing and RF block errors.

An appealing approach to boost the performance of a wireless communication system when its functioning is limited by the performance of the ADC is to apply ADC post-correction by DSP [1]. Using digital processing, we are able to boost the actual performance of the system without adding new hardware or modifying the existing one. There is a limited number of studies available that have investigated the influence of ADC imperfections on the link level performance [2], [3]. In [2], the ADC resolution was found to have a significant effect on the link-level bit-error rate of a wireless multiple-input/multiple-output (MIMO) system. It was shown in [3] that sigma-delta ADCs are more robust than pulse code modulation converters in terms of bit error rate in an orthogonal frequency-division multiplexing (OFDM) system.

The typical ADC structure in RF applications is the pipelined, or subranging, structure [4]. The pipelined ADC comprises several pipelined blocks and a flash ADC at the end. The input signal goes through the subsequent stages where each resolves a fraction of the output code. Each stage outputs a fraction of the ADC output code and a residual that is amplified prior to being fed to the next stage. The residual is the difference between the analog signal at the stage input and its quantized value. Thus, at every clock cycle, each stage resolves the subsequent signal sample, which is the reason behind the high processing speed of the pipeline ADCs (reaching a sampling frequency of 2.5 GHz [5]; See also [6]). The flash ADC at the end converts the least significant bits of the ADC output code.

ADC impairments can be compensated using an in-chip approach by modifying some of the ADC building blocks. Another method is digital post-correction, where the ADC output is compensated for by adding correction values that depend on the ADC output characteristics. Post-correction is

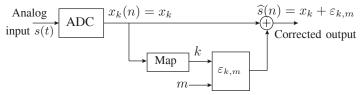


Fig. 2. Dynamic ADC post-correction, where m is an additional parameter addressing the look-up-table. The index m can designate the frequency, slope or previous sample(s) of the ADC output.

done by adding a block at the ADC output through a feedforward loop, as illustrated in Figs. 1 and 2.

A widely used ADC compensation method is the look-up-table (LUT) [7]–[10]. Post-correction using a LUT has been tackled by two basic approaches: static and dynamic correction. The static approach comprises a compensation block that adds a correction term  $\varepsilon_k$  for every ADC output code k, as shown in Fig. 1. However, the ADC performance shows a dependence on input signal characteristics, such as slope and frequency. Thus, a dynamic post-correction in which the compensation term is taken from a multidimensional table can provide enhanced performance. In addition to the code k, the input to such a table may include frequency, slope or previous sample(s). These additional features of the ADC output are denoted by m in Fig. 2.

In [7], a phase-plane LUT approach to correct a subranging and a flash ADC was adopted. The two-dimensional correction table was addressed by the code k and the slope (indicated by m in Fig. 2). ADC performance improvements occurred especially at frequencies near the calibration frequency. In [7], the spurious-free dynamic range (SFDR) improvement ranged from 4 to 14 dB. Smaller improvements were encountered at frequencies distant from the frequency employed for calibration. The compensation scheme in [7] was replaced in [8] by the state-space method, where, referring to the scheme of Fig. 2, the correction table is addressed by the current code k(n) and the previous one m = k(n-1), where n denotes the running time index. Improved results were obtained when three calibration frequencies (instead of one) were used to calculate the LUT entries.

An attempt to avoid real-time estimation of the slope information as in [7], was through the use of adjacent channel sampling [9]. The delay applied on the adjacent channel was optimized to achieve the best possible least mean square estimate of the input slope. A second similar ADC was used to quantize the adjacent channel signal. The experimental results showed the need for two calibration frequencies to achieve a positive SFDR compensation over the entire Nyquist bandwidth.

Static post-correction using LUT was performed on a pipeline ADC in [10]. The best SFDR improvements occurred near the calibration frequencies. In [11], a state-space post-correction was implemented to take into account the slope and frequency dependence of the error. Results showed that using a dynamic post-correction with a limited number of resolution bits achieves an improved compensation over that of the static correction previously done in [10], given a fixed

corrected output samples in combination with a bit-reduction scheme to derive the correcting term in a multi-dimensional LUT. In [12], a mathematical analysis tool was investigated to optimize the correction term bit-resolution and the number of delayed K samples for two different criteria: total harmonic distortion (THD) and signal to noise and distortion ratio (SINAD).

LUT-based ADC post-correction enables effective ADC error compensation. However, LUTs are memory-expensive, so multi-dimensional tables for high-resolution ADCs are not feasible to implement. As an alternative to dynamic LUT approaches for ADC correction, methods based on linear filtering of the ADC output have been proposed in the literature. A model composed of a set of parallel Hammerstein filters, in combination with linear regressors, was used for postcorrection in [13], based on the integral nonlinearity (INL) model in [14], which was divided into two parts: a dynamic low code frequency component (LCF) and a static high code frequency component (HCF). The quantities LCF and HCF were first introduced in [15]. The dynamic LCF component was constructed by a set of parallel Hammerstein time domain filters, and the static HCF segments were computed by linear gain regressors [13]. Theoretical THD, SINAD, SFDR and SNR improvements were also computed in [13].

Another method in ADC post-correction is model inversion. The two used models are Volterra and Wiener. The basic method is composed of: a) computation of the model or filter coefficients (Volterra filter kernels in case of the former approach); b) derivation of the inverse model to be used for compensation; and c) applying the correction scheme at the ADC output to obtain the compensated output. A theoretical investigation of the Volterra and Wiener models was done in [16] from the starting point of analyzing the jitter and distortion caused by an empirical sample-and-hold circuit. Fifth order Volterra and Wiener correction models were derived. The sampler distortion was removed using the postcorrection scheme composed of the 5th order inverse of the 5th order Volterra model. Also, it has been shown that the Volterra model can be derived from the Wiener model [16]. Volterra kernels were measured using a three tone input signal on a pipeline ADC in [17]. A frequency dependence was observed in the Volterra kernels and a parallel Hammerstein scheme was proposed for post-correction. In [18], the inverse Volterra filter coefficients were derived by the least squares (LS) method applied on an "ideal" 12-bit pipeline ADC where a controlled INL is added to. The INL was generated by an amplifier used in the feedback loop of the ADC. Significant improvement in terms of signal-to-noise ratio (SNR) was achieved [18].

In this work, a model-based approach for ADC postcorrection is developed based on dynamic INL models. The INL is modeled with respect to the code k and the frequency  $f_m$  (represented by the integer m). The main advantage of this approach over an LUT is that it requires significantly less parameter storage than does a traditional LUT. The dynamic error compensation is implemented in terms of linear time-invariant filters and static nonlinearities. The work relies on INL models presented and characterized in [19]. The objective of this paper is to derive a proper post-correction scheme

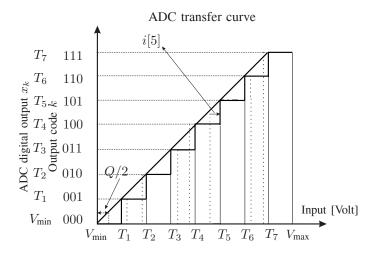


Fig. 3. Ideal (solid line) and practical (dashed line) 3-bit mid-riser ADC transfer curve. The practical ADC is compensated for gain and offset errors. The ideal transition levels  $T_k$  coincide with the solid vertical lines, whereas, the practical transition levels T[k] (not shown for ease of presentation) coincide with the dashed lines.

based on the available models and to show that it results in performance improvement when applied to a commercial pipeline ADC working at RF. In brief, this paper derives a scheme for dynamic post-correction for pipelined ADCs based on a two-dimensional INL model. The post-correction procedure is implemented in software and is used to process ADC data collected by a state-of-the art test-bed [20]. The paper is organized as follows: Sec. II describes the INL entity including an outline about its modeling and estimation. Sec. III presents the concept of ADC INL parameter correction; furthermore, it details the post-correction schemes based on the INL model. The experimental results employing two pipeline ADCs (AD9430) are discussed in Sec. IV. Sec. V concludes the work.

# II. DYNAMIC INL MODELING

The ideal  $T_k$  and practical T[k] code transition levels (in [Volt]) of an ADC are illustrated in Fig. 3. The ideal transition level can be written in terms of the output code k of the ADC, as [21]

$$T_k = Q(k-1) + T_1$$
 [Volt]

where Q [Volt] is the ideal width of a code bin that can be taken as the ratio of the full-scale range of the ADC over the total number of codes, i.e.,  $Q = (V_{\rm max} - V_{\rm min})/2^N$ . The integer N denotes the number of bits of the ADC. Furthermore,  $T_1$  denotes the first transition level of an ideal ADC and is equal to  $V_{\rm min} + Q$  for the 'mid-riser' convention or  $V_{\rm min} + Q/2$  for the 'mid-tread' convention [21]. For a practical ADC subject to a gain G and offset  $V_{\rm os}$ , the INL i[k] is defined as [21]; (see also [22], [23])

$$i[k] = \frac{T_k - GT[k] - V_{\text{os}}}{Q}$$
 [LSB]. (2)

The INL in (2) is expressed in least significant bits (LSBs). The gain and offset can be computed by different procedures as

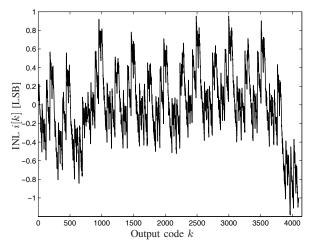


Fig. 4. Averaged INL for a 12-bit pipelined ADC based on 15 sequences corresponding to test frequencies in the interval 30-90 MHz [19].

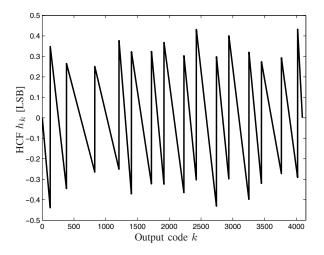


Fig. 5. Estimated static HCF model for the 12-bit 210 MSPS AD9430.

given in [23]. An example INL sequence of a 12-bit pipelined ADC (that is, the AD9430) is shown in Fig. 4.

In [19], the measured INL was described by a parametric model  $i_{m,k}$ , where m corresponds to the test frequency (that is,  $f_m$  in Hz) and k to the ADC output code:

$$i_{m,k} = h_k + \ell_{m,k} \,. \tag{3}$$

The term  $h_k$  is the HCF component, and  $\ell_{m,k}$  is the dynamic LCF component.

The HCF component  $h_k$  is modeled by a set of P disjoint segments centered around zero, whereas the LCF is modeled by a smooth polynomial over the code range for every frequency under test. The HCF model can be written as [19]:

$$h_k \stackrel{\triangle}{=} h_{k,p} = \eta_p \, k + \beta_p \tag{4}$$

for an output code k belonging to the segment p, where  $p=1,\ldots,P$ . In (4),  $\eta_p$  is the slope of the segment p and  $\beta_p$  is an offset. In Fig. 5, an example extracted HCF model is shown.

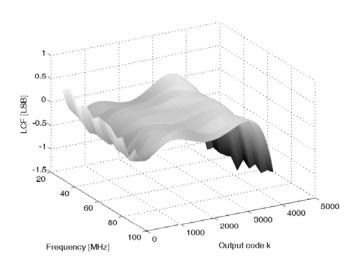


Fig. 6. Estimated LCF model for frequencies between 30 and 90 MHz of the 12-bit 210 MSPS AD9430.

The LCF component is modeled as an L:th-order polynomial [19];

$$\ell_{m,k} = \theta_{0,m} + \bar{k} \, \theta_{1,m} + \ldots + \bar{k}^l \, \theta_{l,m} + \ldots + \bar{k}^L \, \theta_{L,m} \,,$$
 (5)

for a given input frequency  $f_m$ , where  $m=1,\ldots,M$ . Furthermore,  $\bar{k}=(k-2^{N-1})/(2^{N-1}-1)$  is a normalized ADC output code introduced to ensure numerical robustness [19]. An example LCF model is shown in Fig 6.

The model (3)-(5) is linear in the parameters. Accordingly, the unknown parameters may be obtained by a least-squares fit of the measured INL data [19]. This approach is an efficient way to compress the information regarding the INL for effective implementation of post-correction schemes.

## III. INL-BASED POST-CORRECTION

The compensation method is derived from the dynamic INL model presented in the previous section. The post-correction scheme is composed of two components: a static remapping of the ADC output and a filter structure composed of linear time-invariant filters and static nonlinearities. The setup is shown in Fig. 7.

#### A. INL-Based Post-Correction

The endpoint representation for the ADC output is used in this section. A static INL is used for illustrating the post-correction concept prior to generalizing the compensation procedure to dynamic correction. The transition levels of an ideal and a practical ADC (compensated for gain and offset) are illustrated in Fig. 3. Despite having transition levels that deviate from the ideal ones, the digital output of a practical ADC cannot be distinguished from the corresponding output of an ideal ADC. Let the ADC digital output be represented by the transition levels  $T_k$ , that is,

$$x_k = T_k. (6)$$

Then, from (2)

$$x_k = GT[k] + V_{os} + Qi[k].$$
 (7)

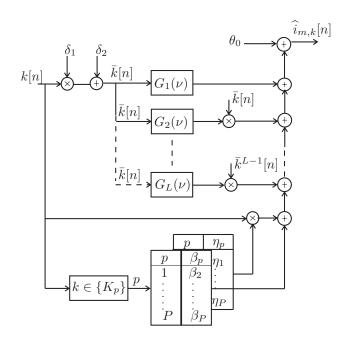


Fig. 7. ADC post-correction block with ADC code k[n], as input.  $\delta_1$  and  $\delta_2$  are defined as  $\delta_1 = 1/(2^{N-1}-1)$  and  $\delta_2 = -2^{N-1}/(2^{N-1}-1)$ . The ADC output code k is indexed by n to indicate its time dependence. The output is the correction term  $\hat{i}_{m,k}[n]$ .

With an endpoint representation, a practical ADC outputs  $T_k$  corresponding to the transition level T[k]. Then, the ADC output  $x_k$  is remapped to the corrected output  $\widehat{s}_k = x_k + \varepsilon_k$  according to Fig. 1, where  $\varepsilon_k$  is to be determined from

$$\widehat{s}_k = T[k]. \tag{8}$$

Inserting (8) into (7), a rearrangement of terms yields

$$\widehat{s}_k = \frac{1}{G}(x_k - V_{\text{os}} - Qi[k]). \tag{9}$$

The gain G and offset  $V_{\rm os}$  do not influence the dynamic properties of the output. Accordingly, the correction term is given by

$$\varepsilon_k = -Q\,i[k]\,. \tag{10}$$

The correction in (10) is valid for a specific frequency corresponding to the frequency of the ADC stimuli during the INL characterization. Formally, we may distinguish the outcome of different stimuli by adding the integer m corresponding to frequency  $f_m$  Hz. In such a case, the static i[k] in the LUT in (10) is in turn replaced by the 2-dimensional i[m,k], where  $m=1,\ldots,M$  and  $k=1,\ldots,N$ . The applied model-based approach implies that the LUT i[m,k] is replaced by a parametric model  $\widehat{i}_{m,k}$ , where "^" is used to denote the least-squares estimated model based on the structure  $i_{m,k}$  in (3), that is,

$$\varepsilon_{k,m} = -Q \,\widehat{h}_k - Q \,\widehat{\ell}_{m,k} \,. \tag{11}$$

The first term in (11) is a static post-correction, whereas the second term depends on the frequency characteristics of the analog input.

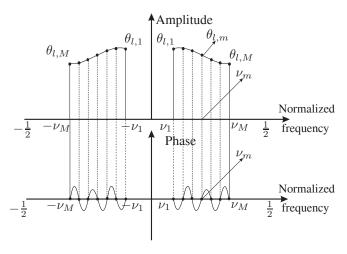


Fig. 8. Frequency response of the designed filter for post-correction, where the response for the negative frequencies is mirrored.

#### B. HCF Post-Correction

The P centered HCF segments mimic the INL behavior that endures disjoint abrupt changes and are used for a direct remapping of the ADC output. The post-correction is illustrated in Fig. 7. The static compensation term derived from the HCF model is given by  $\hat{h}_k$  in (4), that is,

$$\widehat{h}_k = \widehat{\eta}_p \, k + \beta_p \qquad k_{p-1} \le k < k_p \tag{12}$$

where  $\beta_p$  is a known offset,  $\beta_p=-\widehat{\eta}_p(k_p+k_{p-1}-1)/2$ , and  $k_p$  are the segments borders,  $p=1,\ldots,P$  [19].

#### C. LCF Post-Correction

The LCF model is composed of a set of polynomials, each of which represents measured LCF data for a certain frequency  $f_m$  in the bandwidth under test. Thus, for a sine wave input with frequency  $f_m$ , the LCF model is presented as in (5). Examining (5), one can note that an instantaneous (normalized) ADC code  $\bar{k}$  and its powers  $\bar{k}^l$  are weighted by a frequency-dependent factor  $\theta_{l,m}$ . In other words, the output code  $\bar{k}^l$  contributes with a factor of  $\theta_{l,m}$ , where the factor depends on the ADC input. Thus, for a given ADC output code  $\bar{k}$ , the entity  $\theta_{l,m}$  can be considered as sampled points of a filter frequency response  $G_l(\nu)$ . The frequency function  $G_l(\nu)$  can be written as

$$G_l(\nu_m) = \theta_{l,m}$$
 where  $\nu_m = \frac{2\pi f_m}{f_s}$ , (13)

where  $\theta_{l,m}$  are real valued quantities and  $f_s$  is the sampling frequency. See Fig. 8 for an illustration. The ADC post-correction is performed in the time domain by linear filtering of the ADC normalized output  $\bar{k}$ . The output of the filter is multiplied by  $\bar{k}^{l-1}$ . Thus, we need to derive the time response of the filters  $G_l(\nu)$  from their respective frequency responses given by (13). The considered frequency response  $\theta_{0,m}$  for  $m=1,\ldots,M$ , is a set of offsets, each corresponding to a given frequency  $f_m$ . For a practical implementation, the set of LCF polynomials is accordingly transformed into a set having

a common offset  $\theta_0$ ; see Fig. 7. The new polynomial coefficients are derived from the old ones by the method of least-squares. For simplicity of notation, the adjusted polynomial coefficients are still designated as  $\theta_0$  and  $\theta_{l,m}$ .

The time domain pulse response of  $G_l(\nu)$  can be computed by the inverse Fourier transform based on the samples in (13). An adequate method to compute the filter coefficients from the sampled frequency response is to use the inverse fast Fourier transform (IFFT) [24]–[26]. We will not go into detail on the design of the LCF filters. Simply, the concept entails designing a filter based on a specification in the frequency domain. Different approaches can be found in textbooks on this topic [24]–[26]. To continue, denoting the resulting pulse response by  $g_l[n]$  for  $l=1,\ldots,L$ , the dynamic post-correction term  $-Q \hat{l}_{m,k}$  in (11) is given by

$$-Q \theta_0 - Q \sum_{l=1}^{L} (g_l[n] * \bar{k}[n]) \bar{k}^{l-1}[n], \qquad (14)$$

where \* denotes convolution.

One may note that in the case where the LCF data is modeled by a static polynomial, the set of equations (5) reduces to

$$l_k = \theta_0 + \bar{k}\,\theta_1 + \ldots + \bar{k}^l\,\theta_l + \ldots + \bar{k}^L\,\theta_L. \tag{15}$$

In this case, the compensation in terms of linear filters is replaced by a multiplication.

#### IV. EXPERIMENTAL VALIDATION

## A. Test set-up and device under test

The INL has been characterized over a 60 MHz wide frequency band ranging from 30 to 90 MHz for two samples from the Analog Devices AD9430. The ADC output sequences are collected for specific input frequencies spanning the bandwidth with a frequency step of 5 MHz. The two ADC samples are referred to as ADC1 and ADC2. The employed ADC test setup for INL testing is described in [19]. ADC data for INL characterization and for evaluation of the post-correction method were collected, where the frequencies are fine-tuned to fulfill the conditions for coherent sampling [21]. For the INL measurements, the ADC input is slightly overdriven according to [21] whereas the data used for post-correction is measured at -0.5 dBFS. Information about the test bed in general can be found in [20]. The estimated HCF and LCF models for ADC2 were shown in Figs. 5-6. The complete INL model is shown in Fig. 9. The 104-parameter LCF model is shown in Fig. 6; that is, L=7 and M=13. The P=16 segments HCF model is sketched in Fig. 5. Fig. 9 combines the static HCF and dynamic LCF in the representation of the complete INL. The parameters used for post-correction are calculated once for each ADC, out of its INL model as indicated in Sec. III. The obtained correction models corresponding to ADC1 and ADC2 are used throughout the work. A question of importance is ADC aging. We have not encountered any aging effects. One may note that ADC1 is a several years older sample than ADC2. Aging and temperature sensitivity in general are not investigated in this paper. More details on the temperature dependence of post-correction are found in [27].

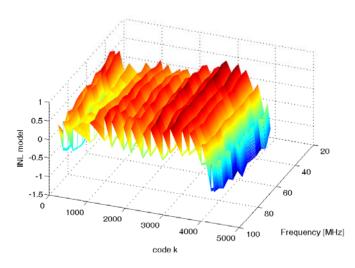


Fig. 9. Estimated INL model for frequencies between 30 and 90 MHz of the 12-bit 210 MSPS AD9430.

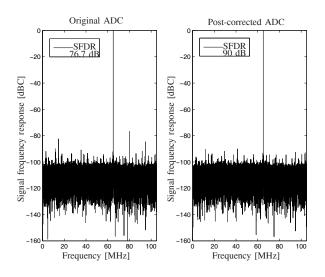


Fig. 10. SFDR improvement of a 65-MHz signal sequence.

Different figures of merit are used to characterize the behavior of an ADC and its post-corrected counterpart. Among them are INL, SFDR, SINAD, noise, intermodulation distortion (IMD), THD or effective number of bits (ENOB) – we refer to [21] and [23] for definitions and procedures for their characterization. In wideband systems, the SFDR, SINAD, noise and IMD of an ADC are the crucial parameters [21]. These parameters are considered here.

## B. SFDR Improvement

The post-correction scheme was evaluated for single-tone input signals spanning the bandwidth of use. As an illustration, the SFDR improvement for a 65 MHz signal sequence is shown in Fig. 10. A 13 dB SFDR improvement is achieved whereas all harmonics are cancelled and the spurious peaks are diminished to the noise level.

Fig. 11 summarizes the improvements in terms of SFDR for ADC1 and ADC2. Three methods are used to compensate

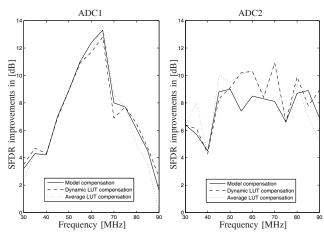


Fig. 11. SFDR improvement for ADC1 and ADC2 over the band of use.

the ADCs: the developed INL model according to Fig. 7; a static compensation based on averaged INL data over the 30-90 MHz band (consisting of a LUT of  $2^N-1=4095\ i[k]$  entries); and the INL sequence for every input frequency (self-calibration or a LUT of  $13\times(2^N-1)=53235\ i[m,k]$  entries). Both ADCs undergo significant improvements in SFDR over the band of use. However, the dissimilarity between the model compensation and the LUT differs for the two ADCs.

Considering ADC1, the INL model can perform an almost identical correction to the dynamic LUT. The model outperforms the self-calibration for some singular frequencies by an order of 0.5 to 1 dB. Self-calibration is superior by 1 dB at the 90 MHz frequency. One can explain this by the fact that the INL at high frequencies is quite noisy; thus, the model cannot grasp some of the INL information, as shown in [19]. Model compensation is constantly superior to the static LUT compensation (except at 65 and 70 MHz), although it consists of significantly fewer parameters (120 and 4095 parameters for the model and static LUT, respectively).

Referring to the similarity in performance between the model correction and the dynamic LUT, we can claim that the post-correction block based on the INL model is reconstructing the INL prior to the compensation. Another observation from Fig. 11 is that the INL model compensation capabilities strongly depend on frequency (especially for ADC1). Referring to Fig. 10 and Fig. 12, one may note that the INL model allows a reduction of harmonics and spurious amplitudes (to some extent) for some frequencies (65 MHz for example) whereas it represents them modestly for other frequencies (30 MHz, for example). In other words, the INL compensation has a dissimilar impact on the harmonics and the spurious peaks at different frequencies.

ADC2 did not encounter the higher improvements of ADC1; however, it shows more consistent improvements over the entire bandwidth. One can deduce when comparing the results of the two ADCs that ADC2 is subject to a more uniform improvement (above 4 dB) because its static HCF is more pronounced [19]. However, the difference in performance between the LUT and the model-based approach is larger when

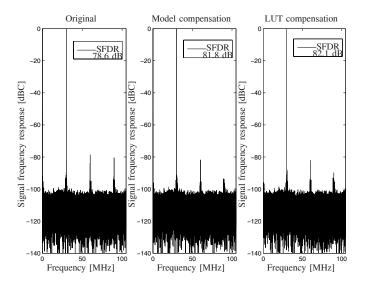


Fig. 12. SFDR improvement for the 30-MHz output sequence of ADC1 using model and LUT methods.

compared to ADC1. Referring to [19], the model was not able to mimic the INL as well as for ADC1, which is due to the noisier INL of ADC2. Moreover, the static part of ADC2's INL is more pronounced than that of ADC1, but the model is mostly comprised of dynamic parameters.

## C. SINAD and Noise Improvements

SINAD is given as the ratio of the root mean square (rms) value of the signal to the rms of the noise and distortion [23]

$$SINAD = 20 \log_{10} \frac{A}{\sqrt{2}P_{MD}}, \qquad (16)$$

where A is the amplitude of the signal and  $P_{\scriptscriptstyle{\mathrm{NAD}}}$  is the rms error

$$P_{\text{NAD}} = \left(\frac{1}{N_s} \sum_{n=0}^{N_s - 1} (x(n) - \tilde{s}(n))^2\right)^{\frac{1}{2}}.$$
 (17)

Here, x(n) is the measured signal sequence,  $\tilde{s}(n)$  is the sine wave fitted to x(n), and  $N_s$  denotes the number of samples.

A theoretical analysis of possible SINAD improvements of the AD9430 was presented in [28] based on a mean square error correction (MSE); i.e., correction values were computed by minimizing the MSE between the ADC output and an ideal sine wave. In [28], it was found that the maximum improvement that can be achieved is 0.7 dB for a postcorrection scheme using an LUT with infinite precision.

Using the proposed model-based correction, ADC1 presented improvements between 0.1 and 0.2 dB in the band of interest. Improvements for ADC2 spanned from 0.3 to 0.5 dB over the bandwidth. The dynamic LUT approach achieved 0.2 to 0.3 dB improvements for ADC1, and 0.4 to 0.7 dB for ADC2.

The noise power for all ADC output data was calculated by removing the harmonics [21] from the ADCs output data spectrum. It is hinted from the SINAD improvements (both theoretically and experimentally obtained) that the noise level

#### TABLE I

ADC IMD IMPROVEMENTS IN DB. THE TABLE ENTRIES '-' DESIGNATE
WHEN THE IMD PRODUCTS ARE BELOW THE NOISE LEVEL. THE
DOMINANT IMD PRODUCT AFTER POST-CORRECTION IS INDICATED BY A
STAR

ADC	$f_1 \& f_2$ [MHz]	$f_1 + f_2$	$f_2 - f_1$	$2f_1 - f_2$	$2f_2 - f_1$
ADC1	28.3 & 29.3	8.2	6.7	0.1*	-1.4
ADC1	60.0 & 65.0	7.0	5.5*	-	-
ADC2	28.3 & 29.3	5.4	-0.1	0.6	1.1*
ADC2	60.0 & 65.0	-	-	-	-

TABLE II
IN-BETWEEN AND OUT-OF-BAND SFDR IMPROVEMENTS.

	ADC1	ADC2		
f [MHz]	Improvement dB	f [MHz]	Improvement dB	
20	5.5	20	8.2	
25	3.2	25	6.0	
52	9.1	64	7.1	
95	-0.5	95	5.7	

cannot be decreased by more than 0.5 dB. ADC2 had improvements of 0.2-0.3 dB with the INL-model-based compensation scheme and up to 0.4 dB with the LUT method, whereas ADC1 had more modest improvements in the order of 0.04 dB for both methods.

#### D. IMD Improvements

The IMD for both ADCs was measured for a two-tone input with  $f_1 = 28.3$  and  $f_2 = 29.3$  MHz at -7.0 dBFS. The INL data was not characterized for frequencies below 30MHz; thus, the filter frequency response [refer to (13)] was not available at this frequency range. Hence, the frequency response in disposition (between 30 to 90 MHz) was extrapolated to those frequencies and down to the DC level, prior to the IFFT process. An additional two tone signal with input frequencies  $f_1 = 60$  and  $f_2 = 65$  MHz at -7.0 dBFS was also used. The improvements for the IMD are summarized in Tab. I, where they are listed for the different IMD product orders. According to the AD9430 datasheet, the IMD ratio is defined for the highest third IMD product (i.e.  $2 f_1 - f_2$  and  $2 f_2 - f_1$ ). The dominant IMD product is indicated by a star in the table. For the first two-tone signal, the largest third intermodulation peak happens to be at  $2 f_1 - f_2$ . For the two-tone test with 60 and 65 MHz, the third-order intermodulation products were below the noise level for ADC1. Therefore, the star points at the dominant second-order IMD product. ADC2 had all its second- and third-order intermodulation products below noise level for the 60 and 65 MHz input, and are thus not listed in the table.

The third IMD products are the most important ones because they lie near the two-tone input; thus, the method works to reduce the IMD. However, the second IMD  $f_1 + f_2$  was most attenuated by the post-correction method (up to 8.2 dB).

## E. In-Between and Out-of-Band Performance

ADC1 and ADC2 have been post-corrected for in-band frequencies (between 30 to 90 MHz) not coinciding with the

frequencies used for INL characterization and for out-of-band frequencies. The improvement results are reported in Tab. II.

The in-between improvements for ADC1 and ADC2 lies between the improvements at characterized frequencies (i.e., the 5 MHz separated frequencies used for INL characterization). ADC2 had positive improvements for the out-of-band frequencies compensated (see Tab. II).

ADC1 had positive out-of-band improvement results except for the the 95 MHz input frequency (-0.5 dB); however, negative results are encountered if the 95 MHz sequence is compensated by the ADC1 mean INL data (average LUT method) and ADC1 90 MHz INL sequence (the negative improvements are -2.3 and -0.1 dB). This result is not surprising because the model is extrapolated at these frequencies; the compensations (model and the LUTs) are poor at the end frequencies where the improvement curve has a downward trend. Obviously the INL data (30 to 90 MHz), and consequently its model, has no similar features with the 95 MHz INL sequence. Measured frequencies below 30 MHz were not available for ADC1; instead, we post-corrected ADC2 at 20 and 25 MHz by the filters' block of ADC1 (cross-compensation).

One can deduce from the results that the method is useful for post-correction and also for ADC inputs not belonging to the training set. This is further shown below.

### F. Input Level Performance

Here, SFDR improvements are investigated with respect to the input power level for the 45 and 47 MHz frequencies using ADC2. The performance at 45 MHz was measured at -4, -5 and -10 dBFS and the obtained improvements in terms of SFDR were 2.3, 4.0 and 4.9 dB, respectively. In addition, the performance for the between-band 47 MHz signal was measured for input levels of -5, -10, and -15 dBFS, where the improvements were 0.2, 4.2 and 2.7 dB, respectively. The ADC still encounters improvements for amplitudes significantly below the nominal operation level despite the fact that the correction method is derived based on full scale inputs. Improvement figures also hold for the in-band frequencies (47 MHz).

## G. Post-Correction with Cross-Validation of the Results

One observation is that the LCF part of the INL is quite similar (in structure and magnitude) in the two ADCs. To illustrate that the correction scheme is valid for several ADCs of the same type, a cross-ADC compensation was performed; that is, ADC1 was corrected using the ADC2 correction block and vice versa. Fig. 13 shows the results of such a crosscorrection compared to the self-compensation, as well as an additional curve where each of the ADCs is compensated by only the LCF model or filters' block of the second ADC. The cross-compensation achieves improvements over the entire band, although they are inferior to those of the selfcorrection. However, the performance of the filter based crosscompensation is quite similar to self-compensation except for some given frequencies. The high improvements encountered by ADC1 at the middle band frequencies are reduced by the ADC2 filters' scheme that, unlike the ADC1 filters' block,

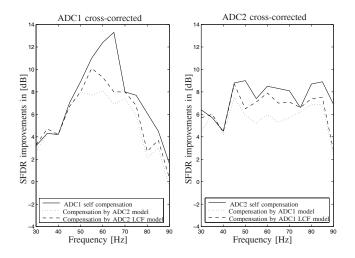


Fig. 13. ADC1 and ADC2 cross-compensation.

does not favor this frequency range. The improvements of ADC2 drop at frequencies near the edge due to the ADC1 filters' scheme (or equivalently the ADC1 LCF model) modest improvements at this range.

Cross-correction by the LCF block is uniformly better than the full cross-correction because the HCF segments are tailored for every ADC. It can occasionally outperform the self-correction. Thus, the frequency dependence of the LCF can be used for cross-ADC correction or for developing a general post-correction scheme.

#### V. CONCLUSIONS

The concept of ADC model-based post-correction based on the INL-model introduced in [19] proved to be a reliable method while presenting low complexity. The developed INL-model-based post-correction method showed similar performance to a dynamic LUT approach.

INL modeling with respect to the frequency of the ADC stimuli (in addition to the ADC output code k) proved to be a versatile tool because the implicit frequency information can be used for developing a post-correction based on linear filtering of the ADC output. The filters demonstrated their capability to reconstruct the INL information. Such a filter approach is preferable to an LUT in the sense that it requires the storage of significantly fewer parameters and needs no additional interpolations or approximations to compensate for input signals that differ from calibration frequencies.

# REFERENCES

- E. Balestrieri, P. Daponte, and S. Rapuano, "A state of the art on ADC error compensation methods," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 4, pp. 1388-1394, August 2005.
- [2] H. Lundin, P. Svedman, X. Zhang, M. Skoglund, P. Händel and P. Zetterberg, "ADC imperfections in multiple antenna wireless systems—an experimental study," 9th European Workshop on ADC Modeling and Testing, Athens, Greece, pp. 808–813, 2004.
- [3] A. Moschitta, D. Petri, "Effects of ADC integral non-linearity on digital transmission," 4th International Conference on Advanced A/D and D/A Conversion Techniques and Their Applications & 7th Europeen Workshop on ADC Modeling and Testing, Prague, Czech Republic, June 26-28, 2002.

- [4] W. Kester, "Analog-Digital Conversion," United States of America: Analog Devices, 2004.
- [5] K.M. Mukund, S. Seshadri, J. Devarajulu, M. Kannan, "A 1 GHz pipelined low power floating point arithmetic unit with modified scheduling for high speed applications," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 377-381, June 2007.
- [6] B. Murmann, "ADC Performance Survey 1997-2010," [Online]. Available: http://www.stanford.edu/murmann/adcsurvey.html
- [7] T. A. Rebold and F. H. Irons, "A phase-plane approach to the compensation of high-speed analog-to-digital converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, 1987, pp. 455-458.
- [8] F. H. Irons, D. M. Hummels, and S. P. Kennedy, "Improved compensation for analog-to-digital converters," *IEEE Trans. Circuits Syst.*, vol. 38, no. 8, pp. 958-961, Aug. 1991.
- [9] D. M. Hummels, F. H. Irons, and S. P. Kennedy, "Using adjacent sampling for error correcting analog-to-digital converter", in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, 1992, pp. 589-592.
- [10] P. Händel, M. Skoglund, and M. Pettersson, "A calibration scheme for imperfect quantizers," *IEEE Trans. Instrum. Meas.*, vol. 49, no. 5, pp. 1063-1068, Oct. 2000.
- [11] H. Lundin, M. Skoglund, and P. Händel, "A criterion for optimizing bitreduced post-correction of AD converters," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 4, pp. 1159-1166, Aug. 2004.
- [12] H. Lundin, M. Skoglund, and P. Händel, "Optimal index-bit allocation for dynamic post-correction of analog-to-digital converters," *IEEE Trans. Signal Process.*, vol. 53, no. 2, pp. 660-671, Feb. 2005.
- [13] N. Björsell and P. Händel, "Achievable ADC performance by postcorrection utilizing dynamic modeling of the integral nonlinearity," EURASIP Journal on Advances in Signal Proces, vol. 2008, Article ID 497187, 10 pages, 2008. doi:10.1155/2008/497187.
- [14] P. Händel, N. Björsell and M. Jansson, "Model based dynamic characterization of analog-digital-converters at radio frequency—Invited paper," International Conference on Signal Processing and its Applications, February 12-15 2007, Sharjah, UAE.
- [15] L. Michaeli, P. Michalko, J. Saliga, "Unified ADC nonlinearity error model for SAR ADC," *Measurement*, Vol. 41, Issue 2, pp. 198-204, February 2008.
- [16] J. Tsimbinos and K. V. Lever, "Applications of higher order statistics to modeling, identification and cancellation of nonlinear distortion in highspeed samplers and analogue-to-digital converters using the Volterra and Wiener models," in Proc. IEEE Signal Processing Workshop Higher-Order Statistics, Jun. 1993, pp. 379-383.
- [17] N. Björsell, P. Suchanek, P. Händel and D. Rönnow, "Measuring the Volterra kernels of analog to digital converters using a stepped threetone scan," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 4, pp. 666-671, April 2008.
- [18] P. Mikulik and J. Saliga, "Volterra filtering for integrating ADC error correction, based on an a priori error model," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 4, pp. 870-875, August 2002.
- [19] S. Medawar, P. Händel, N. Björsell and M. Jansson, "Input dependent integral nonlinearity modeling for pipelined analog-digital converters," *IEEE Trans. Instrum. Meas.*, in press, doi:10.1109/TIM.2010.2045551, 2010.
- [20] N. Björsell, O. Andersen, and P. Händel, "High dynamic range test-bed for characterization of analog-to-digital converters up to 500MSPS," 10th Workshop on ADC Modeling and Testing, Gdynia, Poland, pp. 601-604, 2005.
- [21] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Standard 1241-2000.
- [22] S. Rapuno, P. Daponte, E. Balestrieri, L. de Vito, S. J. Tilden, S. Max and J. Blair, "ADC parameters and characteristics part 6 in a series of tutorials in instrumentation and measurement," *IEEE Instrumentation & Measurement Magazine*, Vol. 8, No. 5, pp. 44–54, December 2005.
- [23] T.E. Linnenbrink, J. Blair, S. Rapuno, P. Daponte, E. Balestrieri, L. de Vito, S. Max and S. J. Tilden, "ADC testing – part 7 in a series of tutorials in instrumentation and measurement," *IEEE Instrumentation & Measurement Magazine*, Vol. 9, No. 2, pp. 39–49, April 2006.
- [24] A. V. Oppenheim and R. W. Schafer, *Digital Signal Processing*, United States of America: Alan V. Oppenheim and Bell Laboratories, 1975.
- [25] T. W. Parks, and C. S Burrus, *Digital Filter Design*, New York: John Wiley & Sons. 1987.
- [26] G. D'Antona and A. Ferrero, Digital Signal Processing for Measurement Systems, United States of America: Springer Science+Business Media, 2006.
- [27] V. Kerzérho, V. Fresnaud, D. Dallet, S. Bernard and L. Bossuet, "Fast digital post-processing technique for INL correction of ADC: validation on a 12-bit F&I ADC," *IEEE Trans. Instrum. Meas.*, submitted, 2010.

[28] H. Lundin, P. Händel, and M. Skoglund, "Bounds on the performance of analog-to-digital converter look-up table postcorrection," *Measurement*, vol. 42, pp. 1164-1175, March 2009.