Potential Design and Transport Property of 0.1-μm MOSFET with Asymmetric Channel Profile

Shinji Odanaka and Akira Hiroki

***Abstract*—This paper describes potential design and transport property of a 0.1-μm n-MOSFET with asymmetric channel profile, which is formed by the tilt-angle ion-implantation after gate electrode formation. The relation between device performance and transport property of the asymmetric 0.1-μm device is explored by Monte Carlo simulations and measured electrical characteristics. The self-consistent Monte Carlo device simulation coupled with a process simulator reveals higher electron velocity at the source end of the channel and velocity overshoot at the source side of the channel, and the smaller high-energy tail of the distribution in the drain. This transport property creates high drain current, large transconductance, and low substrate current of the 0.1-μm n-MOSFET with asymmetric channel profile.**

I. Introduction

MINIATURIZATION of MOSFET's into 0.1-μm regime is an attractive challenge to improve circuit performance and packing density in the future ULSI's. Recently, extensive experimental studies have been conducted on 0.1-μm MOSFET's [1]–[3]. Despite improvement in performance by device scaling, the future scaling of MOSFET's approaches the physical limits of fabrication processes and devices. In the 0.1-μm regime and below, however, the nonequilibrium carrier transport is expected to be one of significant physical phenomena which allows the device design of high performance MOSFET's. The velocity overshoot, that is, velocities above 10^7 cm/s in Si at room temperature, was observed in the form of the high transconductance measured in the 0.1-μm MOSFET [4]. The nonequilibrium transport properties in the 0.1-μm MOSFET have been investigated using a Monte Carlo solution of the Boltzmann transport equation coupled with the Poisson equation [5], [6]. In order to take full advantage of velocity overshoot, the importance of the electric field at the source end of the channel was suggested by using the numerical momentum- and energy-balance equations [7].

This paper describes potential design and transport property of a 0.1-μm n-MOSFET with asymmetric channel profile, which has been proposed to improve the performance of a MOSFET [8]. In quarter-micron regime asymmetric n-MOSFET device structures have been proposed to achieve high current drivability and hot-carrier reliability [9], [10]. Also, circuits applications of CMOS devices with asymmetric source/drain structure have been discussed [11]. In this work, the relation between device performance and transport property of the 0.1-μm n-MOSFET with asymmetric channel profile is explored by Monte Carlo device simulations and measured electrical characteristics. The self-consistent Monte Carlo device simulation coupled with a process simulator provides a means for improving device performance in the actual 0.1-μm MOSFET's. Section II describes a practical fabrication process and electrical characteristics of the 0.1-μm n-MOSFET with asymmetric channel profile. Section III discusses the lateral potential design and transport properties of the asymmetric device in order to realize high performance of the 0.1-μm n-MOSFET. In Section IV, performance and reliability results of the asymmetric device are discussed comparing with those of the conventional device.

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II. Fabrication Process and Electrical Characteristics

The conventional and asymmetric 0.1-μm n-MOSFET's were fabricated, having the gate oxide thickness of 4 nm and the height of the gate polysilicon of 200 nm. The processing sequence of the asymmetric device is the same as that of the conventional device expcept for the channel implant. The impurity concentration of devices was designed by using a process simulator "SMART-P" [12]. For the 0.15-μm gate length, the metallurgical channel length is estimated to be 0.09 μm. The conventional device has a uniform channel profile in the lateral direction and the 40 keV boron ions with a dose of 7.0×10^{12} cm^{-2} were implanted to adjust the threshold voltage before gate electrode formation. The simulated channel profile is obtained, with a surface boron concentration of 1.0×10^{17} cm^{-3} and a peak value of 5.0×10^{17} cm^{-3} at 0.1-μm below the Si-SiO_2 interface. The asymmetric channel profile is formed by the threshold adjustment implantation with appropriate orientation after gate electrode formation. For such a channel implant, the 80 keV BF_2 ions with a dose of 1.0×10^{13} cm^{-2} were implanted with a tilt-angle of 7°. Fig. 1 shows the lateral impurity profiles of the asymmetric device as a function of the channel implant energy. The surface boron concentration reaches 4×10^{17} cm^{-3} at the source end of the channel and the boron concentration is gradually reduced along the channel down to the order of 10^{16} cm^{-3} near the drain. As seen in Fig. 1, the asymmetry in the lateral channel profile becomes weak as the BF_2 implant energy decreases. The result indicates that the 80-keV BF_2 implantation generates an asymmetric channel profile in the 0.15-μm gate length. After gate electrode formation the arsenic ions with a dose of 1.0×10^{14} cm^{-2} were implanted at an energy of 10 keV to form the shallow source/drain extensions, which suppress

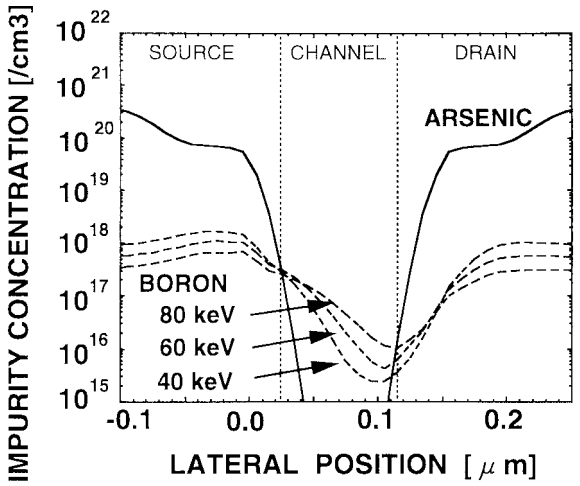

Fig. 1. Lateral impurity profiles of the asymmetric n-MOSFET's at the Si/SiO_2 interface as a function of the channel implant energy.

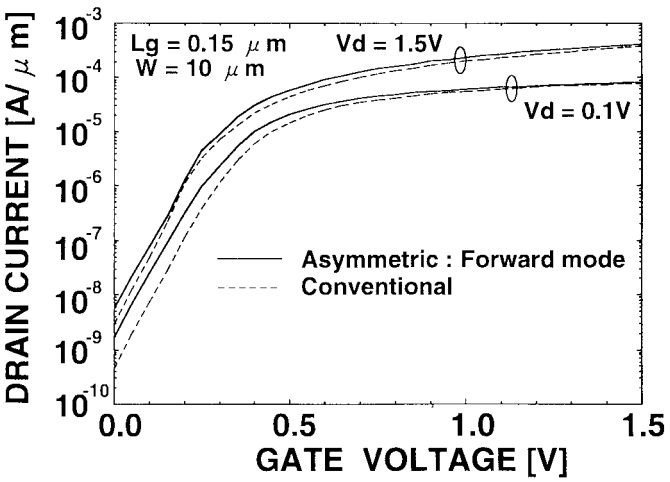

Fig. 3. Measured subthreshold characteristics for the asymmetric and conventional devices with the gate length of 0.15 μm.

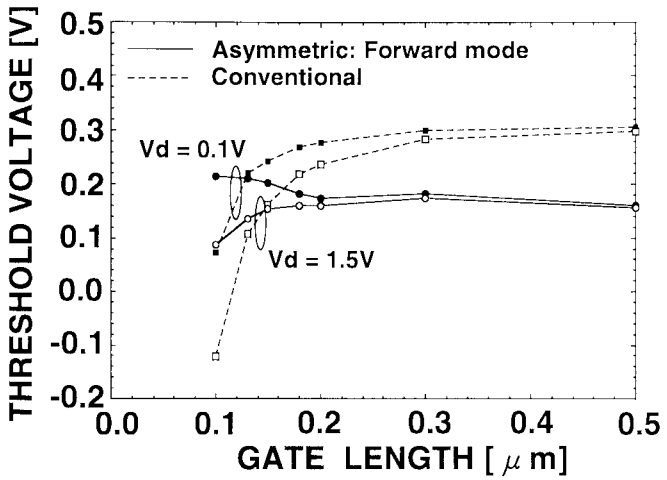

Fig. 2. Linear and saturation threshold voltages as a function of the gate length for the asymmetric and conventional n-MOSFET's.

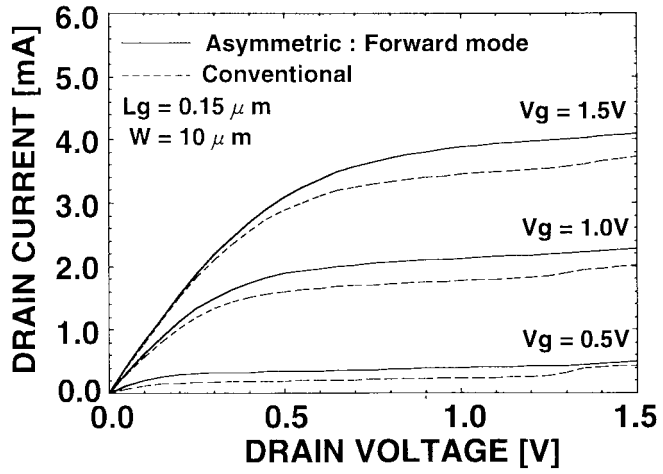

Fig. 4. Measured I–V characteristics of the asymmetric and conventional n-MOSFET's with the gate length of 0.15 μm. Both devices exhibit the same threshold voltage of 0.16 V at $V_{\rm DS} = 1.5$ V.

the short-channel effects, reducing the source/drain parasitic resistance. After sidewall formation at low temperature, the deep source/drain regions are formed with a high arsenic dose of 6×10^{15} cm^{-2} at an energy of 40 keV, followed by a rapid thermal anneal at 1050 °C for 10 s.

In the quarter-micron regime such a lateral channel profile of n-MOSFET was obtained by using a complicated DSA-MOSFET channel formation adding the mask step [10]. For the channel implant, boron ions through source windows were implanted, followed by annealing at 1000 °C for 30 min. Hence the fabricated device suffers from high source junction capacitance and difficulty in scaling down into sub-quarter micron regime due to high heat treatment. Also, the transport mechanism was not cleared in the previous work [10]. The present process provides a practical fabrication process of asymmetric channel profile and allows the scaling of the asymmetric device down to the 0.1-μm regime.

Fig. 2 shows linear and saturation threshold voltages as a function of gate length for both asymmetric and conventional devices. The threshold voltage is defined as the gate voltage for the drain current of $(W/L) \cdot 50$ nA, where L is the gate length and W is the gate width. Also, the measured subthreshold characteristics for the n-MOSFET's with the gate length of 0.15 μm are shown in Fig. 3. Both devices exhibit the same saturation threshold voltage of 0.16 V at $V_{\rm DS} = 1.5$ V and the linear threshold voltages are 0.20 V for the asymmetric device and 0.24 V for the conventional device. The subthreshold slopes at $V_{\rm DS} = 0.1$ V were 88 mV/dec for the asymmetric device and 82 mV/dec for the conventional device, respectively. As shown in Fig. 2, the asymmetric n-MOSFET structure allows the improved short-channel effect down to the 0.1-μm gate length because of the high boron concentration at the source side, resulting in a reverse short-channel effect for the linear threshold. Measured I–V characteristics for these devices with the gate length of 0.15 μm are compared in Fig. 4. As expected, the asymmetric device shows higher drain current than that of the conventional device. The measued result indicates that the saturation current of the symmetric device is 20% larger than that of the conventional device at $V_{\rm GS} = 1.0$ V and $V_{\rm DS} = 1.0$ V.

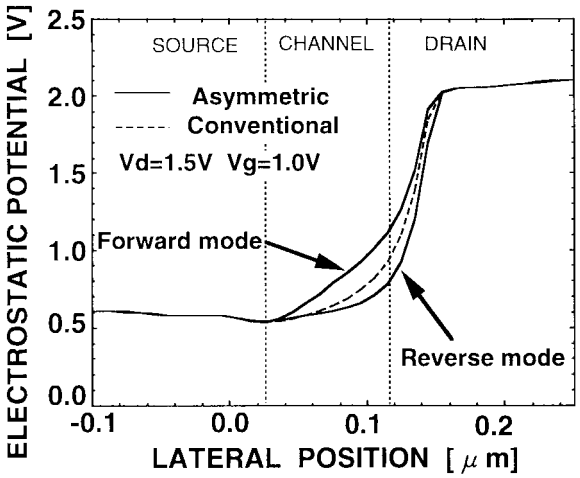

Fig. 5. Simulated surface potentials of the asymmetric and conventional n-MOSFET's at 5 nm below the Si-SiO_2 interface. The metallurgical channel is assumed to extend from 0.025 to 0.115 μm. In the reverse mode of the asymmetric device, the source and drain terminals are interchanged.

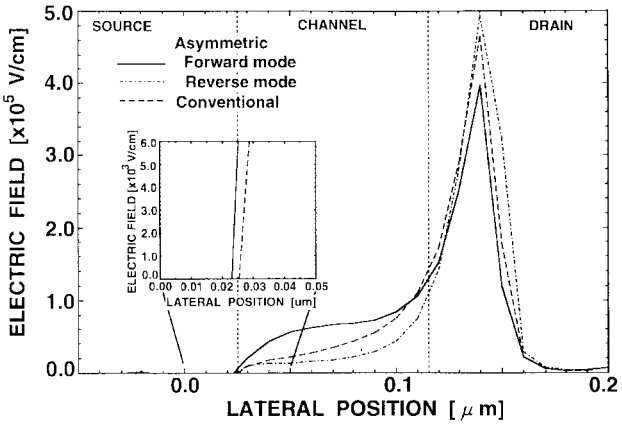

Fig. 6. Simulated electric fields along the channel, corresponding to the surface potentials shown in Fig. 5.

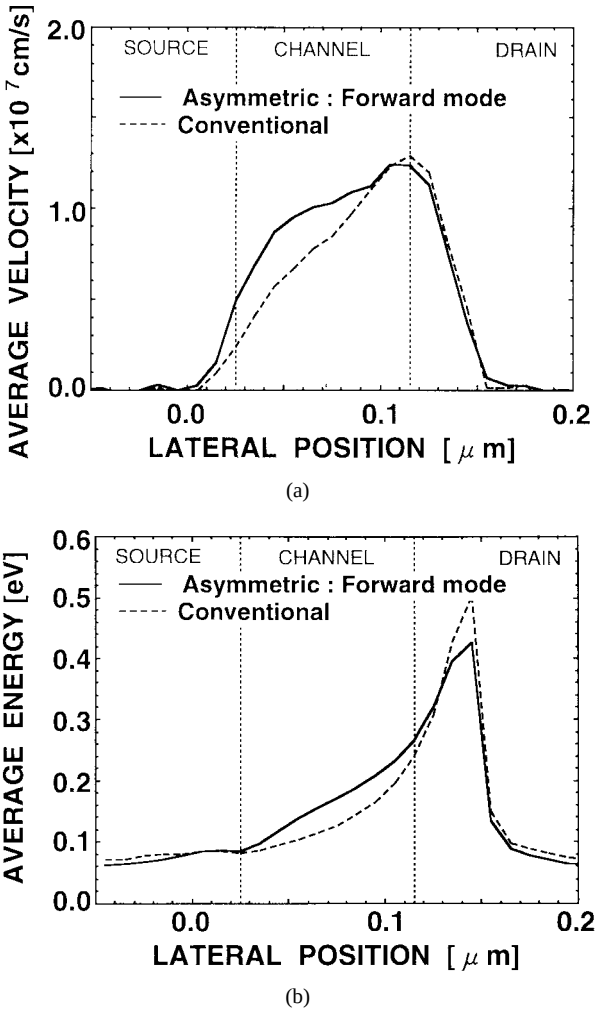

Fig. 7. (a) Average electron velocity and (b) average energy distributions along the channel. It is assumed that $V_{\rm GS} = 1.0$ V and $V_{\rm DS} = 1.5$ V.

III. Potential Design and Transport Property

In this section, the electron transport property of the asymmetric n-MOSFET is investigated by using the Monte Carlo simulation coupled with the Poisson equation. The model for scattering rates and many-band model, described in [13], were adopted for the Monte Carlo transport model. The program of the Monte Carlo transport model is implemented into a process/device integrated simulator "SMART-II" [14] in a parallelized code [15], [16] to obtain an accurate description of the devices. This approach allows the Monte Carlo device simulation using the process simulation results and hence the simulation provides a means for designing of the actual 0.1-μm MOSFET's. The Monte Carlo simulation results shown here were obtained with 15 000 particles.

The lateral potential design over the channel is a key issue to achieve high performance in the 0.1-μm MOSFET. So far, there has been little attention on this design methodology in the 0.1-μm regime. Fig. 5 presents simulated surface potentials of the asymmetric and conventional n-MOSFET's at 5 nm below the Si-SiO_2 interface. The simulation is done at $V_{\rm GS} = 1.0$ V and $V_{\rm DS} = 1.5$ V. As seen in this figure the n-MOSFET with asymmetric channel profile increases the surface potential in the channel at the forward mode, while for the conventional device the surface potential rapidly increases from the drain end of the channel. Such a potential behavior in the conventional device structure is enhanced for the reverse mode of the asymmetric device where the source and drain terminals were interchanged. Electric fields corresponding to these surface potentials are shown in Fig. 6. This figure gives simulation results in the forward and reverse modes of the asymmetric device, together with that of the conventional device. While the electric field of the conventional device is 2.5×10^4 V/cm at the source side of the channel ($x = 0.055$ μm), the asymmetric device provides larger field of 6.0×10^4 V/cm at the same position. Moreover, it is found from the inset of Fig. 6 that the potential design of the asymmetric device creates high electric field of 5.7×10^3 V/cm at the source end of the channel. The magnitude of the electric field over the channel is larger than that of the conventional device, while the electric field of the conventional device exceeds that of the asymmetric device at the drain end of the channel. In the reverse mode of the asymmetric device the electric field becomes lower and more uniform in the channel and grows larger in the drain extension region.

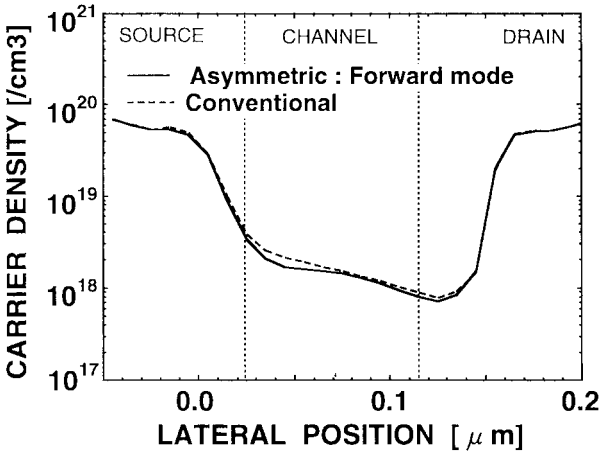

Fig. 8. Simulated electron densities below of the channel, and the smaller high-energy tail of the distribution in the drain. This transport property creates high drain current, large transconductance, and low substrate current of the 0.1-μm n-MOSFET with asymmetric channel profile.

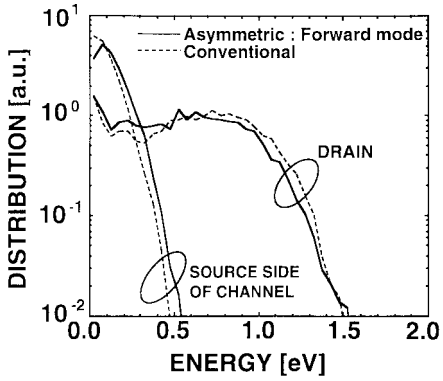

Fig. 9. Electron energy distributions at the source side of the channel ($x = 0.05$ μm) and at the peak of the electric field ($x = 0.145$ μm).

Fig. 7(a) and (b) shows the average electron velocity curves and average energy distributions along the interface. For the asymmetric device the electron velocity rises rapidly at the source due to the high electric field at the source end of the channel. The electrons are further accelerated by the high electric field in the channel and then the velocity reaches a value of 1.0×10^7 cm/s at the source side of the channel ($x = 0.064$ μm), with a peak value at the drain end of the channel. At the same position ($x = 0.064$ μm), the average energy is as low as 0.16 eV because of the nonequilibrium electron transport. This means that electrons cold at the source side of the channel and effectively gain the kinetic energy from the electric field in the channel [8]. In the drain extension region the asymmetric device exhibits lower average energy than that of the conventional device because of the low electric field shown in Fig. 6. In case of the conventional MOSFET structure the velocity grows slowly in the channel and the velocity overshoot occurs at the drain side of the channel even in 0.1-μm regime. Fig. 8 shows simulation results for electron densities of both devices. Since the electron density of the asymmetric device is slightly lower than that of the conventional device, it is confirmed that the enhancement of the drain current ($J = -qnv$) is due to the velocity overshoot near the source side. In fact, the velocity overshoot region for the asymmetric device reaches 57% over the channel.

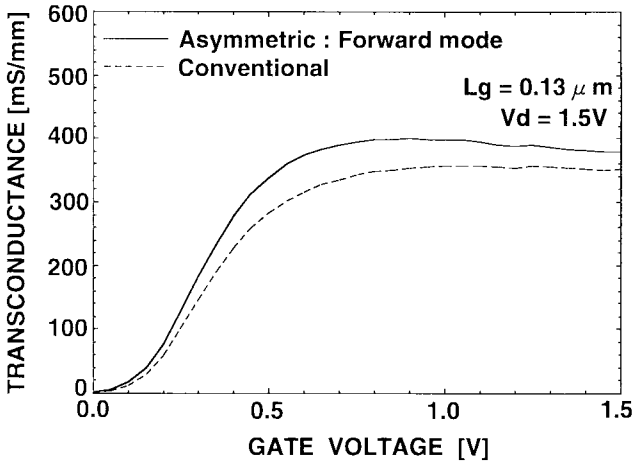

Fig. 10. Measured transconductances as a function of the gate voltage for the conventional and asymmetric devices with the gate length of 0.13 μm. $V_{DS} = 1.5$ V.

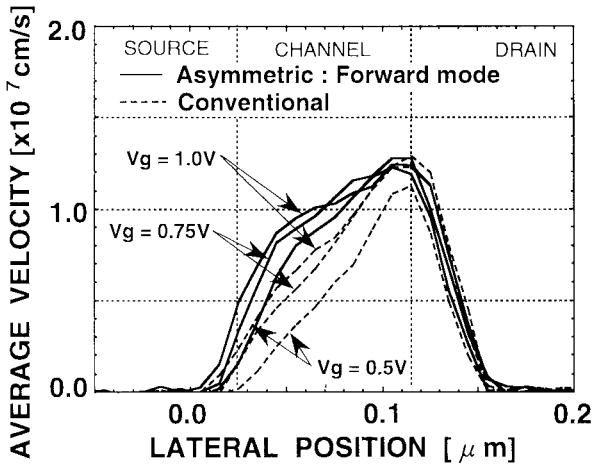

Fig. 11. Average electron velocities in the channel for the conventional and asymmetric devices under various gate bias conditions.

The electron energy distributions of two devices are compared in Fig. 9. The distributions are shown at the source side of the channel ($x = 0.05$ μm) and at the peak of the electric field ($x = 0.145$ μm) in the drain, respectively. It is found that at the source side of the asymmetric device the distribution is more energetic and the peak of distribution shifts to 0.08 eV. On the contrary, at the peak of the electric field the asymmetric device structure results in cooling of the distribution at energies larger than about 0.7 eV.

IV. Performance and Reliability Results

The transport property of the 0.1-μm device is also presented in the form of the transconductance, removing the threshold-voltage variations [17]. Fig. 10 compares the measured transconductances of the asymmetric and conventional devices having a 0.13 μm gate length. The results are for an applied V_{DS} of 1.5 V. It is found that the asymmetric device provides larger transconductance than that of the conventional device. The maximum transconductance of the asymmetric device reaches up to 400 mS/mm at the low gate voltage of 0.9 V, while the transconductance of the conventional device

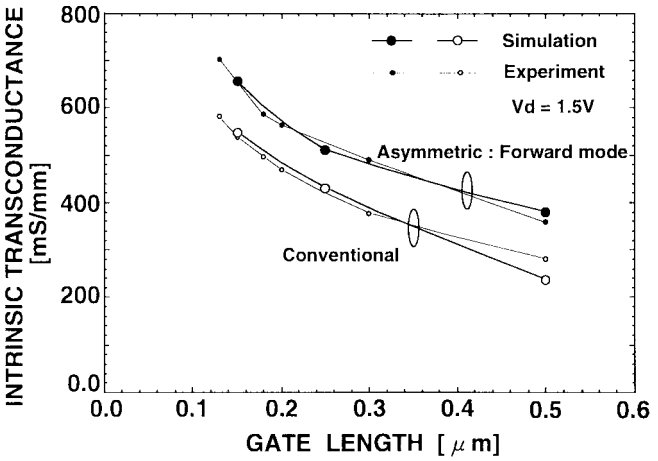

Fig. 12. Intrinsic transconductance g_{mi} versus gate length. g_{mi} is estimated by using the maximum g_m and measured extrinsic resistance.

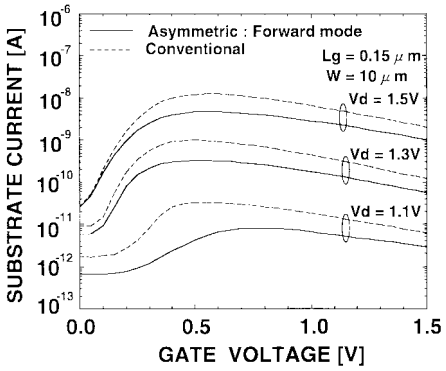

Fig. 13. Substrate current versus gate voltage at different drain voltages of 1.1 V, 1.3 V, and 1.5 V for both asymmetric and conventional devices. The gate length is 0.15 μm.

is 350 mS/mm. In the MOSFET structure the electric field near the source decreases with the decrease of the gate bias, while the electric field near the drain grows larger. Such a gate bias dependent behavior leads to the difference of transconductance between two devices. This is clarified in Fig. 11, where the gate bias dependence of the average velocity in the channel is given for the conventional and asymmetric devices. As the gate bias increases, the high velocity region moves toward the source which is a high-density region. For the asymmetric device the electron velocity rises rapidly at the source due to the large electric field and hence the velocity near the source is higher than that of the conventional device in every case. Moreover, it is confirmed that the variation of the electron velocity with gate bias near the source is larger than that of the conventional device.

Fig. 12 shows the experimental and simulated results for the maximum intrinsic transconductances as a function of the gate length. The intrinsic transconductances are estimated by using the measured maximum transconductance and extrinsic resistance at each gate length [18]. The extrinsic resistance is obtained using a "Paired V_g Method" [19] and the extracted value of the source/drain resistance was $900\ \Omega \cdot \mu$m due to the shallow extensions. The simulated intrinsic transconductances, which are calculated from the simulated maximum transconductance $g_m \equiv \partial I_D/\partial V_G$ and measured extrinsic resistance, are compared directly, supporting the results of the previous section. The simulated maximum values of g_m are obtained by taking the difference of the drain current at the gate bias corresponding to the measured maximum transconductance and hence the simulation results are in excellent agreement with the experimental data when compared with the previous work [8]. The intrinsic transconductance of the asymmetric device with 0.13 μm gate length reaches 704 mS/mm, which is 21% larger than that of the conventional device.

The substrate current versus gate voltage characteristics have been measured to confirm hot-carrier reliability for the n-MOSFET with asymmetric channel profile. Fig. 13 shows the substrate current versus gate voltage at different drain voltages of 1.1 V, 1.3 V, and 1.5 V, comparing with the experimental data of the conventional device. For both devices the bell-shaped substrate current characteristics are observed at drain voltage of 1.1 V, indicating impact ionization at the band gap of silicon. Although the asymmetric device increases the drain current, the substrate current is significantly reduced because of the smaller high-energy tail of the distribution than that of the conventional device as shown in Fig. 9. This implies that the asymmetric device provides an advantage for hot-carrier reliability in the 0.1-μm regime.

V. Conclusion

The transport property of a 0.1-μm n-MOSFET with asymmetric channel profile has been clarified by the self-consistent Monte Carlo device simulations and measured electrical characteristics. The lateral potential design over the channel creates high electric field at the source end of the channel. The 0.1-μm n-MOSFET structure with asymmetric channel profile allows high electron velocity at the source end of the channel, indicating velocity overshoot at the source side of the channel. For a 0.13-μm gate-length device, the intrinsic transconductance is 21% larger than that of the conventional device. The low substrate current characteristics are obtained due to the smaller high-energy tail of the distribution in the drain.

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