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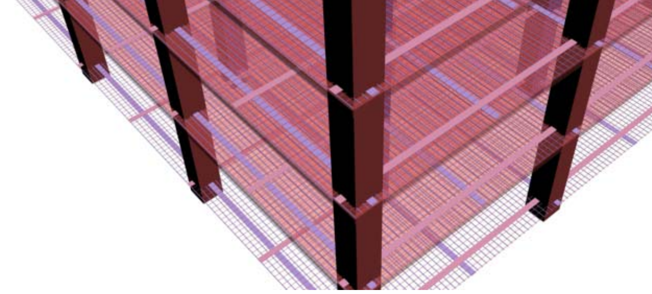
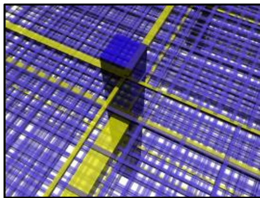
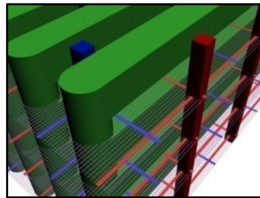
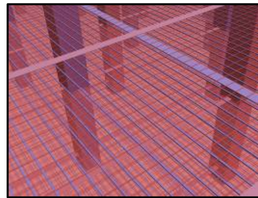
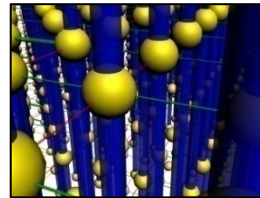


Power and Slew-aware Clock Network Design for Through-Silicon-Via (TSV) based 3D ICs

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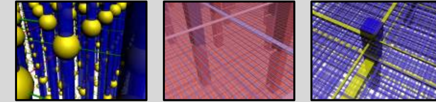
Outline

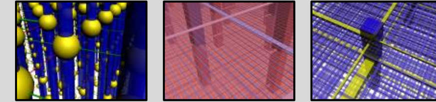
- Introduction
- Problem formulation
- 3D clock tree synthesis
- Simulation and discussions
- Conclusions

Related works

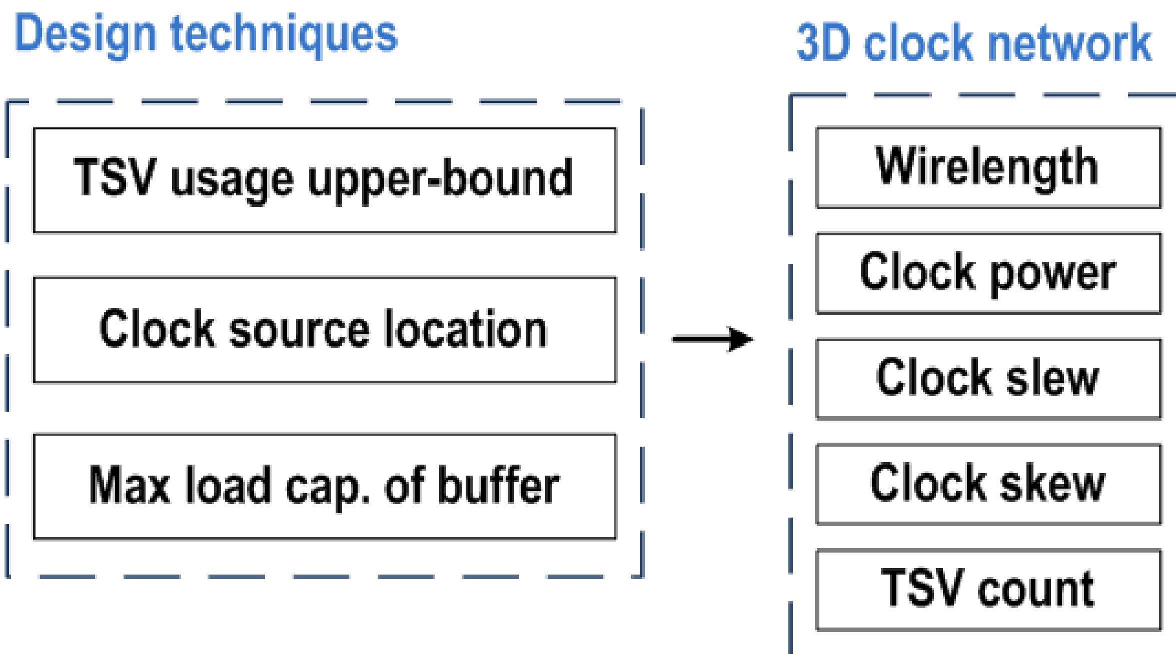


- Through-silicon-via (TSV)
  - Fabrication and characterization
  - Reliability issues [Ramm, etc. ECTC'08] [Wright, etc. ECTC'08]…
- Low-power 3D clock network
  - A fabricated 3D clock distribution network [Pavlidis, etc. CICC'08]
  - A separate layer of clock distribution network for power reduction [Arunachalam, etc. VLSI'08]
- 3D clock network design and optimization
  - Thermal-aware 3D clock design, 3D clock routing algorithm [Minz, etc. ASPDAC'08]
  - Pre-bond testable 3D clock synthesis [Zhao, etc. ICCAD'09]

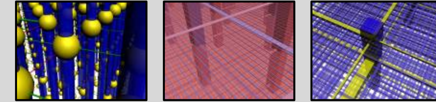
Contributions



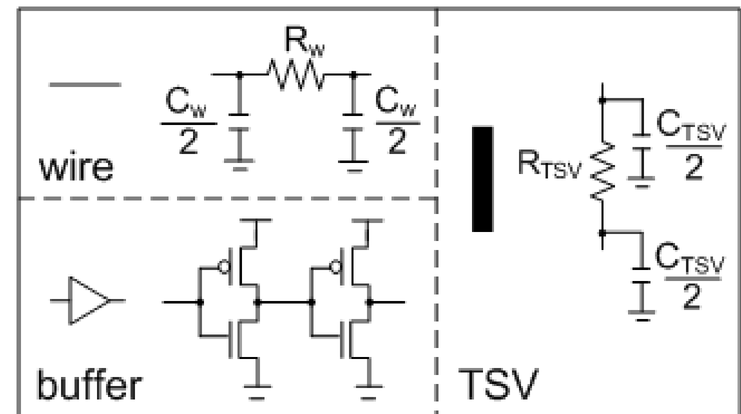
- The major goals
  - Clock skew minimization
  - Clock slew control
  - Clock power reduction
- Investigate the impact of design techniques on 3D clock network

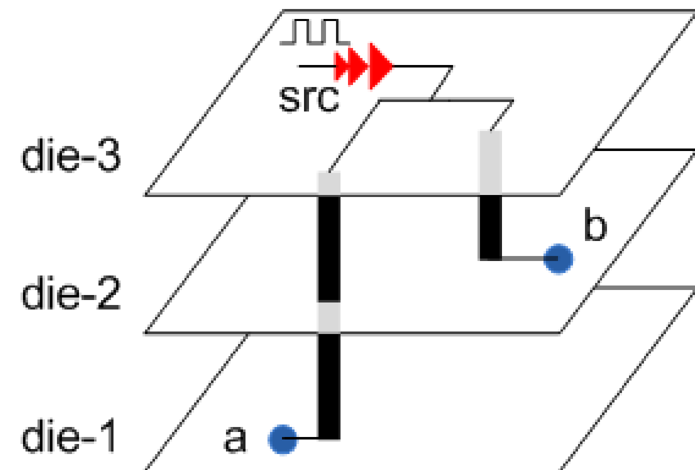


Electrical model and TSV usage

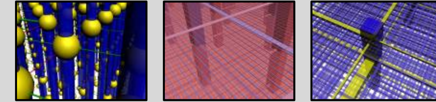


- Electrical model
  - Wire
  - TSV
  - Clock buffer
- TSV upper bound
  - Maximum number of TSVs allowed between adjacent dies
- TSV count (#TSVs)
  - Total number of TSVs used in 3D tree
  - Stacked-TSV



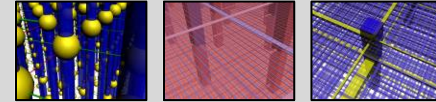


Problem formulation: 3D clock tree synthesis

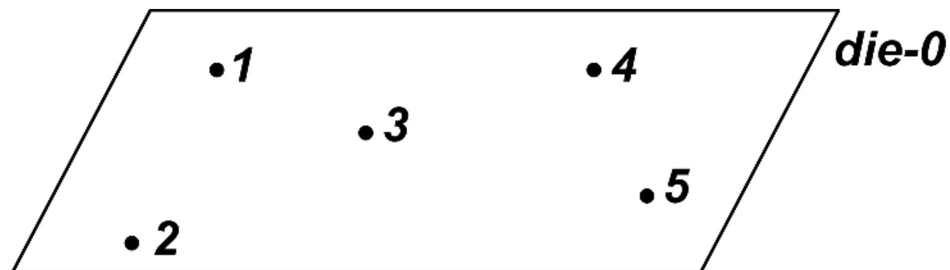


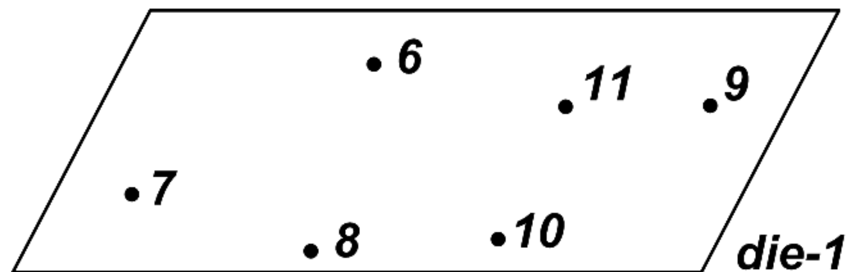
- Input
  - Sink set (N dies), clock source location
  - Upper bound of TSV usage
  - Slew constraint
- Output
  - Zero-Elmore-skew 3D clock tree
- Object
  - Zero-Elmore-skew
  - Minimize wirelength, clock power
- Constraint
  - Maximum slew
  - Upper bound of TSV usage

3D clock tree design flow



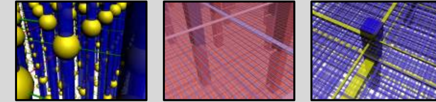
- **Input:**
  - a set a sinks on N die
  - Upper bound of TSV



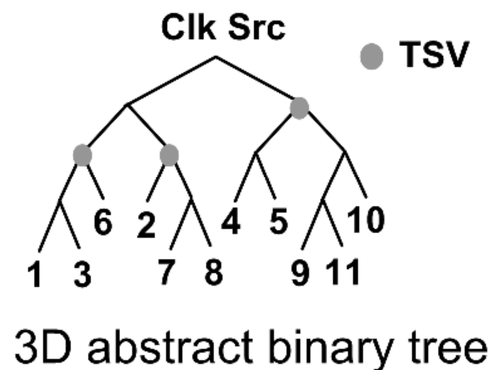


Upper bound of TSV = 3, clock source locates on die-0

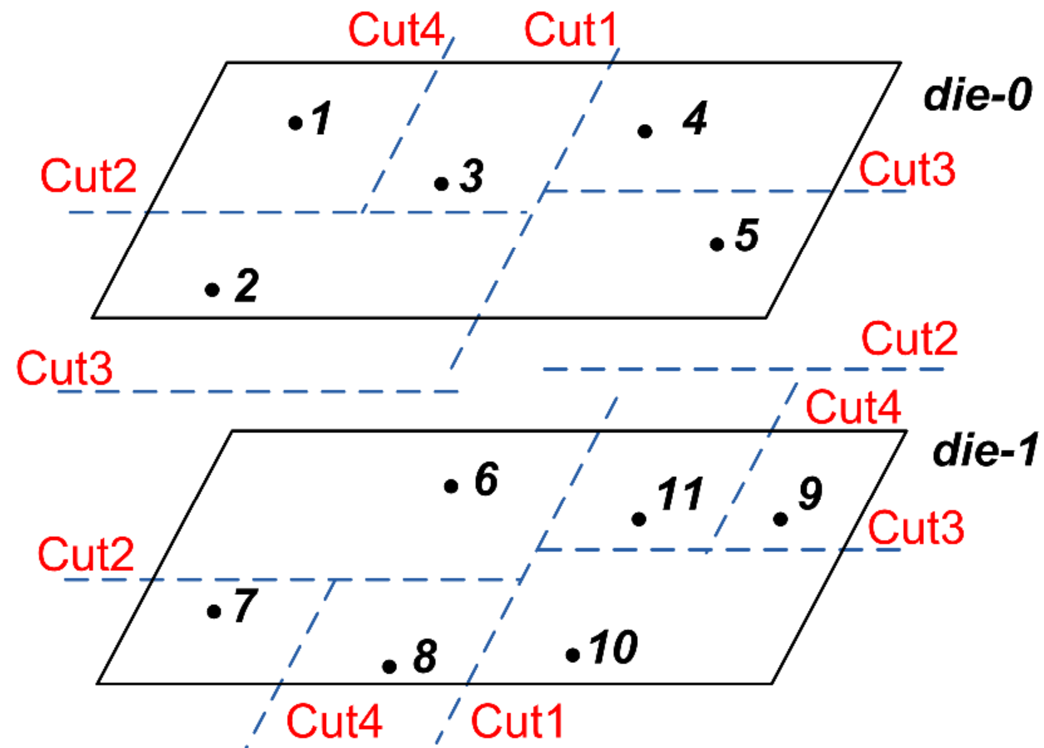
3D clock tree design flow (cont.)



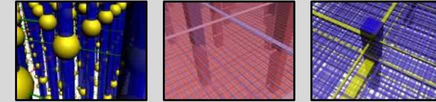
- **Step-1:**
  - Recursive top-down partition
  - 3D Method of Means and Medians (3D-MMM)
  - 3D abstract binary-tree generation



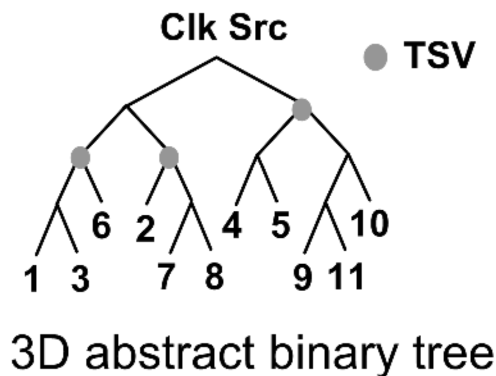
3D abstract binary tree



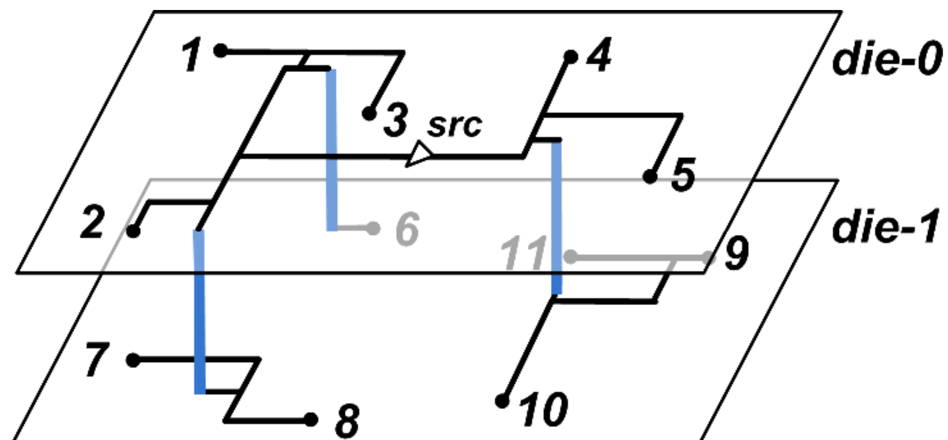
3D clock tree design flow (cont.)



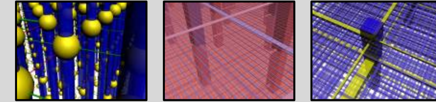
- **Step-2:**
  - Merging and slew-aware buffering, embedding
  - 3D clock tree with multiple TSVs
- **Unique property of 3D clock tree**
  - A complete tree + many sub-trees

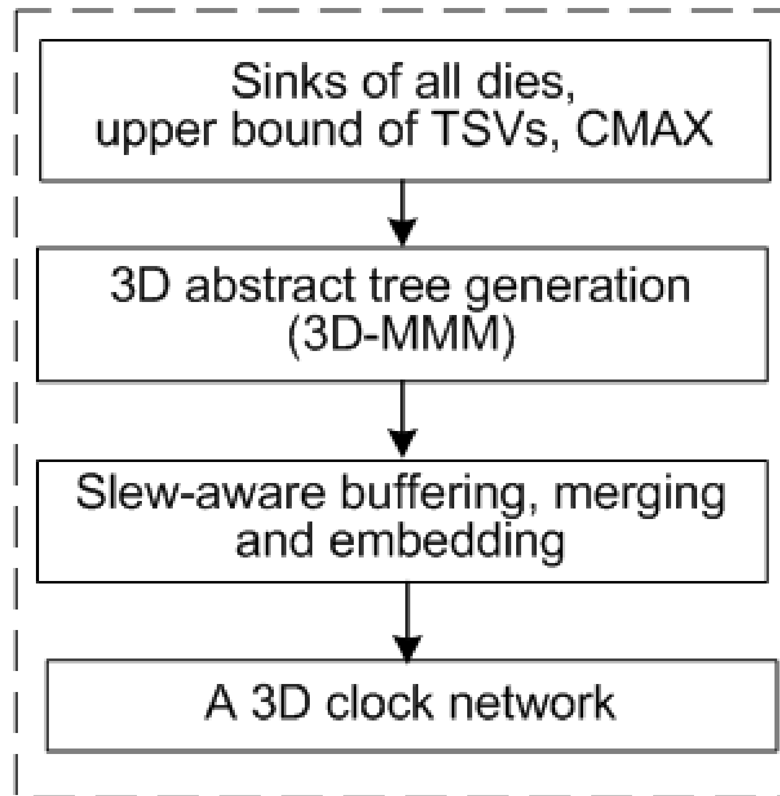


3D abstract binary tree

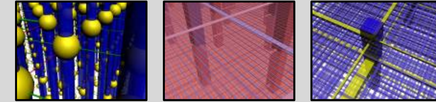


3D clock routing algorithm

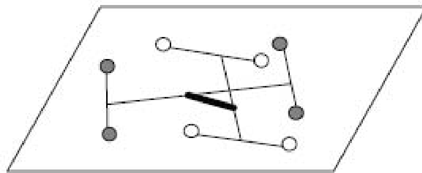
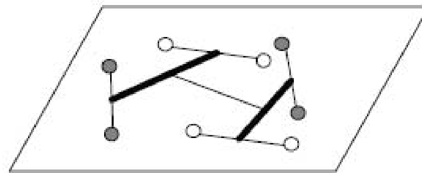
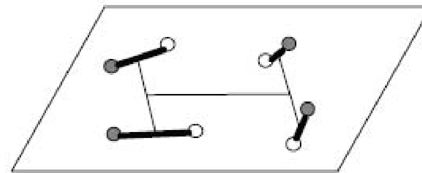




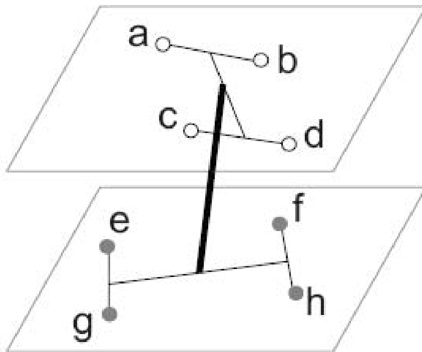
3D-MMM and 3D abstract tree

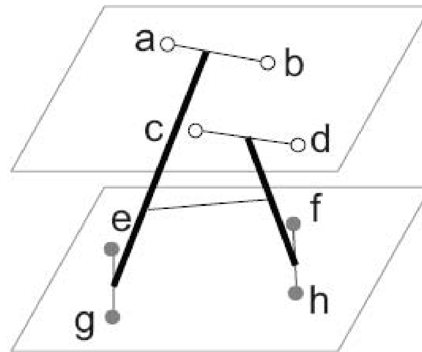


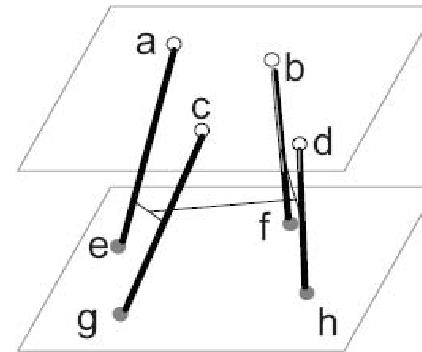
TSV=1 | TSV=2 | TSV=4

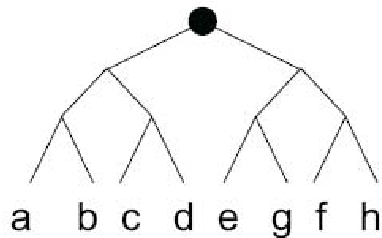
2D version

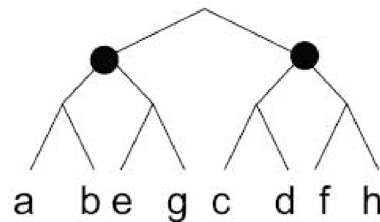


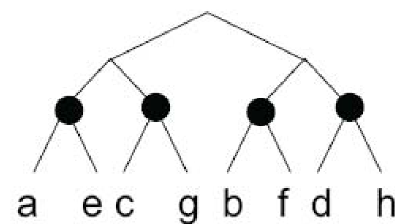




3D version

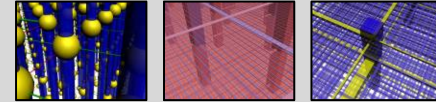






3D abstract tree

3D-MMM and 3D abstract tree (cont.)



- **3D abstract tree for the N-die stack**
  - N-colored binary tree
  - Clock source location

Given three sinks

die-3 A
die-2 B
die-1 C

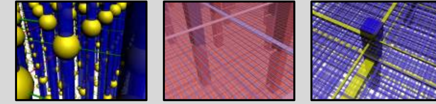
Clk src on die-3
Clk src on die-2
Clk src on die-1

src m1 A B C

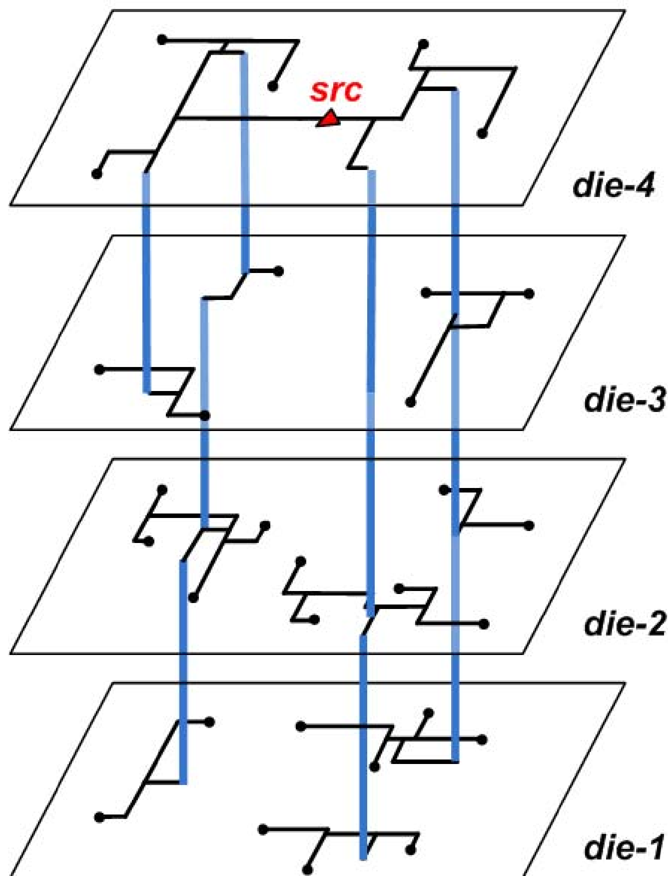
3D abstract tree

3D clock tree

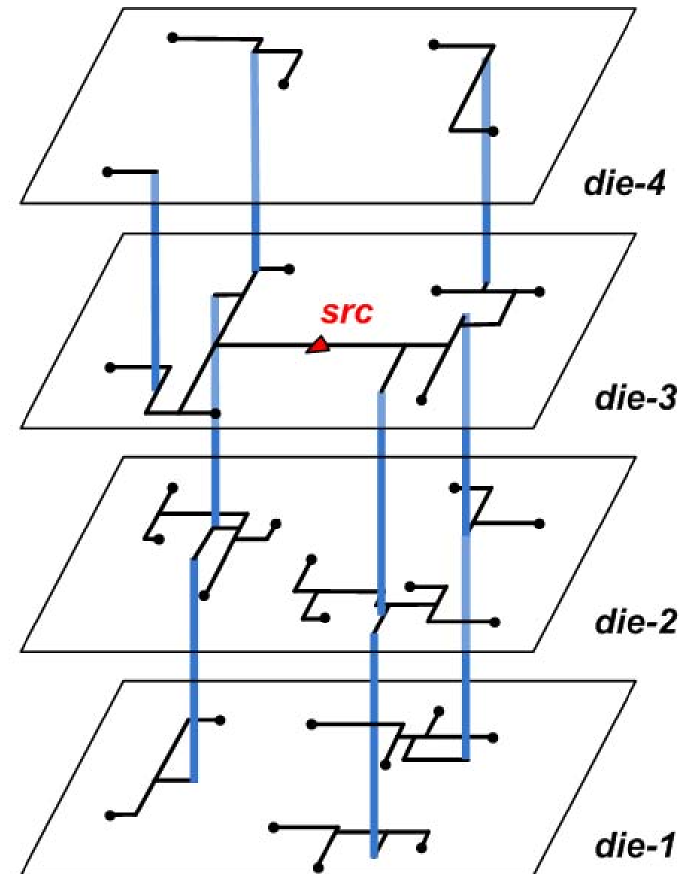
3D clock tree in multiple-die stack



- **A complete tree + many sub-trees**

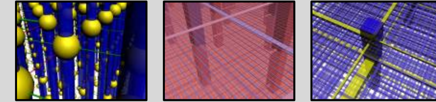


Four-die 3D clock tree, src on die-4



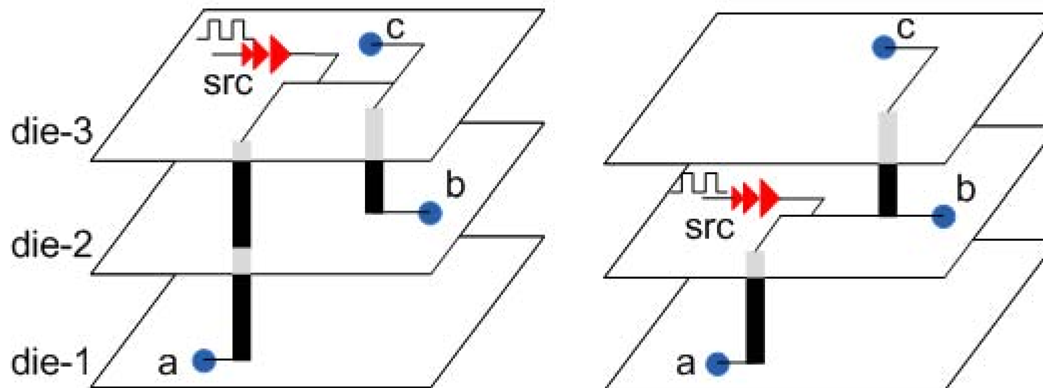
Four-die 3D clock tree, src on die-3

Clock source location

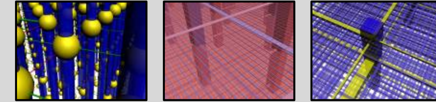


- **Clock source on middle die tends to reduce #TSVs and wirelength**
- **Theoretical maximum TSV usage:**
  - **M sinks evenly distribute on N dies, clock source locates on die-s**

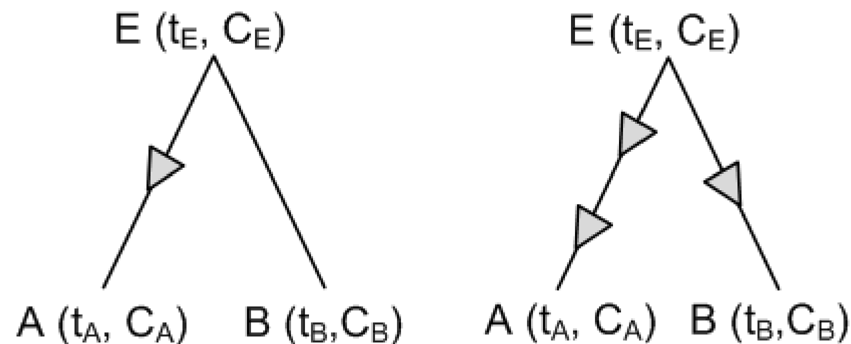
$$\frac{M}{N} \times \left(\sum_{i=1}^{s-1} (s-i) + \sum_{i=s+1}^{N} (i-s) \right)$$



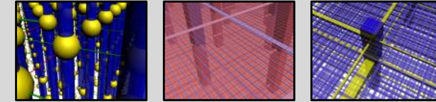
Buffering and merging



- **Goal**
  - Slew control
    - Maximum loading capacitance (CMAX) of clock buffers
  - Wirelength reduction
- **Object**
  - Zero-Elmore skew
  - Clock power minimization



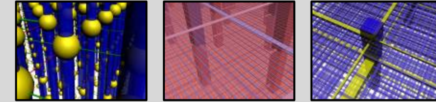
Detail experiment settings



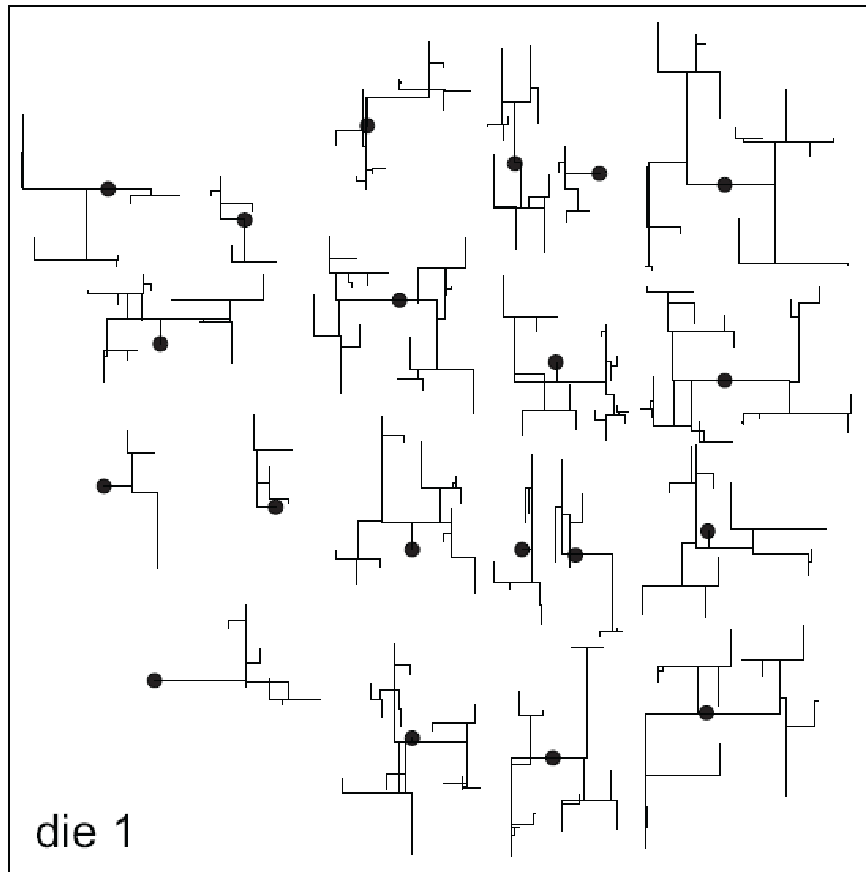
- 45nm technology:
  - Frequency = 1GHz, V_{dd} = 1.2V
  - Clock slew < 10% of clock period (CMAX = 300fF)
  - Clock skew < 3%~4% of clock period
  - Wire: R = 0.1 Ω/um, C = 0.2 fF/um
  - Buffer: R_d=122 Ω, C_L = 24 fF, t_d = 17 ps
  - TSV: R_{TSV} = 0.035 Ω, C_{TSV} = 15.48fF
    - 10 um X 10 um, via-last
    - Thinned-die height = 20 um
- Results are from SPICE simulation
  - Skew, slew, power
- We use two cases: four-die and six-die

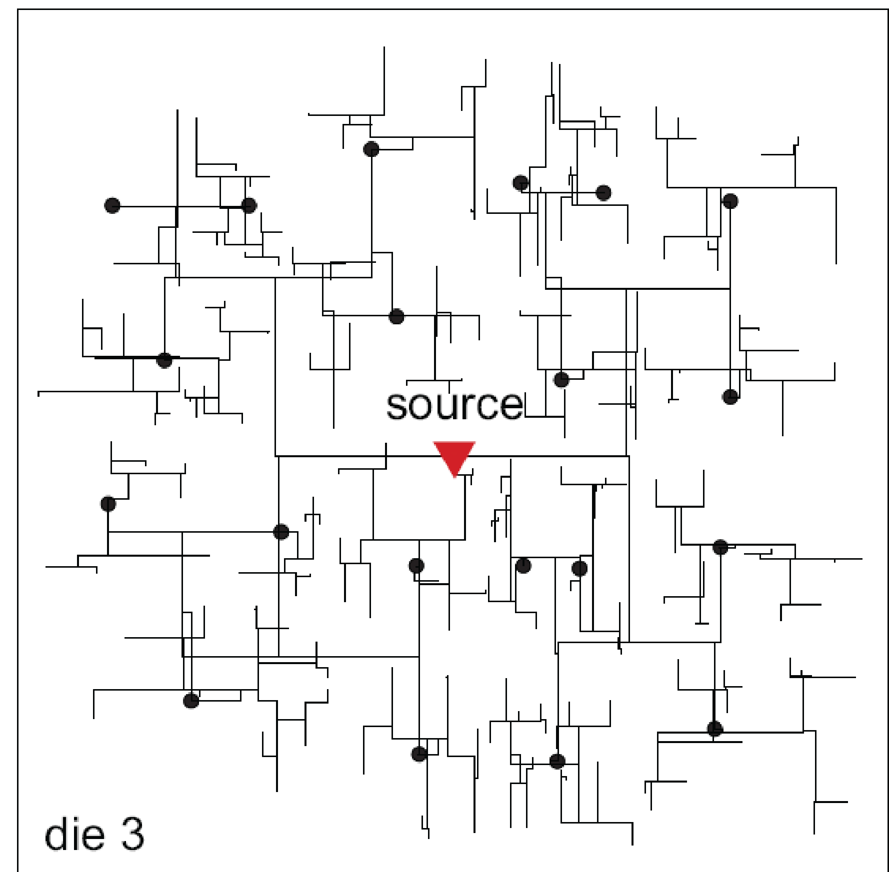
Circuits	# Sinks
r1	267
r2	598
r3	862
r4	1903
r5	3101

Sample 3D clock trees



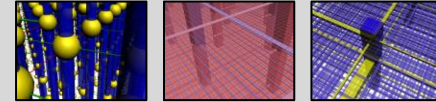
r5, six-die



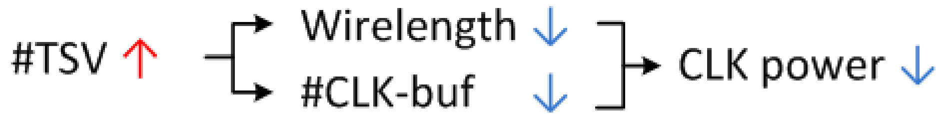


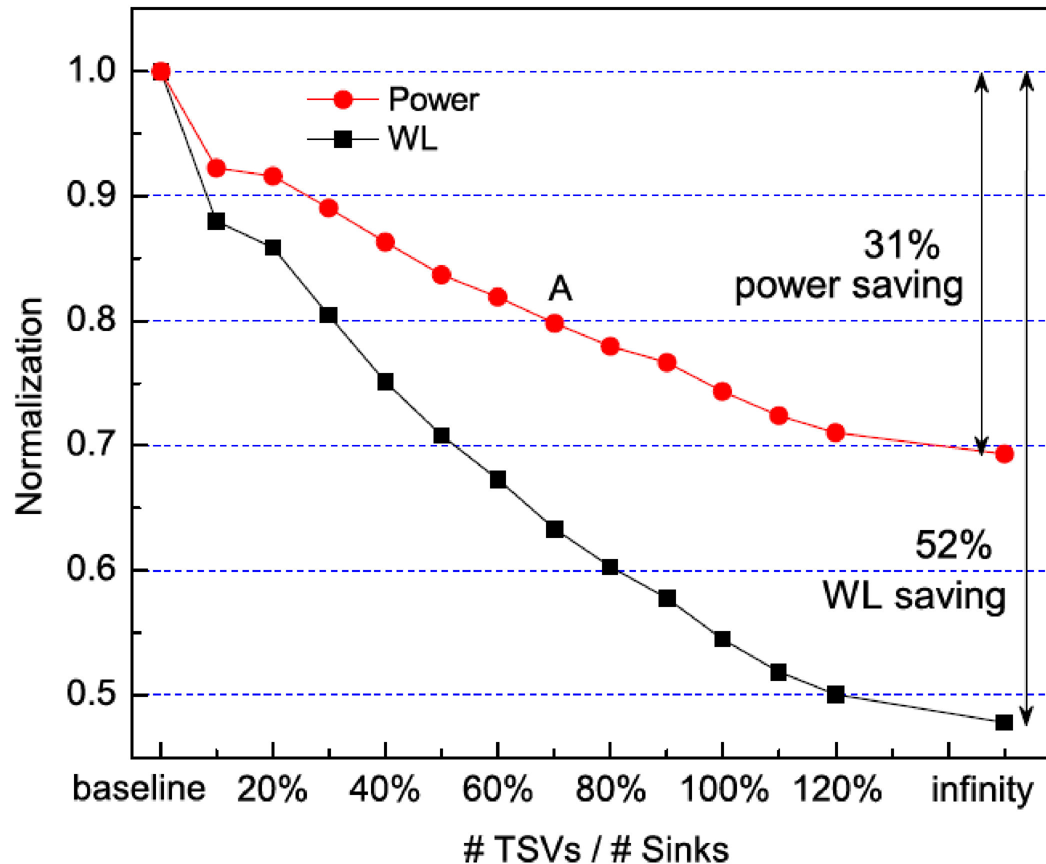
#TSVs = 20

Impact of TSV bound on wirelength and power



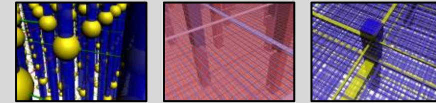
r5, six-die

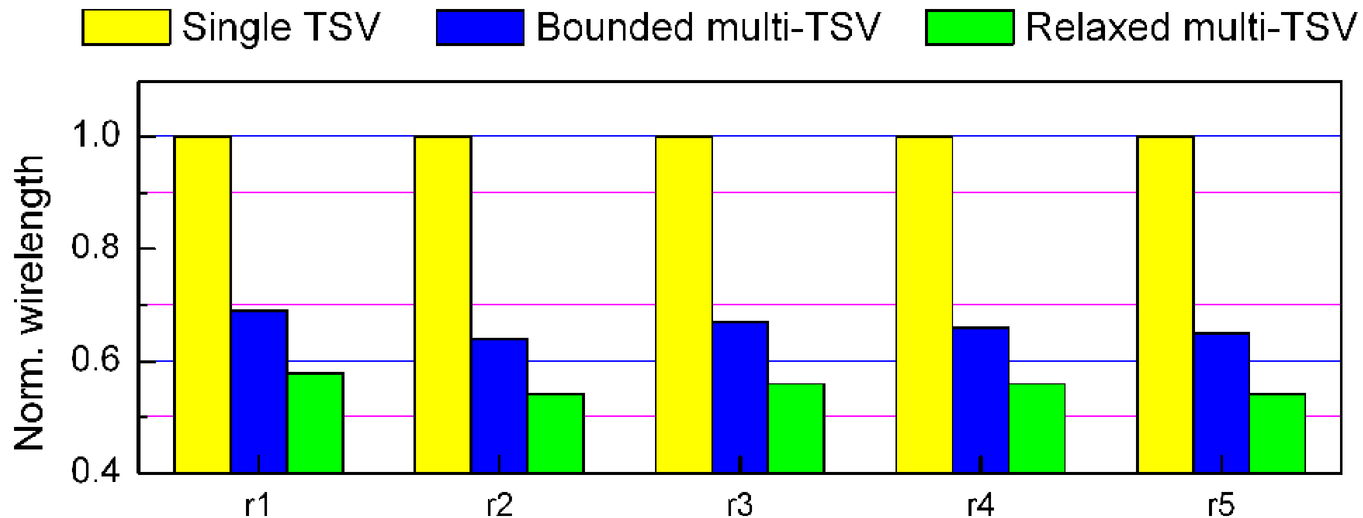


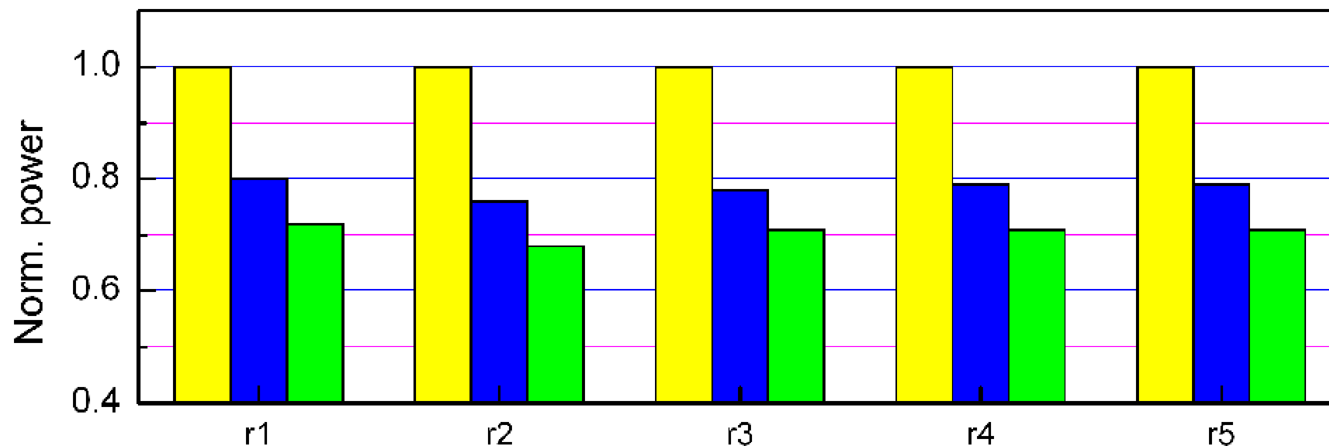


Point A: 20% power saving, TSV bound ⩾ 70% of #sinks

Multi-TSV vs Single-TSV: four-die stack

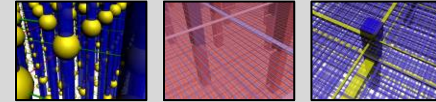


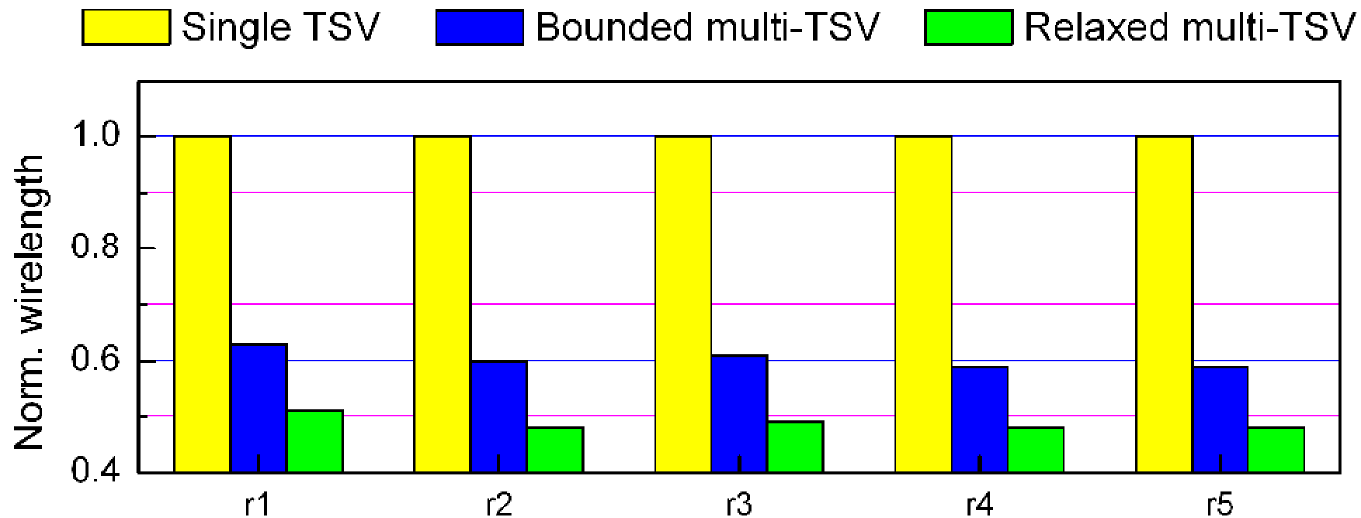


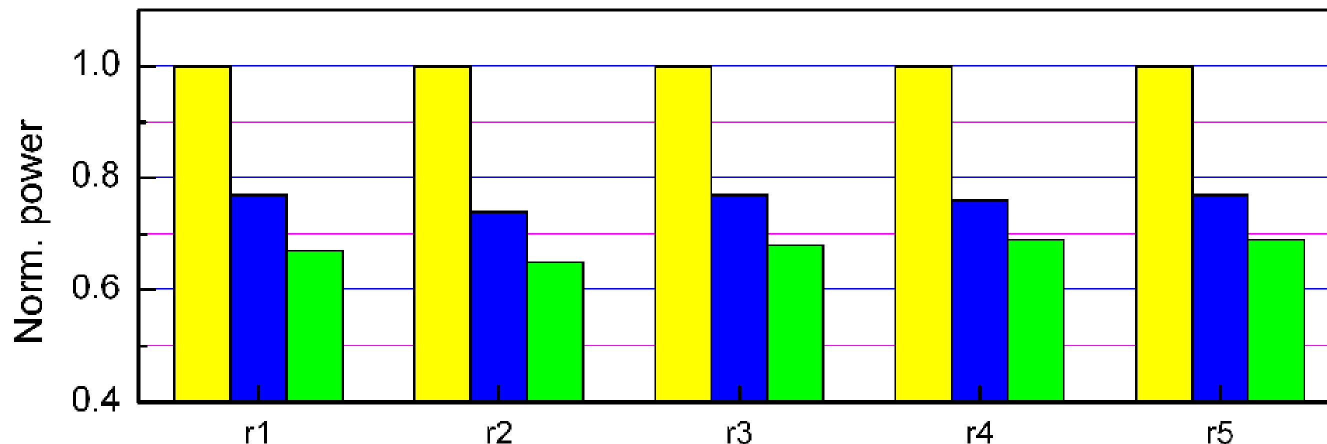


	r1	r2	r3	r4	r5
#TSVs (Bnd):	139	309	432	1003	1631
#TSVs (Relax):	265	579	819	1893	3097

Multi-TSV vs Single-TSV: six-die stack

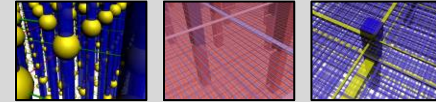






	r1	r2	r3	r4	r5
#TSVs (Bnd):	222	483	701	1594	2588
#TSVs (Relax):	399	908	1301	2980	4782

Clock skew in four- and six- die stack



Single TSV | Bounded multi-TSV | Relaxed multi-TSV

Clk skew (of clk period)

3%
2%
1%
0%

r1 r2 r3 r4 r5

four-die stack

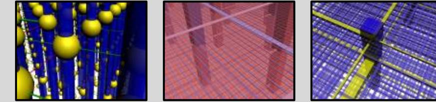
Clk skew (of clk period)

3%
2%
1%
0%

r1 r2 r3 r4 r5

six-die stack

Spatial distribution of clock delay

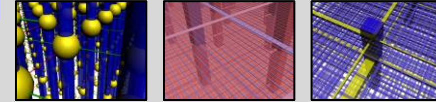


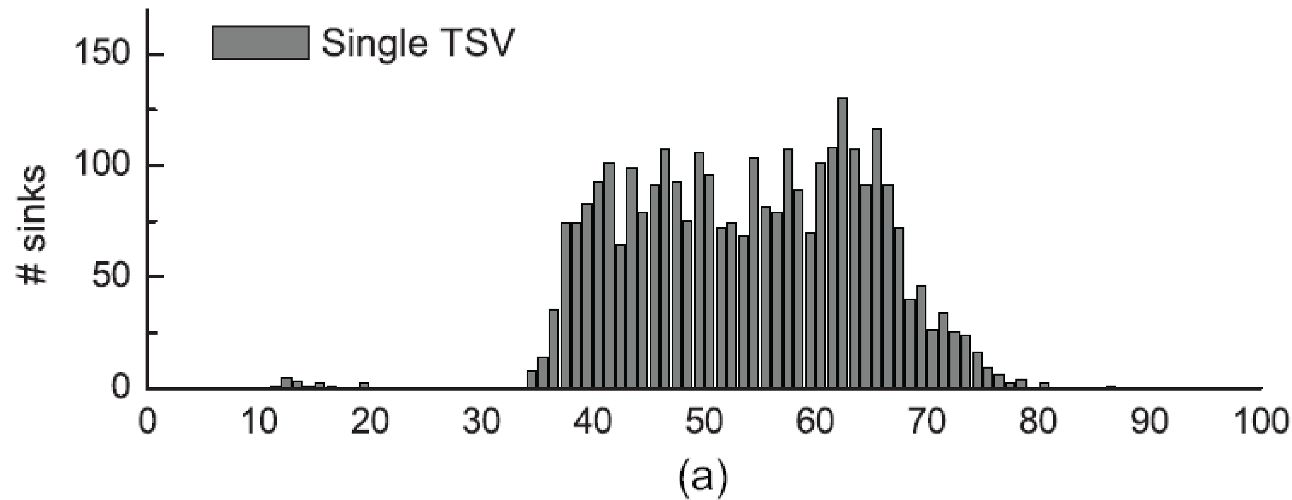
r5, six-die

Delay (ns)
0.560
0.558
0.556
0.554
0.552
0.550
0.548
0.546
0.544
0.542

Skew
17.8 ps

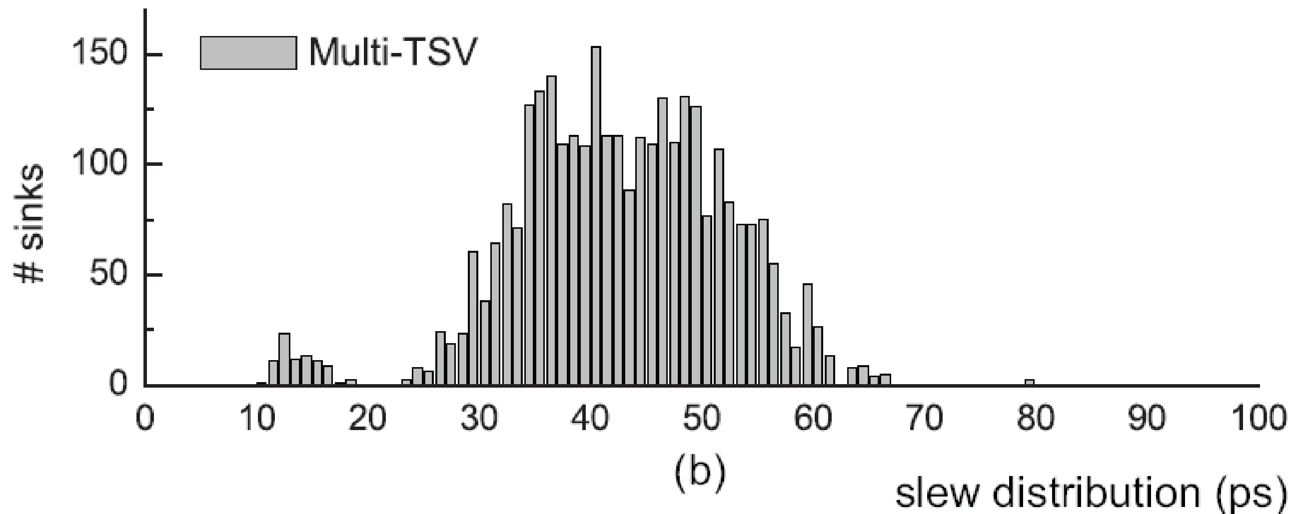
Impact of TSV bound on slew distribution





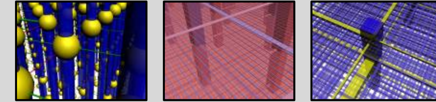
r5, six-die
CMAX=300fF

[11.4ps, 86.2ps]
Avg. 53.9ps
#Bufs: 2933



[10.9ps, 79.6ps]
Avg. 42.6ps
#Bufs: 2638

Impact of CMAX on slew variations



r5, six-die

Power (mW)
1500
1400
1300
1200
1100
1000
900

Rising slew (ps)
0 10 20 30 40 50 60 70 80 90 100

175fF
200fF
225fF
250fF
275fF
300fF
CMAX

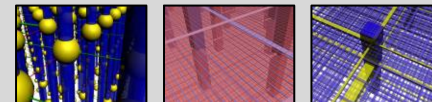
slew range

Using single TSV

175fF
200fF
225fF
250fF
275fF
300fF

Using multiple TSVs

Impact of clock source location on power and wirelength

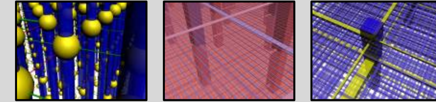


r5, six-die

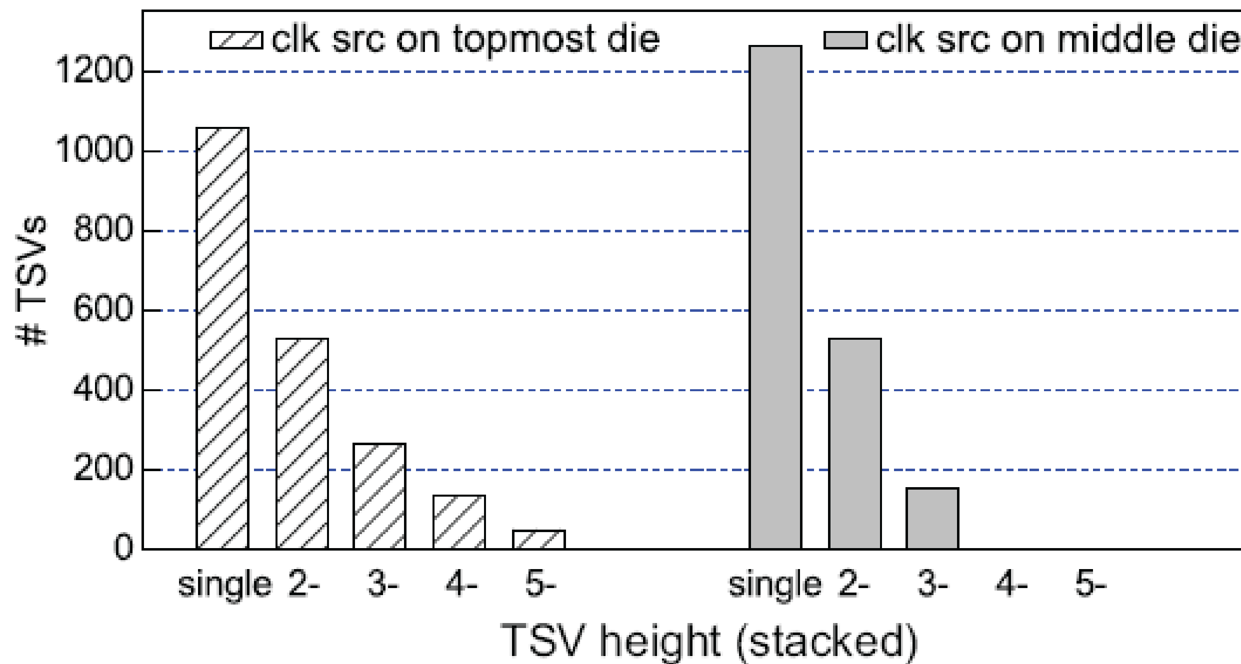
clk src on topmost die
clk src on middle die
33% power saving
53% WL saving
7.7% saving
9.2% saving
A
B
C
D
Normalization
1.0
0.9
0.8
0.7
0.6
0.5
baseline
20%
40%
60%
80%
100%
120%
TSVs / # Sinks

A uses 33% fewer TSVs than B

Distribution of stacked-TSV heights

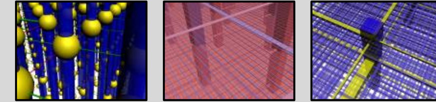


r5, six-die



#TSVs = 3720 **#TSVs = 2791**

Conclusions



- Explored design optimization techniques for reliable, low-power, low-slew 3D clock network design.
- Using multiple TSVs helps to reduce wirelength and power. Multi-TSV also has better control on slew variations.
- Smaller CMAX efficiently lowers the clock slew.
- Clock source location affects wirelength, power and TSV usage of the 3D clock network. Middle-die sourcing policy reduces the TSV usage under the same power budget.

Thank you