Power-Bus Decoupling With Embedded Capacitance in Printed Circuit Board Design

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***Abstract*—This paper experimentally investigates the effectiveness of embedded capacitance for reducing power-bus noise in high-speed printed circuit board designs. Boards with embedded capacitance employ closely spaced power-return plane pairs separated by a thin layer of dielectric material. In this paper, test boards with four embedded capacitance materials are evaluated. Power-bus input impedance measurements and power-bus noise measurements are presented for boards with various dimensions and layer stack ups. Unlike discrete decoupling capacitors, whose effective frequency range is generally limited to a few hundred megahertz due to interconnect inductance, embedded capacitance was found to efficiently reduce power-bus noise over the entire frequency range evaluated (up to 5 GHz).**

***Index Terms*—Conduction loss, decoupling capacitor, embedded capacitance (buried capacitance), power-bus decoupling, power-bus impedance, power-bus noise (delta-I noise, ground bounce noise, simultaneous switch noise), power plane, return plane.**

I. Introduction

A SUDDEN change in the amount of current drawn by an active component on a printed circuit board (PCB) can cause a transient voltage on the power bus. This transient noise voltage can be large enough to interfere with the normal operation of other components on the board. In addition, it may induce currents on the board and any attached I/O cables that result in radiated electromagnetic interference (EMI). Ground bounce or delta-I noise, as this phenomenon is called, is a common problem with high-speed PCB and multichip module (MCM) designs. Discrete decoupling capacitors are generally employed to mitigate delta-I noise in PCB designs. Typical high-speed digital designs require dozens or even hundreds of decoupling capacitors. These decoupling capacitors can take up a considerable amount of surface area on the board, yet their effective frequency range is generally limited due to interconnection inductance [1]. In addition, large numbers of decoupling capacitors on a PCB can reduce the reliability of the final product.

Embedded capacitance is a promising alternative to discrete decoupling capacitors. Boards with embedded capacitance utilize the natural capacitance between the power and return planes to provide power-bus decoupling [2], [3]. By minimizing the spacing between the two solid planes and filling this space with a material that has high relative permittivity, the interplane capacitance can be greatly enhanced. Consequently, it is possible to eliminate most or all of the decoupling capacitors mounted on the surface of the board, freeing up valuable surface routing area, and improving product reliability.

Recently, a project led by the National Center for Manufacturing Sciences (NCMS) evaluated four commercially available embedded capacitance materials for their material properties, reliability, electrical performance, and compatibility with current PCB manufacturing processes. These materials are listed in Table I. The relative permittivity and the loss tangent of each material were measured by the National Institute of Standards and Technology (NIST) at different frequencies. Additional information about these materials can be obtained from NCMS [4].

This paper examines the results of electrical performance tests conducted on boards employing these embedded capacitance materials as well as standard FR4 boards. The measured results illustrate the effects that dielectric thickness, permittivity and loss have on the performance of an embedded capacitance material.

The layer stack ups and layouts of the test vehicles used in this study are described in Section II. Three types of measurements were performed to evaluate the decoupling performance of the embedded capacitance test boards. Power-bus input impedance measurements are presented in Section III. Time-domain and frequency-domain power-bus noise voltage measurements are presented in Sections IV and V, respectively.

II. Description of the Test Vehicles

Test vehicles employing the four embedded capacitance materials listed in Table I and standard FR4 material were designed and manufactured by companies participating in the NCMS embedded decoupling capacitance (EDC) project. The test boards discussed in this paper all have six layers. Fig. 1 illustrates the layer stack up. TV1 is short for Test Vehicle #1. All of the boards discussed in this paper are TV1 boards. TV1–1 boards had power and return planes on Layers 3 and 4, respectively. The spacing between the power and return planes in TV1–1 boards varied depending on the dielectric material employed. FR4 TV1–1 boards had either a 3.3-mil spacing or a 4.5-mil spacing (depending on the preferences of the particular board fabricator). The spacing between the power and the return planes of boards with embedded capacitance was equal to the thickness of the dielectric material as listed in Table I. Consequently, the interplane capacitance ranged from about

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TABLE I
EMBEDDED-CAPACITANCE MATERIALS EVALUATED IN THE STUDY

Material	Dielectric Composition	Thickness[1]	ε_r	tan δ
BC2000™	FR4 epoxy/glass	2.1 mils	3.8~4.2	0.015~0.02
EmCap®	Unsupported epoxy; ceramic powder filled	4.0 mils	36~37	0.01~0.02
Hi-K™	Unsupported polyimide; ceramic powder filled	1.4 mils	11.6~12	0.008~0.012
C-Ply	Unsupported epoxy; ceramic powder filled	0.2 mils	20~22	0.01~0.1

[1] Dielectric thickness is a critical parameter. The samples tested had the thickness indicated in the table. However, these materials are generally not constrained to have the thickness indicated here.

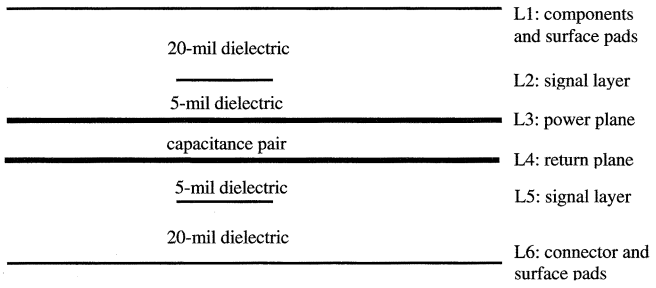

Fig. 1. TV1–1 stack up.

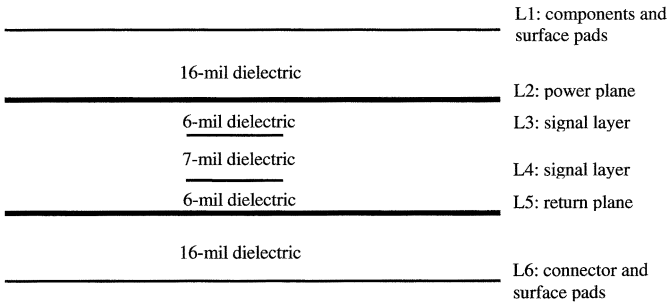

Fig. 2. TV1–2 stack up.

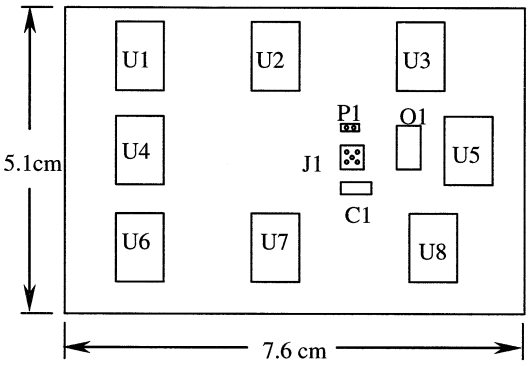

Fig. 3. Basic layout of the test vehicle.

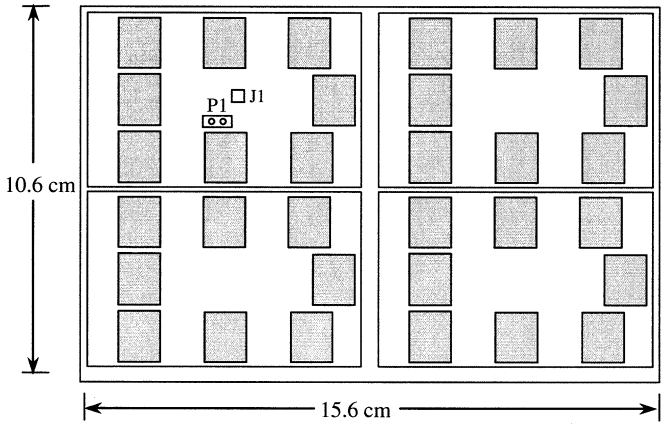

Fig. 4. Layout of four-up boards.

70 pF/cm^2 for the BC2000 board to about 4 nF/cm^2 for the C-Ply board. (The interplane capacitance of both the EmCap and Hi-K boards was about 300 pF/cm^2.) The TV1–2 stack up shown in Fig. 2 had power and return planes on Layers 2 and 5, respectively. This stack up was evaluated because it shields the signals on layers three and four and is the preferred stack up of many FR4 board designers. The spacing between the power and return planes was about 19.4 mils. The TV1–2 stack up was only used in FR4 test boards.

Three board layouts were employed corresponding to three different board dimensions. Fig. 3 shows the basic layout (the one-up board) [5]. This 7.6-cm by 5.1-cm board contains an oscillator (O1), a 22-μF bulk decoupling capacitor (C1), eight octal clock drivers, and a number of load capacitors. The oscillator supplies a 50-MHz signal to the first clock driver, U5, which in turn supplies 50-MHz clock signals to each of six other clock drivers. The clock driver U4 is reserved for noise current measurements and was not active for the tests described in this paper. On the FR4 boards designated as having discrete (or local) decoupling, there are 33 0.01-μF SMT decoupling capacitors mounted on the board's surface. The embedded capacitance boards employed the 22-μF bulk decoupling capacitor, but no local decoupling. An SMA coaxial connector (J1) and a two-pin connector (P1) provided electrical access to the power bus. Both of these connectors were mounted on the bottom of the board (Layer 6), while the rest of the components were mounted on the top of the board (Layer 1).

The four-up layout contains four copies of the basic layout in a 15.6-cm by 10.6-cm area as illustrated in Fig. 4. Although each copy operates independently, the power and return planes are solid (i.e., there is no gap in the planes between the different copies of the basic layout). On some of the four-up boards, all possible components were placed. These were designated "fully populated" boards. On other four-up boards, only the top-left copy (as oriented in Fig. 4) was populated. These were designated "one-copy populated" boards.

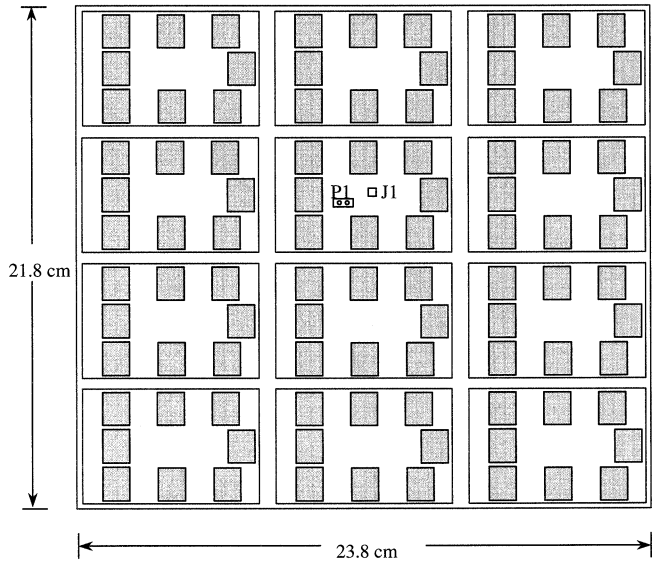

Fig. 5. Layout of 12-up boards.

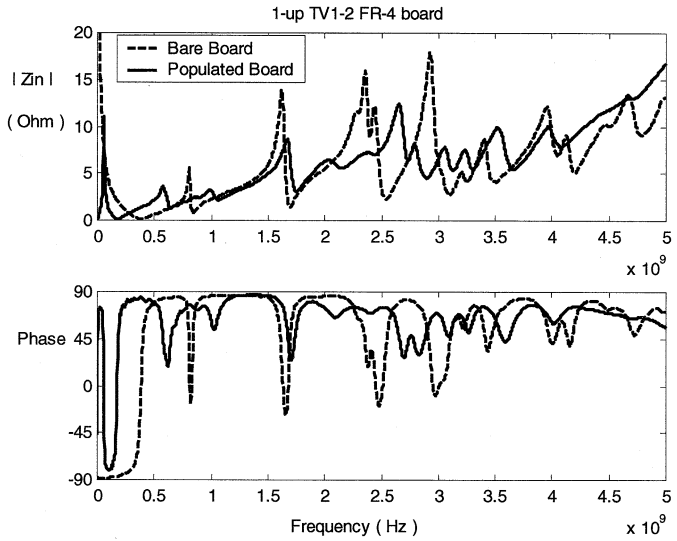

Fig. 6. Power-bus input impedance of one-up TV1–2 FR4 board: bare board versus populated version without discrete decoupling capacitors.

The 12-up layout consists of 12 copies of the basic layout in a 23.8-cm by 21.8-cm area. Again, the power and return planes are solid. Some of the boards were fully populated, while one-copy-populated boards only had components in the circuit located on the second row, second column as oriented in Fig. 5. The size of a 12-up board is approximately equal to the size of a motherboard in a personal computer.

III. Power-Bus Input Impedance Measurements

Since the power bus in an embedded capacitance board is designed to have low impedance at high frequencies (a few ohms or less), the active components look like relatively high-impedance sources due to their connection inductance (generally a nanohenry or more). Therefore, the power-bus voltage at one location due to the current drawn by a component at another location is approximately proportional to the transfer impedance between these two locations. At frequencies where the board is electrically small, the power-bus transfer impedance is equal to the power-bus input impedance. At higher frequencies, the transfer impedance depends on the location of the source and measurement ports. However, input impedance measurements over a broad frequency range still provide a good indication of the relative ability of the power bus to minimize delta-I noise.

The power-bus input impedance of each test board was measured using an HP8753D network analyzer. The SMA connector (J1) on the test board was connected to Port 1 of the network analyzer through a low-loss precision coaxial cable. A one-port calibration was performed to set the measurement plane to the end of the coaxial cable. Then, a port extension was performed with a shorted SMA connector to extend the measurement plane to the connector side (Layer 6) of the board. S11 was measured and converted to input impedance using a built-in function of the network analyzer. The measurements were performed between 30 kHz and 5 GHz.

Fig. 6 compares the measured power-bus input impedance of two one-up FR4 boards with the TV1–2 stack up. One is a bare (unpopulated) board; the other is populated with all the components except the 33 local decoupling capacitors. The spacing between the power and the return planes is about 19.4 mils for both samples. For the unpopulated board, the power-bus input impedance below 400 MHz is similar to that of an ideal capacitor. The peak around 800 MHz represents the first board resonance (TM10 mode of the rectangular power-bus structure). The peaks at higher frequencies represent higher order power-bus resonances. If a noise harmonic happens to occur around a board resonance, the resulting power-bus noise voltage will be pronounced.

The input impedance of the populated board has a sharp peak below 100 MHz due to the interconnect inductance of the 22-μF bulk decoupling capacitor resonating with the interplane capacitance. Power-bus resonances still dominate the impedance of the populated sample above 500 MHz, although they are slightly damped and shifted relative to the unpopulated board.

One disadvantage of discrete decoupling capacitors is their limited effective frequency range due to interconnect inductance. This is demonstrated in Fig. 7, which compares the power-bus impedance of two populated one-up TV1–1 FR4 boards with and without discrete decoupling capacitors [5]. The spacing between the power and return planes is about 4.5 mils for both test boards. The board without decoupling capacitors has a sharp resonance peak below 100 MHz similar to the peak observed in the measurement of the 19.4-mil TV1-2 board. This is not a board resonance, but rather a resonance between the board's inter-plane capacitance and the inductance of the of the 22-μF bulk decoupling capacitor. At low frequencies, the local decoupling capacitors do a good job of eliminating this resonance. However, above 500 MHz, the SMA decoupling capacitors have too much connection inductance of their own to be effective. There is no significant difference between these two curves above 500 MHz other than minor shifts in the power-bus resonance frequencies.

Fig. 8 compares the measured power-bus impedance of two embedded capacitance boards and a 4.5-mil FR4 board. All

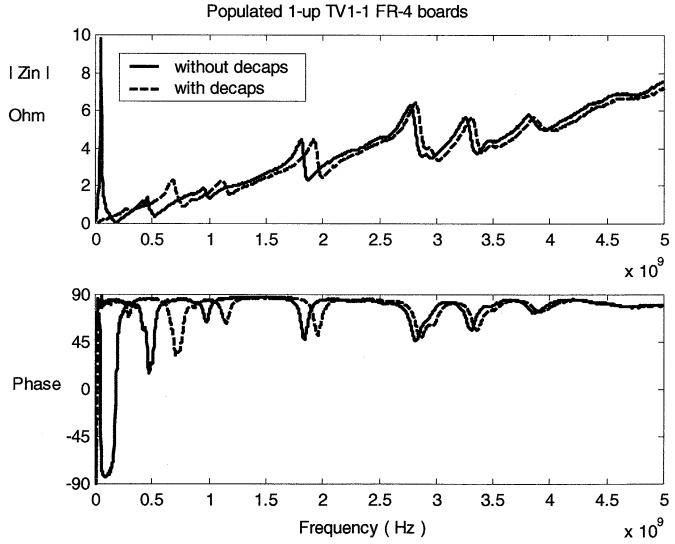

Fig. 7. Power-bus input impedance of populated one-up TV1–1 FR4 boards with and without discrete decoupling capacitors.

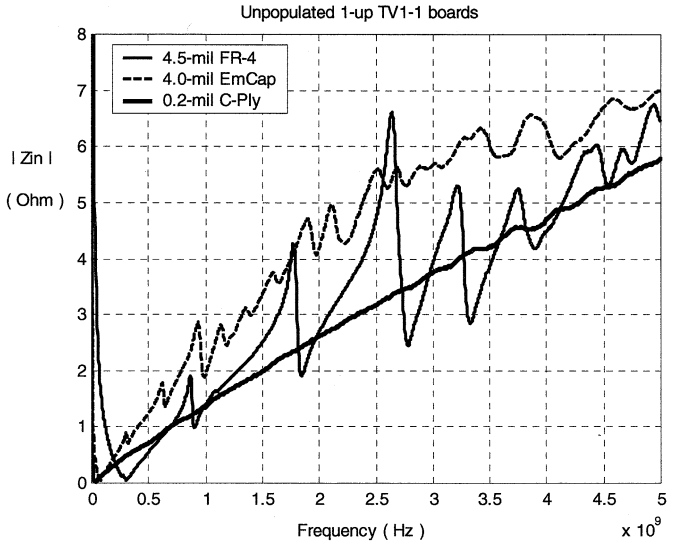

Fig. 8. Power-bus input impedance of unpopulated one-up TV1–1 boards with different dielectric materials.

three samples are unpopulated one-up boards with the TV1–1 stack up. Compared to the FR4 material, the EmCap material has a much higher relative permittivity. Consequently, in the same frequency range, the EmCap board exhibits many more power-bus resonances than the FR4 board. However, the resonance peaks in the EmCap curve are not as distinct as those in the FR4 curve. The resonances are more dampened even though the loss tangent of the EmCap material is slightly lower than that of FR4. The input impedance of the embedded capacitance board employing the 0.2-mil C-Ply material is a rather smooth upward slope. All resonances are significantly damped. The slope of this curve is mainly due to the small ($\sim$ 120 pH) inductance associated with the connection of the SMA jack to the power bus.

The relative performance of the embedded capacitance boards is further demonstrated in Fig. 9, which compares the power-bus input impedance of five one-up TV1–1 boards with

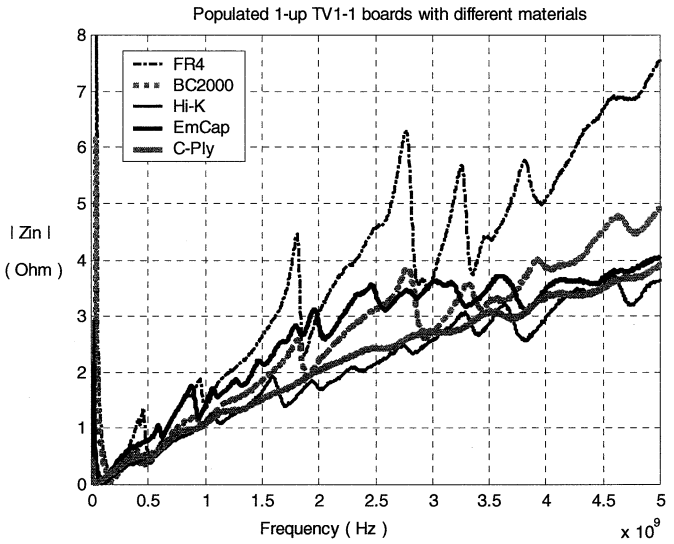

Fig. 9. Power-bus input impedance of populated one-up TV1–1 boards with different dielectric materials.

different dielectric materials [5]. All five samples are populated test boards without discrete decoupling capacitors. The spacing between the power and the return planes is 4.5 mils for the standard FR4 sample, 2.1 mils for the BC2000 sample, 1.4 mils for the Hi-K sample, 4.0 mils for the EmCap sample, and about 0.2 mils for the C-Ply sample. Again, the FR4 board exhibits the most significant power-bus resonance peaks. The power-bus resonances in BC2000 curve are also evident. In the EMCAP and Hi-K curves, power-bus resonances appear as ripples along with the slope. And the C-Ply curve is nearly a straight line.

Prior to this study, a major concern with embedded capacitance materials was that they would introduce more power-bus resonances (due to their higher permittivity) resulting in higher power-bus noise. However, the power-bus input impedance measurements show that the power-bus resonances in test boards with all four embedded capacitance materials are relatively damped compared to their FR4 counterparts. This observation is fully explained by modeling the power bus as a resonant cavity and accounting for the losses in the copper planes [6]. According to the cavity model, the magnitude of the power-bus input impedance near resonance is related to the quality factor (*Q*-factor) of the cavity structure. Among the various losses in the closely spaced power-return plane pair, the quality factor associated with the copper loss is approximately proportional to the spacing between the two solid planes. The conductive loss causes the quality factors to be very low in the embedded capacitance boards, which results in low power-bus resonance peaks. In particular, the calculated quality factor for power-bus resonances in the C-Ply boards is nearly 1 [6]. This explains why the power-bus input impedance curves for the C-Ply boards in Figs. 8 and 9 are almost straight lines.

IV. Time-Domain Power-Bus Noise Measurements

With the boards operational, the power-bus noise voltage of populated test samples was measured using a Tektronix TDS520A two-channel digitizing oscilloscope. The test board was directly hooked to Channel 1 of the oscilloscope through

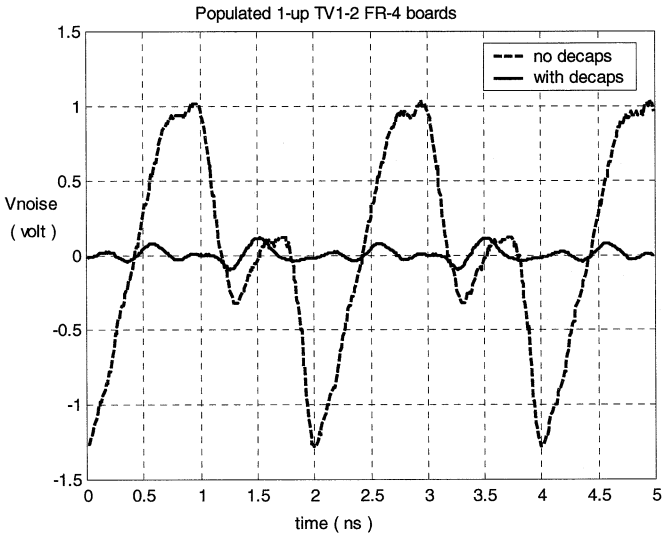

Fig. 10. Power-bus noise voltage on one-up TV1–2 FR4 boards with and without discrete decoupling capacitors.

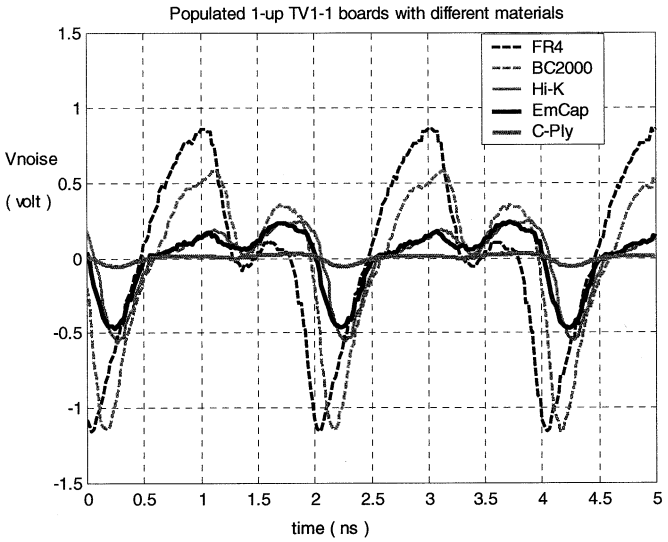

Fig. 11. Power-bus noise voltage on one-up TV1–1 boards with different dielectric materials.

the on-board SMA connector. The oscilloscope input was ac coupled and the input impedance was set to 50 ohms. The 3.3-V dc operating voltage was supplied through the 2-pin connector, P1.

Fig. 10 compares the measured power-bus noise for two one-up TV1–2 FR4 boards with and without decoupling capacitors. Both boards are populated with all the active components and the 22-μF bulk decoupling capacitor. As indicated by the transient waveforms, the time-domain power-bus noise exhibits a strong 50-MHz component with identifiable 100- and 150-MHz artifacts. Without discrete decoupling capacitors, the peak-to-peak noise voltage is more than 2 V for the FR4 board with a 3.3-V power supply. As might be expected, active components on this board had trouble operating consistently. The bulk decoupling capacitor on the FR4 board was not able to supply adequate current fast enough to meet the device requirements. With 33 0.01-μF local decoupling capacitors added to the board, the peak-to-peak noise voltage reduces to about 0.2 V as shown in Fig. 10. This dramatic improvement reflects the fact that the local decoupling capacitors are very effective in the 50–150-MHz frequency range.

Embedded capacitance boards utilize the interplane capacitance to supply the current required by active components. Fig. 11 compares the noise voltage waveforms of several one-up TV1–1 embedded capacitance boards to that of the FR4 sample. The spacing between the power and the return planes for the FR4 board is 4.5 mil. None of these boards has local decoupling capacitors mounted. The peak-to-peak noise voltages of these test boards are listed in Table II. Note that all four embedded capacitance boards exhibit lower noise voltages than the FR4 board without discrete decoupling capacitors. In particular, the peak-to-peak noise voltage of the 0.2-mil C-Ply sample is even lower than that of the FR4 sample with 33 discrete decoupling capacitors.

Table III lists the measured peak-to-peak noise voltages of four-up and 12-up boards made with different dielectric materials. All test samples are one-copy populated TV1–1 boards. Again, all the embedded capacitance boards exhibited less power-bus noise than their 3.3-mil FR4 counterpart without decoupling capacitors. Some embedded capacitance boards performed even better than the FR4 board with decoupling capacitors. For test boards employing the same dielectric material, enlarging the board area increases the interplane capacitance. Consequently, as we compare the data shown in Tables II and III for one-copy populated embedded capacitance boards, a 12-up board exhibits less noise than a four-up board with the same dielectric material, and a four-up board exhibits less noise than a one-up board with the same material.

TABLE II
PEAK-TO-PEAK NOISE VOLTAGE ON ONE-UP TV1–1 TEST BOARDS WITH DIFFERENT DIELECTRIC MATERIALS

Samples	1-up board $V_{p\text{-}p}$ (volt)
4.5-mil FR4 without decaps	2.04
4.5-mil FR4 with decaps	0.23
2.1-mil BC2000 without decaps	1.74
4.0-mil EmCap without decaps	0.71
1.4-mil Hi-K without decaps	0.82
0.2-mil C-Ply without decaps	0.09

TABLE III
PEAK-TO-PEAK NOISE VOLTAGE ON ONE-COPY POPULATED FOUR-UP AND 12-UP TV1–1 TEST BOARDS WITH DIFFERENT DIELECTRIC MATERIALS

Samples	one-copy populated 4-up boards	one-copy populated 12-up boards
	$V_{p\text{-}p}$ (volt)	$V_{p\text{-}p}$ (volt)
3.3-mil FR4 without decaps	1.30	0.46
3.3-mil FR4 with decaps	0.35	0.28
2.1-mil BC2000 without decaps	0.64	0.20
4.0-mil EmCap without decaps	0.31	0.21
1.4-mil Hi-K without decaps	0.17	0.06
0.2-mil C-Ply without decaps	0.03	N/A

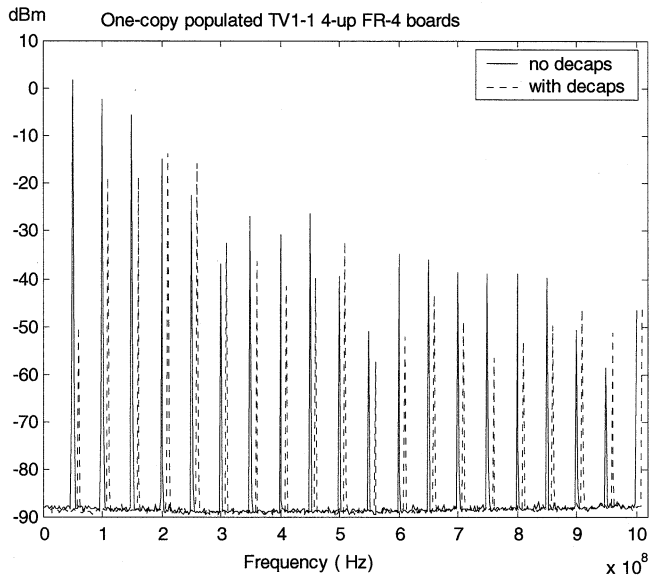

Fig. 12. Power-bus noise on one-copy populated four-up TV1–1 FR4 boards with and without discrete decoupling capacitors: 1 MHz – 1 GHz.

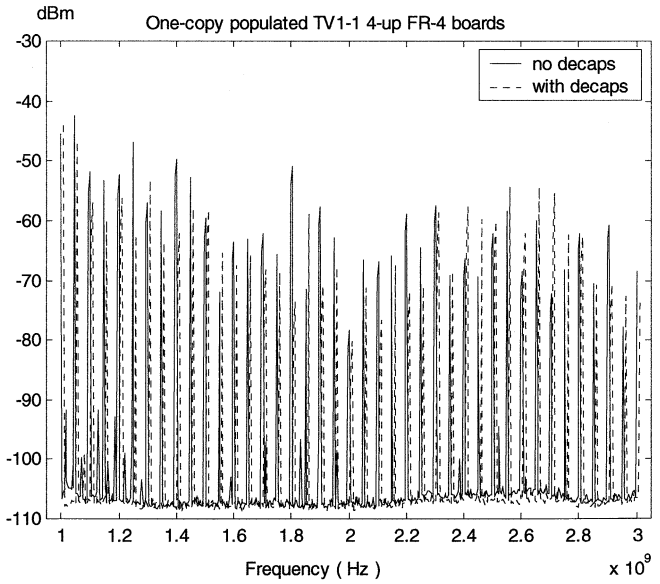

Fig. 13. Power-bus noise on one-copy populated four-up TV1–1 FR4 boards with and without discrete decoupling capacitors: 1 GHz–3 GHz.

In summary, the time-domain noise voltage peaks on these test boards are dominated by the decoupling performance at the first few harmonics of the clock signal. The measurement results indicate that the bulk decoupling capacitor is not capable of supplying enough current at 50 MHz or higher to efficiently attenuate the power-bus noise. Without other sources of decoupling, the noise voltage is so high that it interferes with the correct operation of the test board. Both the discrete decoupling capacitors and the embedded capacitance stabilize the power-bus voltage. However, the impedance measurements presented in Section III suggest that the discrete decoupling capacitors would not have been effective if the fundamental clock frequency had been greater than a few hundred megahertz. This can be demonstrated by measuring the power-bus noise in the frequency domain.

V. Frequency-Domain Power-Bus Noise Measurements

While the time-domain power-bus noise measurements only address the decoupling performance for the first few harmonics of the noise signal, frequency-domain measurement results provide broadband information about the power-bus noise performance. The power-bus noise spectrum of each populated board was measured using a Rohde & Schwarz FSEB30 spectrum analyzer. A 1-m-long SMA precision coaxial cable was used to connect the input port of the spectrum analyzer to the SMA jack on the populated test boards. Two ferrite chokes were placed around this SMA coaxial cable to reduce the common-mode current flowing on the exterior of the cable shield. In addition, a Rohde & Schwarz FSE-Z3 dc block was added to the RF input port of the spectrum analyzer to prevent direct dc input. In order to achieve a low noise floor and to keep the sweep time reasonable, the measurement was broken into three frequency bands: from 1 MHz to 1 GHz, from 1 to 3 GHz, and from 3 to 5 GHz. All boards were powered to 3.3 V for frequency-domain measurements.

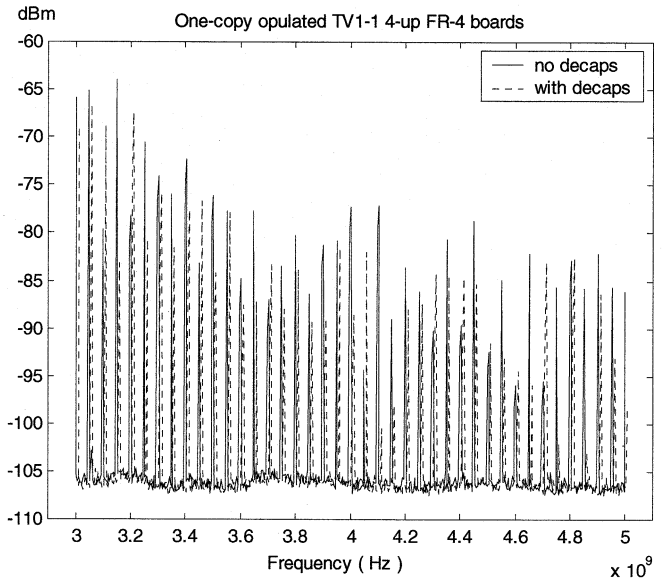

Fig. 14. Power-bus noise on one-copy populated four-up TV1–1 FR4 boards with and without discrete decoupling capacitors: 3 GHz–5 GHz.

The measured data for two one-copy populated four-up FR4 boards is plotted in Figs. 12–14 for each of the three frequency ranges. Both boards employ the TV1–1 stack up with a 3.3-mil spacing between the power and the return planes. One of the boards has the 33 local decoupling capacitors and one does not. The spikes in these plots represent power received at the 50-Ω input of the spectrum analyzer at a specific harmonic frequency. The dotted curves (for the boards with decoupling capacitors) are deliberately shifted by $+10$ MHz in order to make a comparison of the levels easier. As indicated in Fig. 12, adding decoupling capacitors significantly reduces the power-bus noise at the fundamental 50-MHz signal and the first two harmonics. This is consistent with the time-domain and the power-bus impedance measurement results. However, above a few hundred megahertz,

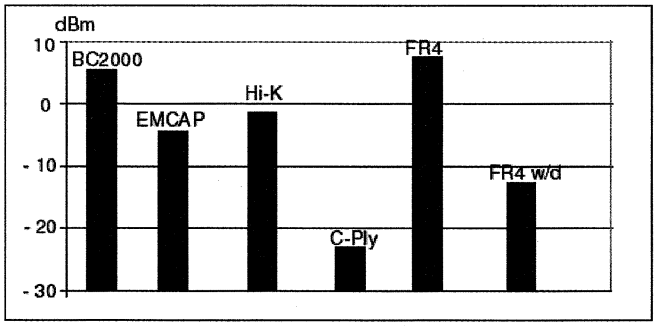

Fig. 15. Total power-bus noise on one-up TV1–1 boards with different dielectric materials between 1 MHz and 1 GHz.

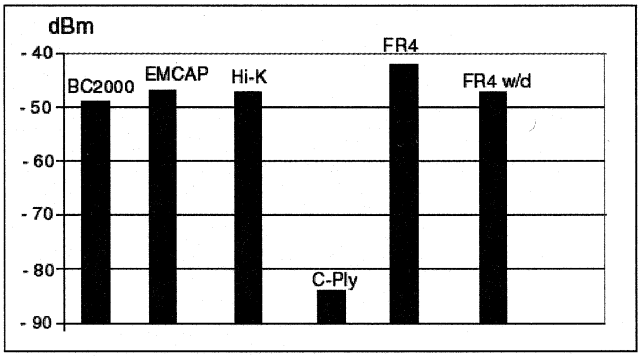

Fig. 16. Total power-bus noise on one-up TV1–1 boards with different dielectric materials between 1–3 GHz.

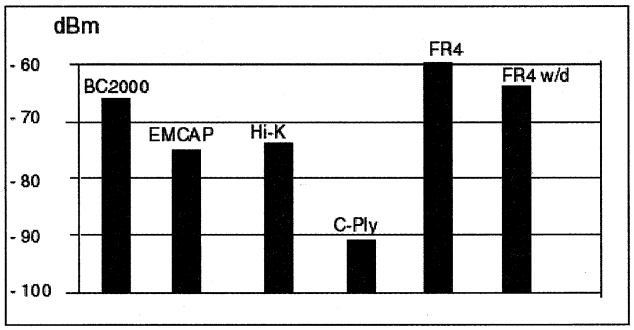

Fig. 17. Total power-bus noise on one-up TV1–1 boards with different dielectric materials between 3–5 GHz.

TABLE IV
POWER BUS NOISE ON ONE-COPY POPULATED BOARDS

Samples	1 MHz – 1 GHz (dBm)	1 GHz - 3 GHz (dBm)	3 GHz – 5 GHz (dBm)
1-up 2.1-mil BC2000	5.8	-47.2	-65.4
4-up 2.1-mil BC2000	-2.5	-48.8	-70.5
12-up 2.1-mil BC2000	-12.4	-50.8	-71.7
1-up 4.0-mil EmCap	-3.9	-46.8	-72.0
4-up 4.0-mil EmCap	-9.0	-51.1	-74.7
12-up 4.0-mil EmCap	-12.2	-53.1	-74.9
1-up 1.4-mil Hi-K	-0.9	-46.3	-72.6
4-up 1.4-mil Hi-K	-14.2	-53.4	-75.3
12-up 1.4-mil Hi-K	-24.1	-56.4	-76.7

the effectiveness of the discrete decoupling capacitors is questionable. Some harmonics are higher without the decoupling capacitors and some are higher with them.

It is inconvenient to evaluate the performance of different test boards by comparing the amplitudes of all 20–40 harmonics in each plot. So, in order to develop a criterion for comparison, the amplitude of the power at all harmonics in a specific frequency range is summed. For example, the total power in the twenty harmonics between 1 MHz and 1 GHz is calculated as

$$P_{\text{total}}(\text{decibel meters}) = 10\log_{10}\left(\sum_{n=1}^{20} 10^{P_n/10}\right)$$

where $P_{\mathbf{n}}$ is the power in the nth harmonic in decibel meters. The total power $P_{\mathbf{total}}$ is then used to determine the relative performance of different test boards.

Power-bus noise measurements for several one-up TV1–1 test samples with different materials are summarized in Fig. 15–17 for each of the three frequency ranges [5]. In these figures, each bar is labeled to indicate the dielectric material between the power and return planes. “FR4” in the label indicates the board is made with 3.3-mil FR4 material. “FR4w/d” indicates a 3.3-mil FR4 board with the 33 local decoupling capacitors mounted. The height of each bar indicates the total noise power in all harmonics within the measurement frequency range.

In the 1 MHz–1 GHz range, adding decoupling capacitors to an FR4 board reduces the power-bus noise by about 20 dB. However, in the medium and high frequency ranges, the difference between FR4 boards with and without decoupling capacitors is negligible. In all three ranges, test boards employing embedded capacitance materials exhibit less power-bus noise than the FR4 board without decoupling capacitors. Different materials perform differently and some are more efficient than others. In particular, boards made with the C-Ply material (which is much thinner than the other materials), consistently exhibit less power-bus noise than similar boards made with the other materials.

As indicated by the time-domain power-bus noise measurement, for one-copy populated embedded capacitance boards, increasing the board dimensions results in higher inter-plane capacitance, which helps to reduce the power-bus noise at low frequencies. However, when the board is no longer electrically small, increasing the board dimensions shifts the resonant frequencies, but does not necessarily reduce the power-bus input impedance or the power-bus noise. Table IV summarizes the power-bus noise results for one-copy populated test boards with three embedded capacitance materials: 2.1-mil BC2000, 4.0-mil EmCap, and 1.4-mil Hi-K. In the 1 MHz–1 GHz frequency range, the power-bus noise decreases considerably as the board area increases. In the higher frequency ranges, the effect of the board area is less significant, although the larger boards tended to have less power-bus noise.

VI. CONCLUSION

Four embedded capacitance materials were evaluated in this study. The experimental results show that embedded capacitance is a practical alternative to discrete decoupling capacitors for reducing power-bus noise. For PCBs with solid power and return planes, at low frequencies, the embedded capacitance was at least as effective as discrete capacitors with the same total capacitance value. At higher frequencies, the embedded capacitance is more efficient because the inductance of the connections

to the discrete capacitors limits the amount of charge they can supply in a very short time. At frequencies above a few hundred megahertz, the inductance of the connections to the local decoupling capacitors makes them relatively ineffective. The frequency at which discrete capacitors become ineffective depends on the relative inductance of their connections as compared to the impedance of the planes [1]. For most practical board geometries, with planes spaced 10 mils apart or less, discrete capacitors are ineffective at frequencies greater than a few hundred megahertz or less. For the boards evaluated in this study, the decoupling capacitors are ineffective above about 500 MHz.

At frequencies where the board is not electrically small, power-bus resonances can be a significant problem. Boards without sufficient loss in the power bus will exhibit very high impedance at power-bus resonances. If a source harmonic happens to occur near a board resonance that is not sufficiently damped, the power-bus noise voltage may be excessive. Loss is required to dampen board resonances. There are four primary sources of loss in PCBs with power-return plane pairs: dielectric loss, copper loss, component loss and radiation loss. Of these four, copper loss dominates if the plane spacing is comparable to the skin depth of the conductor on the two solid planes [6]. All four types of embedded capacitance evaluated in this study did a fair job of damping power-bus resonances. However, the C-Ply material, with its 0.2-mil plane spacing, was the only material to essentially eliminate these resonances.

The results presented here also demonstrated a correlation between power-bus impedance and power-bus noise. For test boards with the same layout, boards with high resonance peaks in the power-bus input impedance curve tended to have high power-bus noise.

In a given frequency range, embedded capacitance boards exhibit more power-bus resonances than FR4 boards due to the higher relative permittivity of the dielectric. However, the thinner plane spacing in embedded capacitance boards causes these resonances to be more damped relative to the FR4 boards. In particular, test boards with the 0.2-mil material essentially eliminated all power-bus resonances, and consistently exhibited less power-bus noise than similar boards made with the thicker materials.

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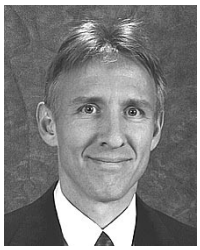

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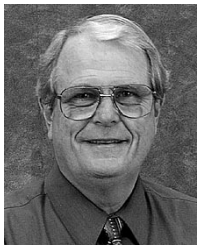

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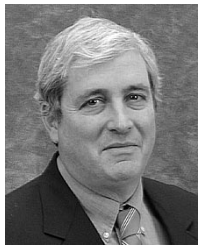

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