Power Decoupling Techniques for Micro-inverters in PV Systems-a Review

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Abstract--***This paper reviews the power decoupling techniques of micro-inverters used in single-phase, grid-tied PV systems. The power decoupling techniques are categorized into three groups: (1) PV side decoupling; (2) DC link decoupling; and (3) AC side decoupling. Various topologies and techniques are presented, compared, and evaluated against the size of capacitance, efficiency and control complexity. Finally, potential topologies and technologies are pointed out as the best options for power decoupling implementation.***

Index term- **Power Decoupling, Single phase Inverter, Photovoltaic, Micro-inverter**

I. INTRODUCTION

Over the past 15 years, the solar electric energy has grown consistently by 30%. The world solar photovoltaic (PV) market installation reached a record high of 7.2 GW in 2009, representing a growth of 130% over the previous year, in which grid-connected systems representing the largest majority of the market[1]. One of the key components of the grid-connected PV system is the grid-tied inverter.

Currently, the grid-tied inverter for PV system can be categorized into three categories: centralized inverter, string inverter, and micro-inverter [2,3]. Micro-inverters with power levels ranging from 150 to 300W have become the trend for future PV system development due to many reasons including (1) improved energy harvest; (2) ease of expandability; (3) lower installation costs; (4) "Plug-and-Play" operation; and (5) modular design with high economies of scale potential. However many challenges remain in the way of achieving low manufacturing costs, high conversion efficiencies, and long life span. Since micro-inverters are typically placed behind the PV panel, and may well be integrated on the PV panel's back skin, having an inverter lifespan that matches the PV panel's life is a major design consideration.

For applications with power level under several kilo-watts, the single phase connection is commonly used. However, single phase connection has the disadvantage that the power flow to the grid is time varying, while the power of the PV panel must be constant for maximizing energy harvest, which results in instantaneous input power mismatch with the output instantaneous AC power to the grid. Therefore, energy storage elements must be placed between the input and output to balance (decouple the unbalance) the different instantaneous input and output power. Usually, a capacitor is used to serve as a power decoupling element. However, the lifetime of different types of capacitors varies greatly, e.g. electrolytic capacitors typically have a limited lifetime, namely 1000~7000 hours at 105°C operating temperature[4]. Most of presently available commercial micro-inverters use electrolytic capacitors as power decoupling storage elements due to their large capacitance and ease of implementation, which tend to limit the lifespan of these micro-inverters. Some researchers have explored various ways to reduce the size of the required capacitance so as to allow for other longer life span capacitor technologies, such as film capacitors, to be used. This paper reviews the various power decoupling techniques that have been proposed and compares their performance in terms of efficiency, cost, and control complexity. The paper is organized as follows. The principle of power decoupling is presented in Section II. A review of the power decoupling techniques is presented in Section III. Section IV compares different power decoupling techniques. Some discussions are given in Section V with conclusion presented in Section VI.

II. PRINCIPLE OF POWER DECOUPLING

In a grid-connected single-phase inverter as shown in Fig.1, the injected current to the grid, $i(t)$, and the grid voltage, $u(t)$, are given by

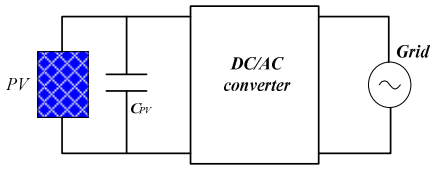


Fig.1: Single-Phase Inverter Architecture.

$$\begin{cases} u(t) = U\sin(\omega_o t) \\ i(t) = I\sin(\omega_o t + \varphi) \end{cases} \quad (1)$$

where ω_o is the grid frequency and φ is the phase difference between the injected current and the grid voltage, which is expected to be zero for unity power factor operation. The instantaneous output power, $P_o(t)$, is given as follows:

$$P_o(t) = \frac{1}{2}UI\cos(\varphi) + \frac{1}{2}UI\cos(2\omega t + \varphi) \quad (2)$$

With zero phase shift, this can be rewritten as

$$P_o(t) = \frac{1}{2}UI + \frac{1}{2}UI\cos(2\omega t) \quad (3)$$

The instantaneous power in (3) consists of two terms: the average output power, $P_{oav}=1/2UI$, which is constant and the second term, $P_{oac}=1/2UIcos(2wt)$, which is a time varying term (pulsating power) with twice the line frequency oscillation. As for the PV input terminals, the input power from the PV-Module, P_{PV}, is controlled to be constant. By ignoring the losses in the inverter stage, the power generated by the PV-module should be equal to the average output power as shown in Fig. 2.

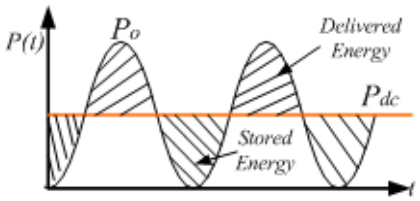


Fig.2: The total power processed by the decoupling capacitor

To maintain power balance, the pulsating power, P_{oac}, must be handled by an energy storage device. Usually, a capacitor (Decoupling Capacitor) is used to mitigate the power ripple effect at the PV-Module. This decoupling capacitor can be embedded within the inverter stage or just connected in parallel with the PV-Module. The value of the decoupling capacitor will be determined based on the amount of the energy that has to be stored in the capacitor, whose size is given by (4)

$$C = \frac{P_{dc}}{2\pi f U_{dc}\Delta u} \quad (4)$$

where f is line frequency, P_{dc} is the rated power from PV panel, U_{dc} is the mean voltage across the capacitor, Δu is the allowed peak-to-peak variations / ripple. As expressed in (4), for a micro-inverter with a given power rating and line frequency, the size of the capacitor is determined by DC voltage and maximum allowable voltage ripple.

III. POWER DECOUPLING TECHNIQUES

Implementing power decoupling techniques depend on the specific micro inverter topology employed. Micro-inverter topologies can be classified into single-stage and multi-stage inverters[2][3]. The single stage inverters, as shown in Fig.3, implement the step-up voltage conversion and sine or rectified sine waveform modulation in a single power stage. In this case, the power decoupling capacitor has to be placed at the PV side. As for multi-stage inverters, they can be further classified into DC-DC-AC, DC-AC-DC-AC, and DC-AC-AC as shown in Fig.4. For the topologies with DC-DC-AC configurations, the first power stage usually is used to boost the low PV voltage to a high DC voltage level compatible with the grid voltage. In this case, it is better to place the decoupling capacitor on the high voltage DC side compared to that at PV side since the size of the capacitor can be smaller.

In DC-AC-DC-AC configurations, a high frequency transformer in the first power stage is used for both boosting the PV voltage and electrically isolating the PV panel from the grid. The power decoupling capacitor can be placed either at the high voltage DC link or at the output AC side. Cyclone converters, changing high frequency AC to line frequency AC, are used in topologies with DC-AC-AC implementation, in which the power decoupling capacitor can only be placed at the PV side or at the AC side. Based on the location of the decoupling capacitor and circuitry, three decoupling techniques can be identified: (1) PV side decoupling; (2) DC link decoupling; and (3) AC side decoupling.

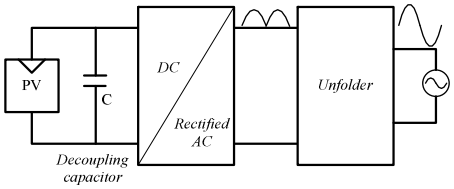
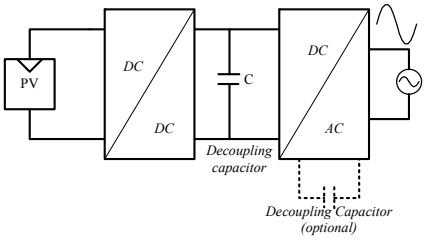
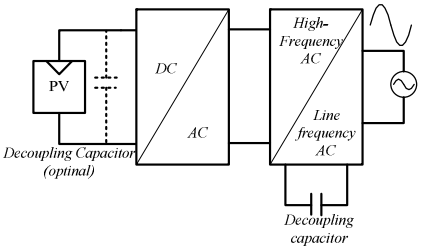


Fig.3: single stage inverter



(a) DC-DC-AC architecture



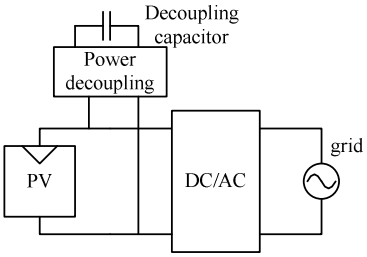
(b) DC-AC-AC architecture

Fig.4: Multi-stage inverter

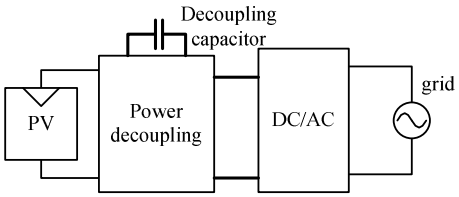
A. PV side Decoupling

In a single stage micro-inverter topology as shown in Fig. 3, having the power capacitor across the PV panel DC output terminals results in a very large capacitor since the allowable voltage ripple must be held to very low values (<1%) to realize an efficient MPPT process. As an example, for a rated 200W micro-inverter, the minimum decoupling capacitance required is 13.9mF in order to achieve a 98% PV utilization factor [2]. This represents a very large value, which increases the size of the micro-inverter and may negatively impact its life span. One potential solution to this problem is to use an

additional circuitry to decouple the AC pulsating power while maintaining the MPP voltage stable as shown in Fig. 5.



(c) Decoupling circuit in Parallel with PV



(d) Decoupling circuit in series with PV

Fig.5: Employing power stage to realize power decoupling

A bidirectional buck-boost converter was proposed by Kyritsis [5] to realize the power decoupling as shown in Fig. 6. With this active filter technique, the decoupling capacitor Cd is reduced from 3000uF to 100uF by increasing the average voltage and ripple voltage across the decoupling capacitor to 62V and 35V, respectively. Current hysteresis control is employed to control the current and make it follow a given reference. Although in [5] no specific number regarding the overall inverter efficiency is mentioned, the power losses associated with the decoupling circuit will reduce the overall efficiency. Moreover, using a smaller decoupling capacitor leads to higher stresses for the power devices, which may result in more losses and lower efficiency.

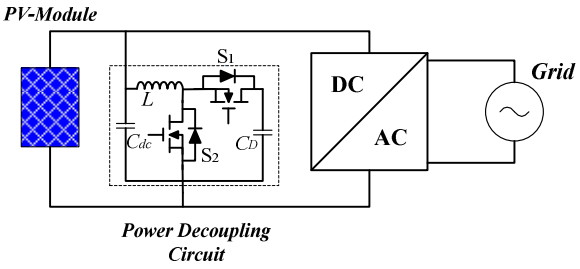


Fig.6: CPS-PAF topology proposed by Kyritsis, et al. [5].

The topology shown in Fig. 7 is a flyback-type single-stage micro-inverter with a decoupling power circuit, in which a 40uF film capacitor was used for a 100Watt micro-inverter design. In this proposed topology, the constant power from PV is first transferred to the decoupling capacitor C_D, which is then modulated with a rectified sine waveform and pumped into the grid. Given the the cascaded conversion process, the projected efficiency will be low, as indicated in [6] where the peak efficiency reported was only 70%.

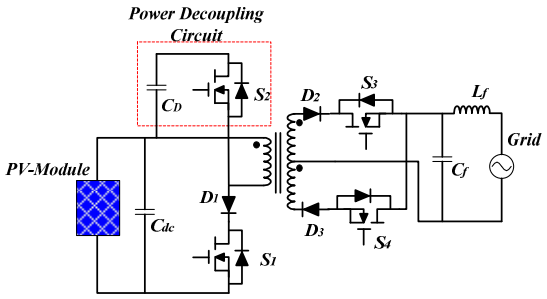


Fig.7: Topology proposed by Shimizu, et al. [6].

Fig. 8 shows a modified topology proposed by Kjaer [7] where the leakage inductance energy is recycled by using a "dual-switch flyback converter". Even with design optimization, the peak efficiency estimated was 86.7%. However, it should be noted that the topology in Fig. 7 already used the decoupling circuit as a snubber to absorb the leakage energy.

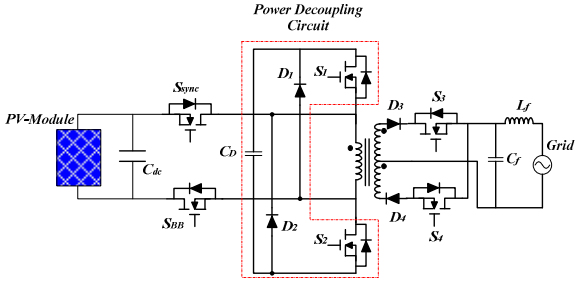


Fig.8: Modified topology proposed by *Kjaer* [7]

Tan [8] combined the boost and flyback topologies to propose a new topology to implement the power decoupling as shown in Fig. 9, which can be viewed as a two-stage power conversion with first stage processing the DC power from PV and the second stage implementing the AC power modulation. Using this technique, the size of the decoupling capacitor will be reduced due to the relatively higher voltage and larger voltage ripple allowed.

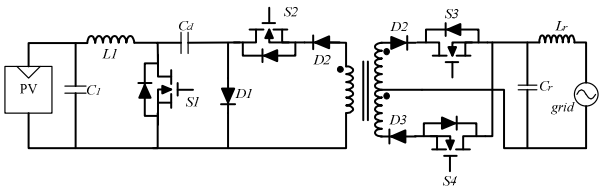


Fig.9: Decoupling power circuit proposed by Tan [8]

B. *DC Link Decoupling*

For a multi-stage micro-inverter design, the main power decoupling capacitor is placed at the high voltage DC link as shown in Fig. 4(a). Unlike PV side decoupling, where the PV nominal voltage is fixed and the voltage ripple should be limited to a very small range to maximize the energy harvest from the PV, DC link decoupling allows for a higher DC link voltage as well as a higher voltage ripple voltage thus reducing the size of the decoupling capacitance. The minimum

required decoupling capacitance can be calculated according to (4).

By reducing the value of decoupling capacitance, a large voltage ripple will be present across the DC link, which may result in deterioration of the output current waveform. To resolve this issue, several control techniques have been proposed. The simple method to mitigate the DC voltage ripple impact on the control system is to decouple the DC voltage as proposed by Enjeti [9], in which a modified modulation strategy to reject the DC-link voltage ripple in the control system is proposed as illustrated in Fig.10. Brekken [10] proposed a control technique (Fig. 11) that allows for 25% ripple voltage without distorting the output current waveform. In this design, the voltage loop cutoff frequency was designed at 10Hz, greatly attenuating the double line frequency DC voltage ripple in the control loop. However, with such low cutoff frequency, the proposed control system definitely degrades the system dynamic performance.

To achieve a higher bandwidth for the voltage control loop, Ninad [11] proposed a DC voltage ripple estimation control strategy as shown in Fig.12, in which no DC voltage ripple is fed to the DC voltage regulator by subtracting DC voltage from the estimated voltage ripple. In this manner, the DC voltage regulator can achieve a faster transient response. Many works have been done in this area[12-18]

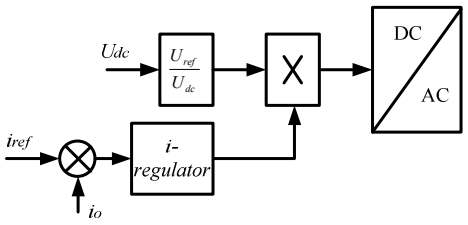


Fig.10. Modulation technique proposed by Enjeti [9]

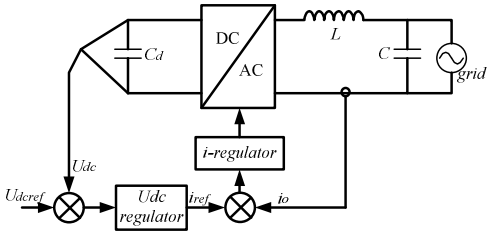


Fig. 11. Control proposed by Brekken[10]

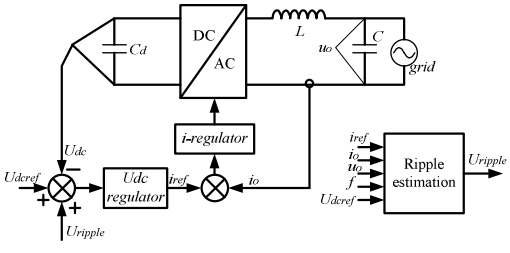


Fig.12: voltage ripple estimation strategy for large DC ripple proposed by Nayeem A. Ninad[11]

C. AC Side Decoupling

In AC side decoupling circuits, the decoupling capacitor is usually embedded in the inverter stage itself, where the voltage across the capacitor terminals is controlled. Because of the high voltage swing at the AC side, the capacitor value can be small and a non-polarized (film) capacitor can be used. In topologies that employ this kind of decoupling, bi-directional switches are required to provide a path for the positive and negative currents. The possible integration of the bi-directional switch and its driver circuit will simplify these topologies and enhance the overall system reliability. Two Topologies that employ AC side decoupling are shown in Fig. 13 and Fig. 14. The concept in both topologies is quite similar. An additional phase leg is added to the ac-side to connect the decoupling capacitor between the inverter and the grid. Both topologies are based on the current source inverter (CSI) implementation.

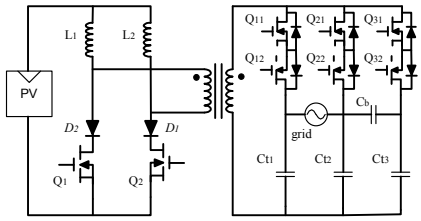


Fig.13: Topology proposed by Q. Li, P. Wolf, S. Senini et. al.[19]

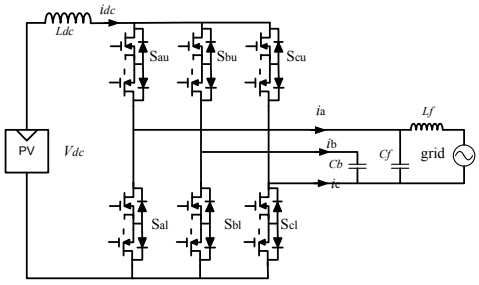


Fig.14: Topology proposed by C. Bush, B. Wang et. al. [20]

IV. Decoupling Circuits' Performance Comparison

The power decoupling techniques presented above will impact the overall system reliability, cost, and efficiency. For the efficiency comparisons, we use η_0 as the conversion efficiency without the power decoupling circuit while η_d is the efficiency with the added power decoupling circuit. The power process in the grid-connected PV system with power decoupling circuit is shown in Fig. 15.

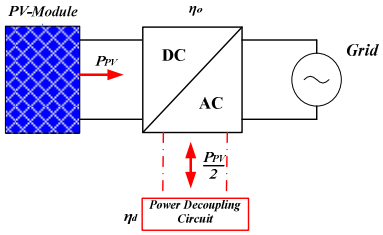


Fig.15: The Power Process in the PV system

The main inversion stage will process the total power from the PV-Module while at least half of that power is processed by the decoupling circuit. For an optimal design of the power decoupling circuit, the average power level processed by the decoupling circuit should be $P_{PV}/2$. Therefore, the best efficiency with the decoupling circuit is expected to be $\eta_0 - \frac{1-\eta_d}{2}$. Table 1 shows the comparison results of the various decoupling techniques with respect to the size of decoupling capacitor, the added cost, the efficiency impact, and the decoupling control circuit complexity. For PV side decoupling techniques, from and efficiency aspect, having the decoupling capacitor directly across the PV output terminals would be the best choice. However, the capacitance is quite large, which will increase the cost, reduce the power density, and lifetime. As for DC link decoupling techniques, the cost is low due to the fact that no additional circuitry or controls is needed, and the efficiency will be relatively high. However, these techniques can only apply to the multi-stage inverters with DC link implementation. As for the AC side decoupling techniques, the capacitance can be very small due to the high voltage swing. However, another leg or phase has to be added, which will increase cost, especially in the aforementioned two current-source based topologies which need bidirectional switches.

Tab.1: Performance Comparison of the Various Power Decoupling Techniques

Decoupling techniques		*Power rating(W)*	*decoupling capacitor*	*Additional Cost*	*Efficiency*	*Control Complexity*
PV side Decoupling	Fig.3	200	13.9mF	Capacitor	η_1	No control
	Fig.6	70	100uF	Capacitor+2 switches+1 inductor	η_0-(1- η_d)/2	Active filter control
	Fig.7	100	40uF	Capacitor+1 switch	η_0-2(1- η_d)	Peak current control
	Fig.8	156	314uF	Capacitor+2 switches	η_0-2(1- η_d)	Peak current control
	Fig.9	500	50uF	Capacitor+1 switch+1 inductor	$\eta_0 * \eta_d$	control for Boost +Flyback
	Fig.10	-	-	Capacitor	η_0	DC voltage Feed-forward control
	Fig.11	200	15uF	Capacitor	η_0	Low voltage loop bandwidth
	Fig.12	100	500uF	Capacitor	η_0	Voltage ripple estimation
AC side Decoupling	Fig.13	100	5.53uF	Capacitor+2 switches	η_0-(1- η_d)/2	three-phase current modulation
	Fig.14	-	-	Capacitor+2 switches	η_0-(1- η_d)/2	Modified three-phase current modulation

V. DISCUSSION

In single-stage micro-inverter designs, power decoupling circuits can reduce the size of the required energy storage capacitor, thus improving the inverter's life span. However, the power decoupling circuit will result in additional power losses since the power flows through the decoupling circuit, resulting in a lower efficiency. Meanwhile, the power decoupling circuit may increase the total system cost due to the additional circuitry required. To reduce the decoupling circuit power loss, the power processed by the decoupling circuit should be minimal and limited to $P_{PV}/2$ as proposed in Fig. 8. On the other hand, to reduce the cost of decoupling circuit, a three-port converter may be one of best choices with one port implementing MPPT and a second port dedicated to power decoupling. Following are two examples using the third port to realize the power decoupling as shown in Figs.16 and17.[21][22]. Other multi-port topologies found in references[23][24] can be also be tailored to implement single-phase inverters.

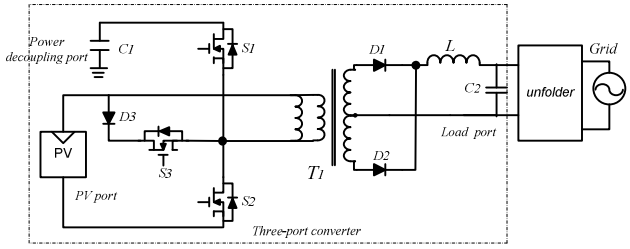


Fig.16: An integrated three-port inverter with power decoupling capability[21]

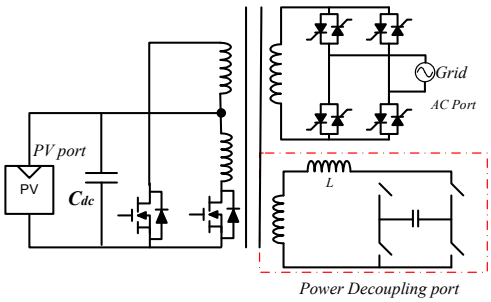


Fig.17: AC link implementation of three-port converter[22]

For multi stage micro-inverter designs, which incorporate a DC link, the power decoupling employing a high voltage DC bus capacitor may be the best choice for its simplicity, low cost, and high efficiency. To reduce the decoupling capacitance, a higher DC link voltage as well as a higher voltage ripple can be used with the constraint that the lowest DC link voltage should be greater or equal than the peak grid voltage. Fig.18 shows the corresponding waveforms of the voltage across the decoupling capacitor and the output AC voltage. The minimum required decoupling capacitance can be calculated according to (4). For a 200W, 110Vac micro-inverter design, the relationship between the minimal capacitance (C_{min}), the DC voltage(V_{DC}), and peak-peak voltage ripple ($r = \frac{\Delta V}{V_{DC}}$) is depicted in Fig.19. With sophisticated control strategies, the voltage ripple can be made much larger[17].

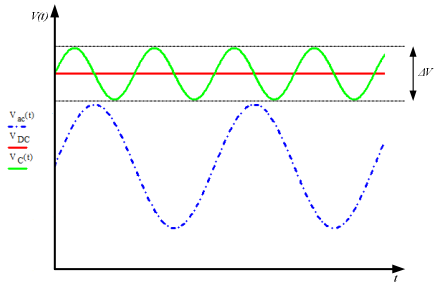


Fig.18: Output voltage and capacitor voltage waveforms.

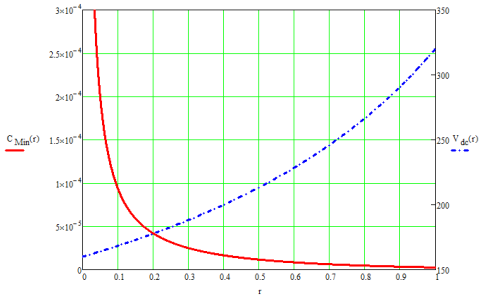


Fig.19: The relationship between the minimum decoupling capacitance, the DC voltage level, and the voltage ripple

AC side decoupling follows the suit of the multi-phase power systems, where the power flow could be constant with time-varying power in each phase. Configuring the second phase with specific constraints will realize the required power decoupling, whose capacitance can be much smaller than the value used in the above mentioned techniques. However, the small capacitance is achieved at the cost of overall efficiency and control complexity.

I. Conclusion

This paper reviews various power decoupling techniques that can be employed in single-phase micro-inverters to reduce the size of the energy storage capacitor size and improve the inverter life expectancy. For single stage inverters, the decoupling capacitor is placed across PV output terminals resulting in a large size capacitor. PV side power decoupling circuits can be employed to reduce the capacitor size. However, the overall inverter efficiency is greatly impacted. Three-port converters may offer better alternatives for single stage inverters due to their lower cost and higher efficiency. For multi stage micro-inverter topologies with DC link, the DC link capacitors offer the best alternative for power decoupling. Sophisticated control strategies can be employed to allow for higher voltage ripple, thus reducing the size of the DC decoupling capacitor. Finally, AC side decoupling involves incorporating a second phase to implement the power decoupling, where a very small capacitance is required.

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