Power Delivery Design for 3-D ICs Using Different Through-Silicon Via (TSV) Technologies

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***Abstract*—3-D integrated circuits promise high bandwidth, low latency, low device power, and a small form factor. Increased device density and asymmetrical packaging, however, renders the design of 3-D power delivery a challenge. We investigate in this paper various methods to improve 3-D power delivery. We analyze the impact of through-silicon via (TSV) size and spacing, of controlled collapse chip connection (C4) spacing, and of dedicated power delivery TSVs. In addition to considering typical cylindrical or square metal-filled TSVs (core TSVs), we also investigate using coaxial TSVs for power delivery resulting in reduced routing blockages and added coupling capacitance. Our 3-D evaluation system is composed of a quad-core chip multiprocessor, a memory die, and an accelerator engine, and it is evaluated using representative SPEC benchmark traces. This is the first detailed architectural-level analysis for 3-D power delivery. Our findings provide clear guidelines for 3-D power delivery design. More importantly, we show that it is possible to achieve 2-D-like, or even better, power quality by increasing C4 granularity and by selecting suitable TSV size and spacing.**

***Index Terms*—3-D integrated circuit (IC), 3-D integration, coaxial through-silicon via (TSV), power delivery, power grid, TSV.**

I. Introduction

MOORE's law has inspired the growth of integrated circuit (IC) technology since its inception in 1965. IC technology has shifted in the last two-decades from being device centric to one where interconnect plays an equally important role. The trend continues. By 2012, for 35-nm technology node, latency for 1-mm-long interconnect is expected to be 100 times larger than that of a corresponding transistor [1]. 3-D stacking technology has the potential to keep pace with the performance improvement projected by Moore's law. The length of global wires can be reduced by as much as 50%, wire-limited clock frequency can be increased by 3.9×, and wire-limited area can be decreased by 84% [2]. Power can be reduced by 51% at the 45-nm technology node [3]. The 2007 International Technology Roadmap for Semiconductor (ITRS) predicts that by 2015, industry will have 14 and 5 dies stacked in a single package for low-cost handheld and high-performance chips, respectively.

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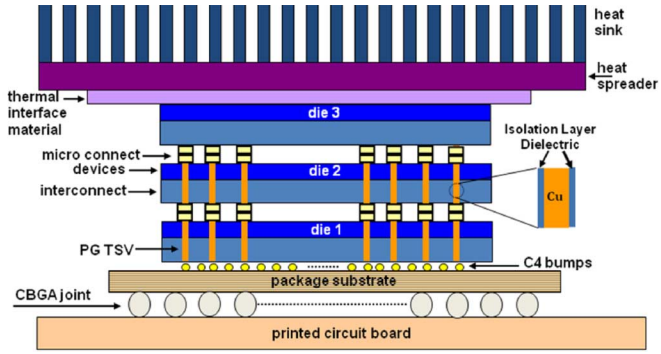

Fig. 1. Illustrative 3-D system assuming face-to-back metallic bonding with microconnects.

Robust power delivery is one of the ITRS scaling grand challenges due to increasing operating frequencies, increasing power density, and decreasing supply voltages. 3-D integration poses grander power delivery challenges for two reasons: increased power density and package asymmetry. Contrast a 3-D IC with a functionally comparable 2-D IC. The average wire length for a 3-D IC drops by a factor of $N^{1/2}$ where N is the number of stacked dies in 3-D, and the wire resistance and capacitance decreases proportionally [4]. Assuming that design is interconnect-dominated, power is expected to drop by a factor of $N^{1/2}$. If the power density of each die in 3-D is similar to that in the 2-D case and each die size is $1/N$ of that in the 2-D case, the power density per square area for the stacked 3-D chip increases by a factor of $N^{1/2}$. The power delivery requirements thus increase with the number of dies in the stack.

To understand the impact of package asymmetry on power delivery, consider the illustrative example in Fig. 1. Three dies are stacked between the heat sink and the package substrate. Electric signals and power are routed from the printed circuit board to the package substrate through ceramic ball grid array (CBGA) joints, and then they are distributed utilizing controlled collapse chip connection (C4) bumps. The dies are bonded using microconnects. Through-silicon vias (TSVs) pass through a die, as shown, and provide electrical connectivity for signals or power delivery among the layers. Clearly, the package asymmetry impacts both power delivery and heat removal, another critical challenge in 3-D ICs.. While thermal issues have received considerable attention (e.g., [5]–[8]), 3-D power delivery has not yet been adequately addressed.

We evaluate in this paper several 3-D power delivery configurations with the goal of understanding the major factors that impact the quality of 3-D power delivery networks (PDN). PDN quality is measured in terms of maximum and average

IR drops, Ldi/dt droop, and their standard deviations. These metrics quantify local and global PDN characteristics in both dc and transient analysis. Our 3-D evaluation is performed in reference to a comparable 2-D PDN for a 2-D chip design of the same functional modules. Our evaluation framework consists of a four-core chip multiprocessor (CMP), a memory, and an accelerator engine (ACCL) that is similar in activity to a core's floating point unit (FPU) representing an FPU accelerator. We use realistic workloads from SPEC benchmarks for each functional module in the system. The PDN for 2-D and 3-D designs has both an off-chip and an on-chip component. In the 3-D PDN, we consider the use of two types of TSVs. A *core TSV* refers to the common TSV scheme where cylindrical or square conductive metal layer is surrounded by an isolation layer. In a *coaxial TSV*, the conductive metal and isolation layer is further surrounded by another layer of conductive metal and isolation material. We analyze the impact of TSV size, TSV spacing, and C4 spacing in our 3-D PDNs. The major contributions of our work are as follows.

- We perform the first comparative study of system-level power delivery for 2-D and 3-D ICs utilizing realistic workloads, and we investigate methods for achieving 2-D-like PDN quality in 3-D PDNs.
- As TSVs occupy valuable die real-estate, we analyze the impact of TSV size and spacing to analyze the tradeoffs between TSV area and PDN quality.
- We study the use coaxial TSVs for power delivery and assess the benefits in terms of the number of routing blockages, coupling capacitance, and sharing signal and power routing.
- We summarize our findings in the form of *"Best Practices for 3-D PDN Design and Optimization*".

This paper is organized as follows. We begin in Section II with relevant background information on 3-D integration technology and a review of the state of the art in 3-D power delivery modeling and analysis. We then provide in Section III the details of our design setup. In Section IV, we perform the analysis to find the optimal TSV size for 3-D PDN. In Section V, we present different comparative studies between 2-D and 3-D PDNs using square TSV. Analysis of power delivery using coaxial TSVs is presented in Section VI. We then present the 3-D PDN design guidelines in Section VII, and conclude our work in Section VIII.

II. Background and Previous Work

A. 3-D Integration Technology

Wafer bonding is a common technique for 3-D integration. Two or more wafers, fabricated using their own process, can be bonded together. Multiple processes exist for bonding wafers or dies. The two common techniques are dielectric, and metallic bonding. In dielectric (oxide or polymer based) bonding, vertical connections are completed after the bonding process. This bonding technique uses through-strata or 3-D vias that pass through the top die and connect to the conventional interconnect in the bottom die [9], [10]. In metallic bonding, the vertical connections are formed by bonding conductive microconnects of Copper (Cu) or Cu with a plating of Tin on each bonding surface as shown in Fig. 1 [11], [12]. The bonded microconnects typically have a pitch in the range of 20 to 60 μm, which is expected to improve with future development to allow for higher density inter-layer connections.

If the bonding orientation is face-to-back, where face refers to the metal interconnect side and back refers to the Si substrate side, a TSV is also required to connect a signal to the microconnect as demonstrated in Fig. 1. TSVs are filled with metal, preferably Cu due to its low resistivity, and separated by dielectric liners from the Si substrate. ITRS predicts that the maximum number of TSVs in a high performance 3-D stacked chip will reach 1000 in 2012 and increase by 1000 in every two years. As TSV area competes with active device area similar to 3-D vias in dielectric bonding, smaller TSV sizes are desirable. Manufacturing constraints associated with TSV etch and via filling dictate the TSV size. Smaller TSV size requires the Si substrate to be thinned to a thickness of 100 to 10 μm or even less in bulk CMOS technology [12]. Using a practical aspect ratio of 10:1 or lower, the TSV size would be 5 μm or more when the Si substrate is thinned to 50 μm. In this work, our model assumes that 3-D chips are formed with metallic microconnect bonding and that Cu-filled TSVs are used for vertical interconnects in conjunction with the microconnects at the bonded interface. While this assumption is an attractive integration scheme in pursuit by many leading manufacturers, our analysis methodologies are not limited to any one form of 3-D. Our analysis methodology can be applied to other forms of stacked 3-D chips using their parasitic elements for vertical interconnects. We consider two types of TSVs in our work, core and coaxial, that are described next.

B. Core Versus Coaxial TSV

A core TSV in this work refers to the most common TSV scheme where a cylindrical or square conductive metal layer is surrounded by an isolation layer [see Fig. 2(a)]. Due to a thin isolation dielectric (ILD) layer and large extension through Si, electrical parasitic coupling and critical substrate noise can occur in neighboring active devices and between two TSVs. Signal transmission in TSVs impacts neighboring transistor body voltage such that circuit performance in both digital and analog applications are significantly impacted despite placing substrate ties to ground next to TSVs [13], [33]. Coaxial TSVs, first proposed in [14] and illustrated in Fig. 2(b), can eliminate substrate noise by grounding the outer metal layer while the inner metal layer is used for signal transmission [33]. While the details of TSV fabrication, a research area on its own, are beyond the scope of this work, we will assume TSV dimensions that adhere to manufacturability constraints, such as TSV aspect ratio and ILD thickness. Readers are referred to [15], [16], and [17] for processes associated with TSV formations. While the maturity of processes and volume manufacturability are in active development, significant value exists in early research on potential usage and circuit design to aid in technology/circuit/system co-development.

TSVs and microconnects can be modeled as resistance–inductance–capacitance (*RLC*) elements. For a Cu-filled TSV of

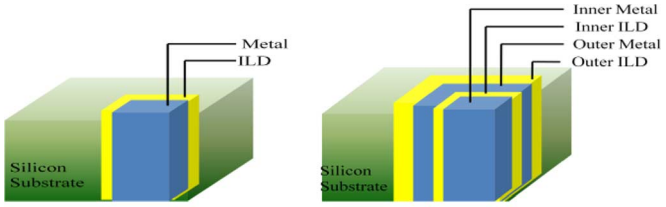

Fig. 2. Cross-section of a core and a coaxial through silicon vias (TSVs): (a) core TSV; (b) coaxial TSV.

height h_{via}, cross-section area A_{eff}, sidewall area S_a, and sidewall dielectric thickness t_{ILD}, we estimate the resistance R and sidewall capacitance C using

$$R = \frac{\rho_{\text{cu}} h_{\text{via}}}{A_{\text{eff}}} \tag{1}$$

$$C = \frac{\varepsilon_r \varepsilon_0 S_a}{t_{\text{ILD}}} \tag{2}$$

where ρ_{cu} is the resistivity of Cu, ε_r and ε_o are the relative permittivity of SiO_2 and permittivity of space, respectively. For a square TSV, (1) and (2) can be applied directly. For a coaxial TSV, each metal layer has its own R and C values. According to an analytical and electrostatic simulation-based study by Alam *et al.* [11], a square TSV of width 5 μm and height 50 μm has a resistance of 43 mΩ and a capacitance of 40 fF. A microconnect of width 5 μm has a resistance of 40 mΩ and a capacitance of 0.4 fF. The outer sidewall capacitance of a coaxial TSV is the same as that of a square TSV. The inner sidewall capacitance, however, can be much higher than that of the square TSV. For example, a coaxial TSV with an inner electrode of the same dimensions as that of the square TSV and an ILD thickness of 20 nm results in a capacitance of $\sim$ 2 pF. We use these values and scale them for different TSV/microconnect sizes while the TSV height will remain fixed at 50 μm. Such TSV scaling is in agreement with the aspect ratio constraint of 10:1 or lower needed for manufacturability.

Accurate inductance characterization is more complex as it is essential to include a return path directly based on the design and layout of specific interface circuitry. However, TSV inductance is expected to be low especially in comparison to off-chip inductance. Multiple studies as in [11], [18], and [19], based on simulation as well as test structure measurements, demonstrate that TSV inductance is low, in the range of 0.3–0.9 pH per μm of TSV length.

C. Previous Work in 3-D Power Delivery Analysis

Previous work on 3-D power delivery can be summarized under two main themes: power delivery techniques and power integrity analysis. Kim *et al.* analyzed a multistory power delivery technique where a higher than nominal Vdd supply voltage is applied from the package and distributed differentially to subsequent power rails using level conversion [20]. Their work utilized lumped off-chip and on-chip models with tungsten filled TSVs in bonded SOI technology to assess the impedance

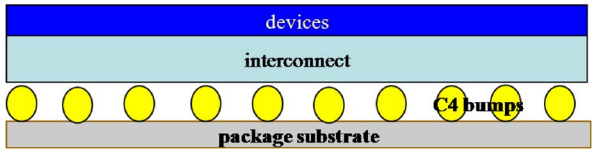

Fig. 3. Cross-section view of the 2-D chip.

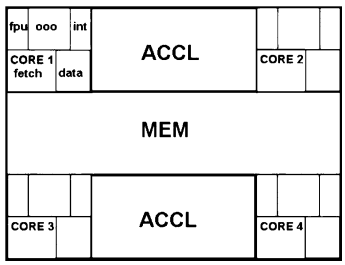

Fig. 4. Floorplan of the 2-D architecture.

response of overly simplified lumped 2-D and 3-D PDNs. Yu *et al.* investigated the impact of via stapling, where a 3-D mesh is created, on both power and thermal integrity [8]. Zhan, Zhang, and Sapatnekar proposed a partition-based algorithm for assigning modules at the floorplanning level to reuse currents between Vdd domains, and to minimize power wasted during circuit operation [21]. In the power integrity analysis area, Huang *et al.* proposed an analytical physical model of 3-D power grid network, accurate within 4% compared to SPICE, to capture the impact of power supply noise [22]. The allocation of decoupling capacitors has also been investigated [23]–[25]. Most of these works assume worst case switching currents and utilize overly simplified power grid network models. In contrast, our work utilizes a more detailed off-chip and on-chip power grid model in a realistic design example where we use a workload derived from SPEC benchmarks. We estimate both IR drop and Ldi/dt droop in 2-D and 3-D PDNs for comparative analysis, and investigate methods for achieving 2-D-like PDN quality for 3-D stacks. In addition to quantifying the impact of TSV size, TSV spacing, and C4 spacing, we investigate the impact of coaxial TSVs and their novel usage in 3-D PDN.

III. Design Setup

A. 2-D Architecture

We use a conventional single-layer die in a flip-chip package to implement the baseline architecture shown is Fig. 3. The die is connected to the package using C4 bumps. The heat-sink is connected to the device side of the die. The die implements three functional modules each occupying a third of the die area. As shown in Fig. 4, the three modules are a quad-core chip-multiprocessor (PROC), a memory (MEM), and an accelerator engine (ACCL).

Each core of the CMP utilizes 10 W of maximum power, and is composed of five functional blocks: floating point unit (FPU), OOO (the rename, register file, result-bus, and window units), INT (integer arithmetic logic unit), Fetch (combines the instruction cache and branch predictor), and Data (represents the data

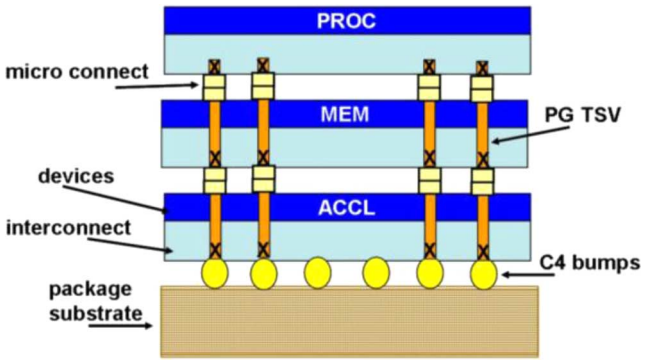

Fig. 5. Normal Stacked (3-D NOR) Configuration.

cache and load-store queue). Memory (MEM) and accelerator engine (ACCL) modules utilize a maximum of 20 and 10 W, respectively. The maximum power consumed by the die is 70 W. We assume a module area of 1 cm^2. The total die area for the 2-D design is thus 3 cm^2. There are 16×16 Vdd C4 connections per cm^2, and there is a similar number for the Gnd connections.

We use an architectural-level power model based on Wattch [26] to estimate the benchmark-specific power dissipation and transient effects in each functional block. Four SPEC benchmarks (apsi, bzip, equake, and mcf) were used to collect the power traces. These benchmarks are representative of a wide variety of current patterns [27]. We assume MEM has the same current trace as the L2 Cache, and that the ACCL has the same current trace as the FPU block representing an FPU accelerator engine. The Vdd supply voltage is 1.1 V.

B. 3-D Stacked Architecture

We use a stack of three dies in facedown orientation as illustrated in Fig. 5. Each of the three functional modules, PROC, MEM, and ACCL, is fabricated on a separate die. We consider the thermal/power activities of the dies while considering their placement in the 3-D chip. Since PROC has the highest power consumption, we place it adjacent to the heat sink. We place ACCL farthest from the heat sink due to its lowest power consumption. MEM is placed at the center of the stack to allow for shorter access paths from/to both PROC and ACCL. As mentioned in Section II, we utilize the electrical characterization approach by Alam *et al.* [11] to calculate the resistance and capacitance of individual TSVs and microconnects. TSVs and microconnects provide connections for external I/Os and power delivery vias in the stacked chip that are connected to C4 bumps at one side of the stacked 3-D chip. Other vertical connections between the dies are used for inter-layer signal and thermal management. The footprint of the 3-D stack is 1 cm^2. This configuration has 16×16 C4s per cm^2, and a similar number of TSVs for power delivery. We refer to this configuration as a *Normal Stacked* (3-D NOR) Configuration to differentiate it from other 3-D configurations investigated later in the paper.

C. Power Delivery Network (PDN)

The PDN consists of off-chip and on-chip networks, as illustrated in Fig. 6 [27]. The off-chip (motherboard and package)

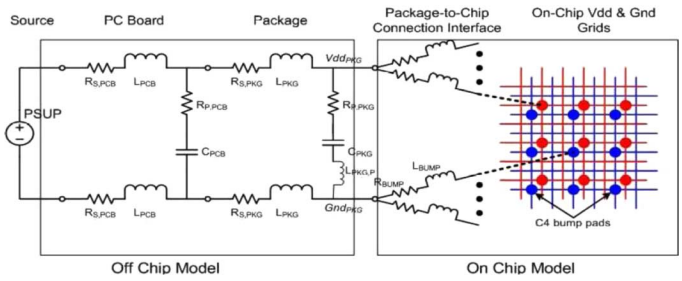

Fig. 6. Power delivery network [27].

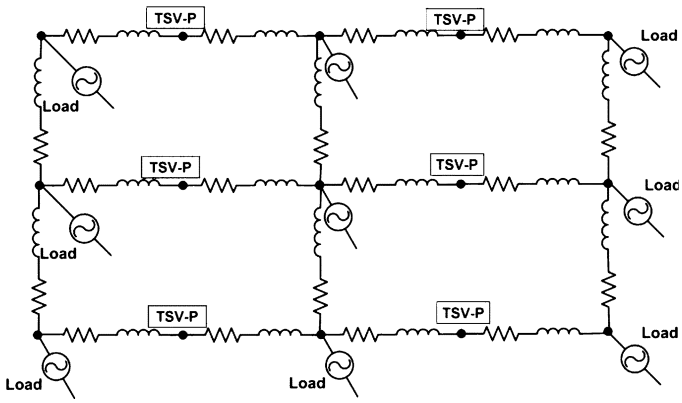

Fig. 7. Portion of the on-chip power grid for each die.

network is modeled as a resistive, inductive and capacitive network. The on-chip network consists of a global level grid-like structure routed in top metal layers. We model the load imposed on the global grid as time varying current sources. The off-chip and on-chip networks are connected using series resistors and inductors representing the flip-chip package.

For the on-chip power grid of each die, each grid element is modeled as a resistance and inductance in series. In addition, current load points and microconnect or TSV points (TSV-P) alternate throughout the grid as shown in Fig. 7. The TSV-Ps are connected to the C4 bumps either directly or through other stacked layers depending on the position of the on-chip PDN in the stack. The length of a grid element is such that we have a 32×32 element grid in a 1 cm^2 area. Such grid granularity was shown to be effective in capturing voltage variations within a multicore processor [27]. We assume wide metal line widths such that the grid collectively occupies 50% of the total die area. We use the predictive technology model [28] to calculate the R & L for grid elements. A fast circuit solver, based on preconditioned Krylov subspace iterative methods [29], is used to solve the SPICE netlist for the modeled configuration. A decoupling capacitance of 33 nF/cm^2 is assumed in our study, corresponding to device capacitance implementation with 1 nm gate oxide thickness (from the ITRS roadmap of 90–65-nm technology) occupying 20% of die area [22]. The decoupling capacitance is distributed along the grid elements in our 2-D and 3-D ICs.

D. Power Delivery Analysis for 2-D Architecture (Base Case)

In this section, we present the IR and Ldi/dt analysis for the baseline 2-D architecture, described in Section III-A. We run

TABLE I
IR DROP AND Ldi/dt VOLTAGE DROOP FOR 2-D ARCHITECTURE

	IR (V)			Ldi/dt (V)		
	PROC	MEM	ACCL	PROC	MEM	ACCL
APSI						
Max.	0.039	0.030	0.030	0.190	0.178	0.174
Avg.	0.032	0.025	0.023	0.021	0.020	0.019
Std.	0.002	0.001	0.001	0.021	0.020	0.020
BZIP						
Max.	0.040	0.034	0.033	0.322	0.276	0.282
Avg.	0.035	0.030	0.027	0.064	0.061	0.060
Std.	0.002	0.001	0.001	0.045	0.042	0.042
EQUAKE						
Max.	0.048	0.041	0.038	0.392	0.334	0.381
Avg.	0.040	0.038	0.030	0.032	0.031	0.030
Std.	0.003	0.001	0.002	0.038	0.038	0.038
MCF						
Max.	0.039	0.031	0.031	0.309	0.307	0.315
Avg.	0.033	0.026	0.025	0.037	0.035	0.034
Std.	0.003	0.001	0.001	0.032	0.029	0.030
AVG. OF ALL 4 BENCHMARKS						
Max.	0.041	0.034	0.033	0.303	0.273	0.288
Avg.	0.035	0.030	0.026	0.039	0.037	0.036
Std.	0.003	0.001	0.001	0.034	0.032	0.032

each of the four benchmarks *apsi, bzip, equake*, and *mcf* for 2048 cycles and observe the max, average, and standard deviation of IR and Ldi/dt drops. The results for this analysis are presented in Table I. These results form our baseline case, and all other analyses in this paper are presented in reference to these values. Examining the results presented in Table I, it is clear that the 2-D architecture is not an ideal one because the maximum IR drop and Ldi/dt voltage droop are considerably higher than their averages. We assume that local adjustments, in the form of increasing interconnect dimensions (for IR) and adding local decoupling capacitors (for Ldi/dt), can be done for both 2-D and 3-D power delivery networks. We therefore keep the architectures and power delivery network parameters the same in all the studies presented in this paper.

IV. OPTIMAL TSV SIZE FOR 3-D PDN

We examine in this section how TSV size impacts 3-D power delivery. TSV size is the dimension of one side of the square TSV footprint on a Si substrate. The TSV height is always equal to die thickness, which is 50 μm in all our 3-D setups. The maximum IR drops in different dies in the 3-D configuration, normalized to the maximum IR drop in the 2-D design, are shown in Fig. 8 for TSV sizes ranging from 5 to 50 μm in the 3-D NOR configuration. The following observations can be made.

- The maximum IR drop is worse in the 3-D configuration, with a worst case degradation of as much as 3.4 $\times$ the 2-D IR drop in the PROC die for the smallest considered TSV size.

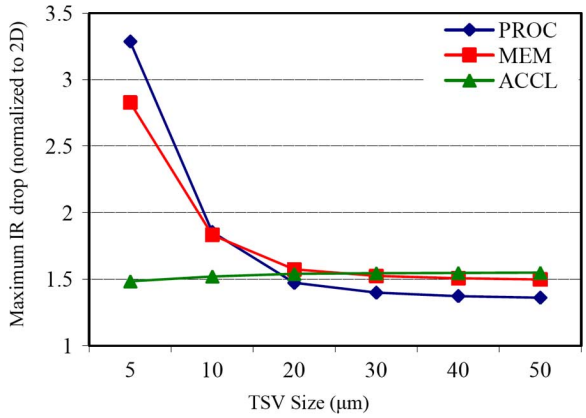

Fig. 8. Maximum IR drop for various TSV sizes.

- The ACCL, in close proximity to the C4 bumps, exhibits nearly constant maximum IR drops across the different TSV sizes. The value of the maximum IR drop is $\sim$1.5$\times$ the IR drop for the 2-D design. In the 3-D design, the number of C4s is reduced by a factor of 3 from the one in 2-D design due to reduced die size. Current through each C4 increases at the same time due to die stacking. Despite that, approximately 1.5$\times$ increase in the maximum IR drop shows that IR drop due to C4 components is not the dominant component in the overall power delivery network.
- More importantly, the IR drop saturates in PROC and MEM for TSV sizes of and greater than 20 μm. Such saturation suggests the lack of benefit of increasing the TSV size beyond a specific size. A TSV size of 25 μm is therefore used in the following analysis for 3-D PDN with core TSVs.

V. POWER DELIVERY ANALYSIS FOR 3-D PDN

A. Normal Stacked Configuration

Static IR Analysis: For static analysis, we remove the inductive and capacitive components in the PDN, and solve for IR drops for each current load from the benchmarks across 2048 cycles. The die footprint for 3-D is one third of that of 2-D. Hence, the number of C4s in the 3-D NOR design are reduced accordingly. More current flows through a single C4. We observe the maximum, average, and standard deviation in IR drops, and we report the results normalized to the values obtained by performing the same analysis for the 2-D architecture. The results are presented in the left half of Table II. We observe the following.

- The 3-D NOR power delivery configuration performs worse resulting in a higher maximum and in a higher average IR drops. The 3-D NOR configuration however has a lower standard deviation.
- A higher increase in IR drops is observed for ACCL and MEM dies over the PROC die. This is an important observation: IR drops get worse even in the die closest to C4 package connections. Our 2-D data indicates that MEM and ACCL have lower IR drops (in magnitude) than PROC. The increase in ACCL and MEM IR drop due to shared

TABLE II
IR DROP AND Ldi/dt VOLTAGE DROOP FOR 3-D NOR CONFIGURATION, NORMALIZED TO 2-D VALUES

	IR			Ldi/dt		
	PROC	MEM	ACCL	PROC	MEM	ACCL
APSI						
Max.	1.348	1.558	1.457	0.984	1.003	1.029
Avg.	1.338	1.616	1.706	1.164	1.236	1.251
Std.	0.663	2.408	1.248	0.938	0.970	0.966
BZIP						
Max.	1.470	1.596	1.527	1.011	1.136	1.113
Avg.	1.399	1.563	1.639	0.958	0.987	1.018
Std.	0.866	3.393	1.692	0.909	0.964	0.987
EQUAKE						
Max.	1.425	1.542	1.544	0.851	0.984	0.813
Avg.	1.418	1.477	1.738	1.085	1.104	1.120
Std.	0.804	2.773	1.418	0.935	0.933	0.936
MCF						
Max.	1.434	1.604	1.527	1.105	1.130	1.101
Avg.	1.367	1.62543	1.6321	1.105	1.134	1.137
Std.	0.846	3.398	2.101	0.914	0.970	0.959
AVG. OF ALL 4 BENCHMARKS						
Max.	1.419	1.575	1.514	0.988	1.064	1.014
Avg.	1.381	1.570	1.679	1.078	1.115	1.131
Std.	0.795	2.993	1.615	0.924	0.959	0.962

TSVs therefore translates into a larger increase in 3-D design when compared to the 2-D architecture.

- While the standard deviation in the IR drop for PROC decreases, the standard deviation in the IR drop for MEM and ACCL increases significantly, indicating a wider distribution of IR drops. This behavior is due to the activity profile of each module as well as 3-D power delivery sharing. For the MEM and ACCL modules, current profiles have a uniform spatial distribution but not a uniform temporal distribution. However, the PROC has a uniform spatial distribution within each functional module but not a uniform temporal distribution. So for the 2-D case, MEM and ACCL have almost-zero spatial standard deviation. However, sharing the power delivery in the 3-D case results in an increase in spatial standard deviation for MEM and ACCL. The net increase in standard deviation for MEM and ACCL is thus due to nonuniform spatial distributions that happened in 3-D stacking. As for the decrease in standard deviation for PROC, this occurs along with an increase in the average IR drop. Thus, stacking reduces variations but worsens the overall power delivery to PROC.

Ldi/dt Voltage Droop Analysis: We run the four benchmarks on the 3-D NOR configuration to investigate the Ldi/dt voltage droop in 3-D PDN normalized to those of 2-D PDN. We observe the Ldi/dt voltage droop at each node over the 2048 cycles and report the maximum, average, and standard deviation in each die in Table II (right half of the table). The droop is strongly dependent on each benchmark activity. From Table II, we make the following observations.

- There are few instances where there is a decrease in the maximum Ldi/dt voltage droop. Unlike in a 2-D design, decoupling caps in a 3-D network can supply current in both horizontal and vertical directions, thus mitigating the effects of di/dt droop. The resulting behavior is dependent on the locality of the droop as well as the state of the neighboring nodes.
- The decrease in standard deviation also indicates the effect of increased locality for decoupling caps in 3-D.
- Investigating the general trend using the average voltage droop for the four benchmarks, we notice an increase in voltage droop with a higher impact on the MEM and ACCL dies. The average voltage droop increase is as much as 25% in the ACCL die for the *apsi* benchmark. In a later section, we investigate how to mitigate this problem.
- Comparing the IR drop and Ldi/dt voltage droop results in Table II, we notice that 3-D stacking has a higher impact on IR drop. 3-D stacking inherently increases the resistance of a PDN which directly impacts IR drop. On the other hand, Ldi/dt voltage droop due to the time varying activities in the modules is caused by dominant off-chip inductive components. We therefore see no significant degradation in Ldi/dt voltage droop when compared to the 2-D architecture.

B. Effects of TSV Granularity (Spacing)

The PDN in 3-D NOR configuration has the same TSV spacing as that of the C4 connections. To design a 3-D stacked configuration that enables increasing the granularity of TSVs for power distribution in any of the dies in the 3-D stack, we introduce an interposer die [30] between the C4 connections and the bottom die as illustrated in Fig. 9. The interposer acts as a redistribution layer that is connected to C4 bumps on one side and bonded microconnects (higher granularity) on the other, thus distributing power all the way to the top die via the TSVs in the 3-D stack. We can therefore decrease the TSV spacing in the PDN to as low as the minimum allowed microconnect pitch while the C4 pitch can remain unchanged. We refer to this setup as the *Stacked Interposer* (3-D SI) configuration. For a fair comparison between the 2-D and 3-D SI configuration, we keep the granularity of C4 bumps (16×16 connections per cm^2) the same as that in 2-D and 3-D NOR configurations described earlier. The off-chip power delivery network also remains unchanged.

To assess the impact of the TSV spacing on power delivery, we vary the TSV granularity from 16×16 in our 3-D NOR configuration to granularities: 32×32, 48×48, and 64×64. At the highest granularity of 64×64, the TSV spacing is well above the minimum TSV pitch limit of 0.4 μm in wafer-to-wafer and of 5 μm in die-to-wafer or die-to-die 3-D bonding technologies [31]. The silicon area consumed by TSVs in the 3-D PDN for the 32×32 and 64×64 granularities are 5% and 20%, respectively, for a TSV size of 25 μm. For each increased granularity, the physical dimensions of each grid element are adjusted, and R and L values are recalculated. The decoupling capacitance is

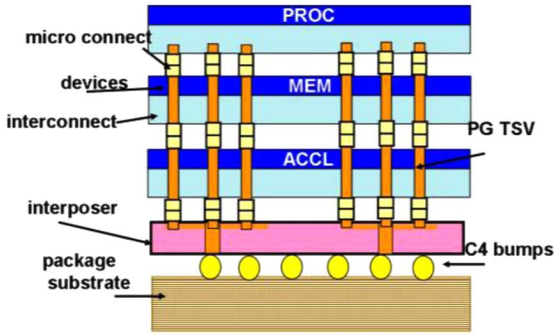

Fig. 9. Stacked Interposer (3-D SI) configuration.

TABLE III
IR DROP AND Ldi/dt VOLTAGE DROOP ANALYSIS FOR DIFFERENT TSV GRANULARITIES IN 3-D SI CONFIGURATION. ALL RESULTS ARE NORMALIZED TO THOSE FROM 2-D VALUES

	IR			Ldi/dt		
	PROC	MEM	ACCL	PROC	MEM	ACCL
32 X 32						
Max.	1.144	1.406	1.394	1.075	1.082	1.055
Avg.	1.250	1.544	1.596	1.059	1.103	1.124
Std.	0.606	1.482	1.201	0.897	0.961	0.956
48 X 48						
Max.	1.093	1.363	1.359	1.065	1.073	1.046
Avg.	1.233	1.537	1.597	1.044	1.091	1.115
Std.	0.399	1.043	0.864	0.887	0.953	0.949
64 X 64						
Max.	1.071	1.342	1.339	1.061	1.069	1.042
Avg.	1.221	1.526	1.589	1.038	1.085	1.111
Std.	0.321	0.859	0.710	0.883	0.950	0.946

uniformly redistributed throughout the on-chip grid on each die and its total value remains same.

Table III reports the results from static IR and transient Ldi/dt voltage analysis with various TSV spacing in the 3-D SI configuration. All values are normalized to those of the 2-D architecture. We only report the results from the *mcf* benchmark, a representative case for the worst case static and dynamic effects on the 3-D PDN. We make the following observations.

- Despite the expectation that increasing TSV granularity in the 3-D PDN would improve the overall quality of power delivery, we notice only marginal improvements in all the metrics for IR drop. The maximum IR drop in the PROC die is improved only 6% by increasing the TSV granularity from 32×32 to 64×64 whereas the TSV silicon area penalty rises from 5% to 20%. Similar observations are made for the transient voltage droop where the improvements in the maximum and average voltage droop figures are less than 2%.
- The marginal improvement suggests that an on-chip grid and TSV granularity of 32×32 reaches a near optimum solution for power grid quality, particularly for IR drops. This observation leads us to consider improving the off-chip network by examining the granularity of C4 bumps, which we explore next.

TABLE IV
IR DROP AND Ldi/dt VOLTAGE DROOP ANALYSIS FOR 3-D NOR CONFIGURATION WITH BOTH C4 AND TSV GRANULARITIES OF 32×32, NORMALIZED TO 2-D VALUES

	IR			Ldi/dt		
	PROC	MEM	ACCL	PROC	MEM	ACCL
Max.	0.731	0.885	0.868	0.970	0.976	0.952
Avg.	0.810	0.992	1.019	0.920	0.958	0.976
Std.	0.339	0.702	0.531	0.943	1.011	1.006

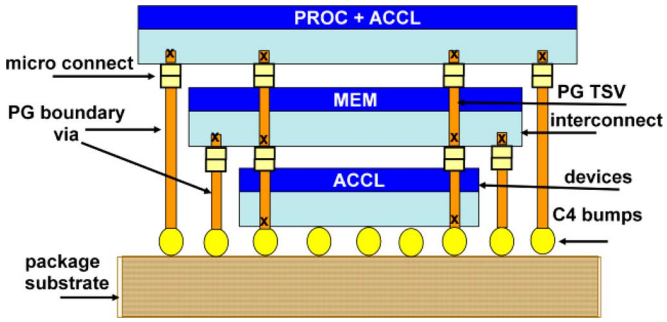

Fig. 10. Tapered stacked (3-D TAP) 3-D configuration.

C. Effects of C4 Granularity (Spacing)

We now assume that the 3-D NOR configuration with both C4 and TSV having equal granularity of 32×32 for both Vdd and Gnd supply networks. This is an increase over the 16×16 C4 granularity used earlier. We perform IR and Ldi/dt analysis, and summarize the results in Table IV. We make the following observations from these results.

- Increased C4 granularity results in significant improvement in IR voltage drop. This $4 \times$ increase in the number of TSV and C4 results in improved 3-D PDN performance, even better than the baseline 2-D architecture.
- Although increasing C4 granularity significantly improves IR drops, the improvement is limited in terms of Ldi/dt voltage droop. This is due to the off-chip PDN components (package and PCB) having a more dominant impact on Ldi/dt voltage droop.

D. Effect of Dedicated Power Delivery in 3-D

The experiments in the previous sections assume that TSVs in the 3-D PDN are shared among all dies. In this section, we study the effect of adding partially dedicated power delivery to each die through a few TSVs connected to only select dies. We define a new 3-D configuration, the *tapered stacked* (3-D TAP) Configuration, shown in Fig. 10.

In the 3-D TAP configuration, dies are progressively sized larger to be able to connect few dedicated vertical connections, called the *boundary vias*, to the PDN in the extended boundary portion of a die. As illustrated in Fig. 10, the boundary vias do not pass through any of the active silicon area and can be formed using advanced package-level routing vias similar to those in

TABLE V
IR DROP AND Ldi/dt VOLTAGE DROOP ANALYSIS FOR 3-D TAP CONFIGURATION, NORMALIZED TO 2-D VALUES

	IR			Ldi/dt		
	PROC	MEM	ACCL	PROC	MEM	ACCL
Max.	1.226	1.403	1.344	1.077	1.084	1.057
Avg.	1.196	1.491	1.538	1.031	1.087	1.107
Std.	1.805	2.788	1.432	0.897	0.960	0.954

redistributed chip packaging [32]. Size of each die is modified such that the tapering ratio is constant between the dies and a total silicon area of 3 cm^2 is achieved for the 3-D chip. Due to die resizing, we modify the module placements: the top die now has PROC and some part of ACCL; the middle die has MEM; the bottom die has ACCL. Parameters for C4 pitch, on-chip power grid R & L, and off-chip network are kept the same as in the original 2-D design. Due to an increase in footprint, there is an increase in the number of C4 and TSVs of 18×18 compared to 16×16 in 3-D NOR configuration.

The results for IR drop and Ldi/dt voltage droop analysis in 3-D TAP configuration are presented in Table V. The results show that partly dedicated power delivery in 3-D TAP configuration does not have the same extent of improvement as increasing C4 granularity (comparing the results to those in Table IV). However, both average IR drop and L/di/dt voltage droop in the 3-D TAP configuration are improved compared to those in the 3-D NOR configuration (see Table II) and the 3-D SI (Table III 32×32 TSV granularity case). This improvement does not have any silicon area penalty as in the 3-D SI because TSV granularity is the same as in the 3-D NOR configuration. Although the concept of dedicated or partly dedicated power delivery in 3-D as in 3-D TAP is interesting and effectively improves quality of 3-D PDNs, there may be additional risk and cost considerations associated with tapered die sizing and nonstandard boundary via packaging process. The tapered die sizes would only permit die-to-die and die-to-wafer bonding techniques excluding the wafer-to-wafer option which requires the same die and wafer sizes. Process considerations aside, the 3-D TAP configuration illustrates a method for isolating some of the most active parts of dies by using dedicated delivery in that area. The proposed method also yields improvement in 3-D PDN vis-à-vis other 3-D PDN configurations. A comparative summary of different 3-D PDN configurations is discussed next.

E. Summary of the Core TSV PDN Studies

We summarize the relative performance of the proposed 3-D PDN configurations in the form of graphs presented in Figs. 11 and 12. We consider the following four configurations each contributing in a unique way to improve 3-D PDN quality.

- *Normal:* This is the 3-D NOR configuration described earlier. This setup has C4 and TSV both at the granularity of 16×16 in 1 cm^2 area
- *Increased TSV:* We increase the TSV granularity while keeping the C4 granularity same. Increased TSV represents the 3-D SI configuration with C4 granularity of 16×16 and TSV granularity of 32×32.
- *Partially Dedicated:* In this configuration we use a combination of shared and dedicated power delivery to isolate some of the noise in the most active areas of the 3-D architecture. This architecture corresponds to the 3-D TAP configuration presented in Section V-D.
- *Increased C4:* Both C4 and TSV are at the granularity of 32×32.

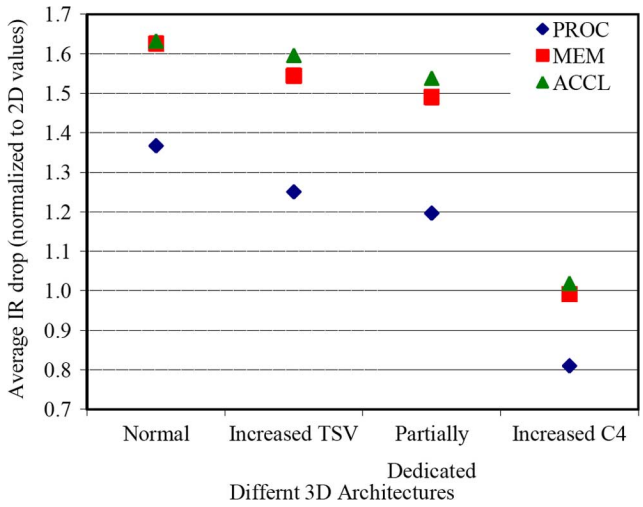

Fig. 11. Comparison of IR Drop from four 3-D PDN configurations representing different improvement methods.

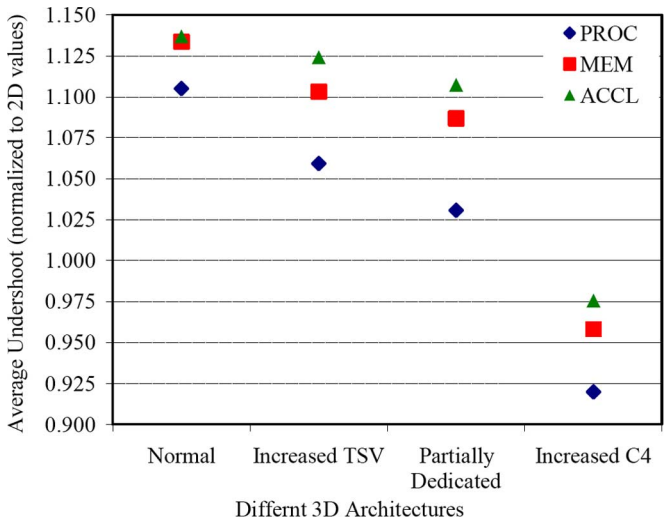

Fig. 12. Comparison of Ldi/dt voltage droop from four 3-D PDN configurations representing different improvement methods.

Going from the Normal to the Increased TSV case in Figs. 11 and 12, we see 11% improvement in IR drop and 4.5% improvement in Ldi/dt droop for the PROC die. This improvement is due to increasing the number of TSVs by a factor of four. As per results in Section V-B, increasing the number of TSVs by another $4\times$ ($16\times$ total) provides an additional 3% improvement in IR drop. The trend indicates that further increasing the TSV granularity returns little benefit. Although partially dedicated power

delivery does not have any area penalty over 3-D NOR configuration, it improves average IR drop and Ldi/dt voltage droop by 17% and 7% respectively in the PROC die. This is due to isolating the power delivery to some of the most active parts of dies by using dedicated delivery in that area. Increased C4 granularity has the maximum impact on the 3-D PDN improvement. As shown in Figs. 11 and 12, a 4× increase in C4 granularity in the Increased C4 case provides a 56% relative improvement when compared to the normal case. Clearly, the C4 increased granularity has a more significant impact on improving IR drops than increased TSV granularity. Similar conclusions can be drawn from the Ldi/dt voltage droop analysis results as well. Reduced standard deviations are achieved with Increased C4 over those obtained using Increased TSV.

VI. Using Coaxial TSV for Power Delivery

Coaxial TSVs have been proposed for noise isolation [14]. We investigate using coaxial TSVs for power delivery for reducing blockages, increasing decap, and overlaying power/signal routing.

A. Reducing Blockages

When power TSVs extend through a die, routing blockages are created in the x-, y-, and z-dimensions in the die. Therefore, reducing the number of power TSVs as well as careful placement can help in eliminating critical routing blockages. We can use a single coaxial TSV to deliver both Vdd and Gnd to a die with a goal of reducing the number of power supply TSVs. The inner and outer metal layers [see Fig. 2(b)] are used to deliver Vdd and Gnd, respectively, in this scheme.

We consider an architectural setup similar to the 3-D NOR configuration described in Section V-A for IR drop and Ldi/dt voltage droop analysis. We keep the cross-section for each of the inner and outer metal layers the same as the square-TSV area used in previous analyses. We assume an inner ILD thickness of 20 nm, resulting in an overall size of each coaxial TSV of width 35.4 μm. The coaxial TSV height is 50 μm similar to that of all core TSVs in our 3-D setups. TSV granularity of 16×16 for each Vdd and Gnd supply with core TSV is now translated to coaxial TSV granularity of 16×16 used for delivering both Vdd and Gnd. While our analysis suggests that this setup does not improve the IR drop or Ldi/dt voltage droop, merging two square-TSVs into single coaxial TSV results in a fewer number of routing blockages.

B. Increasing Decap

A coaxial TSV of width 35.4 μm as mentioned above with an inner ILD thickness of 20 nm has a capacitance of 9.96 pF. This TSV capacitance is approximately 250 times the square-TSV capacitance and acts as additional decap in the 3-D PDN. While the 20 nm inner ILD thickness is for illustrative purpose, further process development work is ongoing for controlling the inner ILD thickness to effectively implement capacitors using coaxial TSVs [15]. In this experiment, we analyze how to exploit coaxial TSVs to maximize on-chip decoupling capacitance in 3-D PDN.

We replace each square Vdd or Gnd TSV with a coaxial TSV with a thin outer metal layer (example thickness of 0.2 μm) connected to the opposite power rail. Thus, the granularities of Vdd and Gnd TSVs do not change while each TSV gets additional decoupling capacitance due to the co-axial implementation. Choosing an inner ILD thickness of 20 nm, the coaxial TSV will have approximately 16% of the original decoupling capacitance. While the 16% increase in decoupling capacitance does not translate to significant improvement in Ldi/dt voltage droop as seen in our analysis, the coaxial decoupling capacitance implementation can be viewed as an opportunity to free silicon area by reducing the silicon area required for implementing device decoupling capacitance. In this example, device decoupling capacitor area will reduce by 16% when using a coaxial TSV implementation.

TABLE VI
IR Drop and Ldi/dt Voltage Droop Analysis for 3-D Nor With Coaxial TSVS Having Signal in the Inner Metal, Normalized to 2-D Values

	IR			Ldi/dt		
	PROC	MEM	ACCL	PROC	MEM	ACCL
Max.	1.427	1.600	1.527	1.104	1.129	1.100
Avg.	1.361	1.621	1.632	0.843	0.861	0.852
Std.	1.231	2.533	1.916	1.355	1.385	1.374

To implement a large amount of decoupling capacitance in coaxial TSVs, researcher in [14] also propose an alternative implementation with more than one layer of inner ILD and inner metal such that multiple inner ILD layers collectively form a large capacitor. Using such multilayer coaxial TSV, if we increase decoupling capacitance by 90%, then the peak Ldi/dt noise improvement from our analysis is approximately 15%. Other researchers also proposed adding large amounts of decoupling capacitance, such as 80% more decoupling capacitor implemented as additional "decap" die stacked in 3-D chips, which provided 22%–36% peak Ldi/dt noise reduction [22]. However, additional decap die would block cooling paths for other dies. Therefore, a coaxial TSV can be considered as a new alternative for decoupling capacitor implementation in 3-D PDN with an opportunity to improve Ldi/dt voltage droop or save silicon area by replacing device capacitors.

C. Overlaying Signal and Power Routing

When the resistance of a particular power TSV, for example one in non-hotspot area, is not highly critical, a coaxial TSV of the same footprint can be used to route an additional (non-VDD and non-Gnd) signal. Signal TSVs are expected to be smaller in size for reduced capacitive load making them ideal to overlay with large size power TSVs that use a coaxial TSV implementation. In this experiment, we study the effect of power/signal overlay in a 3-D PDN using coaxial power TSVs. The coaxial power TSV of width 25 μm with the inner metal of width 5 μm is dedicated for signal transmission and the outer metal is used to deliver power. We incorporate this new coaxial TSV scheme into the 3-D NOR configuration and perform IR drop and Ldi/dt analysis. Note that coaxial TSV footprint is the same as that of the core TSV footprint in the 3-D NOR configuration. Each one of the Vdd and Gnd coaxial TSVs is used to transmit a signal through the inner metal layer which would represent the extreme

TABLE VII
EVALUATION OF COAXIAL TSVS FOR REDUCING BLOCKAGES, INCREASING DECAP, AND OVERLAYING SIGNAL/POWER ROUTING

	NO. OF BLOCKAGES	SIZE OF EACH BLOCKAGE	ADDITIONAL SIGNAL ROUTES DUE TO OVERLAY	BENEFIT
Reducing Blockages	256	1.253E-9m^2	0	Reduced number of blockages
Increasing Decap	512	0.841E-9m^2	0	Additional decoupling capacitance
Overlaying Signal/Power Routing	512	0.600E-9m^2	512	Additional signal routing

case of signal overlay for analyzing worst case impact on PDN quality.

The results of our IR drop and Ldi/dt analysis using the *mcf* benchmark are reported in Table VI. When comparing these results with the corresponding *mcf* benchmark results for the 3-D NOR configuration, with core TSVs (see Table II), we see no significant change in IR drop or Ldi/dt voltage droop of the 3-D PDN with overlay coaxial TSVs. This is due to the fact that we sacrificed less than 4% of the TSV area for signal overlay. This observation is also supported by the IR saturation trend in Fig. 8 where we notice that a TSV size of 25 μm is already near saturation. Hence, reducing effective power TSV area by a small percentage did not significantly degrade the performance of the 3-D PDN.

D. Summary of the Three Analyses

We summarize the above presented three studies to evaluate the potential benefit of using coaxial TSV for 3-D PDN in Table VII. The first column shows the technique used to integrate coaxial TSV into the 3-D PDN. The next three columns quantify three parameters (number of blockages, size of each blockage, and the number of additional signal routes) that we use to compare the implementations. The last column summarizes the main benefit obtained from each integration technique. Clearly, coaxial TSVs have an interesting opportunity to reduce the number of blockages, integrate extra decoupling capacitance, and provide extra signal routes. All these benefits have no extra area or performance penalty as shown in the previous analyses.

VII. BEST PRACTICES FOR 3-D PDN DESIGN AND OPTIMIZATION

Based on our findings, we present a set of guidelines for designing and optimizing power delivery networks in future 3-D designs.

- Locality in the vertical dimension impacts both IR drop and Ldi/dt voltage droop trends in a 3-D PDN. A voltage droop at a node in a 3-D configuration can utilize current from decoupling caps in the vertical neighbors as well as from the ones in the same plane. The resulting behavior is dependent on the locality of the droop as well as the state of the neighboring nodes. Therefore, detailed 3-D PDN analysis with architecture or module level placement using representative workloads is necessary during 3-D chip design.
- A critical observation in our work is the saturation trend of IR drop in 3-D PDNs with increased TSV size. This suggests the need for first finding the optimal TSV size given the on-chip grids in 3-D stacked layers such that the least amount of silicon penalty is incurred.
- While it is generally expected that power delivery would be affected most in the die stacked furthest away from the C4 connections, we report that percentage degradation in power delivery is in fact worse in lower level dies closer to C4s. This is evident when a highly active module, such as PROC, is placed next to heat sink for thermal concerns and furthest away from C4 connections. Therefore, 3-D PDN design needs to carefully consider the impact in all the dies while optimizing the grid.
- Increasing TSV granularity or equivalently decreasing TSV spacing in 3-D PDN improves the standard deviation in IR drop and Ldi/dt voltage droop most, with marginal improvements in maximum and average values. Therefore, physical design for 3-D PDN must consider the impact and choose TSV granularity for minimum silicon penalty.
- Despite selecting the optimal TSV size and TSV spacing, 3-D PDN performs worse in both IR drop and Ldi/dt voltage droop when compared to a 2-D PDN if the package connection, such as C4, pitch or granularity is maintained the same as in the 2-D case. Our study shows that improving off-chip component of the 3-D PDN, for example through reducing the C4 pitch for a higher number of C4s, has the highest relative impact on power grid metrics that enables 2-D-like or even better quality 3-D PDN.
- A combination of shared and dedicated TSV power delivery can be used, as illustrated in 3-D TAP configuration, to achieve improvements in both IR drop and Ldi/dt voltage droop. Further investigation is recommended with dedicated power grid approaches for physical design, such as floorplanning and placement of dedicated TSVs, for optimization of such 3-D PDNs.
- Along with reducing the number of blockages, coaxial TSVs have exciting opportunities to be used for overlaying signals as well as adding more decoupling capacitance into the 3-D integrated chip.

The above guidelines apply to power delivery networks that use C4 and TSVs for the proposed 3-D power delivery networks. For other 3-D PDN designs within different packaging, separate analysis will be required to determine an appropriate set of guidelines.

VIII. CONCLUSION

Power delivery is expected to be a major physical design concern in 3-D ICs due to higher power density and package asymmetries. We compared in this paper the power delivery networks for 2-D and several 3-D configurations (3-D NOR, 3-D SI, and 3-D TAP) that represent different techniques for improving 3-D power delivery. We performed the first detailed architectural analysis to study the IR drop and Ldi/dt voltage droop in the

context of various design parameters in 3-D PDNs: TSV size, TSV and C4 granularity, partially dedicated TSV, and the use of coaxial TSVs. Interestingly, it is possible to achieve 2-D-like or even better power delivery by improving the off-chip component (C4 granularity) in a 3-D PDN. Based on our findings, we presented a set of design and analysis guidelines for 3-D PDNs. While our work emphasized fundamental detailed analyses of core issues needed to implement 3-D power delivery networks, it is possible to extend our study to construct simplified analytical models appropriate for performance evaluation of 3-D designs.

REFERENCES

[1] J. Meindl, "Beyond Moore's law: The interconnect era," *Comput. Sci. Eng.*, vol. 5, pp. 20–24, 2003.

[2] J. Joyner, R. Venkatesan, P. Zarkesh-Ha, J. Davis, and J. Meindl, "Impact of three-dimensional architectures on interconnects in gigascale integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 9, no. 12, pp. 922–928, Dec. 2001.

[3] M. Bamal, S. List, M. Stucchi, A. Verhulst, M. Van Hove, R. Cartuyvels, G. Beyer, and K. Maex, "Performance comparison of interconnect technology and architecture options for deep submicron technology nodes," in *Proc. Int. Interconnect Technol. Conf.*, 2006, pp. 202–204.

[4] W. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. Sule, M. Steer, and P. Franzon, "Demystifying 3-D ICs: The pros and cons of going vertical," *IEEE Des. Test Comput.*, vol. 22, no. 6, pp. 498–510, Nov. 2005.

[5] J. Cong and Y. Zhang, "Thermal-driven multilevel routing for 3D ICs," in *Proc. Asia South Pacific Des. Autom. Conf. (ASP-DAC)*, Jan. 2005, vol. 1, pp. 121–126.

[6] B. Goplen and S. Sapatnekar, "Placement of thermal vias in 3-D ICs using various thermal objectives," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 4, pp. 692–709, Apr. 2006.

[7] C. King, D. Sekar, M. Bakir, B. Dang, J. Pikarsky, and J. Meindl, "3D stacking of chips with electrical and microfluidic I/O interconnects," in *Proc. 58th Electron. Components Technol. Conf.*, 2008, pp. 1–7.

[8] H. Yu, J. Ho, and L. He, "Simultaneous power and thermal integrity driven via stapling in 3D ICs," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des.*, San Jose, CA, 2006, pp. 802–808.

[9] *MITLL Low-Power FDSOI CMOS Process Application Notes*. Lexington, MA: MIT Lincoln Laboratory, 2006. [Online]. Available: http://www.ece.umd.edu/~dilli/research/layout/MITLL_3D_2006/3D_PDK2.3/doc/ApplicationNotes2006-1.pdf

[10] A. Topol, D. La Tulipe, L. Shi, S. Alam, D. Frank, S. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. Robson, E. Duch, M. Farinelli, C. Wang, R. Conti, D. Canaperi, L. Deligianni, A. Kumar, K. Kwietniak, C. D'Emic, J. Ott, A. Young, K. Guarini, and M. Ieong, "Enabling SOI-based assembly technology for three-dimensional (3D) integrated circuits (ICs)," in *Proc. IEEE Int. Electron Devices Meet.*, 2005, pp. 352–355.

[11] S. M. Alam, R. E. Jones, S. Rauf, and R. Chatterjee, "Inter-strata connection characteristics and signal transmission in three-dimensional (3D) integration technology," in *Proc. 8th Int. Symp. Quality Electron. Des.*, 2007, pp. 580–585.

[12] P. Morrow, M. Kobrinsky, S. Ramanathan, C.-M. Park, M. Harmes, V. Ramachandrarao, H. Park, G. Kloster, S. List, and S. Kim, "Wafer-level 3D interconnects via Cu bonding," in *Proc. 21st Adv. Metallization Conf.*, Oct. 2004, pp. 125–130.

[13] M. Rousseau, O. Rozeau, G. Cibrario, G. Le Carval, M. A. Jaud, P. Leduc, A. Farcy, and A. Marty, "Through-silicon via based 3D IC technology: Electrostatic simulations for design methodology," presented at the IMAPS Device Packag. Conf., Pheonix, AZ, 2008.

[14] T. G. Sparks, S. M. Alam, R. Chatterjee, and S. Rauf, "Method of forming a through-substrate via," U.S. Patent Appl. 20080113505, Nov. 15, 2006.

[15] P. Andry, C. Tsang, E. Sprogis, C. Patel, S. Wright, B. Webb, L. Buchwalter, D. Manzer, R. Horton, R. Polastre, and J. Knickerbocker, "A CMOS-compatible process for fabricating electrical through-vias in silicon," in *Proc. 56th Electron. Components Technol. Conf.*, 2006, pp. 831–837.

[16] S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. Lau, "High RF performance TSV silicon carrier for high frequency application," in *Proc. Electron. Components Technol. Conf.*, 2008, pp. 1946–1952.

[17] S. Denda, "Process examination of through silicon via technologies," in *Proc. 6th Int. Conf. Polymers Adhesives Microelectron. Photon.*, 2007, pp. 149–152.

[18] A. Rahman, J. Trezza, B. New, and S. Trimberger, "Die stacking technology for terabit chip-to-chip communications," in *Proc. Custom Integr. Circuits Conf.*, pp. 587–590.

[19] J. H. Wu, "Through-substrate interconnects for 3-D integration and RF systems," Ph.D. dissertation, Dept. EECS, Massachusetts Inst. Technol., Boston, 2006.

[20] P. Jain, T. Kim, J. Keane, and C. H. Kim, "A multi-story power delivery technique for 3D integrated circuits," in *Proc. 13th Int. Symp. Low Power Electron. Des.*, Bangalore, India, 2008, pp. 57–62.

[21] Y. Zhan, T. Zhang, and S. S. Sapatnekar, "Module assignment for pin-limited designs under the stacked-vdd paradigm," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des.*, San Jose, CA, 2007, pp. 656–659.

[22] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. Meindl, "Power delivery for 3D chip stacks: Physical modeling and design implication," in *Proc. IEEE Conf. IEEE Electr. Perform. Electron. Packag.*, 2007, pp. 205–208.

[23] J. R. Minz, S. K. Lim, and C. Koh, "3D module placement for congestion and power noise reduction," in *Proc. 15th ACM Great Lakes Symp. VLSI*, Chicago, IL, 2005, pp. 458–461.

[24] E. Wong and S. K. Lim, "3D floorplanning with thermal vias," in *Proc. Conf. Des., Autom. Test Eur.*, Munich, Germany, 2006, pp. 878–883.

[25] P. Zhou, K. Sridharan, and S. Sapatnekar, "Congestion-aware power grid optimization for 3D circuits using MIM and CMOS decoupling capacitors," in *Proc. Asia South Pacific Des. Autom. Conf.*, 2009, pp. 179–184.

[26] D. Brooks, V. Tiwari, and M. Martonosi, "Wattch: A framework for architectural-level power analysis and optimizations," in *Proc. 27th Int. Symp. Comput. Arch.*, 2000, pp. 83–94.

[27] M. Gupta, J. Oatley, R. Joseph, G.-Y. Wei, and D. Brooks, "Understanding voltage variations in chip multiprocessors using a distributed power-delivery network," in *Proc. Des., Autom. Test Eur. Conf. Exhibition*, 2007, pp. 1–6.

[28] Arizona State Univ., Tempe, "Predictive technology model (PTM)," 2005. [Online]. Available: http://www.eas.asu.edu/~ptm

[29] T. Chen and C. C. Chen, "Efficient large-scale power grid analysis based on preconditioned krylov-subspace iterative methods," in *Proc. 38th Conf. Des. Autom.*, Las Vegas, NV, 2001, pp. 559–562.

[30] C. S. Patel, "Silicon carrier for computer systems," in *Proc. 43rd Ann. Conf. Des. Autom.*, San Francisco, CA, 2006, pp. 857–862.

[31] J. U. Knickerbocker, P. Sandry, B. Dang, R. Horton, M. Interrante, C. Patel, R. Polastre, K. Sakuma, R. Sirdeshmukh, E. Sprogis, S. Sri-Jayantha, A. Stephens, A. Topol, C. Tsang, B. Webb, and S. Wright, "Three-dimensional silicon integration," *IBM J. Res. Develop.*, vol. 52, p. 553, Nov. 2008.

[32] Freescale Semiconductor, Austin, TX, "Redistributed chip packaging (RCP) technology," 2005. [Online]. Available: http://www.freescale.com/webapp/sps/site/overview.jsp?code=ASIC_LV3_PACKAGING_RCP

[33] N. H. Khan, S. M. Alam, and S. Hassoun, "Through-silicon via (TSV)-induced noise characterization and noise mitigation using coaxial TSVs," in *Proc. IEEE Int. Conf. 3D Syst. Integr., (3DIC)*, pp. 1–7.

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