Power Distribution Networks for System-on-Package: Status and Challenges

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***Abstract*—The power consumption of microprocessors is increasing at an alarming rate leading to 2X reduction in the power distribution impedance for every product generation. In the last decade, high I/O ball grid array (BGA) packages have replaced quad flat pack (QFP) packages for lowering the inductance. Similarly, multilayered printed circuit boards loaded with decoupling capacitors are being used to meet the target impedance. With the trend toward system-on-package (SOP) architectures, the power distribution needs can only increase, further reducing the target impedance and increasing the isolation characteristics required. This paper provides an overview on the design of power distribution networks for digital and mixed-signal systems with emphasis on design tools, decoupling, measurements, and emerging technologies.**

***Index Terms*—Impedance, mixed signal, power delivery, power distribution.**

I. INTRODUCTION

A MAJOR bottleneck faced by systems today is the supply of clean power to the integrated circuits. The replacement of the quad flat pack (QFP) with ball grid array (BGA) packages in the 1990s has resulted in a substantial decrease in the inductance from the 50 nH range to the tens of pico-henry range. Today, the core power supply inductance has been reduced to $\sim$10 pH for high-performance computer products using state of the art packages and boards [1]. With the trend in microprocessors toward higher power and lower supply voltages, the power supply inductance has to continuously decrease. In addition, the noise in the system is being generated by bouncing planes due to the propagation of electromagnetic waves, resulting in significant coupling and radiation. With increase in frequency and convergence toward mixed-signal systems, supplying clean power to the integrated circuits and managing the noise coupling in the system can be a major bottleneck, which is the subject of this paper.

The power consumption and supply voltage for some microprocessor products in the last decade are shown in Fig. 1. The power has increased from 5 to 150 W, the supply voltage has decreased from 5 to 1.2 V and the frequency has increased from 16 MHz to 3 GHz from the 386 to the Itanium processor families. This has resulted in an exponential increase in the current being supplied to the microprocessor. In the mid-1990s, design of power distribution networks using the target impedance was proposed by Smith *et al.* [2]. The target impedance, which is calculated from the power supply tolerance (5% of supply voltage), current and switching activity (50%), has to be satisfied by the system over a broad range of frequencies, from dc to at least the first harmonic of the clock frequency. The target impedance is a useful quantity for evaluating the relative merit of a system. Using the parameters from the 2001 International Technology Roadmap on Semiconductors (ITRS) [3] for high-performance products, the target impedance is expected to decrease for every product generation, as shown in Fig. 2, reaching 0.1 mΩ in 2010 for a microprocessor operating at 218 W @ 0.6 V with a clock frequency of 10 GHz. As a comparison, the Itanium microprocessor which operates with a power of 150 W @ 1.2 V has a target impedance of 1 mΩ. Similarly, for the 22-nm technology from ITRS in 2016, the target impedance to be met is 60 $\mu\Omega$. The impact of reducing power supply noise through reduced impedance on microprocessor performance has been described in detail by Waizman *et al.* [4] wherein it was shown that the frequency of the microprocessor can be increased by reducing the power supply tolerance.

With the evolution in technologies, system-on-package (SOP) is fast becoming a promising solution for integrating heterogeneous functions such as high-speed digital processing, memory, radio-frequency circuits, sensors, microelectromechanical systems (MEMS), and optoelectronic devices. This integration is required for convergent microsystems that support communication and computing capabilities in a tightly integrated module. By embedding functionality in the package (such as inductors, capacitors, resistors, waveguides, and filters), SOP provides for the co-design of the chip and the package for system integration. A major problem with such heterogeneous integration is the noise coupling between the various dissimilar blocks constituting the system. The noise is primarily generated by the high-speed digital processor and coupled through the power distribution network, resulting in significant jitter for the phase-locked loop (PLL) and phase noise for the RF oscillator, resulting in the reduction of timing margin, noise margin, and degradation in the bit error rate (BER). The noise coupling is conceptually depicted in Fig. 3 where the maximum power supply noise is transmitted through interconnections and vias at resonance in the power/ground planes of the package. Due to the low noise floor required for analog circuits, at frequencies below the substrate resonance

Manuscript received February 1, 2004; revised April 8, 2004.

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Digital Object Identifier 10.1109/TADVP.2004.831897

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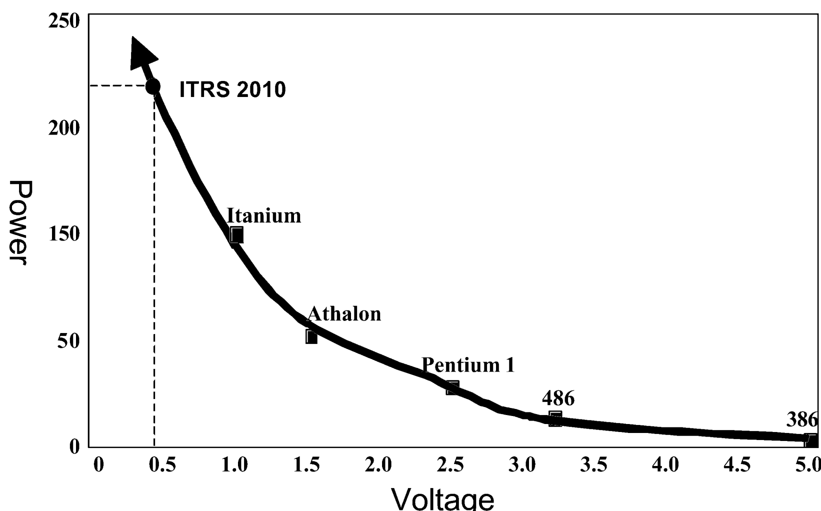


Fig. 1. Microprocessor power distribution trends (Courtesy: L. Smith-SUN).

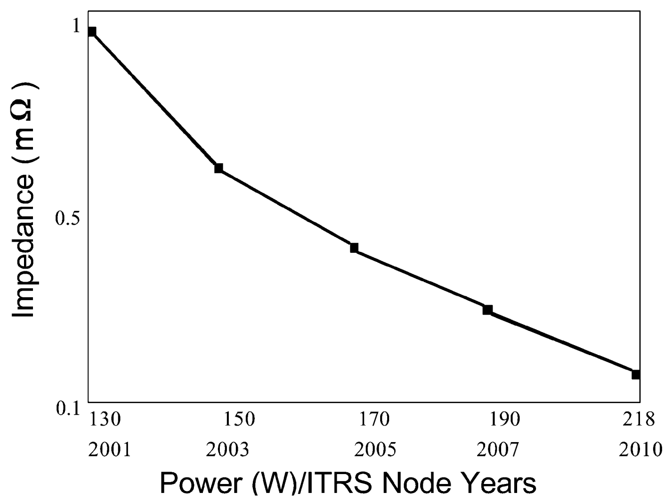


Fig. 2. Target impedance projections based on ITRS'01.

frequencies, considerable noise coupling occurs in the form of crosstalk and through the common inductive impedance of the power/ground return current path. In addition, the resonance generates edge radiation, causing electromagnetic interference in the system.

Any system can be partitioned into the chip containing the active circuits, the package supporting routing with embedded passives and the board providing connection between chips and to the outside world. With the evolution in system integration technologies, the goal is always to reduce the interfaces by eliminating the packaging levels in a system. This translates to higher system speed. The power distribution network consists of interconnections in the chip, package and board, which together provide the required target impedance over a range in frequencies. With the trend toward SOP, the power distribution network in the chip and package has to be viewed as a single network, warranting a chip-package co-design methodology for minimizing the resonance in the system. This requires a clear understanding of the system blocks, design tools and technologies available for power distribution, in terms of their status and challenges, which is the focus of this paper.

This paper is organized as follows. In Section II, the issues related to the powering of microprocessors and systems are discussed with emphasis on the chip and package/board power distribution. Section III describes the modeling of power distribution networks. In Section IV, recent results and challenges for SOP are described followed by the conclusions in Section V.

II. Powering of Microprocessors and Digital Systems

The elements of the power distribution network are shown in Fig. 4, which consists of the chip level power distribution with thin-oxide decoupling capacitors, the package level power distribution with planes and midfrequency decoupling capacitors and the board level power distribution with planes, low-frequency decoupling capacitors, and voltage regulator module. The frequency ranges covered by these elements are also shown in the figure where the power distribution operates at a higher frequency as the proximity to the active devices decreases. This is due to the parasitic inductance and resistance of the interconnections between the active circuitry and the various elements of the power distribution network. The status and challenges for each block in the power distribution are explained in detail in this section.

A. Voltage Regulator

The trend of increasing power and lowering supply voltage requires designers to move ac-dc and dc-dc converters closer to the electronics they feed. A representative class of low-voltage high-current application is the core supply of central processing units (CPU), digital signal processors (DSP), and large switching chips. The voltage may be in the 0.8 to 2.5 V range with the current being in excess of 100 A for the largest devices. Since the core voltage is often unique and may be required only by the particular device, the dc-dc converters usually feed

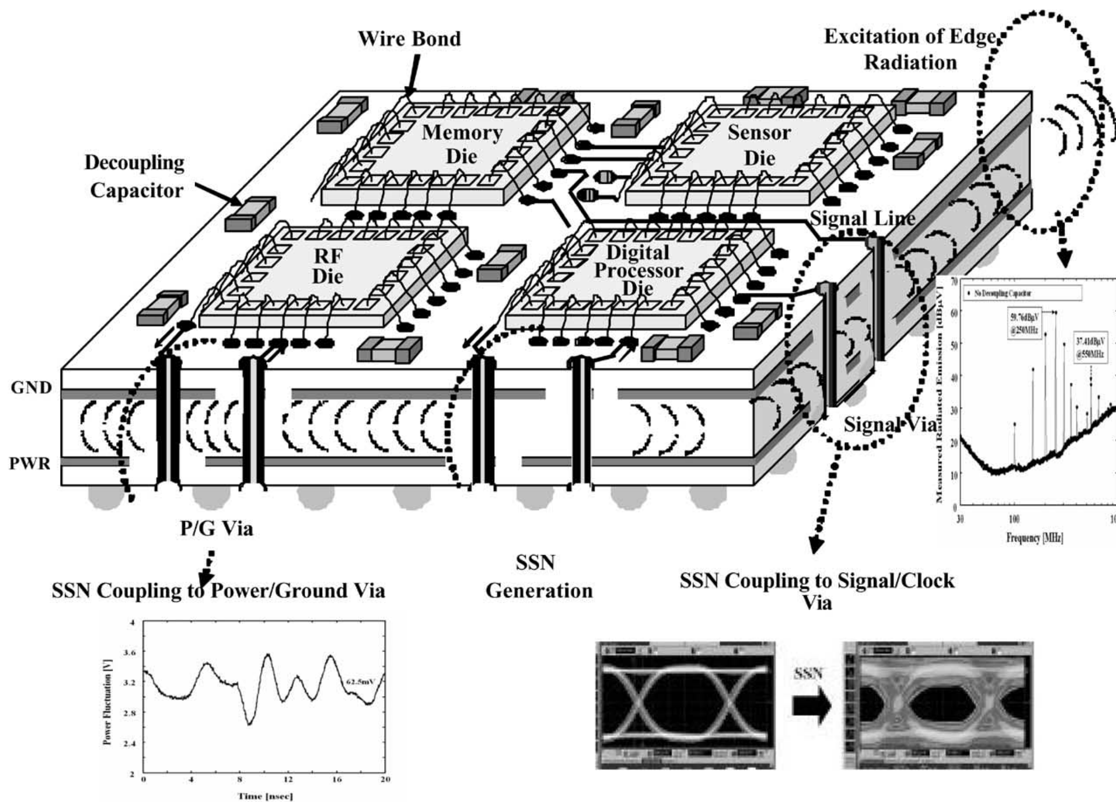


Fig. 3. Power distribution noise coupling in SOP.

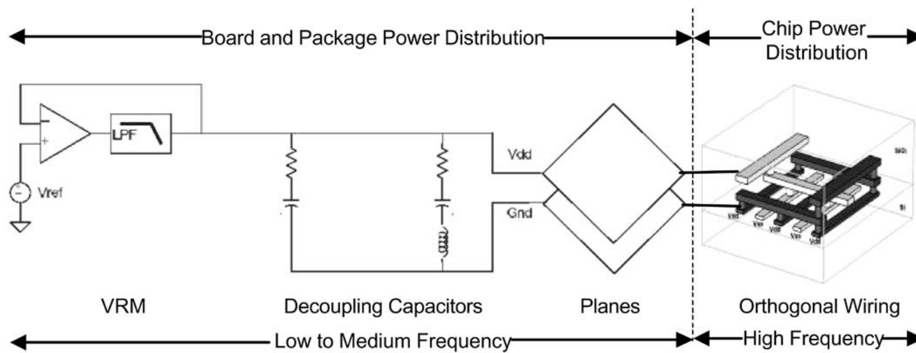


Fig. 4. Chip, package, and board power distribution network.

only one load, and hence, are also called point of load (POL) converters.

Besides the large current requirements, modern electronic circuits contain elements with several different supply voltages. Legacy 5 and 3.3 V logic devices are still common, but newer devices often require 2.5, 1.8, 1.5 V or even lower supply voltage. The pressing need for optimizing device speed while minimizing current consumption leaves little room to combine supply rails with similar but not exactly the same nominal voltage. The solution is, therefore, to place several dc-dc converters on the board to create the different supply voltages. The topology of these dc-dc converters is determined by two major system constraints, namely: 1) most of the supply voltages are lower than the voltage of the primary source to the board (output of ac-dc converter or battery), therefore, these converters usually have to step down the voltage and 2) isolation is very seldom required in these converters. In ac-powered systems, the isolation can be easily provided in the ac-dc converters.

Due to the aforementioned constraints, the single-phase, non-isolated buck converter is the most widely used dc-dc converter topology today, though for high-current applications multiphase converters are also becoming popular. In a few applications, step-up boost converters and polarity-reversing buck-boost converters are also used.

The challenges for the dc-dc converters are multifold. As a first challenge, the converters have to feed the low-voltage load with reasonable efficiency over a widely varying load-current range, which often requires synchronous rectification to keep losses low. The requirement of high efficiency in POL applications, however, is more a convenience than a technical necessity for reducing heat dissipation in the converter. Since the

POL converters have to be placed close to the load, which will eventually dissipate the full output power, increasing the efficiency of the POL converter barely reduces the total power dissipation. However, higher converter efficiency can result in a smaller converter volume, which is usually the driving factor. Depending on the size and cost of the converter, their efficiencies are in the 85–95% range. A second challenge is to optimize the converter's control loop to provide sufficiently low output transient ripple against the varying load current. Especially in the case of cascaded dc-dc converters, where the converter's input may have little transient filtering, the upstream converter's output has to deal with large current fluctuations. For example, a POL converter with 1.0 V output voltage and 30 A maximum current rating with a maximum of 60 mV_{pp} load transient noise (excluding switching ripple), requires an output impedance below 2 mΩ (including the capacitors). At dc, providing low-output resistance is relatively easy. With increasing frequency, however, the drooping loop gain creates an increasing output impedance of the converter. For guaranteeing unconditional stability against the unknown load impedance, some converters have very low bandwidth. If the converter's output impedance, for instance, exceeds the required 2 mΩ at 1 kHz, the on-board capacitors have to provide the impedance. At 1 kHz, 80 000 μF capacitance is required for providing a 2–mΩ capacitive reactance. As an illustration, Fig. 5 shows the small-signal output impedance of a POL converter at 1.5-V 20-A load, with a 680-μF external capacitor. A third challenge is to keep the conducted and radiated emissions of the converters under control. The converters are often placed very close to high-speed low-swing digital interconnections and sensitive analog circuits. Since the peak ac current ripple is always higher in the converters than their dc output current, care has to be taken to minimize the switching noise the converters introduce to nearby circuits. To reduce this interference, spread-spectrum converters have been introduced [5].

B. Bypass Capacitors

For wide frequency portions, the target impedance requirement may be flat, which corresponds to resistive impedance. Most available decoupling capacitors, however, have moderate or high quality factor (Q), making it a challenge to create the flat impedance profile required. It has been shown ([6], [7]) that bypass capacitors with $Q \ll 1$ help to create flat impedance profiles with a minimum number of components. For fixed equivalent series resistance (ESR) and equivalent series inductance (ESL), the Q of the capacitor varies inversely with capacitance. Therefore, creating smooth impedance transitions with large bulk capacitors, even with a low ESR, is an easier task. Providing a smooth impedance profile with multiple lower-valued low-ESR ceramic capacitors is difficult and challenging, especially when the frequency dependency of capacitance, resistance and inductance are taken into account. In [6] the bypass quality factor (BQF) was introduced as a measure of effectiveness of the capacitor to cover a wide frequency range where $\mathrm{BQF} = \mathrm{C/L}$ (C: Capacitance; L: Inductance), indicating that a capacitor is more effective if the C/L ratio is higher.

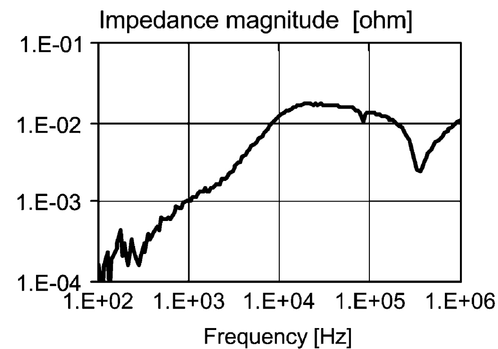


Fig. 5. Measured small-signal output impedance of a $V_{in} = 3.3$, $V_{out} = 1.5$ V, 20-A POL converter with full dc load.

For several hundred microfarad and higher capacitance values tantalum, niobium and various electrolytic capacitors have been used. The large capacitance dictates relatively large capacitor bodies, which in turn represents large inductance. Electrolytic capacitors in standard radial packages require a bottom seal in the can, creating few nano-henries of inductance. Tantalum and niobium capacitors are usually offered in brick case styles. The typical construction has a clip connection for the anode, introducing more than one nano-Henry inductance in spite of the smaller case style. Recently low-inductance face-down constructions have been introduced with significantly lower inductance [8].

Using multiple via connections can decrease the overall loop inductance [9]. With state-of-the art low-inductance capacitor constructions, the inductance limitation becomes the external connections formed by pads, escape traces, and vias. Using multiple via connections can decrease the overall loop inductance. This realization has given rise to capacitor case styles with multiple terminals. Today the lowest inductance can be achieved with the various C4 or BGA capacitor packages [10]. When connected to the power/ground planes inside a board or package substrate, the vertical via connections remain as the ultimate limiting factor for lowering inductance. This limitation can be removed by using embedded discrete or distributed capacitors, which is a major challenge due to the high capacitance values required.

High frequency measurements represent a very important part of evaluating the effectiveness of decoupling capacitors. Measured data show that the magnitude and slope of change in resistance and inductance above the Self Resonant Frequency (SRF) depends on the ESR and on the relative dimensions of the capacitor body, pads, vias, and closest planes. Since ESR(f) and ESL(f) are frequency dependent parameters that depend on the geometry, it is important to measure the parts in a fixture, containing pads, vias and planes with geometries similar to actual usage. This ensures that the measured complex impedance reflects both the device under test and the fixture. Since only the resistance of the fixture can be de-embedded and not the inductance, through appropriate compensations [11], the capacitance versus frequency and inductance versus frequency functions can be extracted over a wide band range. The low impedance values associated with today's bypass capacitors can be conveniently measured using Vector Network Analyzers in two-port connections [12]. Fig. 6 shows the construction and connection to a

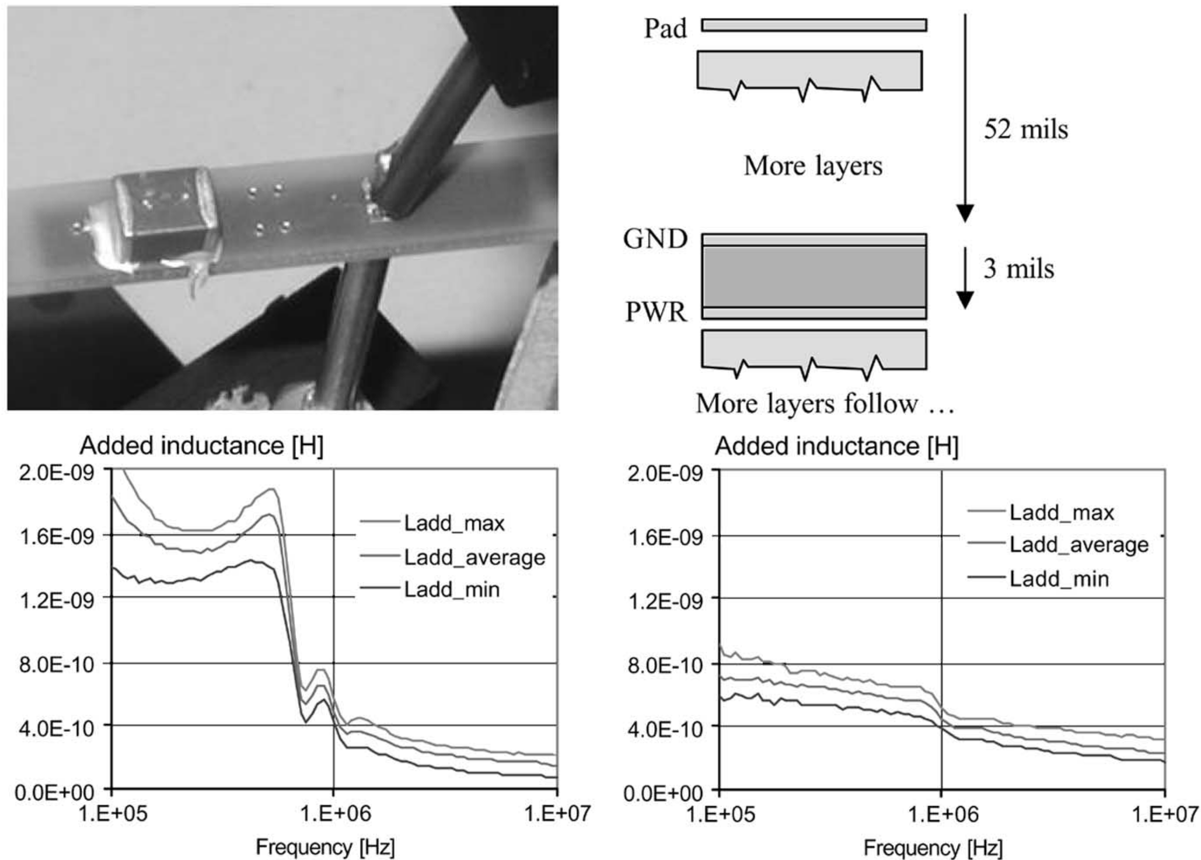


Fig. 6. Top left: Photo of test fixture with a mounted capacitor and two probes. Top right: Vertical stack up of fixture. Lower left: Added inductance statistics of ten samples with horizontal orientation. Lower right: Added inductance statistics of the same samples with vertical orientation.

small test fixture. Capacitors were connected to the fixture's surface pad with uncured conductive epoxy. The measured data in Fig. 6 compares the added inductance of parts with horizontal and vertical orientation.

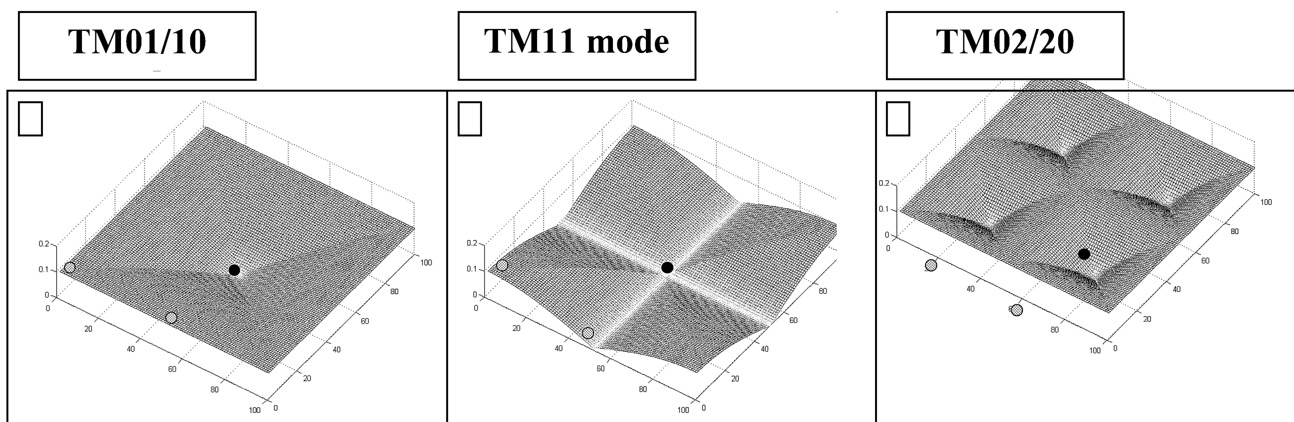
C. Package and Board Planes

Package planes are effective for power distribution in the mid-frequency range. However, a major problem with power/ground planes is their behavior as electromagnetic resonant cavities, where dielectric constant of the insulator and the dimensions of the cavity determine the resonance frequency. When excited at the resonance frequency, the planes become a significant source of noise in the package and the board and also act as a source of edge radiated field emission. The standing waves in the cavity at resonance can produce significant coupling to neighboring circuits and transmission lines [13].

Fig. 7 depicts the voltage distribution of simultaneous switching noise on the power and ground planes for an open-ended board of size $\mathrm{a} \times \mathrm{b}$. As can be seen from the figure, voltage distribution depends on the resonance mode, while the resonance frequency is determined by the mode number, dielectric constant of the insulator, and physical size of the planes. Since the size of the package is smaller than the board, the plane resonance frequencies of the board appear at a lower frequency than the package. When numerous decoupling capacitors are connected to the package power/ground plane cavity through the power/ground vias, the resonance frequency and the associated field distribution change due to the change in the effective capacitance and inductance of the plane cavity. The degree of the field distribution change and the resonance frequency shift depends on the effective ESL of the decoupling capacitors and vias. Furthermore, the field distribution and the resonance frequencies can be slightly modified by the die attachment onto the package substrate. Unless the bonding inductance is extremely small, the number of the power/ground bonding pads is large, or the on-chip decoupling capacitor is large, the change in the field distribution and resonance frequency are minimal.

At the plane resonance frequency, the power distribution impedance reaches its highest value, with the maximum value dictated by the losses in the structure. The loss includes radiation loss, conductor loss, dielectric loss, and component loss. The loss lowers the quality factor at resonance and hence reduces the noise [14]. In general, radiation and dielectric loss do not provide enough damping to completely eliminate resonance. Conduction loss can damp the resonance between power and ground planes when thin dielectrics are used [14].

At the modal resonance frequencies of the power and ground planes, the self-impedance and transfer-impedance magnitudes may be large enough to create signal-integrity and Electromagnetic Interference (EMI) problems. The resonance may be suppressed in several ways. It has been shown that dielectric thickness below $\sim$10 um forces a large part of the electromagnetic



$$(f_r)_{mn} = \frac{1}{2\pi\sqrt{\mu_0\varepsilon_0\varepsilon_r}}\sqrt{\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2}$$

Fig. 7. Voltage distribution and resonance frequencies generated by the power/ground plane cavity resonance on a open-ended PCB of size $(a \times b)$. Depending on the resonance mode, the voltage distribution and the resonance frequency varies.

field to travel in the conductor rather than in the dielectric, thus effectively suppressing the plane resonance through conductive loss [15]. Lossy dielectric layers have also been proposed [16], though their potential impact on signals have not been published yet. For power-ground laminates with thickness greater than 50 μm, the plane resonance needs to be suppressed by other means. The smoothest impedance profile can be achieved with the lowest number of parts if the cumulative ESR of bypass capacitors equals the characteristic impedance of the planes [17]. This requires either ceramic bypass capacitors with controlled ESR, or low-inductance external resistors in series with low-ESR bypass capacitors [17].

D. Chip Power Distribution

High performance on-chip power distribution networks are typically constructed as multi-layer grids as shown in Fig. 4. Designing on-chip power distribution networks in high performance microprocessors has become very challenging due to the continual scaling of CMOS process technology [18]. Each new technology generation results in rapid increase in circuit densities and interconnect resistance, faster device switching speeds, and lower operating voltages. These trends lead to microprocessor designs with increased current densities and transition rates, and reduced noise margins. The large currents and interconnect resistance cause large resistive IR voltage drops while the fast transition rates cause large inductive LdI/dt voltage drops in on-chip power distribution networks. Along with large voltage drops due to large dI/dt, Electro-migration (EM) is one of the critical interconnect failure mechanisms in integrated circuits [19]. Electro-migration, which is the flow of metal atoms under the influence of high current densities, causes increased resistance and opens in on-chip interconnects, causing further IR drops and potential reliability problems.

On-chip power distribution systems for high performance CMOS microprocessors must provide a low impedance path over a wide frequency range. The impedance of the power distribution inductance increases with frequency according to $\mathrm{Z} = \mathrm{j}\omega\mathrm{L}$, where $\omega = 2\pi\mathrm{f}$, f is the frequency, and L is the inductance. On-chip decoupling capacitance is used as a local power source, which effectively lowers the power distribution impedance at high frequencies. Hence, high frequency switching currents are "decoupled" from the inductance in the power distribution system and switching noise is, therefore, reduced. The on-chip decoupling capacitance includes both the intrinsic decoupling capacitance (N-well and quiet circuit) and the add-on capacitance [18]. Intrinsic decoupling capacitance alone is not sufficient for acceptable noise suppression in high performance microprocessor designs. Additional capacitance, many times in the form of thin-oxide capacitors, which uses a thin-oxide layer between the n-well and poly silicon gate, is required.

A major problem in combining the chip and package power distribution is chip-package resonance. The package inductance and chip decoupling capacitance form a parallel *RLC* circuit which resonates at the frequency $f = 1/2\pi\sqrt{LC}$, where L is the equivalent inductance of the package and C is the total non-switching capacitance on-chip between the voltage and ground nodes. At this frequency, the power distribution seen by the circuits on the chip is in its high impedance state. If the chip operating frequency is near or at the chip-package resonant frequency, the circuits will be starved for current. A large voltage fluctuation can build up over many cycles if the resonant frequency is sufficiently high. In future generations of CMOS microprocessors, large amounts of on-chip decoupling capacitance has to be used to aggressively control switching noise that maintains the chip-package resonant frequency well below the operating frequency [20]. A typical signature of ac differential noise at the center of a microprocessor operating at 3 GHz that consumes 150 W of power with a 1 V supply is shown in Fig. 8. In Fig. 8, 210 nF of on-chip decoupling capacitance was used along with a low inductance flip-chip package. The mid frequency step response occurs when chip power changes abruptly from 0 W to the maximum power. The magnitude is decreased with on-chip decoupling capacitance. The oscillation frequency is the chip-package *LC* resonance. The midfrequency noise is

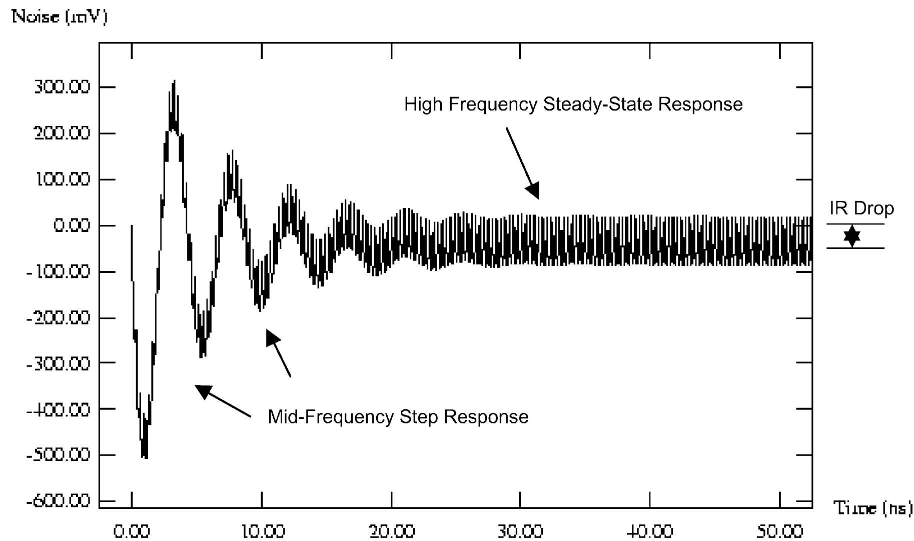


Fig. 8. On-chip ac differential noise for ITRS 2003 node. Includes 210 nF of on-chip decoupling capacitance.

eventually damped, resulting in a residual high frequency ac noise in the steady state. This steady-state response is due to the periodic switching of the microprocessor. The high-frequency steady-state noise rides on a dc offset, which is the IR drop due to the chip power distribution resistance.

In the past, CMOS active power has been the main focus with respect to power delivery and management. However, as CMOS scales to 90 nm and below, process related device leakage current represents a significant passive power component. This passive power includes many sources of device leakage current, such as junction leakage, gate-induced drain leakage, subthreshold channel currents, gate-insulator tunnel currents, and leakages due to defects [21]–[24]. Two of these leakage currents, the gate-insulator tunnel current and the subthreshold channel current, are fundamental to the scaling of technology. Gate leakage current can be reduced by using high-k dielectric materials as a replacement for silicon dioxide as the gate dielectric. The subthreshold component of power remains one of the most fundamental challenges as it approaches the active component near the 65-nm technology node. This passive power component places a further strain on the on-chip power distribution system as it erodes the dc IR drop noise budget and compounds the electromigration problem.

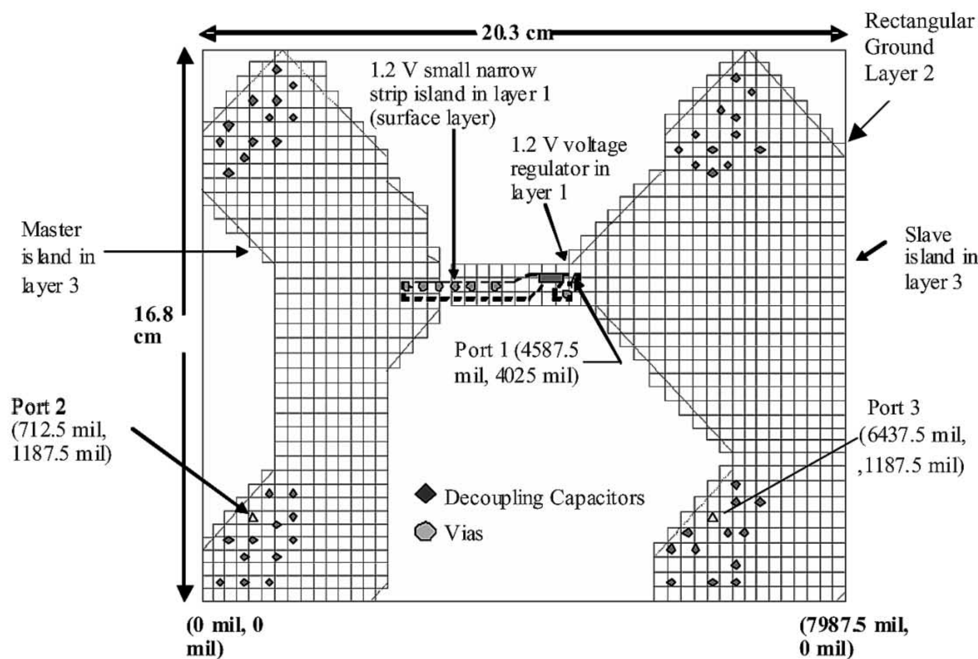
On-chip voltage islands (logic and memory regions on chip supplied through separate, dedicated power feeds) is becoming a design approach for managing the active and passive power problem for high-performance designs [24]. In such designs, the voltage level of an island is independent of other islands and is supplied from an off-chip source or on-chip embedded regulators. The design goal is to define regions of circuits within the chip, which can be powered by a lower supply while maintaining performance objectives and providing a reduction in active and passive power. Performance limited critical paths are powered by the maximum voltage that the technology is optimized for, while paths with sufficient timing slack are powered with a lower supply. Voltage islands in on-chip power distribution present challenges since isolation of decoupling capacitance reduces its effectiveness for nearby islands. Additional transients due to the activation and deactivation of islands must be managed. The distribution of multiple power supplies complicates the on-chip power grid design and introduces a potential wiring density loss.

III. Modeling of Power Distribution Networks

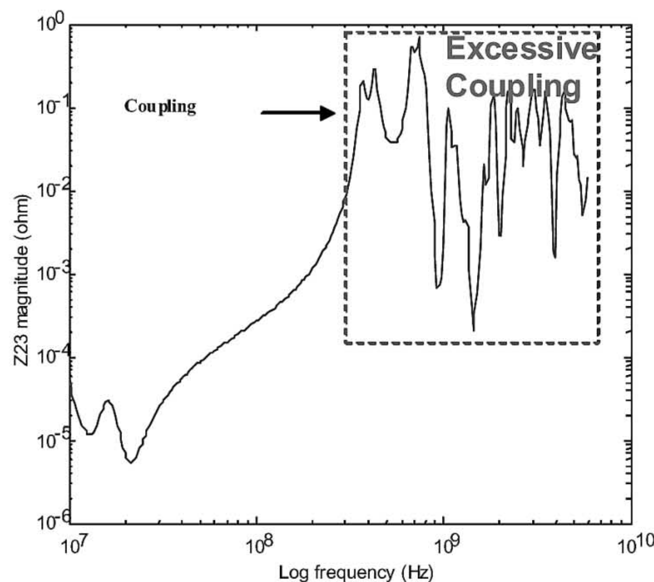
Modeling of power distribution networks represents an integral part of the power delivery design process. In the last 15 years, the modeling methods have evolved to a point where complex power distribution structures can be modeled accurately, with minimum CPU time. This has led to design methodologies for the prelayout analysis and postlayout verification of the packages, which has enabled the design of multigigahertz microprocessors and systems.

In the early 1990s, the partial element equivalent circuit (PEEC) based methods were developed for analyzing power distribution structures. These methods were based on the seminal paper by Ruehli [25], which enabled the representation of interconnections using partial inductances. The PEEC-based methods were used to analyze Delta I or power supply noise in high-performance computers [26], packaged CMOS devices [27] and first level packages [29]. In [27], the effect of negative feedback due to power supply noise on nonlinear CMOS inverters has been discussed. A birthday cake approach was used in [29] using PEEC, where multilayered packages were represented using a network of inductors. Finally, Fast Henry, a multipole based PEEC method was developed in [30] for speeding computations. With increase in clock frequencies, the frequency behavior of the power and ground planes became important, and hence, their distributed modeling became necessary.

Distributed modeling of power distribution networks requires the descritization of Maxwell's equations, which can be formulated in the frequency or time domain by solving integral or differential equations. Examples include the finite difference time domain (FDTD) [28], [33], [44] method and frequency domain methods such as the transmission line



(a)



(b)

Fig. 9. (a) Power islands. (b) Coupling between islands.

method [31], cavity resonator [32], [34] method, transmission matrix method (TMM) [38], and integral equation method [37]. Since, package power distribution networks are resonant circuits with high quality factor, the frequency domain methods provide better accuracy and efficiency than the time domain methods. However, since on-chip power distribution structures are lossy and have low quality factor, time domain methods are preferable due to the size of the network that requires analysis. Using these methods, multilayered planes with vias can be modeled with relative ease [38].

As an example, consider the irregular structure shown in Fig. 9(a), which was modeled using the TMM [39] for extracting the coupling between the master and slave power distribution islands. A rectangular grid was used, as shown in Fig. 9(a), with a unit cell size of 0.385 cm $\times$ 0.385 cm, which corresponds to an electrical size of $\lambda/6$ at 6 GHz. This resulted in 1087 unit cells for approximating the structure which included the narrow rectangular strip on layer 1, voltage regulator on layer 1, the continuous ground plane on layer 2, and the split plane in layer 3, as shown in Fig. 9. The seven vias connecting layers 1 and 3 were represented as short circuits and modeled in TMM by enforcing the continuity of the currents and voltages at these sections. TMM was used to compute the 3×3 impedance matrix which provides the self and transfer impedance at the three port locations. The transfer impedance of the master and slave sections in layer 3 was simulated across

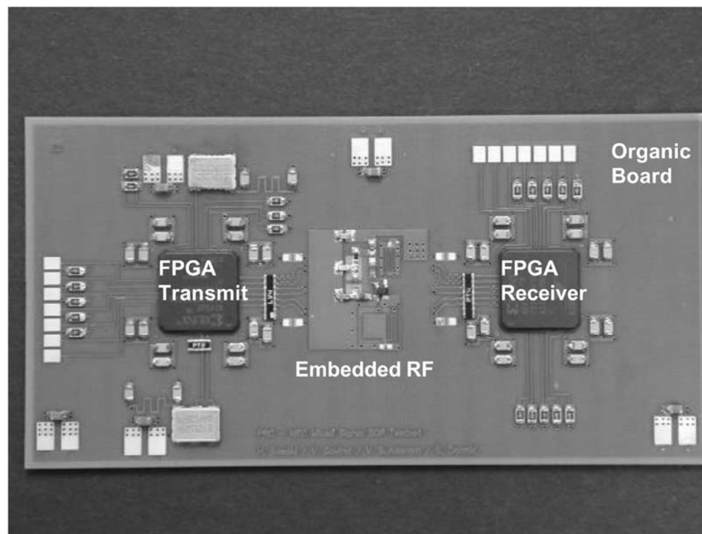


Fig. 10. SOP integrating digital and RF functions.

the master and slave split sections from 10 MHz to 6 GHz. In Fig. 9(b), the transfer impedance between the master and slave split sections shows little coupling at low frequencies since separate islands were used to supply power to the master and slave sections. However, substantial coupling between the master and slave sections can be observed at high frequencies even though these sections are separated. This is because the narrow strip from the voltage regulator that is used to maintain the same potential on the two islands induces inductive and capacitors coupling between the islands. When the two islands resonate, they couple energy through the coupling capacitance [39], which is a source of problem for sensitive digital and mixed-signal packages.

Model reduction [35] and macromodeling methods [36], [40]–[42] have been developed and applied to power distribution structures for reducing the problem size and for black-box representations. The frequency response from linear time invariant networks have been interpolated using vector fitting in [36] and broad-band macromodeling in [41], which enables the representation of the network as a reduced spice netlist to which other circuit elements can be connected. In [40] and [42], radial basis functions and spline functions (with time derivatives) have been used for the macromodeling of nonlinear drivers. Macromodeling of nonlinear drivers results in a computational speedup of $20\mathrm{X}$–$250\mathrm{X}$ as compared to transistor level circuits with no reduction in accuracy. The noise on the power supply rails of a transistor circuit affects its output current slew rate $(\mathrm{dI}/\mathrm{dt})$ through negative feedback effect [27], and hence the modeling of power distribution networks in the presence of nonlinear circuits becomes necessary.

Simulation of power supply noise requires the frequency response of the power distribution network and the current source exciting it. A good estimation of the current source is necessary without which the modeling of power supply noise is not possible. Surprisingly, though many methods have been developed for modeling the interconnections in the power distribution network, few methods are available for representing the source waveform. In [43], a preliminary method has been described for extracting models for the noise current signatures. After denoising the measured voltage waveform through wavelet transform and thresholding, noise current source models have been developed using the complex pencil of function method in [43]. Considerable work is still required in this area.

Modeling of power distribution is incomplete without analyzing the on-chip power distribution network. The interaction between the on-chip and package power distribution is important for addressing issues such as chip-package resonance, I/O planning and decoupling capacitor optimization. Though numerous methods have been developed by the IC community for modeling on-chip power distribution, the effect of package parasitics is completely ignored. Hence, the burden is on the packaging community to ensure that the package power distribution models interface well with the on-chip power distribution tools. Some aspects of chip—package co-simulation is available in [53]. In [44], the models in [53] have been extended for analytically extracting the parasitics of the on-chip power distribution through conformal mapping and simulation of the noise voltage using FDTD method.

As the technology migrates toward mixed-signal integration, numerous challenges arise for the modeling and simulation of power distribution networks. A major issue is the accuracy where noise levels in the -100 dB range need to be computed, which requires sophisticated modeling methods. Methods for computing the electromagnetic coupling between power islands and their impact on digital and analog circuits need to be developed. Since on-chip and package power distribution need to exist in perfect harmony, co-design methods need to be developed wherein the modeling of the chip and package power distribution can be combined. This can lead to optimum assignment of the I/Os and the distribution of capacitance between the two networks. Since testing high-frequency mixed-signal systems is difficult, modeling may be the only choice for evaluating the functionality of these systems.

IV. System on a Package Technologies

In mixed-signal packaging technologies that integrate heterogeneous functions, a major source of coupling is the power

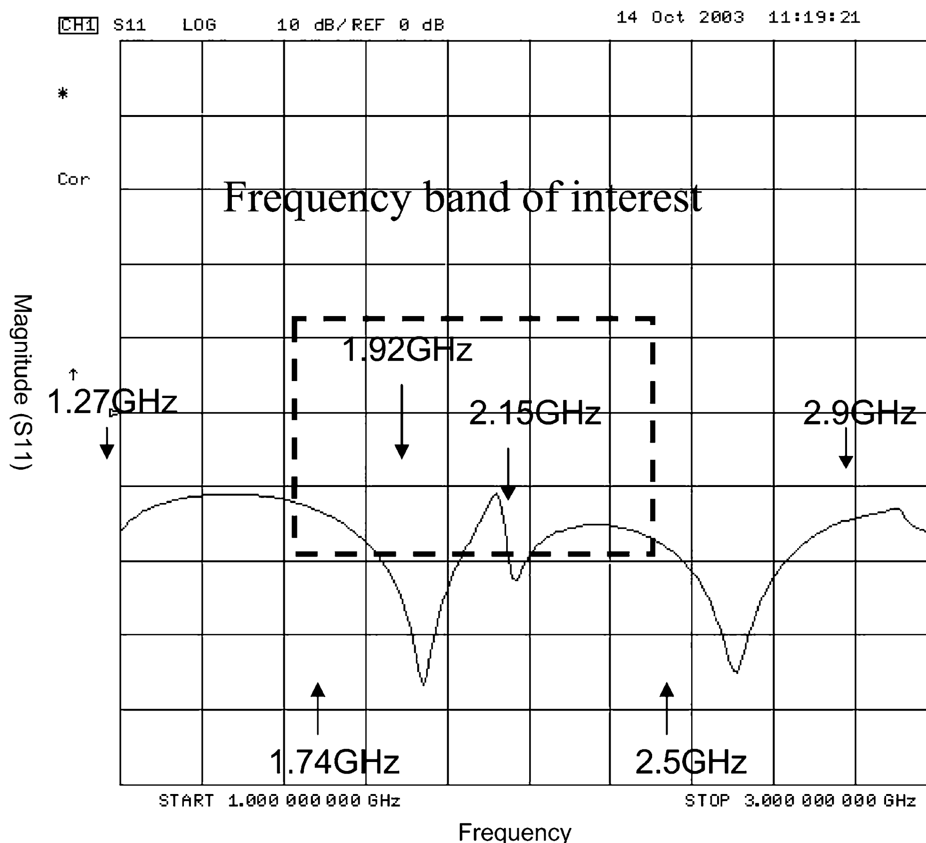


Fig. 11. Power plane resonance for digital—RF module.

distribution. Unlike digital circuits with large voltage swings, analog circuits are susceptible to noise through the power supply due to low voltages used. Hence, good decoupling and filtering schemes are necessary. With package level integration in SOP technologies, the coupling mechanisms increase and hence it becomes difficult to achieve the isolation levels required. With the reduction in voltage swing for digital circuits and increase in switching activity, the power supply noise has to be minimized both for the digital and analog circuits. In this section, the challenges and possible solutions associated with digital—RF integration in an SOP platform is discussed.

Consider Fig. 10, which consists of two field programmable gate arrays (FPGAs) on either side of an RF block. The FPGAs are digital ICs for transmitting and receiving digital data streams. The RF block uses embedded passive circuits for realizing low-noise amplifiers (LNAs). The board in Fig. 10, which measures the size of a cell phone, was fabricated using a sequential build-up process with A-PPE dielectric material on an FR4 printed circuit board with copper metallization. The board stack-up consists of signal, ground, power and signal layers with the embedded passives occupying the top two layers. The dielectric thickness separating the power and ground layers is 50 μm. Both the digital and RF circuits are powered using a common power supply. The FPGAs were operated at a frequency of 100 MHz with the RF carrier for the LNA at 1.83 GHz. The architecture in Fig. 10 mimics that of a mobile communication/computing device with integrated RF front end and baseband processing and, therefore, represents a good test vehicle [46] for illustrating the challenges associated with power distribution for mixed-signal packages.

The measured transmission coefficient (S21) for the power and ground planes is shown in Fig. 11. The response exhibits the typical standing wave pattern described earlier with peaks occurring at the 1.83-GHz RF carrier range. With digital circuits switching, substantial energy can be coupled to the RF circuits at the frequencies corresponding to the peaks in the standing wave pattern. The isolation level of -60 dB shown in Fig. 11 in the power distribution network between the digital and RF circuits is insufficient for most embedded RF circuits, and, therefore, needs to be improved to -100 dB or better. This is possible only through the integration of new technologies within the package. It is important to note that even though the digital interconnects are routed in the bottom layer with the power serving as a shield from the embedded passives, substantial coupling can still result due to the return currents that excite the cavity formed by the power and ground planes [45], [46].

One method for power supply isolation is through split island design whereby the power distribution for the digital and RF circuits can be separated. To enable the use of a common power supply, embedded filters can be inserted between the power islands. Four different filtering schemes that are possible are shown in Fig. 12. The filtering schemes in Fig. 12 have been experimentally investigated in [47] using discrete devices wherein it has been shown that the C-ferrite-C filter scheme achieves greater than -40 dB isolation over a broad frequency range. The isolation property worsens at the resonance frequencies of the

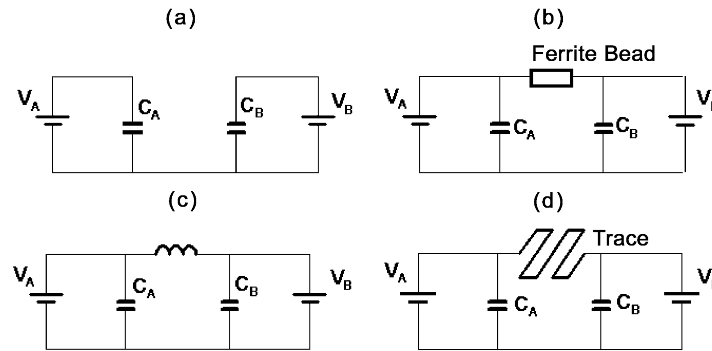


Fig. 12. Four possible power supply filtering schemes for SOP. (a) Filter type A: plane split. (b) Filter type B: Ferrite bead. (c) Filter type C: Chip inductor. (d) Filter type: Trace inductance.

discrete devices and hence there is a clear need for embedded passive devices for power supply filtering in SOP technologies. Even with embedded filtering, it is very challenging to achieve the -100-dB isolation required.

A technology that is beginning to mature is embedded decoupling where capacitance layers can be integrated into the substrate. The capacitance layers help reduce the power distribution impedance and provide good filtering and isolation capabilities. The advantages of embedded decoupling are two fold, namely: 1) it minimizes the parasitic inductance between the chip and the capacitor, thereby improving the capacitance effectiveness over a broader frequency range and 2) it serves as a reservoir of charge in the midfrequency range. Two embedded capacitor technologies are currently available, namely the discrete embedded capacitor [48] where islands of capacitors are embedded in the package and the distributed embedded capacitor where the area between the power and ground planes contains the capacitance [49]. In [49], the distributed capacitance using nanocomposites is described in detail with the fabricated test vehicle and cross section shown in Fig. 13. The cross section consists of three metal layers namely, signal, power, and ground with a 15–20-μm separation between the power and ground planes. The nanocomposite material with relative permittivity of $\varepsilon r = 15$ fills the region between the power and ground resulting in a capacitance of ~ 1 nF/cm^2, while a low dielectric material is used for the signal layers. Though the capacitance is not high, the low inductance between the power and ground planes lowers the impedance of the structure at a high-frequency range (self and transfer impedance), reduces power supply noise and serves as a good filter for isolating the digital and RF blocks. In [49], a 10X reduction in power supply noise has been reported using the structure in Fig. 13. A major problem with using the structure in Fig. 13 for multiple layers is the capacitive loading of signal vias traversing the high dielectric constant layer and pin-hole defects creating a short between the layers. Patterning the capacitance layers and converting the distributed capacitance to embedded discrete capacitors can solve this problem. However, this requires an additional layer of metallization. In Fig. 13, a better solution could be the use of a low dielectric constant but thin dielectric material (<300 nm) between the power and ground planes, which can be made multilayered and can reduce the inductance by 50X compared to the solution in [49]. In addition, to accommodate the capacitance requirements in the future, new technologies are required that provide embedded capacitance in the range of 1–10 μF/cm^2.

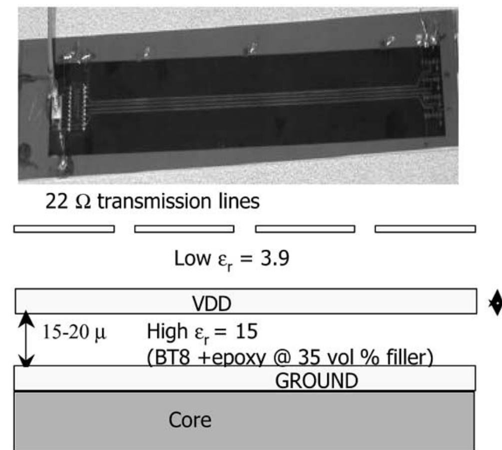


Fig. 13. Fabricated board (top) and board cross section (bottom) with nanocomposite capacitance layer integrated in the board.

Recently, electronic bandgap structures (EBG) has been proposed for minimizing the coupling through the power distribution networks for digital systems [50], [51]. These structures can be modified and applied to mixed-signal packages for achieving isolation levels of -100 to -120 dB [52]. Embedded low-pass filters in the vicinity of a digital IC can be used for ensuring that the fundamental frequency of the clock does not create intermodulation products at the output of an RF circuit. In addition the EBG structures can be used to provide further isolation at higher frequencies by ensuring that the harmonics of the clock do not get coupled. EBG structures are periodic structures in which propagation of certain bands of frequencies is prohibited. The EBG structures can be designed as part of the power distribution network for achieving broadband isolation and is tunable, cost-effective, and compact. One embodiment of the EBG structure consists of a two-dimensional (2-D) square lattice with each element consisting of a square metal pad with two connecting branches, as shown in Fig. 14(a). This structure can be realized with metal pads etched in the ground plane connected by narrow branches to form a distributed LC network. In this structure, narrow branches introduce inductance and the small gap between neighboring metal pads increases capacitance. The

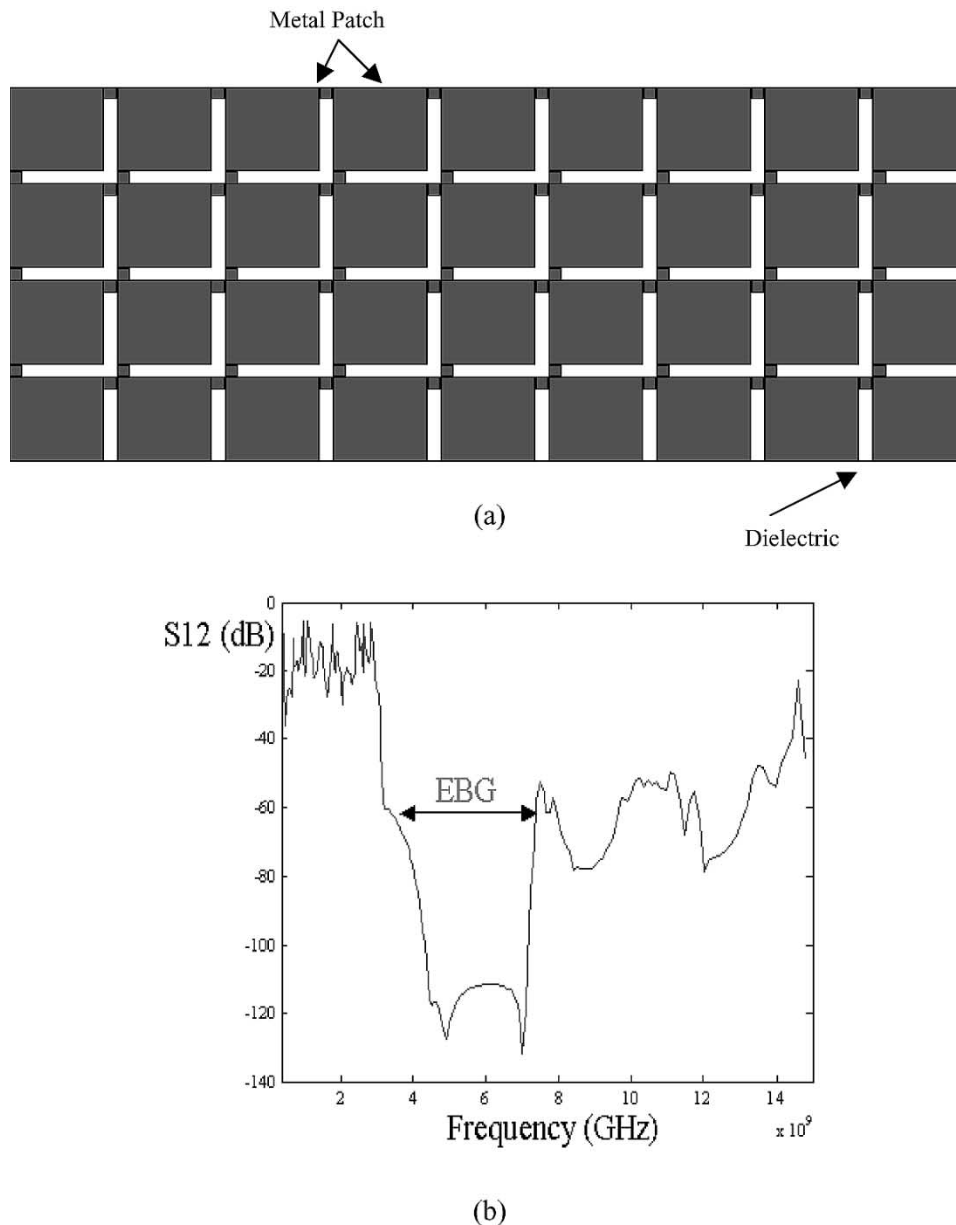


Fig. 14. (a) EBG using patterned ground plane. (b) Transmission coefficient (S_{12}) between input port and output port for mixed-signal SOP.

structure is via-less with a thin dielectric (4 mils) separating the layers. The transfer characteristics (S12) of the EBG structure for the mixed-signal board in Fig. 10 is shown in Fig. 14(b). The structure consists of a two-layer board with dimensions of 10 cm by 5 cm. The dielectric material of the board is FR4 with a relative permittivity $\varepsilon_{\rm r} = 4.5$, the conductor is copper with conductivity $\sigma_{\rm c} = 5.8 \times 10^7$ S/m, and dielectric loss tangent $\tan(\delta) = 0.02$ at 1 GHz. The copper thickness for the power and ground planes was 35.56 μm with a dielectric thickness of 4 mils. The input and output ports were placed on either side of the board. Preliminary results with no decoupling capacitors show -120 dB stopband rejection over a frequency range of 3 to 8 GHz. With thin dielectric layers, the stopband can be tuned by modifying the structure such that the center frequency and bandwidth can be controlled. In general, at least six metal patches are required to obtain isolation levels of -120 dB between two points on the structure in Fig. 14(a).

It is important to note that the primary source of power supply noise is the inductance in the package and board. The power supply noise varies linearly with inductance $(\mathrm{LdI/dt})$ and provides high impedance to the integrated circuit at high frequencies. With CMOS scaling and integration in an SOP platform, power supply inductance has to be reduced from the 10-pH range in today's high-performance computers to the sub-picohenry range. This is possible only through the elimination of the first level package, direct chip attach on the board, and the availability of integrated boards with high-density wiring and micro-via technology. Though numerous mechanical and reliability problems need to be solved, wafer level packaging provides for a good electrical solution with minimum power supply noise. A conceptual power distribution scheme for a wafer level package (WLP) on an integrated board is shown in Fig. 15(a) which uses rigid or compliant interconnects between the WLP and board on 100–200-μm pitch and uses multiple

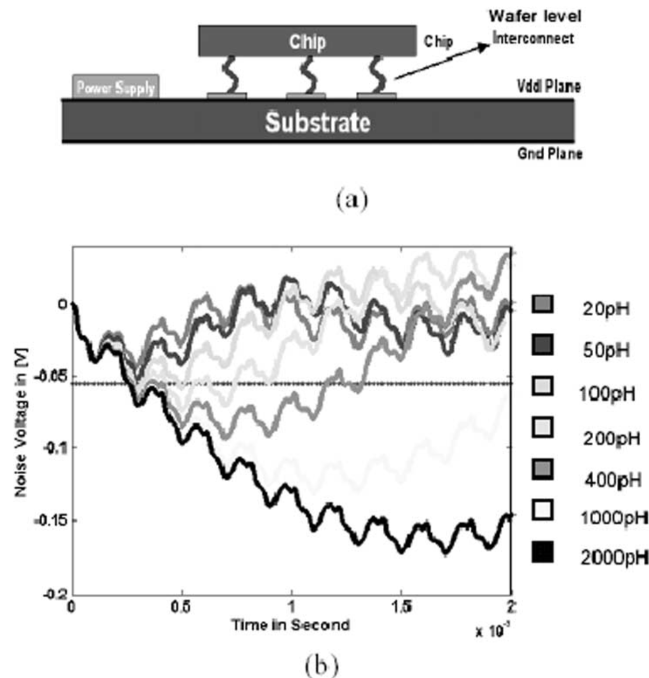


Fig. 15. Power integrity simulation using various wafer level interconnect inductance for 5-GHz chip operation. (a) Simulated wafer level packaging structure. (b) Differential noise induced on power supply with 40% switching activity.

planes in the board with the voltage regulator module placed close to the WLP. The goal is to minimize the inductance by using short horizontal (planes) and vertical (micro vias, solder bumps, nanosprings) interconnections for minimizing inductance, which allows for a noise free environment in which to integrate RF electronics with embedded functions in the same package. An important parameter for wafer level packaging to be attractive is the loop inductance between the voltage and ground rails, which is dictated by the compliant (or rigid) interconnect length and pitch. Preliminary simulations [53] based on ITRS 2005 (and beyond) indicate an inductance of 50 pH per interconnection for 5% noise tolerance on a 100–200-μm pitch. In [53], the power supply noise was simulated for various interconnect technologies with inductances in the range 20 pH– 2 nH to determine the optimum inductance required for the ITRS'05 node. The simulation assumed that the number of layers in Silicon was 4, the size of the chip was 20.1 mm $\times$ 27 mm, the number of power/ground interconnects was 2464, the number of CMOS inverters switched was 77616, 40% of the total power was switched and the on-chip decoupling capacitance was 400 nF. The switching frequency assumed was 5 GHz with the driver rise and fall time of 20 ps and period 200 ps. The droop in the voltage across the voltage and ground rails of the chip are shown in Fig. 15(b) along with a specified noise tolerance of 55 mV. A noise tolerance of 5% (of Vdd) indicates a WLP interconnect inductance of 50 pH, which translates to a 50-μm diameter bump on 100-μm pitch, details of which are available in [54].

V. Conclusion

In this paper, the status and challenges associated with power distribution has been discussed. Power distribution issues associated with the powering of digital and mixed-signal systems has been addressed with emphasis on the voltage regulator module, decoupling (surface mount and embedded), chip power distribution, modeling methods, and new technologies.

Acknowledgment

The authors would like to thank H. Sasaki of NEC Corporation for his work on the mixed-signal package while he was a visiting scholar with the Packaging Research Center, Georgia Tech. The authors would also like to thank J. Choi for his help with the EBG structure and the many researchers who are working on power distribution related issues around the world.

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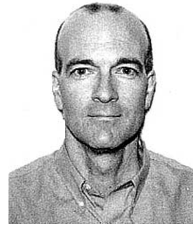
He is a Signal-Integrity Senior Staff Engineer with SUN Microsystems, Inc. Besides signal-integrity verification of high-speed buses, he designs and characterizes power-distribution networks, bypassing and decoupling of packages, and printed-circuit boards for workgroup servers. He has more than 27 years of experience with high-speed digital, RF, and analog circuit and system design, as well as teaching related subjects at Universities as regular courses and in industry short courses.

Dr. Novak was elected Fellow of the EEE for his contributions to the signal-integrity and RF measurement and simulation methodologies.



James P. Libous (SM'02) received the B.S. degree in electrical engineering from Union College, Schenectady, NY, and the M.S. degree in electrical engineering from Syracuse University, Syracuse, NY, where he is currently working toward the Ph.D. degree in electrical engineering.

Since 1981, he has worked in several areas within IBM, including logic and memory integrated circuit development, system signal and power integrity and noise containment design, CMOS ASIC technology development, and complex project and engineering team leadership. He was responsible for the development and application of advanced CMOS VLSI circuit and package technologies for System/390 midrange processors. In 1992, he joined the Advanced CMOS ASIC Technology Development Group, Microelectronics Division. He was a key member of the team responsible for the development of the first 1 000 000-circuit CMOS ASIC logic family. He was responsible for the development of several advanced nanometer CMOS ASIC products, leading cross-divisional teams of development engineers and serving as a consultant to senior management. He was also responsible for identifying strategic package technology requirements to complement future nanometer CMOS ASIC and microprocessor products. He currently is a consultant to senior management and provides technical leadership, guidance, and consulting in advanced nanometer CMOS chip and package electrical design. He is a Senior Technical Staff Member with IBM's System and Technology Group, Endicott, NY. He holds U.S. patents in the area of CMOS ASIC design and delta-I noise avoidance and has published several technical papers in refereed journals and conference proceedings. His research interests include signal and power distribution electrical design and the modeling of advanced nanometer CMOS circuits, chips, and packages, including design for noise avoidance and switching noise modeling, simulation, and laboratory characterization.

Mr. Libous serves on the Semiconductor Research Corporation Interconnect and Packaging Sciences and Student Relations Technical Advisory Boards. He serves as a Liaison/Mentor for SRC-funded research at Georgia Tech and IBM-funded research at Union College, where he established undergraduate SRC research. He is the Recipient of the 2002 Semiconductor Research Corporation Mahboob Khan Outstanding Mentor Award, a lifetime award that recognizes individuals who have had a significant impact on the technical contributions of SRC research, have been instrumental in transferring the research results to industry, and are deeply committed to the education of the graduate students. He contributes to the SIA and NEMI technology roadmaps and has participated in Georgia Tech's Packaging Research Center, Cornell University's Packaging Alliance, and the Interconnect Focus Center Workshop at Albany NanoTech. He was the Recipient of the Shri Mukhopadhyay Best Paper Award at the International Conference on Electromagnetic Interference and Compatibility in 2003. He serves on the IBM Invention Review Board and received the IBM Division Award, several formal and informal awards, and Invention Achievement Awards. He was the Recipient of IBM Valuable Patent Awards in 2002 and 2003 for having patents in the top 5% of the IBM Microelectronics patent portfolio. He was an invited speaker at the IMAPS Workshop on Next Generation IC and Package Technology and at the Integrated Electronics Engineering Center (IEEC) at the Watson School of Engineering, Binghamton University. He also serves on the IBM System and Technology Group Electronic Package Technology Technical Community Council and has served on task forces conducted by the IBM Academy of Technology. He was Cochair for the InterPack Electrical Design, Simulation, and Test track. He serves on the TC-EDMS, the technical committee on Electrical Design, Modeling, and Simulation, and TC-NANO, Nano Packaging, both within the IEEE CPMT Society. He has been a session chair and short course instructor for the IEEE Topical Meeting on Electrical Performance of Electronic Packaging. He is a Guest Editor and reviewer for the IEEE TRANSACTIONS ON ADVANCED PACKAGING. He also serves on the International Advisory Committee for the IEEE Electrical Design for Advanced Packaging and Systems (EDAPS).