Power Loss and Junction Temperature Analysis in the Modular Multilevel Converters for HVDC Transmission Systems

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Abstract

The power loss of the controllable switches in modular multilevel converter (MMC) HVDC transmission systems is an important factor, which can determine the design of the operating junction temperatures. Due to the dc current component, the approximate calculation tool provided by the manufacturer of the switches cannot be used for the losses of the switches in the MMC. Based on the enabled probabilities of each SM in an arm, the current analytical models of the switches can be determined. The average and RMS currents can be obtained from the corresponding current analytical model. Then, the conduction losses can be calculated, and the switching losses of the switches can be estimated according to the upper limit of the switching frequency. Finally, the thermal resistance model of the switches can be utilized, and the junction temperatures can be estimated. A comparison between the calculation and PSCAD simulation results shows that the proposed method is effective for estimating the junction temperatures of the switches in the MMC.

Key words: Analytical model, Conduction losses, Insulated gate bipolar transistors (IGBT), Junction temperature, Modular multilevel converters (MMC), Switching frequency, Switching losses

I. INTRODUCTION

In a modular multilevel converter (MMC) HVDC transmission system, it must be guaranteed that the operating junction temperatures T_j of controllable switches do not exceed the temperature limit in the whole operating range [1]. Therefore, the estimation of T_j is a key part of the MMC design procedure. At present, some switch manufacturers use approximate calculation tools for this purpose [2], [3]. The current of the switches in the MMC include dc and ac current components. Since these simulation tools can only calculate the losses and junction temperatures of the switches under sinusoidal currents, these tools can be used for 2-level voltage source converters (VSCs). However, they cannot be used for the MMCs.

Usually, the estimation of the junction temperature in the MMC design is based on datasheet values, conduction losses,

switching losses, and the thermal characteristics of the switches. In addition, the analysis of the conduction losses and switching losses of the switches is the first task. Annex B of IEC/TR 62543 [4] gives a general method to evaluate the losses of the converters in VSC systems. However, the International Standard does not provide the details to evaluate the losses of MMCs. Thus, finding a well understood and accepted method to evaluate these losses is very important.

For the losses in a 2-level VSC, the authors of [5]-[7] have studied the switching losses of the converter by fitting the corresponding parameters of the switching and conduction losses. The fitting parameters methods are validated by experiments. As for MMCs, the authors of [8] have provided a mathematical analysis for the average current and RMS current of the switches in a converter based on sinusoidal pulse width modulation (SPWM). However, this may result in excessive switching losses.

Masserant and Stuart [9] utilized the average current and root mean square (RMS) current to calculate the IGBT conduction and switching losses in a boost type power factor controller (PFC). The arm current of the MMC may flow through the upper IGBT or the lower free-wheeling diode
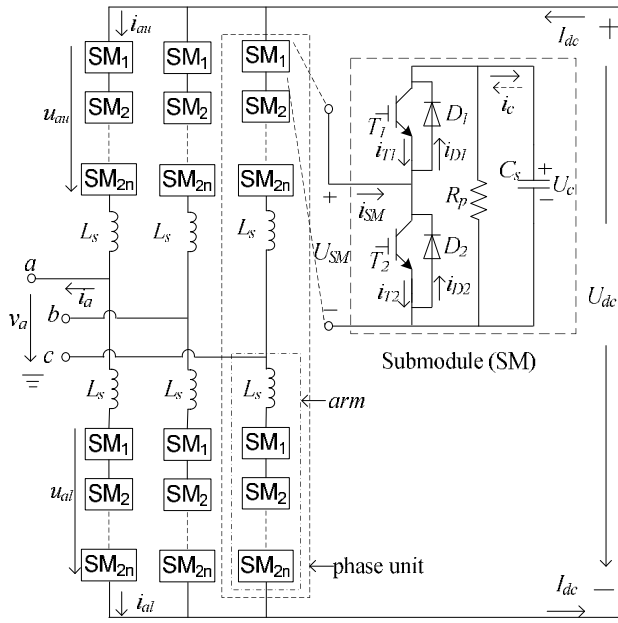
Fig. 1. Schematic representation of the MMC HVDC.

(FWD), and then through the lower IGBT or the upper FWD. Therefore, the RMS currents of the IGBT and FWD cannot be determined directly. The authors of [10], [11] proposed mathematical analysis to calculate the conduction and switching losses of the switches in a MMC. The two methods have good precision for loss estimation. However, they are computationally demanding and time consuming.

This paper has proposed using the enabled probabilities of each SM in the upper arm or lower arm considering the path of the arm current. The expression of the average current and RMS current of the upper/lower switches can be determined. Then, it is possible to obtain the conduction losses of the IGBT or FWD, and the switching losses of the IGBT or FWD from the point of the analytical method. This paper provides an estimation method for the junction temperature of the switch in the MMC.

II. MMC IN VSC-HVDC SYSTEMS

A. Basic Structure

A diagram of a three-phase MMC is shown as Fig. 1. The MMC mainly consists of three phase units. Each phase unit consists of one upper arm and one lower arm connected in series between two dc terminals. Each arm is made up of $2n$ series-connected half-bridge SMs and one arm inductor. The inductor L_s can be used to control the transmission power, to restrain the circulating current between different phases, and to limit fault currents under dc side faults.

The structure of the SM is shown on top right of Fig. 1. The SM is mainly made up of two IGBT-diode pairs with the IGBT and FWD connected in inverse parallel, one dc

capacitor C_s, and one DC grading resistor R_p. The output voltage U_{SM} of the SM has two values ($U_{SM}=U_c$ or 0), which depend on the switch-statuses of T_1 and T_2. The output voltage is U_c when the upper IGBT is switched on and the lower one is switched off. The output voltage is 0 when the upper IGBT is switched off and the lower one is switched on. The voltages of the SM with the output voltage U_c and 0 are enabled and bypassed, respectively. The reference directions of the voltage and current in the MMC are shown in Fig. 1.

B. Operating Mechanisms

The ac voltage of each phase can be obtained by controling the number of enabled and bypassed SMs in each arm. Under normal operation, the phase to ground voltage v_a and ac side current i_a (take phase a for example) can be defined as:

$$v_a(t) = E_m \sin(\omega_N t) \tag{1}$$

$$i_a(t) = I_m \sin(\omega_N t + \varphi) \tag{2}$$

where E_m is the peak value of v_a, ω_N is the fundamental angular frequency, I_m denotes peak value of i_a, and φ denotes phase delay.

Since three identical phase units are in parallel connection, the dc current I_{dc} of the dc transmission lines (cables/overhead lines) should equally distribute among the three phase units. In addition, the upper arm and lower arm in the phase unit are connected in parallel for i_a, which can equally divide between the upper arm and lower arm while neglecting the circulating current between the different phases. Thus, the currents in the upper and lower arms can be expressed as:

$$\begin{cases} i_{au}(t) = I_{dc}/3 + i_a(t)/2 \\ i_{al}(t) = I_{dc}/3 - i_a(t)/2 \end{cases} \tag{3}$$

From (2) and (3), the current in the upper and lower arms can be rewritten as:

$$\begin{cases} i_{au}(t) = [1 + k \cdot \sin(\omega_N t + \varphi)]I_{dc}/3 \\ i_{al}(t) = [1 - k \cdot \sin(\omega_N t + \varphi)]I_{dc}/3 \end{cases} \tag{4}$$

where current ratio k is:

$$k = \frac{I_m/2}{I_{dc}/3} \tag{5}$$

where i_{au} and i_{al} are the currents of the upper and lower arms, respectively.

III. CAPACITOR VOLTAGE BALANCING OF SMs

The capacitor voltage of each SM is a fluctuation voltage due to the charge or discharge current. In order to achieve voltage balance, the capacitor voltage must be monitored and kept within a small range of voltage deviations among the SMs. In addition, the capacitor voltages are sorted in ascending order. Under the inverter operation of the MMC,
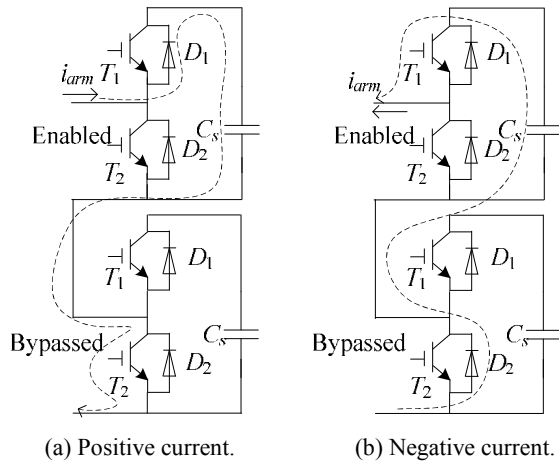
(a) Positive current.　　　(b) Negative current.

Fig. 2. Current paths and SMs state under inverter operation of the MMC.

the current paths and states of the SMs are shown in Fig. 2. In Fig. 2, the left current path is the positive current, and right current path is the negative current flowing through the enabled and bypassed SMs under the inverter operation. The voltage balancing algorithm has a significant impact on the circulating current, which obviously leads to the average and RMS currents of the switches. Here, the circulating current between the different phases is neglected [12].

From Fig. 2, it can be seen that, when the arm current i_{arm} is a positive current, the arm current flows through the capacitor of the enabled SM, and the capacitor is charged. On the other hand, when the arm current i_{arm} is a negative current, the arm current flows through the capacitor of the enabled SM, and the capacitor discharges. It can also be seen that, when the SM is bypassed, the arm current flows through T_2 or D_2 rather than the capacitor, and that the voltage of the bypassed SM can be kept constant. In order to keep the voltage balance between the different arms and phase units, the selection of the SMs depends on the state of the SMs and the path of the arm current. To obtain a desired arm voltage, the selection of the SMs can refer the following principles:

- When the arm current is positive or zero, if the arm needs to increase one SM, the chosen SM should be the bypassed SM with the lowest capacitor voltage, and the frequency of the switch action is the necessary switching frequency. When the capacitor voltage of the enabled SM is more than the allowable value, the enabled SM needs to be bypassed, and the bypassed SM with the lowest capacitor voltage should be enabled to maintain the number of enabled SMs. In addition, the frequency of the switch action is an additional switching frequency;

- When the arm current is a negative current, if the arm needs to increase one SM, the chosen SM
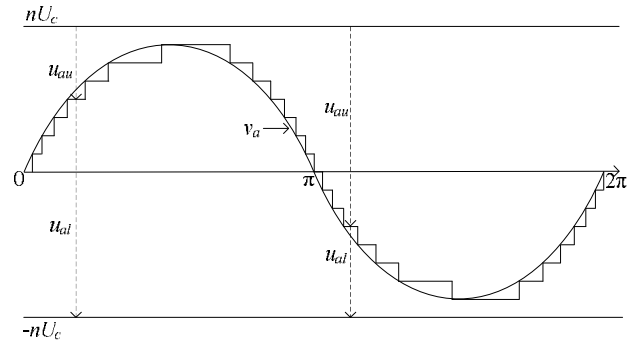
should be the bypassed SMs with the highest capacitor voltage, and the frequency of the switch action is the necessary switching frequency. When the capacitor voltage of the enabled SM is less than the allowable value, the enabled SM needs to be bypassed, and the bypassed SM with the highest capacitor voltage should be enabled to maintain the number of enabled SMs. In addition, the frequency of the switch action is an additional switching frequency.

In accordance with the above principles, the voltage balance between different arms and phase units and the safe operation of the SMs can be obtained effectively.

IV. SM ENABLED PROBABILITY

Since the terminal voltage U_{dc} from the positive terminal to the negative terminal of the MMC is constant, when one SM is bypassed in the upper arm, one SM should be enabled in the lower arm, and vice versa. With the nearest level control (NLC) modulation technology [13], the voltage of the upper and lower arms are shown in Fig. 3 (take phase a and $n=4$ for example).

According to Fig. 3, the voltages of the upper arm and lower arm satisfy:

$$\begin{cases} u_{au}(t) = U_{dc}/2 - v_a(t) \\ u_{al}(t) = U_{dc}/2 + v_a(t) \end{cases} \tag{6}$$

If the number of SMs is large enough, the output voltage of the MMC can be taken as a roughly sinusoidal voltage. Equation (6) can be rewritten as:

$$\begin{cases} u_{au}(t) = (1 - m\sin(\omega_N t))U_{dc}/2 \\ u_{al}(t) = (1 + m\sin(\omega_N t))U_{dc}/2 \end{cases} \tag{7}$$

where the modulation index m is:

$$m = \frac{E_m}{U_{dc}/2} \tag{8}$$

The voltages u_{au} and u_{al} are the total voltages of the enabled SMs in the upper and lower arms, respectively. With the assumption that the SM capacitor voltage $U_c(t)=U_{dc}/2n$,

Fig. 3. Staircase output voltage on ac side of the MMC with the example of n=4.

the number of enabled SMs in the upper and lower arms can be expressed as:

$$\begin{cases} n_{au}(t) = u_{au}(t)/U_c = n(1 - m\sin(\omega_N t)) \\ n_{al}(t) = u_{al}(t)/U_c = n(1 + m\sin(\omega_N t)) \end{cases} \quad (9)$$

where $n_{au}(t)$ and $n_{al}(t)$ are the numbers of the enabled SMs in the upper and lower arms, respectively.

According to (9), the enabled probabilities of each SM in the upper and lower arms are:

$$\begin{cases} p_{au}(t) = n_{au}(t)/2n = (1 - m\sin(\omega_N t))/2 \\ p_{al}(t) = n_{al}(t)/2n = (1 + m\sin(\omega_N t))/2 \end{cases} \quad (10)$$

For each SM, the current path has only two paths. The current may flow through the upper switch T_1 or D_1, which means that the SM belongs to the enabled SM. It may also flow through the lower switch T_2 or D_2, which means that the SM belongs to the bypassed SM.

By neglecting the power losses in the MMC and using energy conservation between the ac and dc sides of the MMC, the following is obtained:

$$U_{dc}I_{dc}/3 = I_m E_m \cos\varphi/2 \quad (11)$$

Using (5) and (8), k can be rewritten as:

$$k = 2/m\cos\varphi \quad (12)$$

Equation (12) shows that k is infinite when the MMC only exchanges reactive power.

V.   AVERAGE VALUE AND RMS VALUE OF THE SWITCHES CURRENT

In (8), the modulation index m is a lot greater than zero and less than 1. From (12), k should be greater than 2. Thus, the arm voltage is unipolar, and the arm current is bipolar, which shows that i_{au} has two zero points in one fundamental period. The two points are:

$$\begin{cases} \omega_N t_1 = -\arcsin(k^{-1}) - \varphi \\ \omega_N t_2 = \pi + \arcsin(k^{-1}) - \varphi \end{cases} \quad (13)$$

When the MMC operates the inverter mode, i_{au} and the two zero points are shown in Fig. 4.

From Fig. 4, it can be seen that the forward current time is $\pi + 2\arcsin(k^{-1})$ for D_1 and T_2, and that the reverse current time is $\pi - 2\arcsin(k^{-1})$ for T_1 and D_2 under the inverter operation in a fundamental period. Due to the dc current component in the arm, the conduction times of the switches of the SMs are different, which is neglected in [8].

According to the enabled probability and conduction time, the average and RMS currents can be determined. Here, the schematic diagram of the switch conduction is taken as an example under the inverter operation of the MMC. The arm current i_{au} and switching characteristics of T_1, D_1, T_2, and D_2 are shown in Fig. 5, during a fundamental period T.

In Fig. 5, from the instant t_1 to t_2, i_{au} is a positive current, which flows through D_1 during Δt_1, Δt_3 and Δt_5, or through T_2
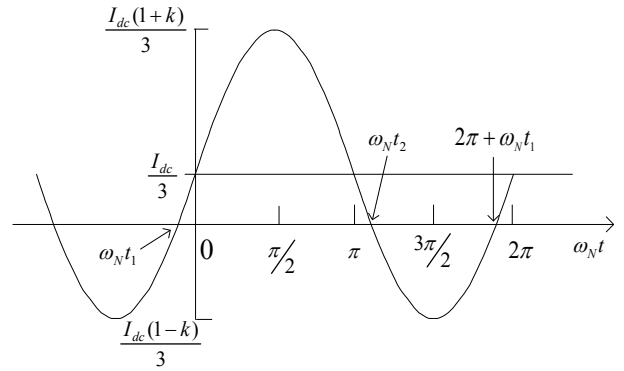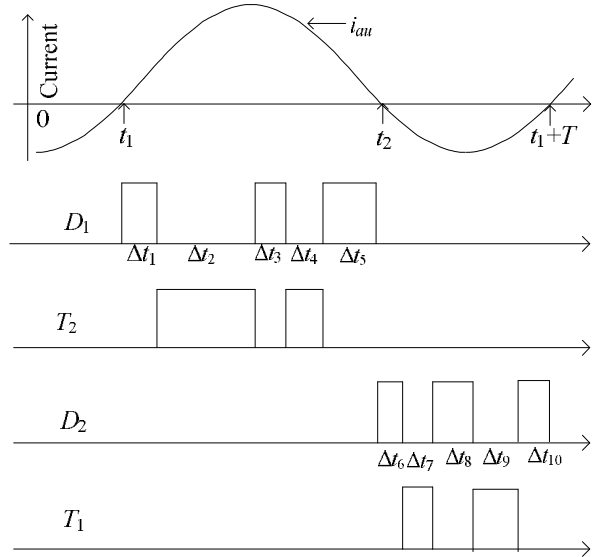

Fig. 4 Schematic diagram of arm current.

Fig. 5. Schematic diagrams of switch conduction of T_1, D_1, T_2, D_2.

during Δt_2 and Δt_4. For D_1 and T_2, the total conduction times of the corresponding conduction sequences are the sum of Δt_1, Δt_3 and Δt_5, and the sum of Δt_2 and Δt_4, respectively. The conduction time can be expressed as:

$$t_{D1} = (t_2 - t_1)(1 - m\sin(\omega_N t))/2 \quad (14a)$$

$$t_{T2} = (t_2 - t_1)(1 + m\sin(\omega_N t))/2 \quad (14b)$$

where t_{D1} and t_{T2} are respectively the total conduction times of D_1 and T_2.

From the instant t_2 to t_1+T, i_{arm} is a negative current, which flows through T_1 during Δt_7 and Δt_9, or through D_2 during Δt_6, Δt_8 and Δt_{10}. With the same method, the total conduction times of T_1 and D_2 are:

$$t_{T1} = (T + t_1 - t_2)(1 - m\sin(\omega_N t))/2 \quad (15a)$$

$$t_{D2} = (T + t_1 - t_2)(1 + m\sin(\omega_N t))/2 \quad (15b)$$

The procedures for the corresponding total conduction time of the switches in lower arm are the same as the above procedures and can be neglected here.

According to the conduction times of the switches and the characteristics under the non-conduction state (the current of the switch is 0), the average and RMS currents in the SM

upper switches (T_1 and D_1) and lower switches (T_2 and D_2), referring to the solid arrow shown in Fig. 1, are computed as follows:

According to Fig. 5 and (15), the average current of T_1 is:

$$I_{T1\_avg} = \frac{1}{2\pi}\left[\int_{\omega(t_2+\Delta t_6)}^{\omega(t_2+\Delta t_6+\Delta t_7)} i_{au} d\omega t + \int_{\omega(t_2+\Delta t_6+\Delta t_7+\Delta t_8)}^{\omega(t_2+\Delta t_6+\Delta t_7+\Delta t_8+\Delta t_9)} i_{au} d\omega t\right]$$

$$= \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} \frac{I_{dc}}{6}(1-m\sin\omega t)(1+k\sin(\omega t+\varphi))d\omega t \quad (16)$$

$$= -\frac{I_{dc}}{6\pi}(k-1/k)\cos(\arcsin k^{-1})$$

According to Fig. 5 and (15), the RMS current of T_1 is:

$$I_{T1\_rms}^2$$

$$= \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} \frac{1}{2}(1-m\sin\omega t)\frac{I_{dc}^2}{9}(1+k\sin(\omega t+\varphi))^2 d\omega t \quad (17)$$

$$= \frac{I_{dc}^2}{36\pi}[(\frac{k^2}{2}-1)(\pi-2\arcsin k^{-1})-\frac{k}{3}\cos(3\arcsin k^{-1})]$$

According to Fig. 5 and (14), the average and RMS currents of D_1 are:

$$I_{D1\_avg} = \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2} \frac{I_{dc}}{6}(1-m\sin\omega t)(1+k\sin(\omega t+\varphi))d\omega t$$

$$= \frac{I_{dc}}{6\pi}(k-1/k)\cos(\arcsin k^{-1}) \quad (18)$$

$$I_{D1\_rms}^2$$

$$= \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2}\frac{1}{2}(1-m\sin\omega t)\frac{I_{dc}^2}{9}(1+k\sin(\omega t+\varphi))^2 d\omega t \quad (19)$$

$$= \frac{I_{dc}^2}{36\pi}[(\frac{k^2}{2}-1)(\pi+2\arcsin k^{-1})+\frac{k}{3}\cos(3\arcsin k^{-1})]$$

According to Fig. 5 and (14), the average and RMS currents of T_2 are:

$$I_{T2\_avg}$$

$$= \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2} \frac{I_{dc}}{6}(1+m\sin\omega t)(1+k\sin(\omega t+\varphi))d\omega t \quad (20)$$

$$= \frac{I_{dc}}{6\pi}[\pi+2\arcsin k^{-1}+(k+1/k)\cos(\arcsin k^{-1})]$$

$$I_{T2\_rms}^2$$

$$= \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2}\frac{1}{2}(1+m\sin\omega t)\frac{I_{dc}^2}{9}(1+k\sin(\omega t+\varphi))^2 d\omega t$$

$$= \frac{I_{dc}^2}{36\pi}[(\frac{k^2}{2}+3)(\pi+2\arcsin k^{-1})+6k\cos(\arcsin k^{-1}) \quad (21)$$

$$-\frac{k}{3}\cos(3\arcsin k^{-1})]$$

According to Fig. 5 and (15), the average and RMS currents of D_2 are:

$$I_{D2\_avg}$$

$$= \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} \frac{I_{dc}}{6}(1+m\sin\omega t)(1+k\sin(\omega t+\varphi))d\omega t \quad (22)$$

$$= \frac{I_{dc}}{6\pi}[\pi-2\arcsin k^{-1}-(k+1/k)\cos(\arcsin k^{-1})]$$

$$I_{D2\_rms}^2$$

$$= \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1}\frac{1}{2}(1+m\sin\omega t)\frac{I_{dc}^2}{9}(1+k\sin(\omega t+\varphi))^2 d\omega t$$

$$= \frac{I_{dc}^2}{36\pi}[(\frac{k^2}{2}+3)(\pi-2\arcsin k^{-1})-6k\cos(\arcsin k^{-1}) \quad (23)$$

$$+\frac{k}{3}\cos(3\arcsin k^{-1})]$$

From (16) and (18), it can be seen that the sum of the average current of T_1 and D_1 is zero, which shows that the capacitor voltage of the SMs can maintain its balance.

When the MMC operates in the rectifier mode, the calculation of the average and RMS currents flowing through the switches is similar to the calculation under the inverter operation. According to the current reference direction under the inverter and rectifier operation, the following current relationships can be found: the average and RMS currents of T_1, D_1, T_2 and D_2 under the inverter operation are the same as the average and RMS currents of D_1, T_1, D_2 and T_2 under the rectifier operation of the MMC.

VI.   MMC IN VSC-HVDC SYSTEMS

A. IGBT and FWD Conduction Losses

The average conduction losses P_{con} of an IGBT or a diode are approximated as:

$$P_{con\_x} = |I_{x\_avg}| \cdot U_{0\_x} + r_{0\_x} \cdot (I_{x\_rms})^2 \quad (24)$$

where P_{con_x} represents the average conduction losses of device x; U_{0_x} presents the bias voltage of device x; r_{0_x} indicates the dynamical resistance of device x; and I_{x_avg} and I_{x_rms} are the average and RMS currents flowing through device x, respectively.

B. IGBT and FWD Switching Losses

Switching losses consist of essential switching losses and additional switching losses. The essential switching losses are generated due to the enabled probabilities of each SM. The additional switching losses are generated to maintain voltage balancing with additional switching actions. The additional switching frequency is hard to determine analytically. The upper limit of the total switching frequency f_p (including the necessary switching frequency and the additional switching frequency) is 3 times the fundamental frequency f_N [11], [14].

Brückner and Bernet [15] have found that the turn-on losses E_{on} and turn-off losses E_{off} of the IGBT have an almost linear relation with the average current. The recovery losses E_{rec} of the diodes are less than the switching losses of the IGBT. The IGBT switching losses P_{sw} and the FWD recovery losses P_{rec} can be approximated as:

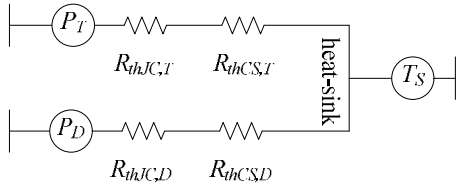$$P_{sw} = (E_{on} + E_{off})\frac{U_c \cdot |I_{T\_avg}| f_p}{U_{ref\_T} \cdot I_{ref\_T}} \quad (25a)$$

Fig. 6. Thermal model of the IGBT-pair module with heat-sink.

$$P_{rec} = E_{rec} \frac{U_c \cdot |I_{D\_avg}| f_p}{U_{ref\_D} \cdot I_{ref\_D}} \qquad (25b)$$

where E_{on}, E_{off}, and E_{rec} can obtained from the corresponding device manufacturer; U_{ref_x} and I_{ref_x} are the reference voltage and current of the IGBT or FWD when the turn-on and turn-off losses or recovery losses are measured, respectively.

The turn-on losses of the FWD are rather small, and may be not considered [15]. Using (24) and (25), the total losses of the IGBT and FWD are roughly the sum of the conduction losses and switching losses

$$P_T = P_{sw} + P_{con\_T} \qquad P_D = P_{rec} + P_{con\_D} \qquad (26)$$

where P_{con_T} is conduction loss of the IGBT, and P_{con_D} is conduction loss of the FWD.

C. Equivalent Thermal Circuit Model

In order to calculate the average junction temperature of one IGBT-diode pair with a heat-sink, the equivalent thermal model is shown in Fig. 6 [16]. The thermal capacitances are not included here.

In Fig. 6, $R_{thJC,X}$ and $R_{thCS,X}$ are the thermal resistances of the junction-to-case and case-to-heat-sink for device X, respectively, and T_S is the temperature of the heat-sink.

The thermal resistance of the junction-to-case (IGBT and FWD) can be taken from the datasheet. By neglecting the coupling between the IGBT and FWD, the values of R_{thCS_x} are usually stated separately for the IGBT and FWD. They can be obtained from newer datasheets.

The junction temperatures of the IGBT and FWD can be obtained by:

$$T_{j,T} = P_T \times (R_{thJC,T} + R_{thCH,T}) + T_S \qquad (27a)$$

$$T_{j,D} = P_D \times (R_{thJC,D} + R_{thCH,D}) + T_S \qquad (27b)$$

D. IGBT and FWD Losses Calculation with a Heat Sink

In order to calculate the losses of the temperature-dependent switches, the conduction losses were determined in an iterative calculation procedure. The initial junction temperature $T_{0j,x}$ of device X is 125℃, which is the one case operating point provided by the device manufacturer. According to (26), the losses of device X can be obtained. It is assumed that the temperature of the heat sink is constant. Then, the junction temperature $T_{j,x}$ can be determined from (27). The junction temperature rise ΔT_x is
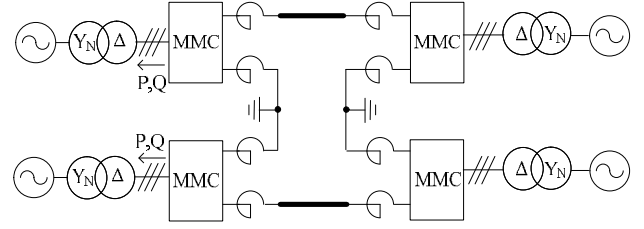

Fig. 7. Single-line diagram of the simulated system.

Specification	Parameter	Specification	Parameter
U_{dc}	320 kV	E_m	147 kV
I_{dc}	1562 A	I_m	2265 A
m	0.92	n	200
ω_N	314 rad/s	U_c	1600 V
L_s	52 mH	L_r	26 mH
IGBT module		ABB HiPak 5SNA 1500E330305	
V_{CES}		3300 V	
$I_{C\,nom}$		1500 A	

$T_{j,x}$ minus $T_{0j,x}$. Thus, the dynamical resistance r'_{0_x} is changed as:

$$r'_{0\_x} = r_{0\_x}(273 + T_{0j,x} + \Delta Tx)/(273 + T_{0j,x}) \qquad (28)$$

The iterations are repeated until ΔT_x within -0.1 ℃~0.1 ℃.

VII. LOSS ESTIMATION OF AN MMC

A. Specifications of an MMC

To verify the derived analytical formulas for the estimation of the junction temperature in the MMC IGBTs, a bipolar MMC-HVDC system with 1000 MW/±320 kV is established with the simulation tool PSCAD/EMTDC as shown in Fig. 7. When compared with the symmetrical monopolar HVDC system proposed in [17], the operational reliability of the bipolar MMC-HVDC system can improved.

For the effectiveness of the simulation, each arm was made up of 200 SMs. Each converter station was connected to a 180 kV ac system. The main circuit parameters of the simulated system are listed in Table I. An ABB HiPak IGBT module 5SNA 1500E330305 was applied to the switches of the SMs in this paper. Its related turn-on losses, turn-off losses and recovery losses are listed in the data sheets in [18], [19]. Based on these specifications, the conduction and switching losses of the MMC can be estimated. This IGBT module has a 3300 V collector–emitter voltage V_{CES} and a 1500 A dc collector current $I_{C\,nom}$.

B. IGBT Module Specifications

To calculate the losses of the IGBT model in the MMC, the semiconductor specifications from the manufacturer can be used to evaluate related losses. These losses consist of the

TABLE II
IGBT MODULE SPECIFICATIONS FOR 5SNA 1500E330305 (Tvj
=125 ℃)

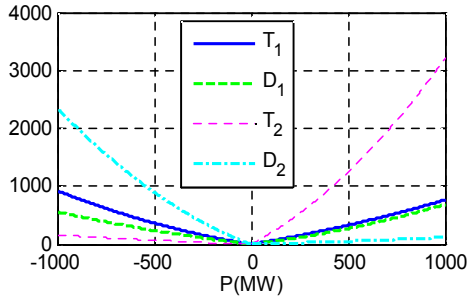| Parameter	U_{T0}(V)	r_0(mΩ)	E_{on}(mJ)	E_{off}(mJ)	E_{rec}(mJ)
T	3.1	2	2150	2800	
D	2.25	1.5			1900
$R_{thJC,T}$	0.0085K/W		$R_{thJC,D}$	0.017K/W	
$R_{thCS,T}$	0.009K/W		$R_{thCS,D}$	0.018K/W	

Fig. 8. Conduction losses of IGBT and FWD parts changing with the transmission power of MMC under $\cos(\varphi)$=1.
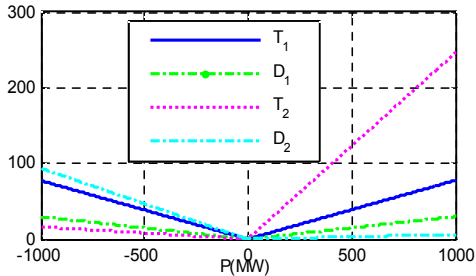

Fig. 9. Switching losses of IGBT and FWD changing with the transmission power of MMC under $\cos(\varphi)$=1.

conduction and switching losses. The specifications of the ABB IGBT module (5SNA 1500E330305) can be obtained from references [17], [18]. These specifications include the bias voltage, the dynamical resistance, the switching or recovery losses, and the thermal resistances shown as in Table II.

Note: test conditions of the switching loss or recovery losses are collector-emitter voltage V_{cc}=1800 V, DC collector current I_c=1500 A and DC forward current I_F=1500 A, and junction temperature T_{vj}=125 ℃.

*C. Losses and Junction Temperature with the Analytic Method*

According to (28)-(30) and Table I, the conduction and switching losses of the IGBT and FWD in the upper arm of phase *a* are shown in Figs. 8 and 9, respectively, with the transmission power of the MMC under $\cos(\varphi)$=1. From Figs. 7 and 8, it can be seen that the conduction losses of the switches are more than one order of magnitude of the corresponding switching losses with the MMC technology. It can also be seen that the total losses of T_2 and D_2 are larger than the total losses of T_1 and D_1 under the inverter and
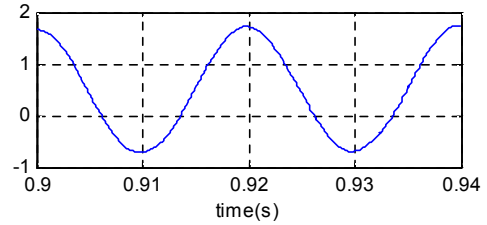
(a) Current waveform of the arm current.
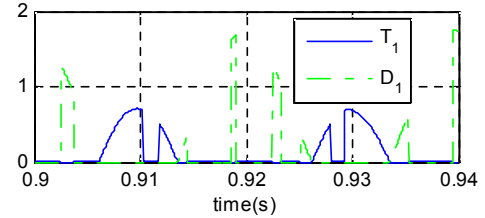
(b) Current waveform of T_1 and D_1.
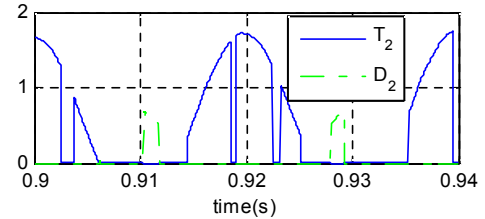
(c) Current waveform of T_2 and D_2.

Fig. 10. Simulation current waveforms of the arm, and T_1, D_1, T_2, D_2 when P=1000MW (inverter operation).

rectifier operation, respectively. Thus, the junction temperature of T_2 or D_2 should be taken care of first.

Figs. 8 and 9 show that the losses distribution of the four switches is rather unequal. When the MMC transmits its rated power, the simulation current waveforms of the arm and the switches (T_1, D_1, T_2, D_2), under the inverter and rectifier operation, are shown in Figs. 10 and 11, respectively. Due to the dc component of the arm current, the conduction current and time of T_2 reach their largest values under the inverter operation, and the conduction current and time of D_2 reach their largest values under the rectifier operation. The bias voltage, dynamical resistance of T_2, is larger than that of D_2 in Table II. This is the main reason that the total loss of the SM under the inverter operation is larger than that of the SM under the rectifier operation.

When the MMC under the rectifier or inverter operation transmits its rated power, the conduction losses and switching losses obtained from the analytical method are listed in Table III. It is assumed that the temperature of the heat-sink is about 65 ℃. Using these losses and the resistances for the junction-to-case and case-to-heat-sink of the IGBT or FWD, the respective junction temperatures are also listed in Table III.

From Table III, it can be seen that the junction temperature of T_1, D_1, T_2 and D_2 at the maximum transmission capacity under the rectifier and inverter operation, are 76.9 ℃, 79 ℃, 66 ℃, 150.3 ℃, and 75 ℃, 81.9 ℃, 123.4 ℃, 66℃

(a) Current waveform of the arm current.

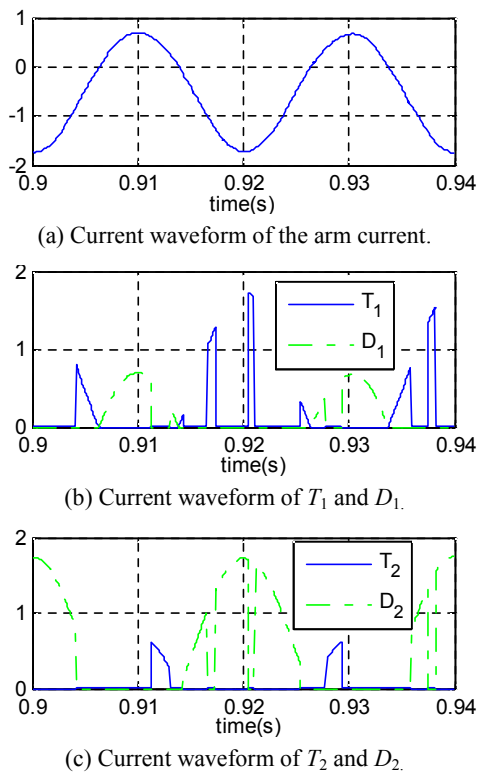(b) Current waveform of T_1 and D_1.

(c) Current waveform of T_2 and D_2.

Fig. 11. Simulation current waveforms of the arm, and T_1, D_1, T_2, D_2 when P=1000MW (rectifier operation).

TABLE III
LOSSES AND JUNCTION TEMPERATURE WITH ANALYTIC METHOD

	1000MW(Rec.)			1000MW(Inv.)		
	C. Losses	S. Losses	T. (℃)	C. Losses	S. Losses	T. (℃)
T_1	626.7	55.6	76.9	517.1	55.6	75
D_1	378.3	21.4	79	460.4	21.3	81.9
T_2	48.7	5.6	66	3100.3	234.8	123.4
D_2	2291.2	90.1	150.3	35.6	2.2	66.3
Total	3344.9	172.7		4113.4	313.9	

TABLE IV
LOSSES AND JUNCTION TEMPERATURE WITH PSCAD SIMULATION

	1000MW(Rec.)			1000MW(Inv.)		
	C. Losses	S. Losses	T. (℃)	C. Losses	S. Losses	T. (℃)
T_1	585.2	52	76.2	490	20.4	74.9
D_1	346.3	8.3	77.4	447.2	18.3	82.8
T_2	67.5	4.8	66.3	2939.9	206.3	120.6
D_2	2300.4	87.8	150.8	53.8	2	67.3
Total	3299.4	152.9		3930.9	246.9	

respectively. In addition, the junction temperatures of the switches are below the maximum junction temperature 150 ℃ under the inverter operation. This shows that the temperature of the heat-sink can be properly increased. However, under the rectifier operation, the junction temperature of D_2 is over 150 ℃. The heat-sink temperature of D_2 should be kept below 64.7℃.

D. Losses and Junction Temperature with the Simulation

To verify the analytical formulas for the evaluation losses of the SM, a simulation model of the MMC-HVDC is established in the PSCAD/EMTDC environment. Under the transmission rated power of the MMC, the conduction losses, switching losses and junction temperatures of T_1, D_1, T_2 and D_2 from the simulation results are listed in Table IV.

From Tables III and IV, it can be seen that the conduction losses of the switches, except T_2 under the rectifier operation and D_2 under the inverter operation, are relatively close. The main reasons for the deviation of the conduction losses are (1) neglecting the reactive power consumption of the arm inductor; (2) neglecting the harmonic components of the current in the arm. It is interesting that for different switches with the larger conduction losses, the deviation is smaller. The relative errors $\varepsilon = (P_{calculation} / P_{simulation} - 1) \times 100\%$ of T_2 under the rectifier operation and D_2 under the inverter operation are below 5%. Since $3f_N$ is taken as the switching frequency, which is its upper limit, the switching losses obtained from the analytical method are correspondingly larger than ones obtained from simulation. In comparison, the evaluation losses and junction temperature by the analytical formulas are simpler and faster than by the PSCAD simulation, which requires a simulation model and consumes time.

From Tables III and IV, it can also be seen that the junction temperatures of D_2 under the rectifier operation are over 150 ℃. This shows that the heat-sink temperature of the rectifier station should be lower than that of the inverter station.

VIII. CONCLUSION

Using the voltage of the upper and lower arms, the enabled probabilities of each of the SMs in the upper and lower arms have been proposed. According to the enabled probabilities, the average and RMS currents of the switches of the SMs can be obtained from the analytical method. Thus, the conduction and switching losses can be calculated or estimated. According to the thermal model of an IGBT-diode pair with a heat-sink, the junction temperatures of the switches can be determined. Based on a 1000 MW ±320 kV MMC–HVDC system, the simulated results show that the analytical method is effective enough to estimate the reliability of a cool system.

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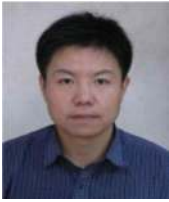
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