Power Magnetics @ High Frequency

State-of-the-Art and Future Prospects

Other Conference Item

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State-of-the-Art and Future Prospects

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Magnetics
Committee

"Transforming Magnetics 'Black Magic' into Engineering"

A Workshop prior to APEC 2017
Sponsored by the PSMA Magnetics Committee

And

IEEE Power Electronics Society (PELS)

Saturday, March 25th, 2017
7:00 am –6:00 pm

Sessions

- **AC Power Loss Measurements**
- **Technology Demonstration**
- **Technical Issues**
- **AC Power Loss Modeling**

Outline

- ► Impact of Magnetics on Conv. Performance
- ► *Losses Due to Stresses in Ferrite Surfaces*
- ► *The Ideal Switch is NOT Enough!*
- ► *Challenges in MV/MF Power Conversion*
- ► *Future Prospects*

E. Hoene / FH IZM
St. Hoffmann / FH IZM
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Th. Guillod
J. Miniböck
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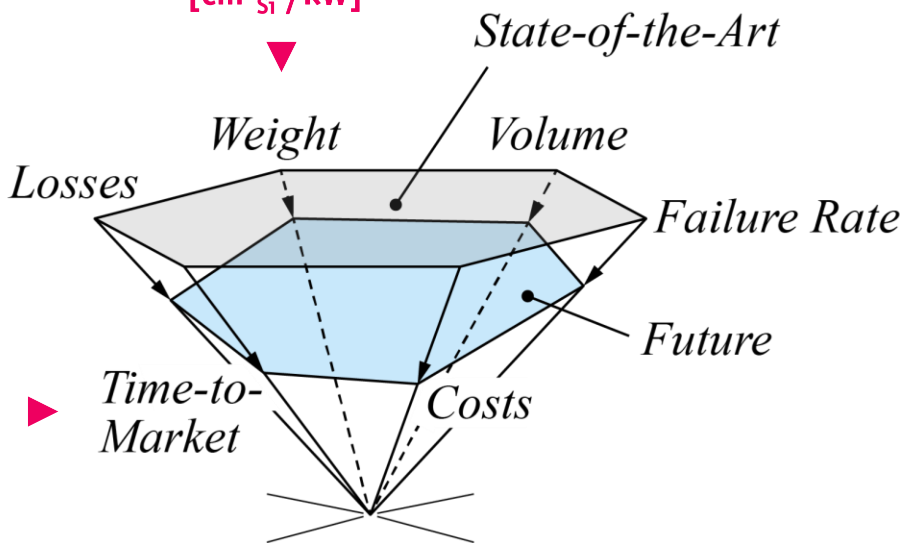
Introduction

Converter Performance Indicators
Design Space / Performance Space

Power Electronics Converter Performance Indicators

Environmental Impact...
[kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]



- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]

▶ Performance Limits (1)

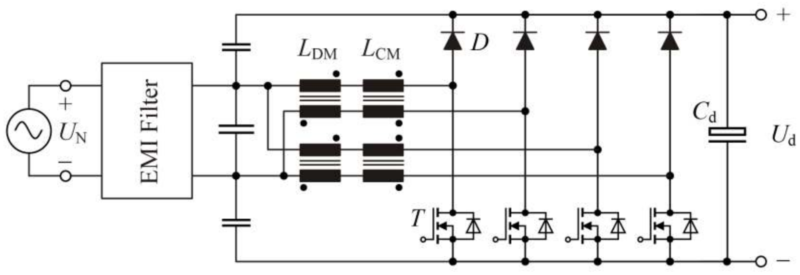
- **Example of Highly-Compact 1-Φ PFC Rectifier**
- **Two Interleaved 1.6kW Systems**

CoolMOS
SiC Diodes

$P_O = 3.2\text{kW}$
$U_N = 230\text{V}\pm10\%$
$U_O = 400\text{V}$

$f_P = 450\text{kHz} \pm 50\text{kHz}$

★ $\eta = 95.8\%$ @ $\rho = 5.5\ \text{kW/dm}^3$



→ High Power Density @ Low Efficiency
→ *Trade-Off Between Power Density and Efficiency*

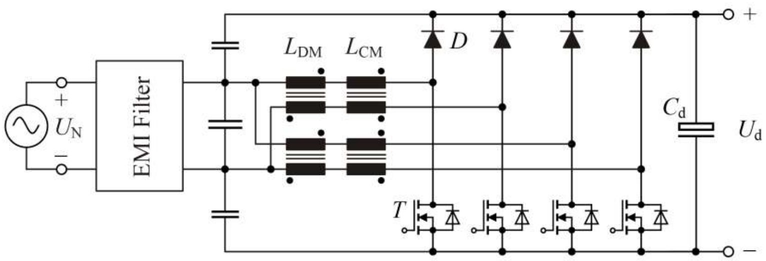
▶ Performance Limits (2)

- **Example of Highly-Efficient 1-Φ PFC Rectifier**
- **Two Interleaved 1.6kW Systems**

$P_O = 3.2\text{kW}$
$U_N = 230\text{V}\pm10\%$
$U_O = 365\text{V}$

$f_P = 33\text{kHz} \pm 3\text{kHz}$

★ $\eta = 99.2\%$ @ $\rho = 1.1\ \text{kW/dm}^3$

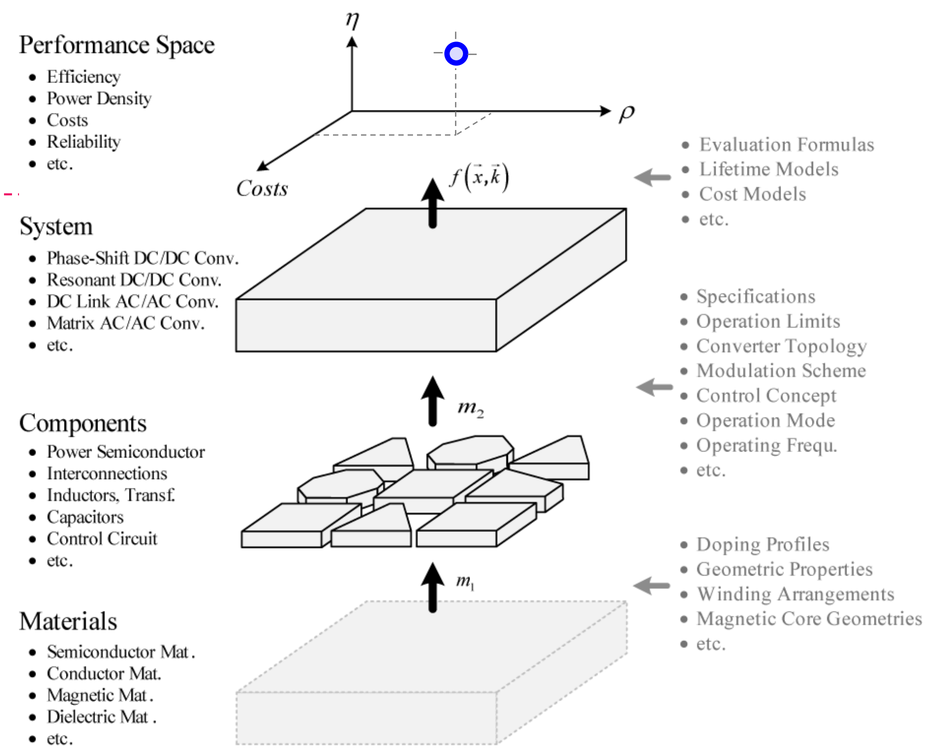


→ High Efficiency @ Low Power Density
→ *Trade-Off Between Power Density and Efficiency*

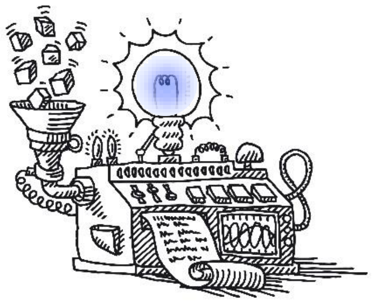
Abstraction of Power Converter Design

Performance Space

Design Space



→ *Mapping* of *"Design Space"* into *"Performance Space"*

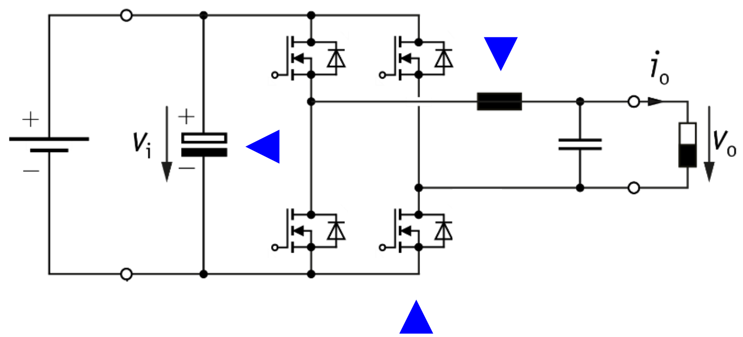


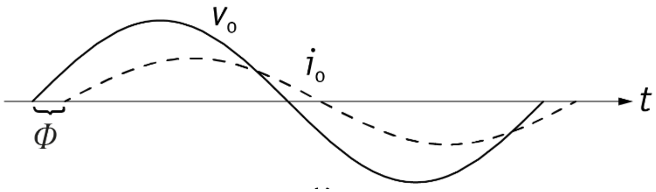
Derivation of η-ρ-Performance Limit of Converter Systems

Component η-ρ-Characteristics
Converter η-ρ-Pareto Front

Derivation of the η-ρ-Performance Limit

Example of DC/AC Converter System

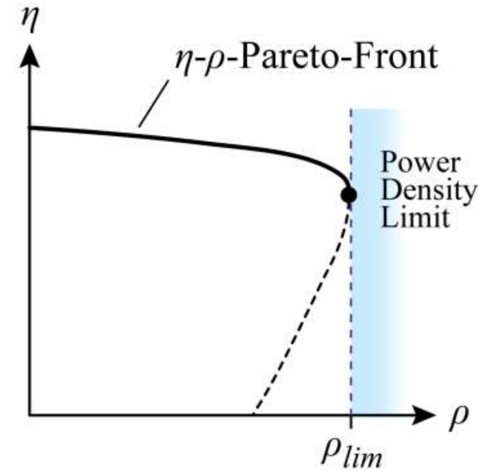




Key Components

- Storage Capacitor
- Semiconductors & Heatsink
- Output Inductor
- Auxiliary Supply

→ Construct η-ρ-Characteristics of Key Components
→ Determine Feasible *System* Performance Space



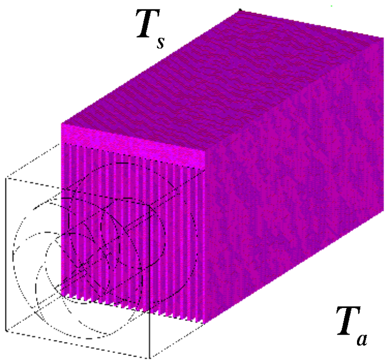
► η-ρ-Characteristic of Power Semiconductors / Heatsink

- Semiconductor Losses are Translating into Heat Sink Volume
- Heatsink Characterized by *Cooling System Performance Index* (*CSPI*)
- Volume of Semiconductors Neglected

$$P_H = (1-\eta_H)P_I = (1-\eta_H)\frac{P_O}{\eta_H}$$

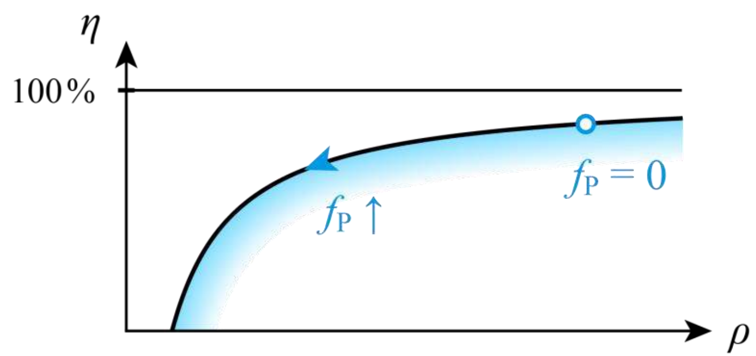
$$P_H = \frac{\Delta T_{s-a}}{R_{th}} = \Delta T_{s-a} G_{th} = \Delta T_{s-a} \underbrace{CSPI \cdot V_H}_{G_{th}}$$

$$CSPI = \frac{G_{th}}{V_H}\left[\frac{\text{W}}{\text{dm}^3\text{K}}\right]$$



$$\frac{(1-\eta_H)}{\eta_H} P_O = \overbrace{\Delta T_{s-a} CSPI}^{\alpha_H} \cdot V_H$$

$$\rho_H = \frac{P_O}{V_H} = \alpha_H \cdot \frac{\eta_H}{(1-\eta_H)}$$



→ Heatsink Defines a Converter Limit $\rho \leq \rho_H$

► *η-ρ*-Characteristic of *Storage+Heatsink+Auxiliary*

- **Overall Power Density Lower than Lowest Individual Power Density**
- **Total Efficiency Lower than Lowest Individual Efficiency**

$$V = V_C + V_H + V_{\text{aux}} \; \Big| \cdot \frac{1}{P_O} \qquad \rho_i = \frac{P_O}{V_i} \qquad P_I = P_O + \sum_i P_i = \frac{P_O}{\eta} \rightarrow \eta = \frac{1}{(1 + \frac{\sum_i P_i}{P_O})}$$

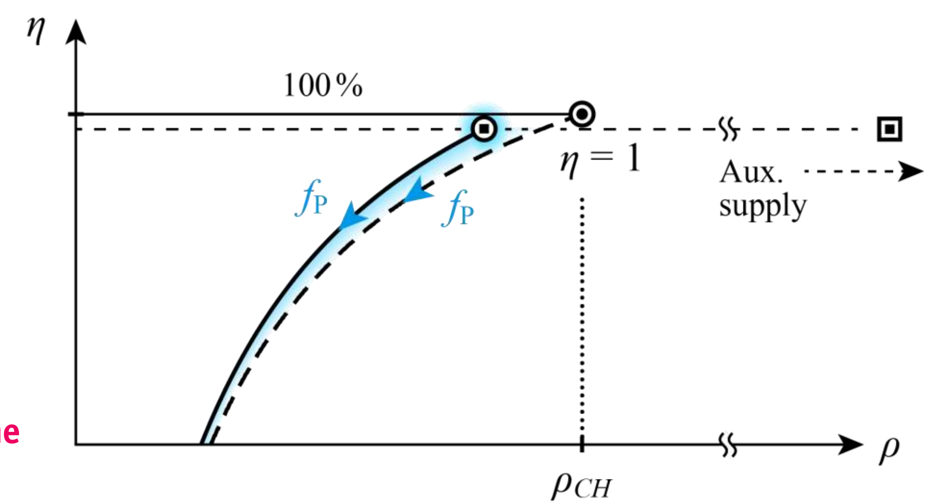
$$\rho^{-1} = \rho_C^{-1} + \rho_H^{-1} + \rho_{\text{aux}}^{-1}$$

– **Example of *Heat Sink+Storage* (No Losses)**

$$\rho_C = \beta_C \gamma_C$$

$$\rho_H = \underbrace{\Delta T_{s-a} CSPI}_{\alpha_H} \cdot \frac{\eta_H}{(1-\eta_H)}$$

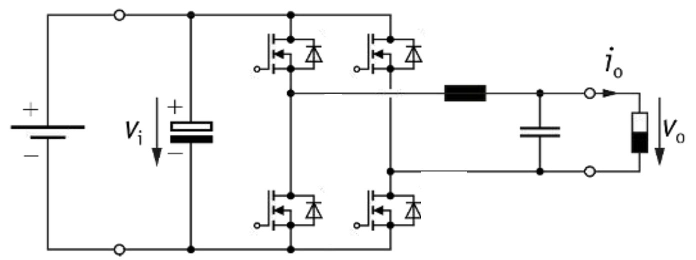
$$\rho_{CH} = \frac{\beta_C \gamma_C}{1 + \frac{(1-\eta_H)}{\eta_H} \beta_C \gamma_C \alpha_H^{-1}}$$

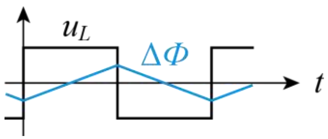


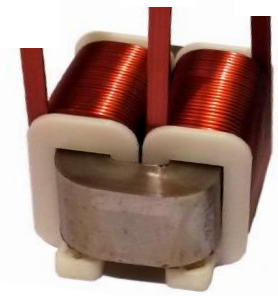
→ ***η-ρ*** **Characteristic w/o Magnetics**
→ **Higher Sw. Frequ. Leads to Larger Volume**

► *η-ρ*-Characteristic of Inductor (1)

■ **Inductor Flux Swing Defined by DC Voltage & Sw. Frequ. (& Mod. Index)**







■ **"-1"-Order Approx. of Volume-Dependency of Losses**

$$\Delta\hat{B} = \frac{U_{DC}\frac{1}{4}T_P}{NA_E} \propto \frac{U_{DC}}{f_P A_E} \propto \frac{1}{A_E} \propto \frac{1}{l^2} \rightarrow P_E \propto f_P^{\alpha}\Delta\hat{B}^{\beta}V_E \propto \approx (\frac{1}{l^4})l^3 \propto \frac{1}{l}$$

$$P_W = I_{rms}^2 R_W \propto \frac{l}{\kappa A_W} \propto \frac{l}{l^2} \propto \frac{1}{l}$$

■ **„0"-Order Approx. (N_{opt})**

$$P_L = k_{\Sigma}\, V_L^{\frac{4(2-\beta)}{3(2+\beta)}-\frac{1}{3}} f_P^{\frac{2(\alpha-\beta)}{2+\beta}} I_{rms}^{\frac{2\beta}{2+\beta}} U_{DC}^{\frac{2\beta}{2+\beta}} \Big|_{\substack{\alpha=1\\ \beta=2}} \rightarrow \propto \frac{U_{DC}I_{rms}}{\sqrt{f_P}\,V_L^{\frac{1}{3}}}$$

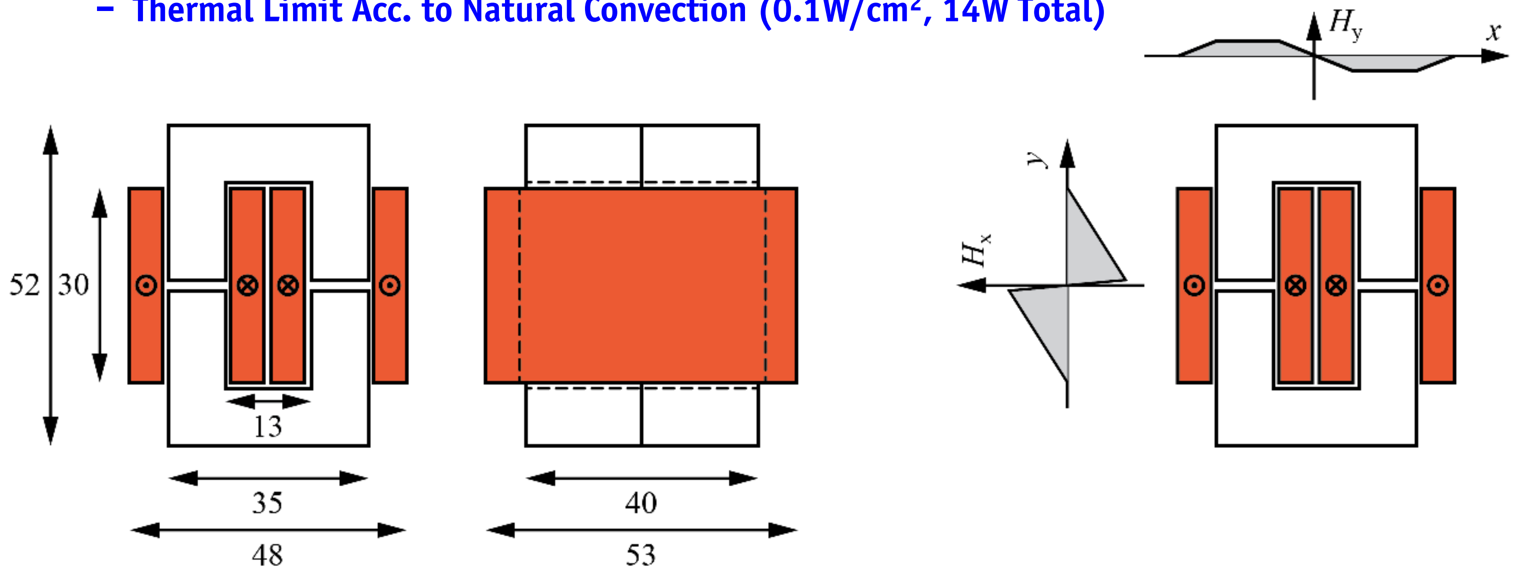
▲ $\propto l$

→ **Losses are Decreasing with Increasing Linear Dimensions & Sw. Frequency**

► η-ρ-Characteristic of Inductor (2)

■ Minimization of the Losses of an Inductor of a 3 kW Step-Down DC/DC Converter

- U_1= 400V / U_2 = 200V
- N87 Magnetic Cores
- 71um Litz Wire Strand Diameter (35% Fill Factor)
- Consideration of HF Winding and Core Losses
- Thermal Limit Acc. to Natural Convection (0.1W/cm², 14W Total)

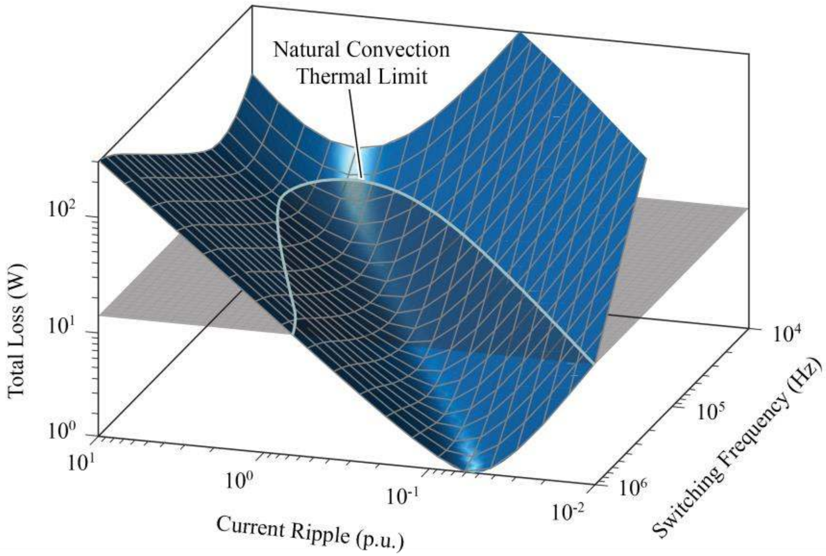


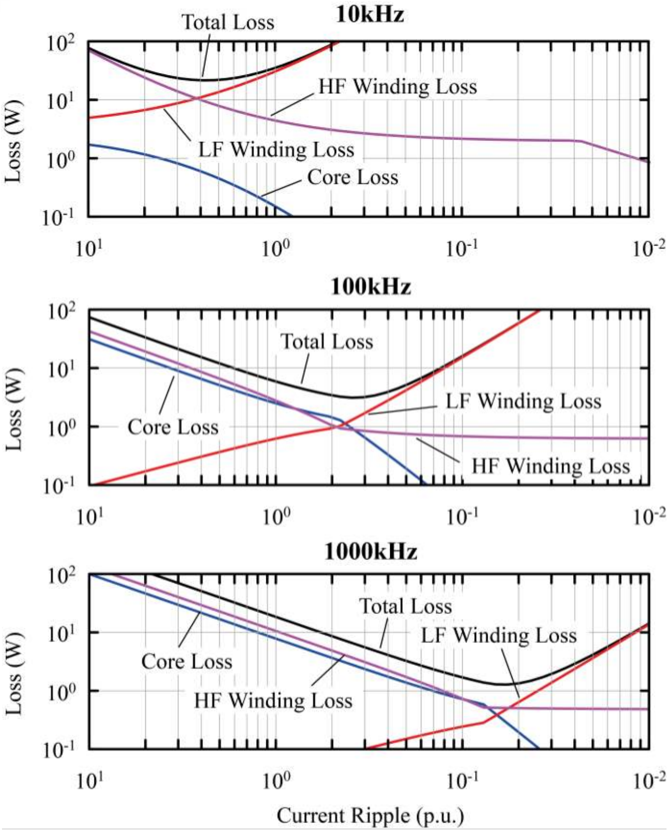
→ Calc. of Opt. # of Turns in Limits: $N \geq 1$, N_{min} Avoiding Sat. (incl. DC Curr.), N_{max} as for Air Core
→ HF Wdg. Losses: 2D Analy. Approx. / HF Core Losses: iGSE (DC Premagetization Not Consid.)

▶ η-ρ-Characteristic of Inductor (3)

- Loss Minimiz. by Calculation of Opt. # of Turns
- Consideration of HF Winding and Core Losses
- Thermal Limit Acc. To Natural Convection

- *Assumption:* Given Magnetic Core





→ Higher Sw. Frequ. – Lower Min. Ind. Losses – Overall Loss Red. Limited by Semicond. Sw. Losses

► η-ρ-Characteristic of Inductor (3)

- Overall Power Density Lower than Lowest Individual Power Density
- Total Efficiency Lower than Individual Efficiency

$$P_L \propto \frac{U_{DC} I_{rms}}{\sqrt{f_P} V_L^{\frac{1}{3}}} \propto \frac{P_O}{\sqrt{f_P}\, V_L^{\frac{1}{3}}} \quad (= k_{L,\max} V_L^{\frac{2}{3}})$$

$$P_L = (1-\eta_L) P_I = (1-\eta_L)\frac{P_O}{\eta_L}$$

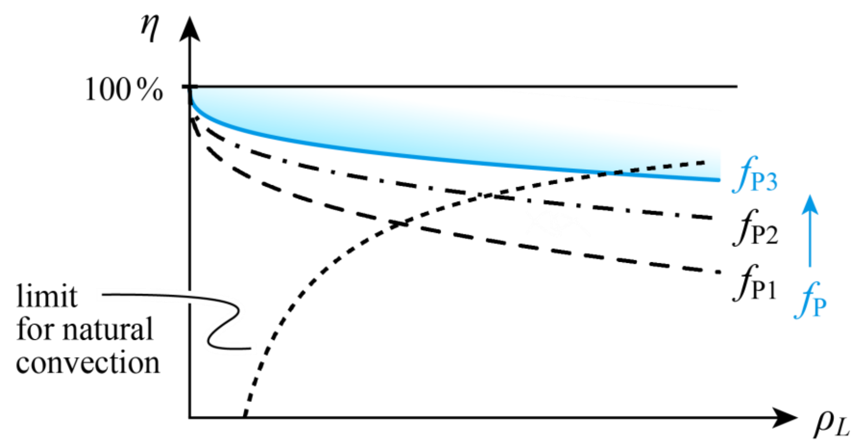
$$\rightarrow \frac{P_L}{P_O} = \frac{(1-\eta_L)}{\eta_L} \propto \frac{1}{\sqrt{f_P}\, V_L^{\frac{1}{3}}}$$

$$\rho_L = \frac{P_O}{V_L} \propto P_O f_P^{\frac{3}{2}} \frac{(1-\eta_L)^3}{\eta_L^3}$$

- Natural Convection

$$\rho_{L,\max} \propto \sqrt{f_P}$$

→ η-ρ Characteristic of Inductors
→ Higher Sw. Frequ. Leads to Lower Vol.
→ Allowed Losses Defined by Cooling

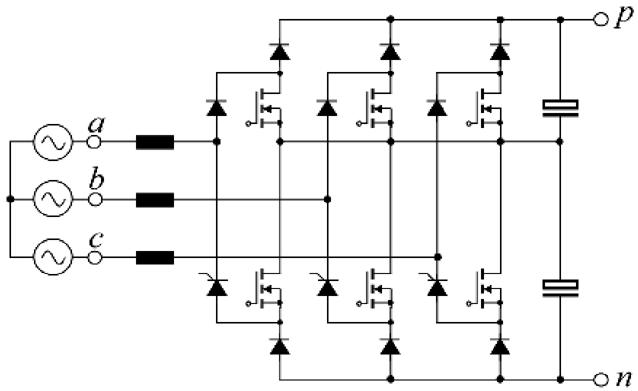


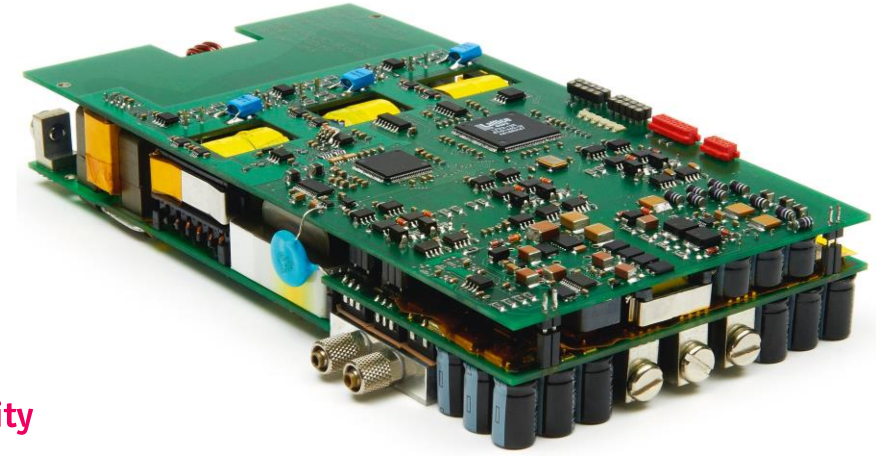
▶ Remark – Natural Conv. Thermal Limit (1)

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

P_O= 10 kW
U_N= 230V_{AC}±10%
f_N = 50Hz or 360…800Hz
U_O= 800V_{DC}

f_P= 250kHz





★ ρ =10 kW/dm³ @ η =96.2%

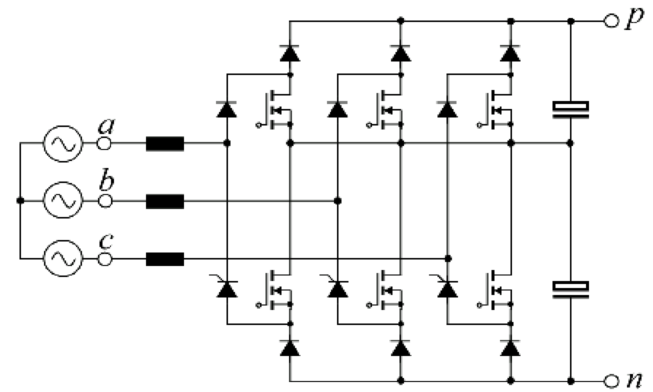
→ Systems with f_P= 72/250/500/1000kHz
→ Factor 10 in f_P – Factor 2 in Power Density

▶ Remark – Natural Conv. Thermal Limit (2)

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

P_O= 10 kW
U_N= 230V_{AC}±10%
f_N = 50Hz or 360…800Hz
U_O= 800V_{DC}

f_P= 250kHz



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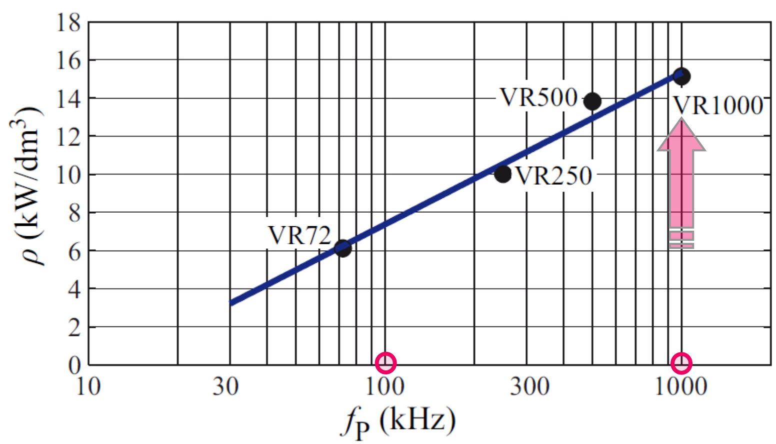


→ Systems with f_P= 72/250/500/1000kHz
→ Factor 10 in f_P – Factor 2 in Power Density

▶ η-ρ-Characteristic of Inductor (4)

- Natural Convection Heat Transfer Seriously Limits Allowed Inductor Losses
- Higher Power Density Through Explicit Inductor Heatsink

– Natural Convection

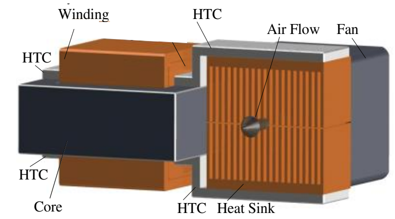
$$P_L = \frac{(1-\eta_L)}{\eta_L} P_O \leq k_{L,\max} V_L^{\frac{2}{3}} = k_{L,\max} \left(\frac{P_O}{\rho_L}\right)^{\frac{2}{3}}$$

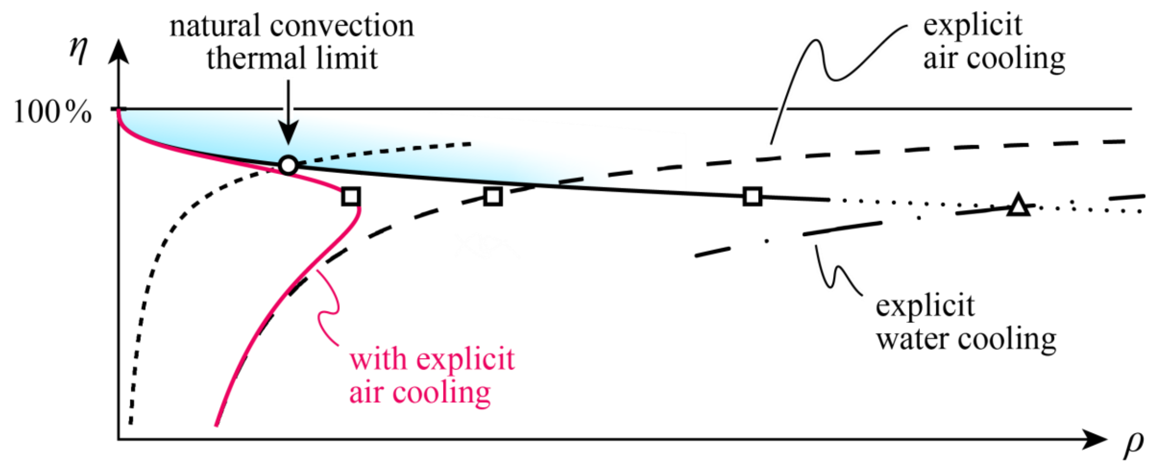
$$\rho_{L,\max} = k_{L,\max}^{\frac{3}{2}} \left(\frac{\eta_L}{1-\eta_L}\right)^{\frac{3}{2}} P_O^{-\frac{1}{2}}$$

$$\rho_{L,\max} \propto \sqrt{f_P}$$

– Explicit Heatsink

$$\rho_{LH,\max} \approx \frac{1}{2} \rho_{H,\max}(\eta_L)$$





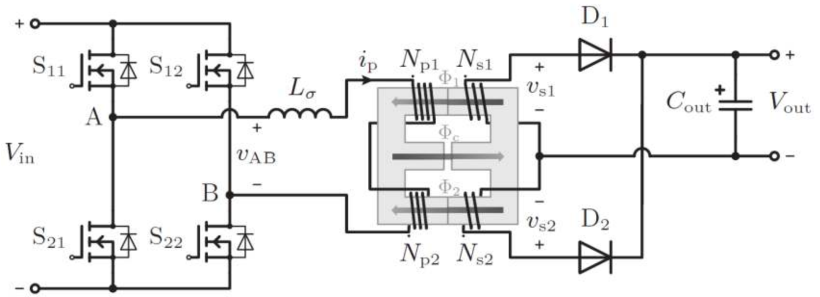
→ Heat Transfer Coefficients k_L and α_L Dependent on Max. Surface Temp. / Heatsink Temp.
→ Water Cooling Facilitates Extreme (Local) Power Densities

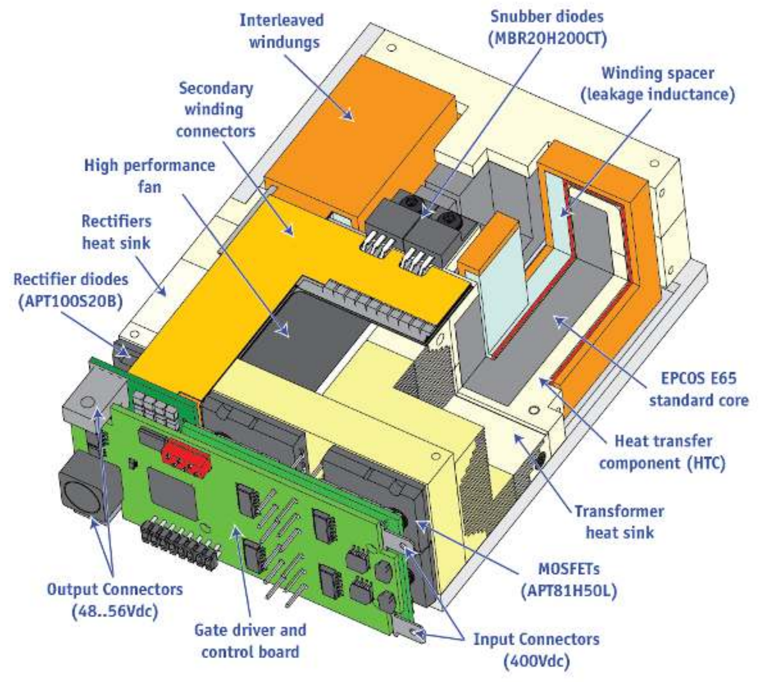
► Remark – Example for Explicit Heatsink for Magn. Component

- Phase-Shift Full-Bridge Isolated DC/DC Converter with Current-Doubler Rectifier
- Heat Transfer Component (HTC) & Heatsink for Transformer Cooling
- Magn. Integration of Current-Doubler Inductors

P_0 = 5kW
U_{in} = 400V
U_0 = 48...56V (300mV_{pp})
T_a = 45°C

f_P = 120kHz





★ 9 kW/dm³ (148W/in³) @ 94.5%

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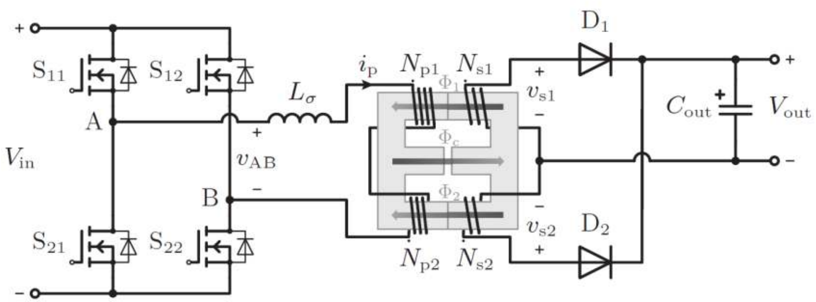
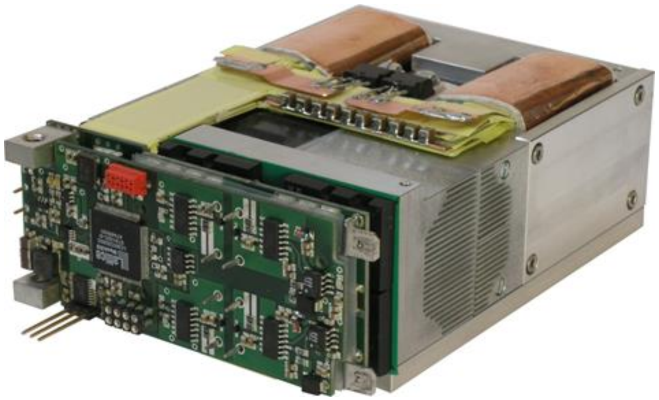




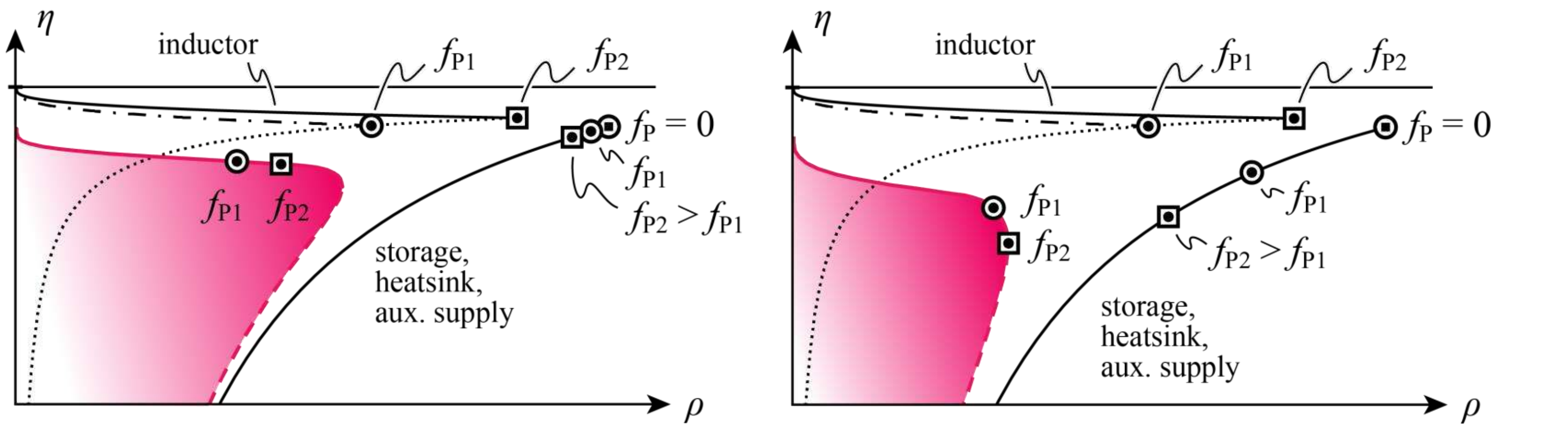
★ 9 kW/dm³ (148W/in³) @ 94.5%

▶ Overall Converter η-ρ-Characteristics

- Combination of Storage/Heatsink/Auxiliary & Inductor Characteristics
- Sw. Frequ. Indicates Related Loss and Power Density Values !

– *Low* Semiconductor Sw. Losses

– *High* Semiconductor Sw. Losses



→ Low Sw. Losses / High Sw. Frequ. / Small Heatsink / Small Ind. / High Total Power Density
→ High Sw. Losses / Low Sw. Frequ. / Large Heatsink / Large Ind. / Low Total Power Density

Reduction of Inductor Requirement

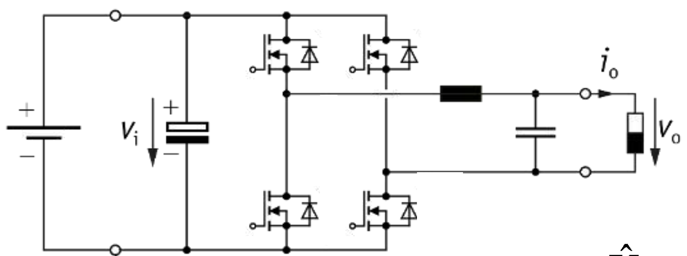
→ Parallel Interleaving
→ Series Interleaving

▶ Inductor Volt-Seconds / Size

- Inductor Volt-Seconds are Determining the Local Flux Density Ampl.
- Output Inductor has to be Considered Part of the EMI Filter

$$\Delta \hat{B} \propto \frac{T_P U_{DC}}{A_E} \propto \frac{U_{DC}}{f_P A_E}$$

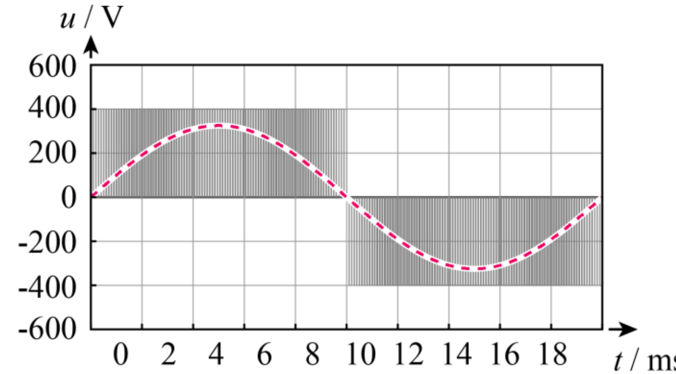
- Multi-Level Converters Allow to Decrease Volt-Seconds by Factor of N^2
- Calculation of Equivalent Noise Voltage @ Sw. Frequency (2nd Bridge Leg w. Fund. Frequ.)

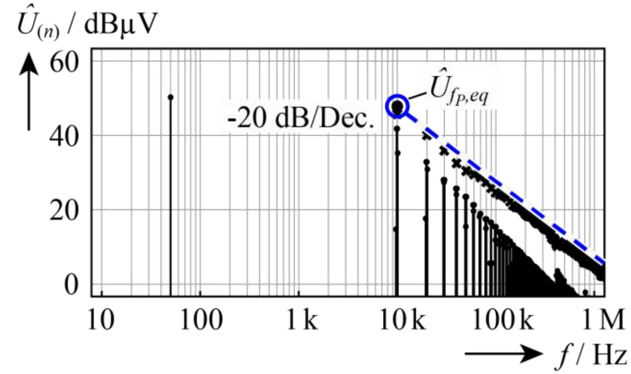


$$M = \frac{\hat{U}_O}{U_{DC}}$$

$$U^2_{f_P,eq,rms} = U^2_{AC,rms} - U^2_{O,rms}$$

$$U_{f_P,eq,rms} = \sqrt{M\left(\frac{2}{\pi} - \frac{M}{2}\right)}\, U_{DC}$$



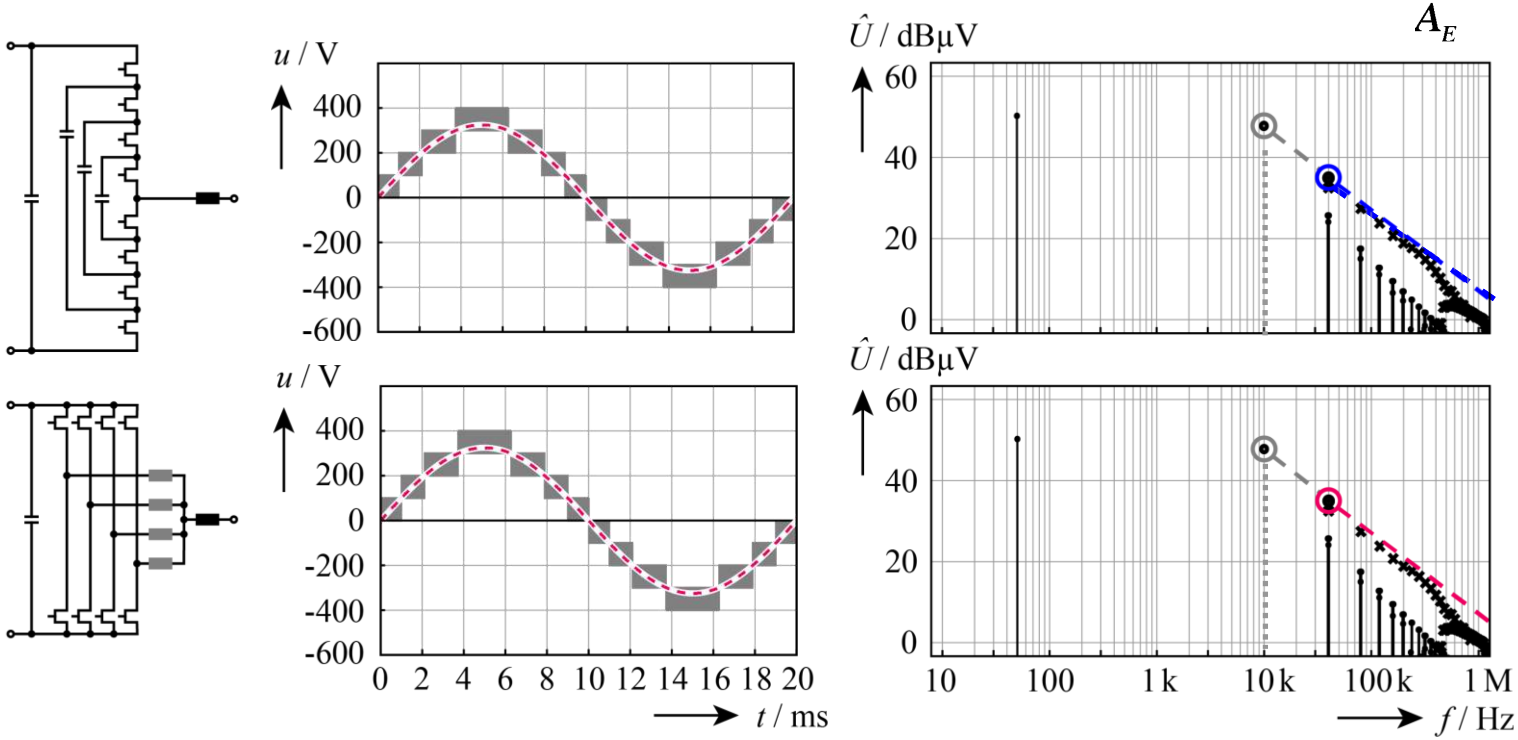


→ EMI Filter Design Can be Based on Equiv. Noise Voltage

▶ Reduction of Inductor Volt-Seconds / Size

- Multi-Level Characteristic through *Series-Interleaving*
- Multi-Level Characteristic through *Parallel Interleaving*

$$\Delta\hat{B} \propto \frac{\frac{T_P}{N}\,\frac{U_{DC}}{N}}{A_E}$$



→ Identical Spectral Properties for Both Concepts
→ Series Interleaving Avoids Coupling Inductor of Parallel Interleaving !

$$\Delta\hat{B} \propto \frac{\frac{T_P}{N}\,\frac{U_{DC}}{N}}{A_E}$$

▶ Multi-Level Converter Approach

- Multi-Level PWM Output Voltage – Minimizes Ind. Volume
- Flying Cap. Conv. – No Splitting of DC Inp. Voltage Required
- Low-Voltage GaN or Si Power Semiconductors

(19) Europäisches Patentamt / European Patent Office / Office européen des brevets

(11) EP 2 779 410 A2

(12) EUROPEAN PATENT APPLICATION

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Designated Extension States:
BA ME

(30) Priority: 14.03.2013 US 201313826556

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45240 Hod Hasharon (IL)

(72) Inventor: Yoscovitch, Ilan
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V.O.
Johan de Wittlaan 7
2517 JR Den Haag (NL)

(54) Multi-level inverter

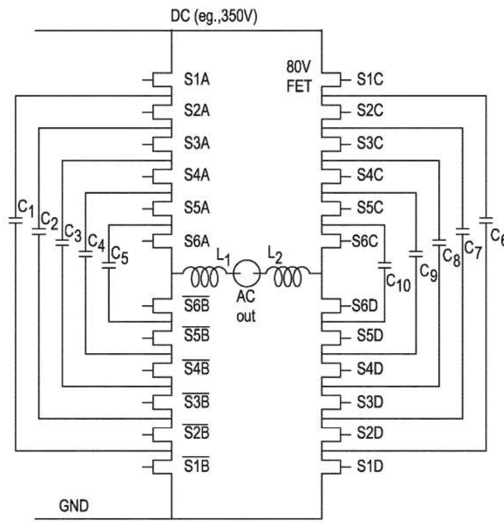


FIG. 1

Full-Bridge Topology or DC/|AC|Buck-Type + Unfolder

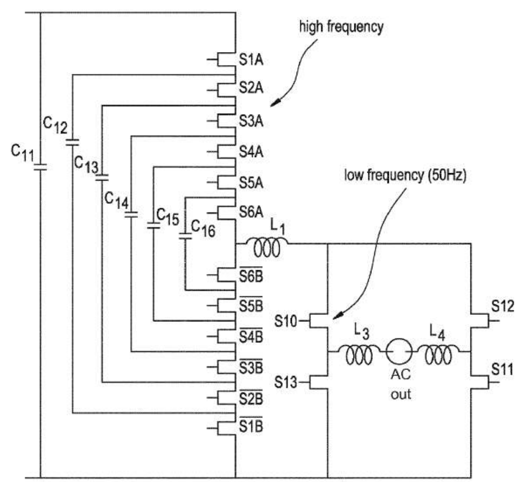


FIG. 4

→ Basic Patent on FCC Converter – Th. Meynard (1991) !

Transformers

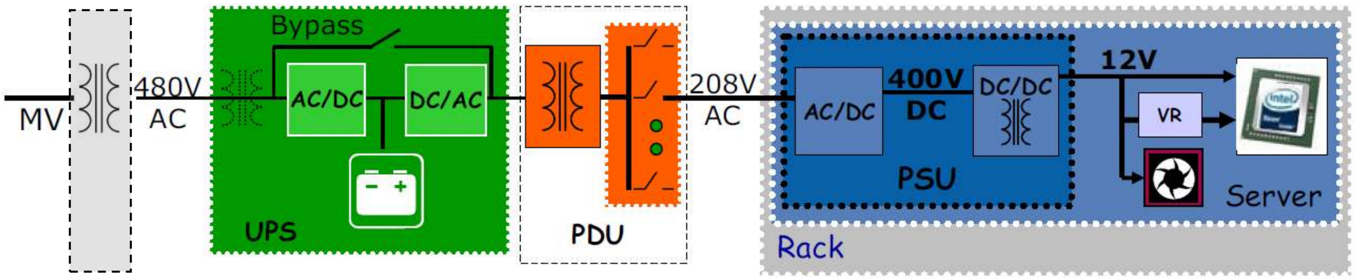
Optimal Operating Frequency
Example of MF/MV Transformer

▶ Future Direct MV Supply of 400V DC Distribution of Datacenters

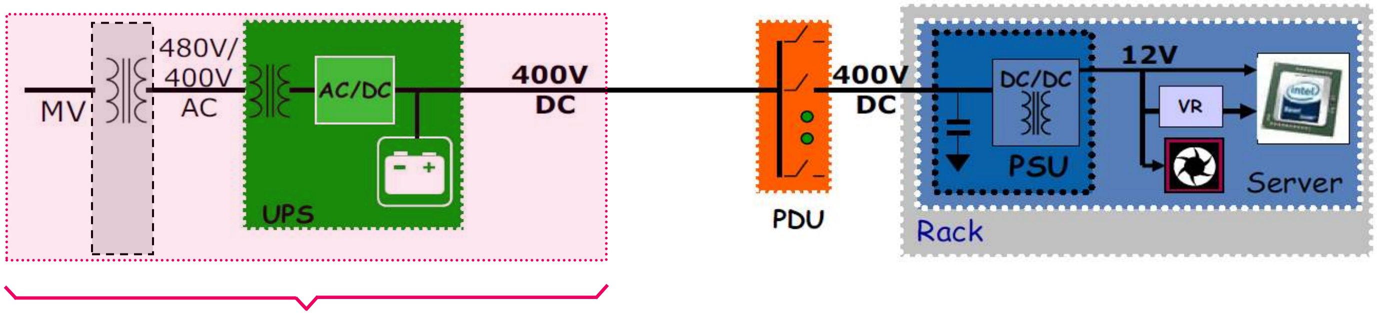
- Reduces Losses & Footprint / Improves Reliability & Power Quality
- Unidirectional Multi-Cell Solid-State Transformer (SST)
- AC/DC and DC/DC Stage per Cell, Cells in Input Series / Output Parallel Arrangement

— Conventional US $480V_{AC}$ Distribution

Source: intel 2007



— Facility-Level 400 V_{DC} Distribution

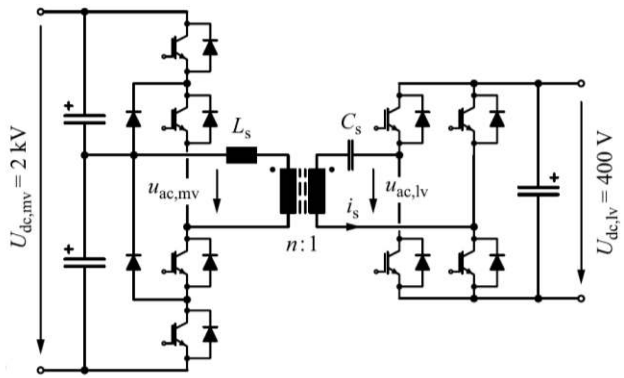


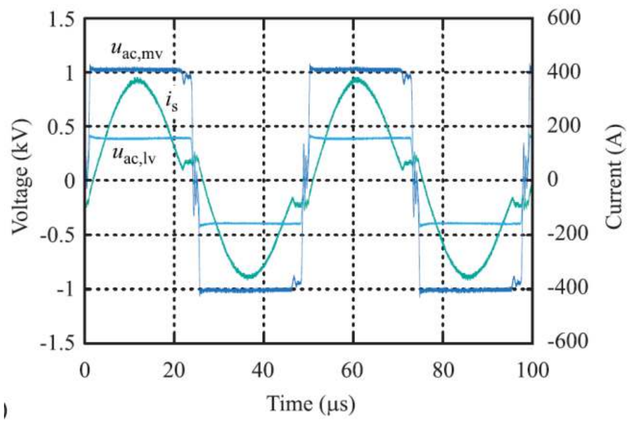
→ Unidirectional SST / Direct 6.6kV AC → 400V DC Conversion

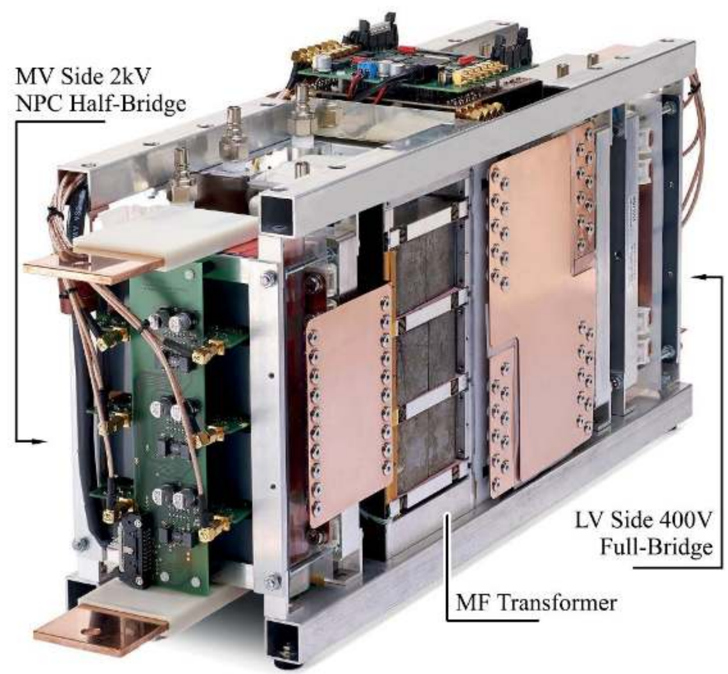
▶ Example of a 166kW/20kHz SST DC/DC Converter Cell

- Half-Cycle DCM Series Resonant DC-DC Converter

- Medium-Voltage Side 2kV
- Low-Voltage Side 400V

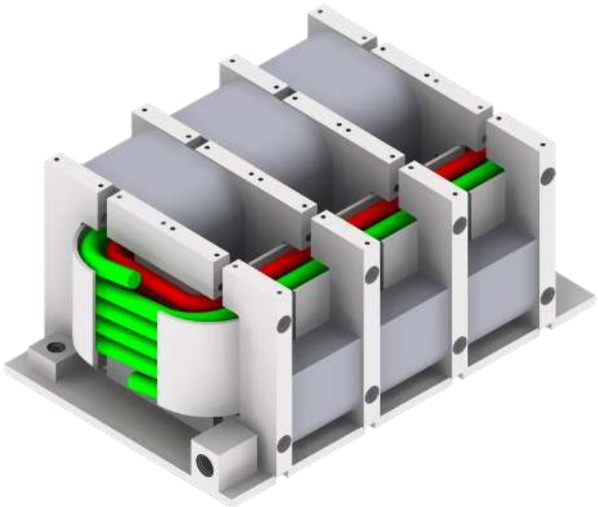


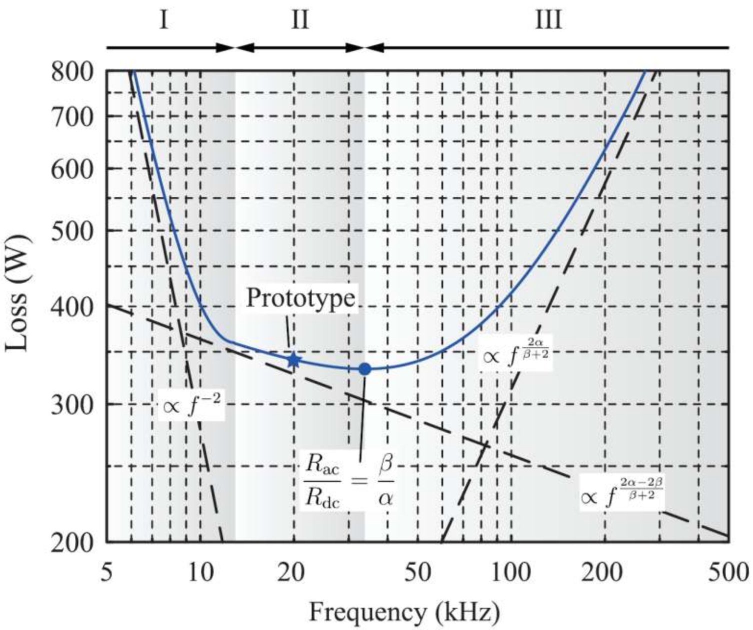




MF Transformer Design

- DoF – Electric (# of Turns & Op. Frequ.) / Geometric / Material (Core & Wdg) Parameters
- Cooling / Therm. Mod. of Key Importance / Anisotr. Behavior of Litz Wire / Mag. Tape
- 20kHz Operation Defined by IGBT Sw. Losses / Fixed Geometry





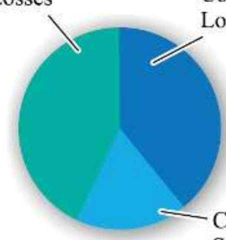
→ Region I: Sat. Limited / Min. Loss @ $P_C/P_W = 2/\beta$ ($R_{AC}/R_{DC} = \beta/\alpha$) / Region III: Prox. Loss Domin.
→ Heat Conducting Plates between Cores and on Wdg. Surface / Top/Bottom H_2O-Cooled Cold Plates

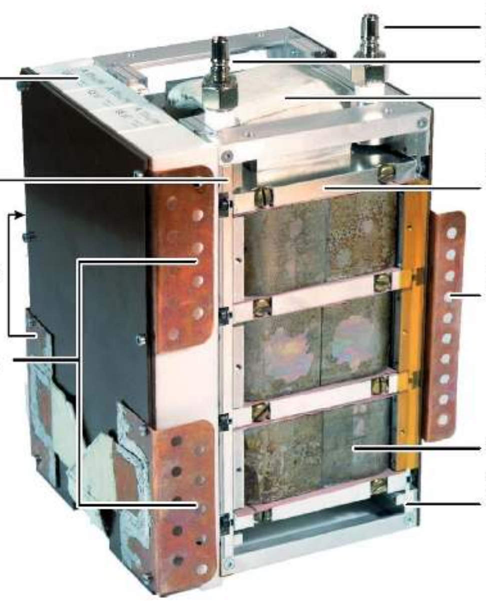
▶ MF Transformer Prototype

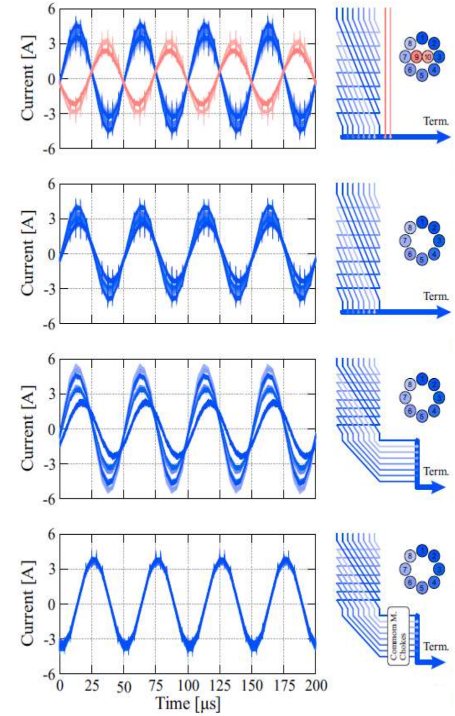
- **Power Rating** 166 kW
- **Efficiency** 99.5%
- **Power Density** 44 kW/dm^3

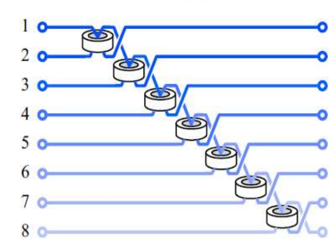
– **Nanocrystalline Cores with 0.1mm Airgaps between Parallel Cores for Equal Flux Partitioning**

– **Litz Wire (10 Bundles, 950 x 71µm Each) with CM Chokes for Equal Current Partitioning**









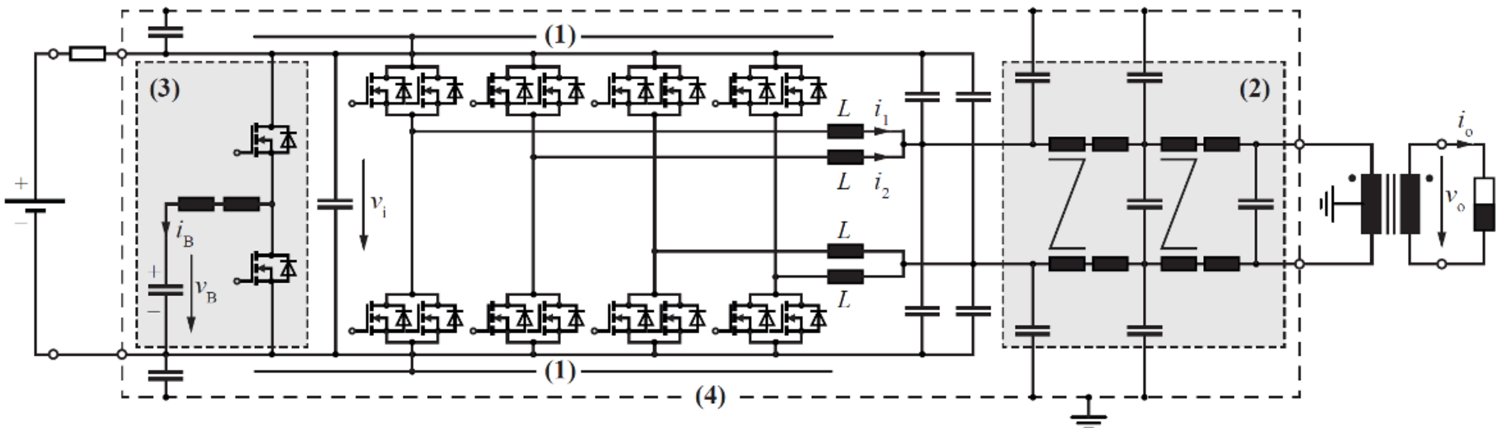
Calculation of Converter η-ρ-Performance Limits

Google Little Box Challenge
Ultra-Efficient 3-Φ PFC Rectifier

Selected Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

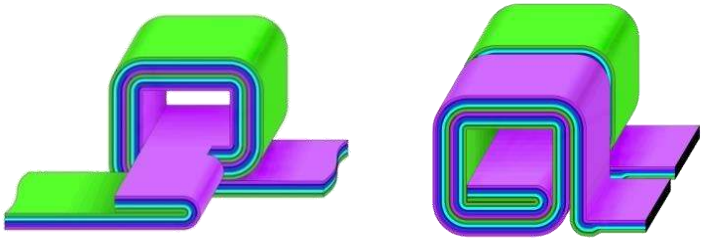
(1) Heat Sink
(2) EMI Filter
(3) Power Pulsation Buffer
(4) Enclosure



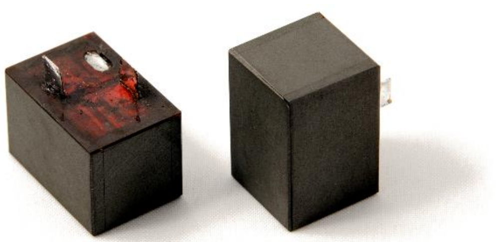
→ ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
→ Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

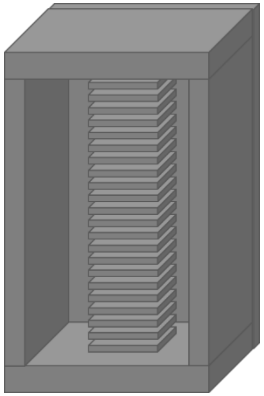
High Frequency Inductors (1)

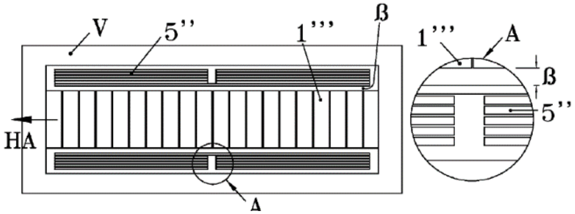
- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

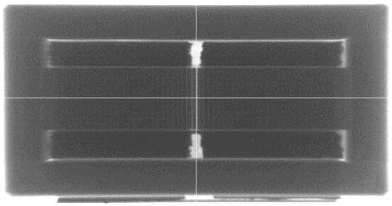


- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area







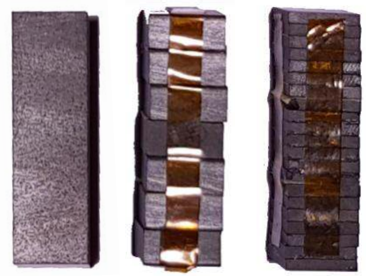


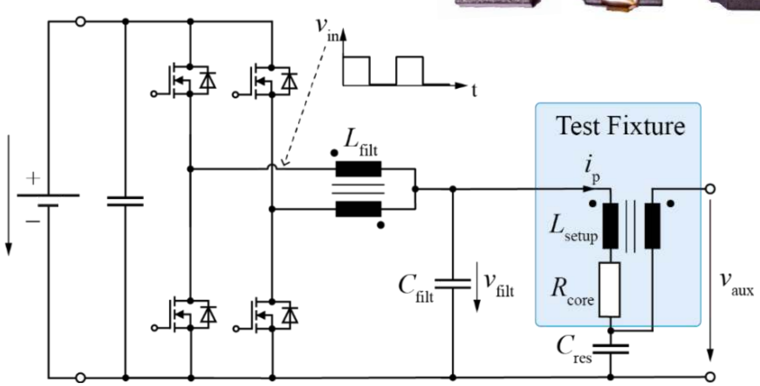
→ Dimensions - 14.5 x 14.5 x 22mm^3

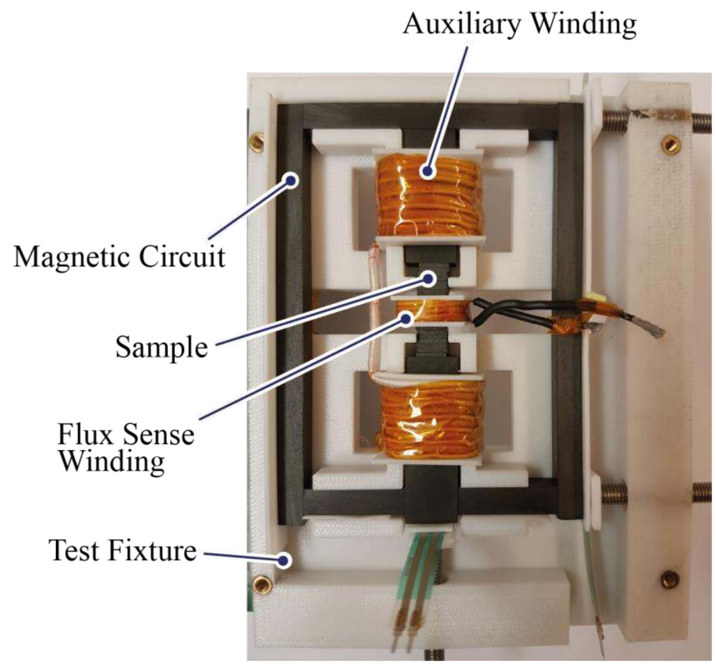
Multi-Airgap Inductor Core Loss Measurements (1)

- Investigated Materials - DMR51, N87, N59
- 30 µm PET Foil with Double Sided Adhesive Between the Plates
- Varying Number *N* of Air Gaps Assembled from Thin Ferrite Plates
- Number of Air Gaps:

Solid *N=6* *N=20*





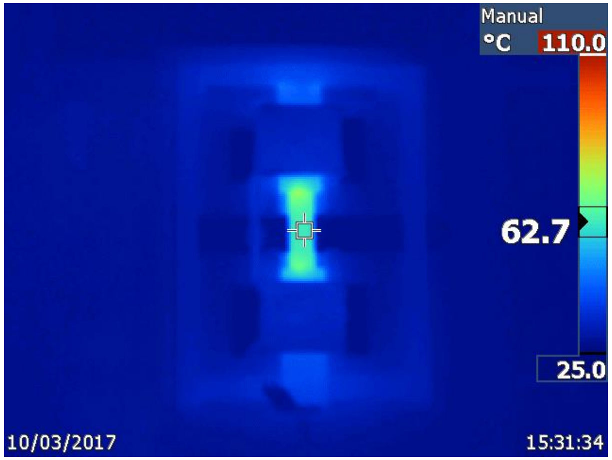


→ Sinusoidal Excitation with Frequencies in the Range of 250 kHz ...1MHz

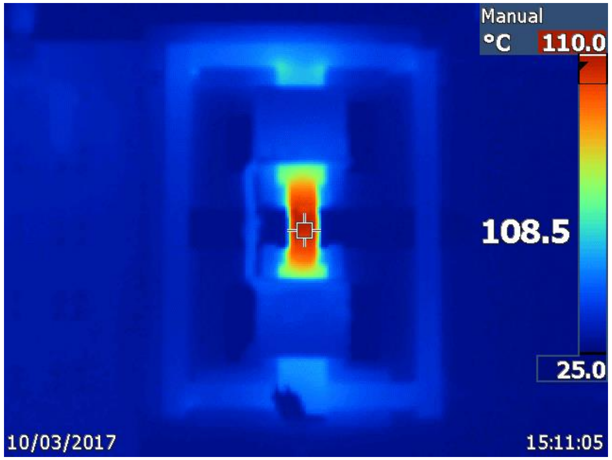
Multi-Airgap Inductor Core Loss Measurements (3)

- Losses in Sample – Increasing Temperature
- Excitation with 100 mT @ 750 kHz
- Start @ T=35°C
- Excitation Time = 90 s

Solid, ΔT =27.7°C

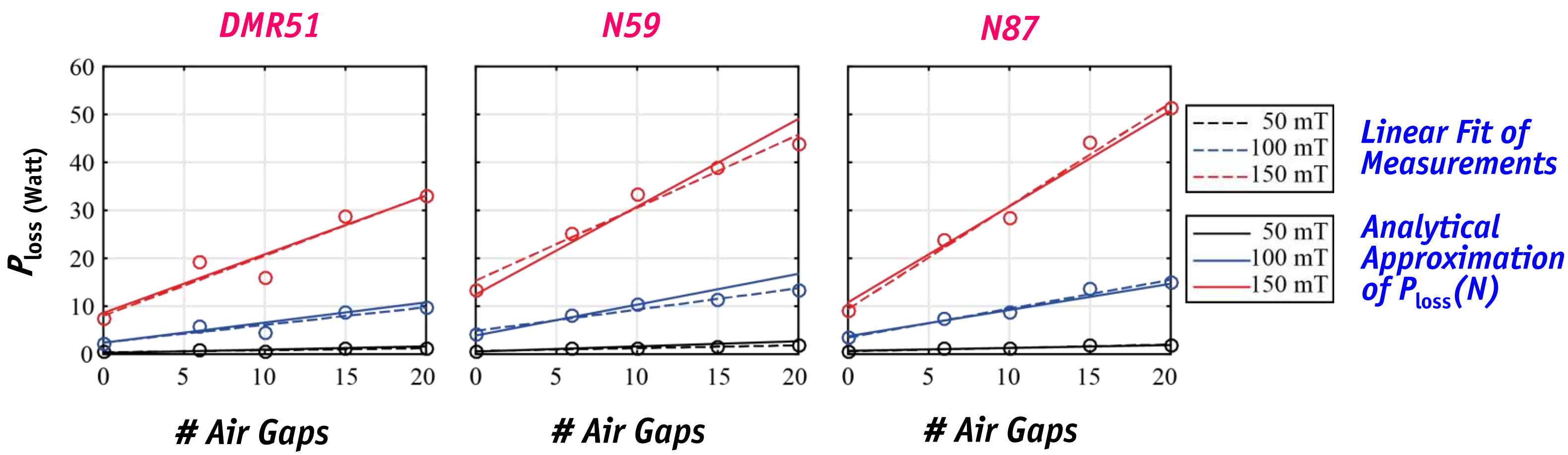


N=20, ΔT =73.5°C



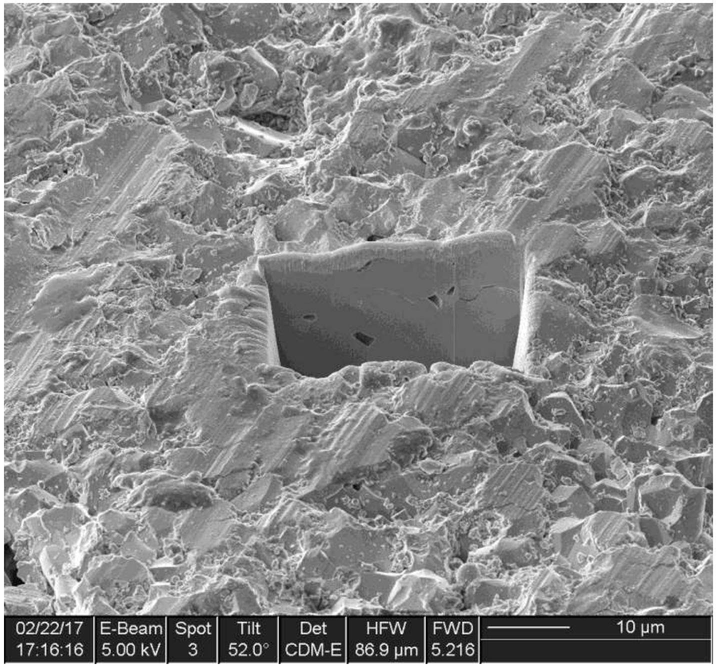
Multi-Airgap Inductor Core Loss Approximation (2)

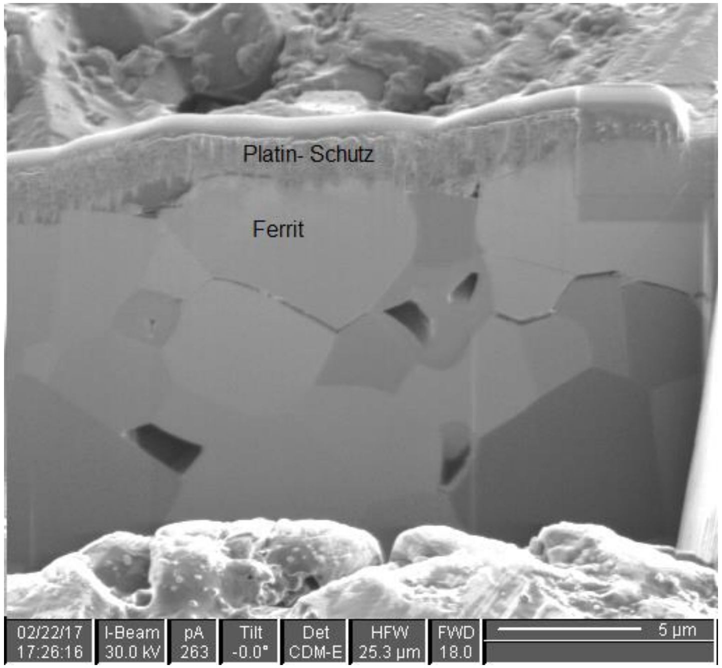
- **Total Core Loss in Sample with Varying Air Gaps and Test Fixture**
- **Excitation @ 500 kHz**



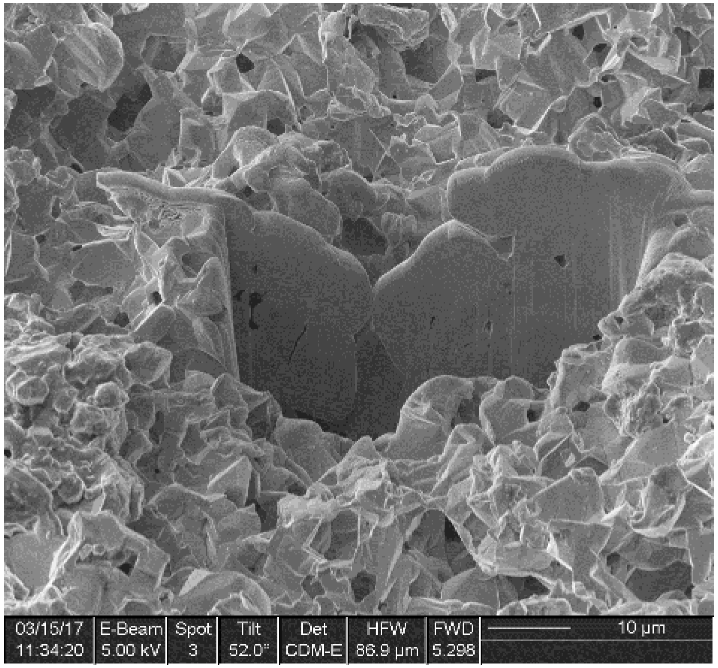
→ **Ext. of Steinmetz Eq.** $P_V = k_0 f^{\alpha} \hat{B}^{\beta} (V_C (\frac{A_S}{A_C})^{\beta} + V_S) + k_S f^{\alpha_S} \hat{B}^{\beta_S} \cdot N \cdot A_S$ **Sufficiently Accurate**

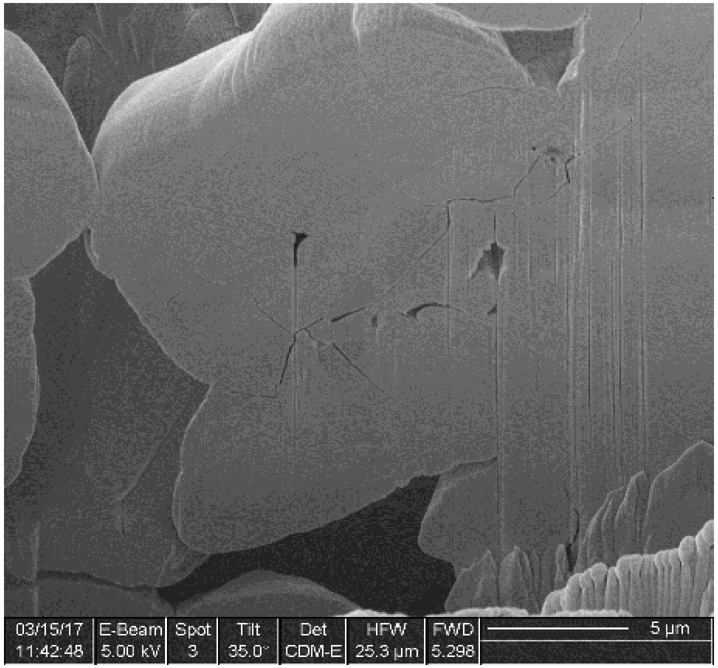
DMR 51 Untreated – FIB Preparation (1)





DMR 51 ETCHED – FIB Preparation (2)





Little-Box 1.0 Prototype

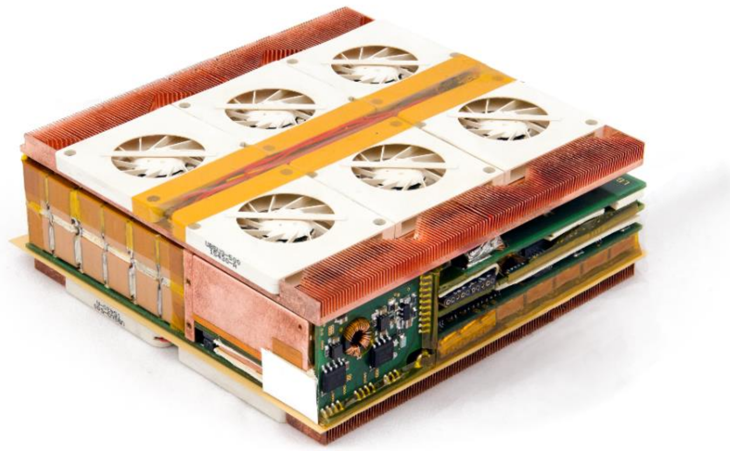
- **Performance**

– 8.2 kW/dm^3
– 96,3% Efficiency @ 2kW
– T_c=58°C @ 2kW

★ 135 W/in^3

- **Design Details**

– 600V IFX Normally-Off GaN GIT
– Antiparallel SiC Schottky Diodes
– Multi-Airgap Ind. w. Multi-Layer Foil Wdg
– Triangular Curr. Mode ZVS Operation
– CeraLink Power Pulsation Buffer



→ Analysis of Potential Performance Improvement for *"Ideal Switches"*

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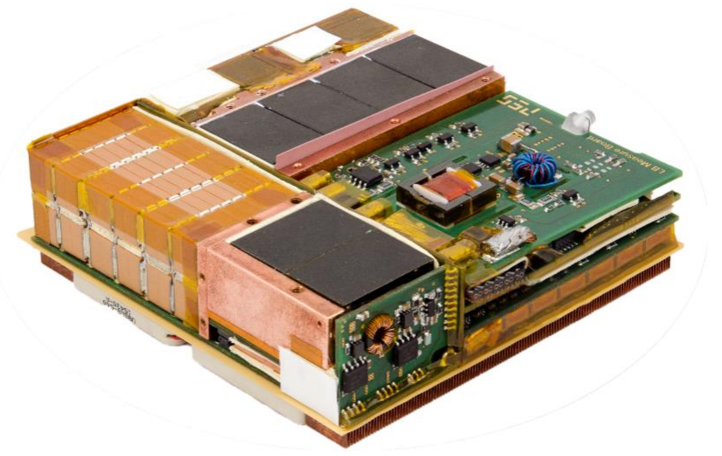
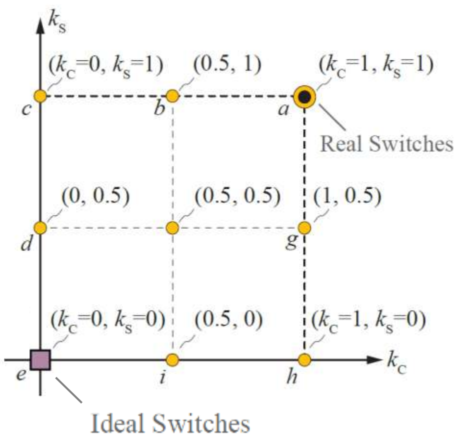
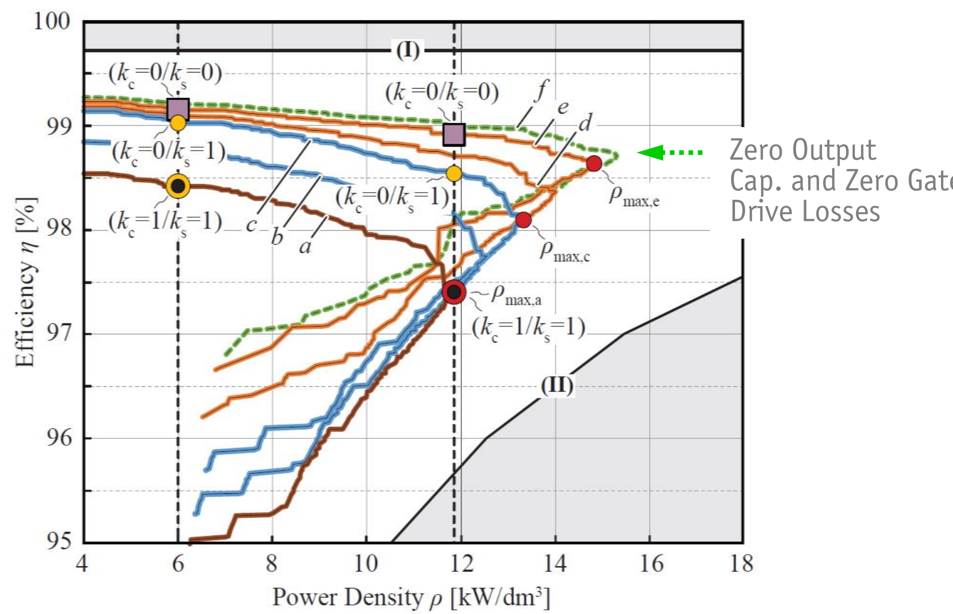


→ Analysis of Potential Performance Improvement for *"Ideal Switches"*

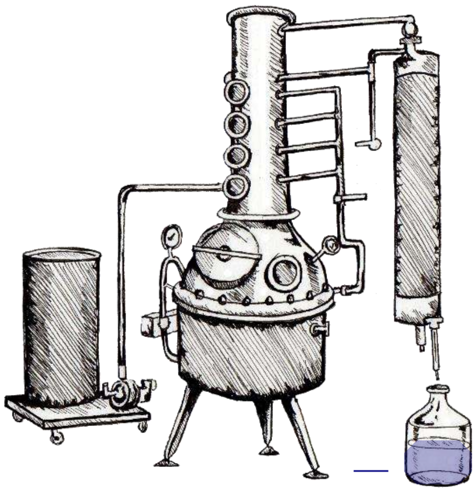
Little Box 1.0 @ Ideal Switches (TCM)

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_C = 0$ (Zero Cond. Losses); $k_S = 0$ (Zero Sw. Losses)





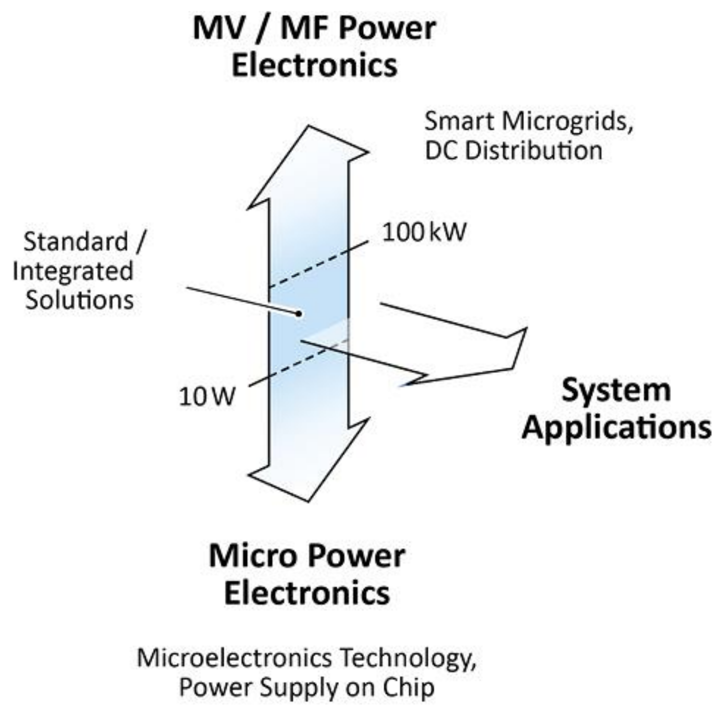
→ Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density
→ *The Ideal Switch is NOT Enough* (!)



Source: whiskeybehavior.info

Overall Summary

▶ Future Prospects of Power Electronics



→ **Future Extension of Power Electronics Application Area**

▶ Future Prospects of Magnetics

■ **Side Conditions**

- Magnetics are Basic Functional Elements (Filtering of Sw. Frequ. Power, Transformers)
- Non-Ideal Material Properties (Wdg. & Core) Result in Finite Magnetics Volume (Scaling Laws)
- Manufacturing Limits Performance (Strand & Tape Thickness etc.) @ Limited Costs

■ **Option #1: Improve Modeling / Optimize Design**

- Core Loss Modeling / Measurement Techniques (Cores and Complete Ind. / Transformer)
- Multi-Obj. Optimiz. Considering Full System
- Design for Manufacturing

■ **Option #2: Improve Material Properties / Manufacturing**

- Integrated Cooling
- PCB-Based Magnetics with High Filling Factor (e.g. VICOR)
- Advanced Locally Adapted Litz Wire / Low-μ Material (Distributed Gap) / Low HF-Loss Material

■ **Option #3: Minimize Requirement**

- Multi-Level Converters
- Magnetic Integration
- Hybrid (Cap./Ind.) Converters

→ **Magnetics/Passives-Centric Power Electronics Research Approach !**

■ **End**

Thank You !