Power Quality Enhancement in Residential Smart Grids through Power Factor Correction Stages

Víctor M. López-Martín, Francisco J. Azcondo, *Senior Member, IEEE*, and Alberto Pigazo, *Senior Member, IEEE*

***Abstract*—The proliferation of non-linear loads and the increasing penetration of Distributed Energy Resources (DER) in Medium-Voltage (MV) and Low-Voltage (LV) distribution grids, make it more difficult to maintain the power quality levels in residential electrical grids, especially in the case of weak grids. Most household appliances contain a conventional Power Factor Corrector (PFC) rectifier, which maximizes the load Power Factor (PF) but does not contribute to the regulation of the voltage Total Harmonic Distortion (THD_V) in residential electrical grids. This manuscript proposes a modification for PFC controllers by adapting the operation mode depending on the measured THD_V. As a result, the PFCs operate either in a low current Total Harmonic Distortion (THD_I) mode or in the conventional resistor emulator mode and contribute to the regulation of the THD_V and the PF at the distribution feeders. To prove the concept, the modification is applied to a current sensorless Non-Linear Controller (NLC) applied to a single-phase Boost rectifier. Experimental results show its performance in a PFC front-end stage operating in Continuous Conduction Mode (CCM) connected to the grid with different THD_V.**

***Index Terms*—Harmonic distortion, Non-linear carrier control, Power factor correction.**

I. Introduction

HARMONIC limits in AC electrical grids are established by international standards and grid codes in order to ensure an efficient and proper operation of the subsystems and equipment connected to the grid, i.e. generators, loads and storage systems. The IEEE 519-2014 recommended practice and requirements for harmonic control in electric power systems [1] defines the limits on specific harmonics as well as on the current Total Harmonic Distortion (THD_I) and the current Total Demand Distortion (TDD). Voltage and current harmonic distortion levels in electrical distribution systems are closely related, and the recommended THD_V limits in distribution feeder tap points are likely exceeded if highly nonlinear loads are connected [2]. Exceeding voltage or current harmonic limits reduces the overall efficiency and might produce critical faults in weak or critical Electrical Power Systems (EPS). Among others, harmonic distortion causes heating of induction motors [3], accelerated aging of insulation [4] and harmonic resonances in capacitors for reactive power compensation [5]. Moreover, the harmonic distortion might affect the normal operation of medical equipment [6], [7] and distribution transformers in residential areas might suffer excessive loading, contributing to accelerate their aging [8].

The voltage harmonic distortion is mainly due to background harmonic sources, but residential loads contribute to increase the THD_V, especially at 3^{rd}, 11^{th} and 13^{th} harmonics [9]. The effects of harmonics in residential areas are attenuated applying local or wide area mitigation approaches. Local ones are employed at the load or Distributed Energy Resource (DER) side, i.e. distributed generation and storage active front-ends, operated as adjustable harmonic impedances [10], [11] or including active power filter functionalities [12]. Wide area mitigation strategies are based on the coordination of local solutions, i.e. assigning compensation priorities to DERs [13]. The THD_V is improved by means of a droop-based approach [14], adjusting the equivalent DER admittance [15] or the deployment of distributed low-power low-voltage equipment for current harmonic filtering [16]. The integration of mitigation equipment at distribution feeder level, i.e. hybrid active power filters, also contributes to increasing the PF and mitigating the effect of voltage disturbances on household appliances [17]–[19]. The compensation capability and availability using DERs is limited by their nominal rating, i.e. the LCL filter characteristics [20], and the operation mode, i.e. reactive power compensation [21], respectively. Dedicated local filtering solutions require the integration of additional equipment, increasing the overall cost, and involve a previous analysis of their impact on the grid [16], e.g. resonances in passive filters. Moreover, coordination of local solutions would require communications that increase the deployment complexity. In contrast, this manuscript proposes a local load side approach, with no extra hardware cost, achieved by extending the functionality of available PFCs.

PFC is widely employed in household appliances as an active front-end AC/DC converter imposing unity power factor and supplying the load with the required constant DC

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voltage, while ensuring a high efficiency [22]. PFC stages have traditionally been utilized to improve the electrical power quality of EPS by emulating an input resistance for all system frequencies, so that in the case of a sinusoidal grid voltage the input current is sinusoidal with very high-frequency harmonic distortion, linked to the switching ripple. However, this resistor emulator behavior will result in line current harmonics in the case of harmonically distorted grid voltages, which would contribute to maintain THD_V levels at the Point of Common Coupling (PCC). A digitally controlled boost PFC with variable input impedance is proposed in [23]. The resistor emulator behavior is adjusted at different harmonic frequencies to contribute to the improvement of the grid stability.

Diverse works on PFC, impressing sinusoidal input currents (*sinPFC*), have previously been published. In [24], [25], a sine wave generator is employed within the current loop to generate the appropriate reference current in single-phase systems. The sine wave generator can be replaced by a Phase-Locked Loop (PLL), as in [26], to generate the reference signal. Predictive controllers with a current sensor, showing immunity to input voltage distortion are utilized in [27]. These approaches are also employed in three-phase PFC in [28] and [29], respectively. The accurate synchronization of the modulation signals with the grid, the harmonics injected to compensate the distortion effect and the implementation of adaptive controllers to find the best response under distorted or non-distorted grid voltage motivate the utilization of digital controllers. The adoption of a sensorless solutions represents a step forward in terms of simplicity and reliability. As long as the resulting power factor is satisfactory, the elimination of the current sensor also eliminates the circuitry associated to the adoption of a reference for the current measurement, signal conditioning circuits and an analog-to-digital converter, in the case of a the controller implementation in a digital circuit. Since the current signal is not affected by the sensor size, the resulting controller covers a wider power rate. Several sensorless approaches have been presented recently. A voltage sensorless controller with adjustable power factor is proposed in [30] for a three-phase three-switch Vienna rectifier. A current sensorless technique with an artificial input voltage, stored in a Look-Up Table (LUT) to gain immunity under distorted input voltage, is presented in [31]. A more sophisticated technique, which precalculates the duty-cycle sequence, extending the load range of application with no input voltage or current acquisition, assuming that the reference is sinusoidal is presented in [32]. In [33], [34], a current sensorless technique is extended for multiphase current interleaved topologies. Since the actual current shape depends on the volt-seconds across the input inductor, the distortion of the AC input voltage produces input current distortion when the resistor emulator technique is used.

This paper proposes to improve the PF at the PCC by applying an adaptive PFC controller to the grid-connected AC/DC converters of a residential grid, introducing the concept of Power Quality Enhancer (PQE) (Fig. 1). This PQE adapts the AC/DC converter current depending on the grid distortion. In this way, the PFC controller can operate in both resistor emulator and sinusoidal input current modes, allowing the THD_V minimization in residential electrical grids while maintaining maximum PF at the PCC. The proposed PQE PFC helps to reach advanced specifications required in residential smartgrids, such as peak load reduction [35] and energy management [36]. The paper is organized as follows. The main contributions are presented in Section II and III. Section II introduces the definitions of electrical power quantities and the effect of THD_I on the PF measured at the PCC and presents the PQE's operation principles. Details of the controller selected to develop the proof of concept [37] and the experimental results with the controller modified by the PQE are presented in Section III and IV respectively.

II. Effect of the Proposed Controller on the Electrical Power Quality of Residential Grids

The proposed PQE PFC consists of a conventional PFC stage with an enhanced digital controller, which adjusts the operation mode to maximize the PF while contributing to reduce the THD_V at the PCC. The proposed controller modification is shown in Fig. 1, where the local THD_V measurement is employed to adjust the PFC operation mode. For analysis purposes, as depicted in Fig. 1, the Low-Voltage (LV) residential grid and household appliances are modeled through their Thévenin and Norton equivalents respectively. In [38], an individual residential house is modeled by its equivalent impedance and a current source, representing the linear and non-linear loads respectively. Considering that most of the Conventional Household Appliances (CHA) are connected to the grid through unidirectional AC/DC converters, the house impedance is approximated by a pure resistor, R_{CHA}, and a current source, corresponding to the sum of $N-1$ current harmonics i'_{CHA}. Therefore, i'_{CHA} is given by (1), where N represents the maximum harmonic order, n, of the CHA current:

$$i'_{CHA}(t) = \sum_{n\neq 1}^{N} i'_{CHA,n}(t) \tag{1}$$

Similarly, PQE PFC based household appliances are modeled through an equivalent resistor R_{eq} and the harmonically distorted current i'_{PQE},

$$i'_{PQE}(t) = -k\frac{v_{PCC}(t) - v_{PCC,1}(t)}{R_{eq}} = -k\frac{\sum_{n\neq 1}^{M} v_n(t)}{R_{eq}} = -k\frac{v_{PCC,H}(t)}{R_{eq}}, \tag{2}$$

calculated with the difference between the PCC voltage (v_{PCC}) and its fundamental frequency component ($v_{PCC,1}$), with M representing the maximum harmonic order of v_{PCC}. The factor k is selected depending on the PCC THD_V. By applying $k = 0$, the PQE PFC behaves as a resistor emulator and with $k = 1$, a sinusoidal input current is achieved. Moreover, it must be considered that, behaving as a front-end converter and assuming a resistive load (R_{DC}) fed by the stationary voltage (V_{DC}) imposed by the PQE PFC outer voltage controller (Fig. 1), the input power of the PQE PFC (P^{in}_{PQE}) is imposed by the PFC output power, with no dependence on the operation mode selected through k. The

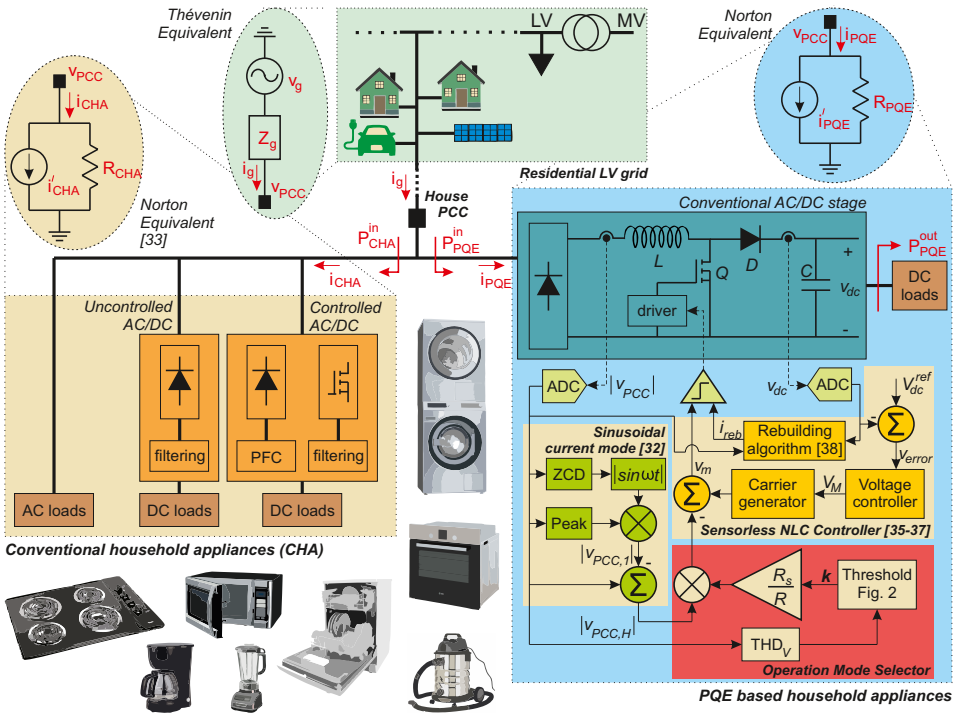


Fig. 1. Residential LV grid with household appliances feed through conventional AC/DC stages (without the proposed operation mode selector) and the proposed PQE controller.

LV electrical grid, from the point of view of the household appliances, is modeled through the impedance Z_g and v_g:

$$v_g(t) = v_{g,1}(t) + \sum_{n\neq 1}^{L} v_{g,n}(t), \tag{3}$$

where $v_{g,1}$ is the fundamental component of the grid voltage (v_g), $v_{g,n}$ its n^{th} harmonic component, and L the maximum harmonic order of v_g, with $L \leq M < N$.

Assuming the approach in IEEE Std. 1459 [39], where the electrical power quantities under sinusoidal, non-sinusoidal, balanced and unbalanced conditions are defined, the instantaneous input power of the PQE PFC in Fig. 1 is written as

$$p^{in}_{PQE}(t) = v_{PCC}(t) i_{PQE}(t) = v_{PCC}(t)\left(\tfrac{v_{PCC}(t)}{R_{eq}} + i'_{PQE}(t)\right) \tag{4}$$

Averaging p^{in}_{PQE} over a grid period T results in the active power of the PQE PFC (P^{in}_{PQE}):

$$P^{in}_{PQE}(t) = \tfrac{1}{T}\int_{t-T}^{t} p^{in}_{PQE}(\tau)d\tau = \frac{V^2_{PCC,1}}{R_{eq}} + \frac{(1-k)}{R_{eq}}\sum_{n\neq 1}^{M} V^2_{PCC,n} = \frac{P^{out}_{PQE}(t)}{\eta} \tag{5}$$

where it has been assumed that the PCC voltage and R_{eq} change slowly enough, η is the PQE PFC efficiency and P^{out}_{PQE} its output power, which, being employed as a front-end converter, means $P^{out}_{PQE} = \frac{V^2_{DC}}{R_{DC}}$ (Fig. 1). Hence, the equivalent resistance of the PQE PFC is

$$R_{eq} = \frac{\eta/100}{P^{out}_{PQE}} V^2_{PCC,1}\left(1 + (1-k)THD^2_V\right), \tag{6}$$

which, having P^{out}_{PQE} imposed by the PFC outer voltage control loop, depends on the PCC voltage and the selected operation mode (k). As a consequence, in the resistive emulator mode ($k = 0$) R_{eq} increases with the THD_V. For simplicity's sake, it will be assumed that $\eta = 100\%$ in the subsequent analysis.

A. PF at the PCC with the PQE PFC controller in both operation modes

As will be proved in this subsection, the PF at the PCC can be improved by the PQE PFC in household appliances. The PF is evaluated through the definition in IEEE Std. 1459 [39] and both operation modes ($k = 1$ and $k = 0$) are considered. From Fig. 1:

$$PF = \frac{P^{in}_{PQE} + P^{in}_{CHA}}{V_{PCC} I_g} = \frac{P^{out}_{PQE} + \dfrac{V^2_{PCC,1}(1+THD^2_V)}{R_{CHA}} + P_{harm}}{\sqrt{V^2_{PCC,1}(1+THD^2_V)}\sqrt{I^2_g}} \tag{7}$$

$$\text{and } P_{harm} = \sum_{n\neq 1}^{M} V_{PCC,n} I'_{CHA,n} \cos\theta_n, \tag{8}$$

where P^{in}_{CHA} is the active power due to the CHA and the term P_{harm} corresponds to the active power transferred by the harmonic current components due to the conventional load nonlinearities and the harmonic distortion of the PCC voltage.

The overall household appliance current (i_g) can be obtained from Kirchhoff's Current Law (KCL) at the PCC:

$$\begin{aligned} i_g(t) &= i_{PQE}(t) + i_{CHA}(t) \\ &= i'_{PQE}(t) + i'_{CHA}(t) + \tfrac{R_{eq}+R_{CHA}}{R_{eq}R_{CHA}} v_{PCC}(t) \end{aligned} \tag{9}$$

and, then, the squared rms value of the overall household appliance current is evaluated using (10):

$$\begin{aligned} I_g^2 &= \tfrac{1}{T}\int_{t-T}^{t} i_g^2(\tau)d\tau = \frac{\left(1+(1-k)^2THD_V^2\right)\left(P_{PQE}^{out}\right)^2}{V_{PCC,1}^2\left(1+(1-k)THD_V^2\right)^2} \\ &+\frac{2P_{PQE}^{out}(1-k)P_{harm}}{V_{PCC,1}^2\left(1+(1-k)THD_V^2\right)}+\frac{2P_{PQE}^{out}}{R_{CHA}} \\ &+\frac{V_{PCC,1}^2}{R_{CHA}^2}THD_{I'_{CHA}}^2+\frac{2P_{harm}}{R_{CHA}}+(1+THD_V^2)\frac{V_{PCC,1}^2}{R_{CHA}^2} \end{aligned} \tag{10}$$

Substituting (10) into (7), the PF at the PCC is obtained:

$$PF=\frac{P_{PQE}^{out}+\dfrac{V_{PCC,1}^2(1+THD_V^2)}{R_{CHA}}+P_{harm}}{\sqrt{S_0^2+S_k^2}}, \tag{11}$$

where S_0^2 and S_k^2 are given in (12) and (13) respectively:

$$S_0^2=\frac{2V_{PCC,1}^2(1+THD_V^2)}{R_{CHA}}\left(P_{PQE}^{out}+P_{harm}+\frac{V_{PCC,1}^2}{2R_{CHA}}\left(1+THD_V^2+THD_{I'_{CHA}}^2\right)\right) \tag{12}$$

$$S_k^2=\frac{1+THD_V^2}{1+(1-k)THD_V^2}\left(\frac{1+(1-k)^2THD_V^2}{1+(1-k)THD_V^2}(P_{PQE}^{out})^2+2(1-k)P_{PQE}^{out}P_{harm}\right) \tag{13}$$

Eq. (12) does not depend on k while S_k^2 depends on the selected operation mode. Considering that $k\in[0,1]$ and $P_{harm}+P_{PQE}^{out}>0$, the value of k required to maximize the PF is obtained from (11) by minimizing the denominator, resulting in

$$k=\frac{P_{harm}(1+THD_V^2)}{\left(P_{harm}+P_{PQE}^{out}\right)THD_V^2}=\frac{1+\frac{1}{THD_V^2}}{1+\frac{P_{PQE}^{out}}{P_{harm}}}. \tag{14}$$

Identification of the optimal continuous value of $k\in[0,1]$ requires P_{harm} to be known. In the following analysis only $k=0$ or $k=1$ values are allowed. Then, depending on the selected operating mode for the PQE PFC, the overall PF becomes

$$PF=\begin{cases}\dfrac{P_{PQE}^{out}+\dfrac{V_{PCC,1}^2(1+THD_V^2)}{R_{CHA}}+P_{harm}}{\sqrt{S_0^2+(1+THD_V^2)(P_{PQE}^{out})^2}}, & k=1 \text{ (sinusoidal)} \\ \dfrac{P_{PQE}^{out}+\dfrac{V_{PCC,1}^2(1+THD_V^2)}{R_{CHA}}+P_{harm}}{\sqrt{S_0^2+(P_{PQE}^{out})^2+2P_{PQE}^{out}P_{harm}}}, & k=0 \text{ (resistive)}\end{cases} \tag{15}$$

where P_{PQE}^{out} only depends on the DC load of the PQE PFC, being independent on the selected k. Under the same grid and load conditions, a change in k results in a different PF at the PCC. The operation in a sinusoidal line current mode is the most beneficial if the following relationship is fulfilled

$$(1+THD_V^2)(P_{PQE}^{out})^2<(P_{PQE}^{out})^2+2P_{PQE}^{out}P_{harm} \tag{16}$$

because this mode results in higher PF at the PCC than the resistive emulator mode. This condition can also be expressed as

$$THD_V<\sqrt{2}\sqrt{\frac{P_{harm}}{P_{PQE}^{out}}} \tag{17}$$

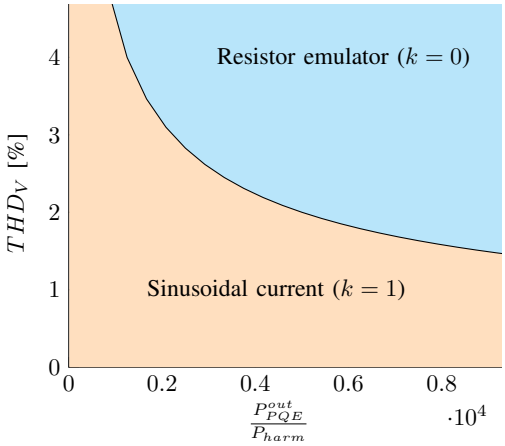


Fig. 2. Operation region of the PQE PFC resulting in a higher PF ($P_{harm}>0$).

Therefore, the active power ratio $\frac{P_{PQE}^{out}}{P_{harm}}$, which depends on the nonlinear household appliances, and the measured THD_V at the PCC are used to select the most appropriate k. It must be considered that in the case of $P_{harm}\leq 0$, (16) cannot be verified and the resistive emulator mode is the most beneficial. Condition (16) is depicted in Fig. 2, showing the operation mode that results in a better PF at the PCC depending on the THD_V and the $\frac{P_{PQE}^{out}}{P_{harm}}$ ratio. By increasing the power processed through the proposed PQE PFCs, the overall PF will benefit from the resistor emulator mode ($k=0$) or the sinusoidal current mode ($k=1$) depending on the measured THD_V at the PCC. In the case of highly non-linear loads as CHA, the most beneficial operation mode in residential EPS (with relatively low THD_V) is the sinusoidal current one ($k=1$). If the power processed through the PQE PFCs is high enough, the resistor emulator mode ($k=0$) would be the most beneficial one. As an illustrative example, given a certain $\frac{P_{PQE}^{out}}{P_{harm}}$, for instance 5000, the threshold value provided by eq. (17) is 2 %. Below this THD_V value, the PQE must operate in sinusoidal current mode to maximize the overall PF.

The overall system conditions allowing the operation in a sinusoidal line current mode are evaluated below. As has been established before, this operation mode requires

$$P_{harm}=\sum_{n\neq 1}\frac{1}{2}\Re e\left\{\vec{v}_{pcc}(n\omega)\times\vec{i}_{CHA}^{\,*}(n\omega)\right\}>0, \tag{18}$$

where $\vec{v}_{pcc}$ and $\vec{i}'_{CHA}$ are the phasor representation of the PCC voltage and the harmonic current due to the conventional loads in Fig. 1. By applying the superposition principle, and replacing Z_g in Fig. 1 by R_g+jL_g, the condition (18), in terms of IEEE Std. 1459 definitions and considering the PQE PFC operation mode through k, can be rewritten as

$$P_{harm}=P_A(k)-P_B(k)>0\rightarrow P_A(k)>P_B(k) \tag{19}$$

where the term $P_A(k)$, given in (20), corresponds to the power term resulting from the interaction of conventional non-linear loads and the grid voltage harmonics while $P_B(k)$, the power term which is consequence of the voltage across the grid

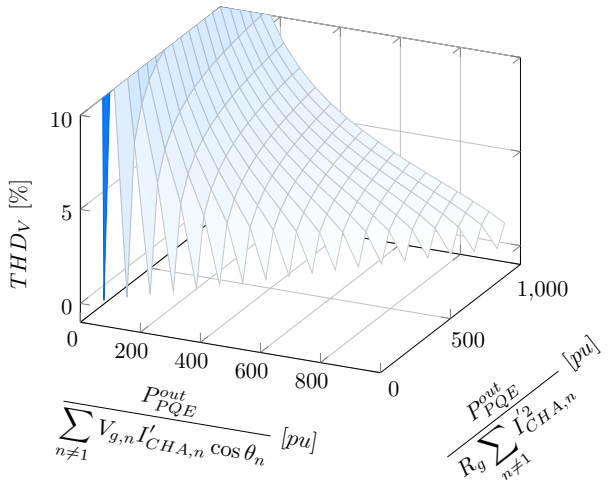


Fig. 3. Operation surface of the PQE PFC resulting in a higher PF ($R_{CHA} \approx R_{eq}$, $R_g << R_{CHA}$, $L_g << R_g$).

impedances due to the harmonics caused by the non-linear loads, is directly computed by (21).

From (19), having a grid voltage harmonically distorted above a given rate, the PFC operation in sinusoidal input current mode improves the PF. Otherwise, the resistor emulator mode results in better PF. Under the assumption of $R_{CHA} \approx R_{eq}$, $R_g << R_{CHA}$, $L_g << R_g$ and considering that $I'_{CHA,n}$ decreases while increasing n, (19) can be approximated by

$$\sum_{n\neq 1} V_{g,n} I'_{CHA,n} \cos\theta_n > R_g \sum_{n\neq 1} I'^2_{CHA,n} \tag{22}$$

where the contribution of the grid voltage harmonics to the active power must be greater than the effect of the harmonic currents through the grid impedance.

By substituting (22) into (17), under the previous assumptions, the following relationship must be accomplished in order to improve the overall PF by operating in sinusoidal input current mode

$$\begin{aligned} THD_V &< \sqrt{2}\sqrt{\frac{P_{harm,grid}}{P^{out}_{PQE}} - \frac{P_{harm,R_g}}{P^{out}_{PQE}}} \\ &\approx \sqrt{2}\sqrt{\frac{\sum_{n\neq 1} V_{g,n} I'_{CHA,n} \cos\theta_n}{P^{out}_{PQE}} - \frac{R_g \sum_{n\neq 1} I'^2_{CHA,n}}{P^{out}_{PQE}}} \end{aligned} \tag{23}$$

Condition (23) is depicted in Fig. 3. The sinusoidal input current mode leads to a higher PF between the depicted surface and the $THD_V = 0$ % plane, i.e. underneath the surface.

B. PQE PFC concept simulations

The PQE PFC concept has been tested with simulations considering a typical feeder in a distribution grid. A scenario with 20 houses connected to the feeder, where the house and grid parameters have been obtained from [40]–[42], and CHA are a combination of Compact Fluorescent Lights (CFL) and Personal Computers (PC) adjusted to a nominal house power of 2.2 kW and a 230 V 50 Hz feeder voltage with harmonic distortion levels due to 5^{th} and 7^{th} harmonics, $L_g = 0.08$ mH, $R_g = 60$ $m\Omega$. The simulations are carried out changing the number of conventional non-linear loads and PFCs ($\frac{P^{in}_{PFC}}{P_{PCC}}$), while maintaining the overall active power at the PCC (P_{PCC}), and measuring the overall PF at the PCC according to the scheme depicted in Fig. 1. The simulations have been carried out in MatLab/Simulink and show the applicability of the PQE PFC concept in residential EPS.

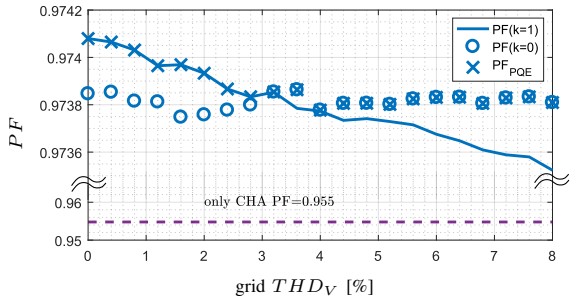
Fig. 4 shows the PF at the PCC due to the PQE PFC. The PQE controller selects the most beneficial operation mode ($k = 1$ or $k = 0$) following the approach in Section II.A. The alternative operation mode, discarded by the PQE, is also plotted for comparison purposes. As it is shown, the PCC PF increases by replacing conventional loads with PFCs but, at low grid THD_V (due to v_g in Fig. 1), $k = 1$ performs better than $k = 0$ mode and the PQE controller assumes this operation mode to maximize the PF at the PCC. With PQE applying $k = 1$, and $k = 0$ discarded, the maximum difference between modes arises at pure sinusoidal grid voltage and $\frac{P^{in}_{PFC}}{P_{PCC}} = 50\%$, where the PQE increases the PF from 0.988 to 0.989, meaning 120 VA. If all the power is processed through PQE PFCs and the grid THD_V reaches 8%, then $k = 0$ increases the PF with respect the $k = 1$ case, from $PF = 0.995$ up to virtually unity, reducing the reactive component by 4.17 kVA. The worst PF corresponds to only CHA loads, with $PF = 0.955$.

III. Implementation of the PQE Controller

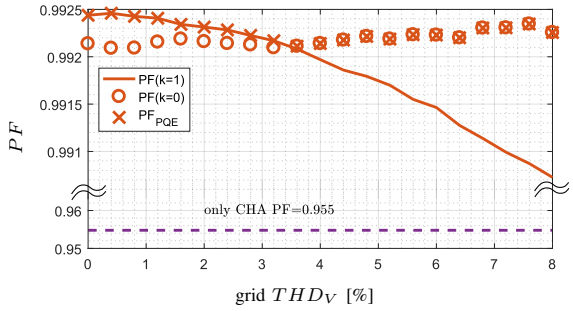
According to the previous discussion, a sinusoidal line current contributes to increasing the efficiency and performance of the residential EPS within the conditions depicted in Fig. 2. The PQE can be included in any PFC controller. Without losing generality, this section describes the proposed single-phase sensorless controller for PFC achieving this behavior. The proposed approach extends the performance of the digital sensorless Non-Linear Controller (NLC) in PFC [37], [43]–[46] by including a new term, which depends on the measured voltage harmonic distortion and the DC load. This term achieves low THD_I current impression regardless of the line voltage distortion.

$$P_A(k) = \sum_{n\neq 1} V_{g,n} I'_{CHA,n} \frac{(R_g R_{eq} + (1-k) R_g R_{CHA} + R_{CHA} R_{eq}) \cos\theta_n + n\omega L_g (R_{eq} + (1-k) R_{CHA}) \sin\theta_n}{(R_g R_{eq} + (1-k) R_g R_{CHA} + R_{CHA} R_{eq})^2 + n^2\omega^2 L_g^2 (R_{eq} + (1-k) R_{CHA})^2} \tag{20}$$

$$P_B(k) = \sum_{n\neq 1} I'^2_{CHA,n} \frac{R_g (R_g R_{eq} + (1-k) R_g R_{CHA} + R_{CHA} R_{eq}) + n^2\omega^2 L_g^2 (R_{eq} + (1-k) R_{CHA})}{(R_g R_{eq} + (1-k) R_g R_{CHA} + R_{CHA} R_{eq})^2 + n^2\omega^2 L_g^2 (R_{eq} + (1-k) R_{CHA})^2} \tag{21}$$



(a)



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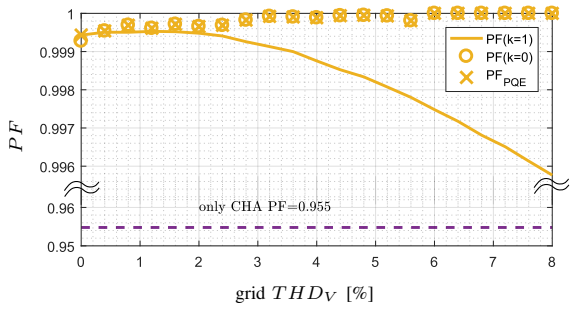

(c)

Fig. 4. PF at the PCC due to the PQE and the discarded operation modes. a) $\frac{P^{in}_{PFC}}{P_{PCC}} = 25\%$ b) $\frac{P^{in}_{PFC}}{P_{PCC}} = 60\%$ c) $\frac{P^{in}_{PFC}}{P_{PCC}} = 90\%$.

The NLC has been selected to connect this proposal with recent research work [47]. It shows a better dynamic performance compared to the linear controllers based on current averaging, especially for high-frequency grids. The main drawback is its poor noise immunity, overcome with the sensorless approach. A typical bandwidth of the linear current control loop recommended for utility line frequencies ($50-60\ Hz$) is units of kHz, with switching frequencies close to $100\ kHz$. If the line frequency increases, the typical distortion around the line zero-crossing makes it impossible to fulfill the harmonic limits. This issue is addressed in detail in [48] and [49]. Nonlinear controllers solve this problem, achieving responses as fast as the switching cycle [50]. The NLC sensorless controller represents a solution suitable for universal voltage (85 to 250 V_{rms} and grid frequencies up to 400 Hz), being attractive to prove the contribution of this paper.

The NLC is defined for the Boost converter switching at constant frequency, $f_{sw} = 1/T_{sw}$, and with Pulse-Width

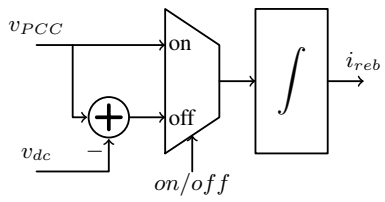

Fig. 5. Block diagram of the basic current rebuilding algorithm.

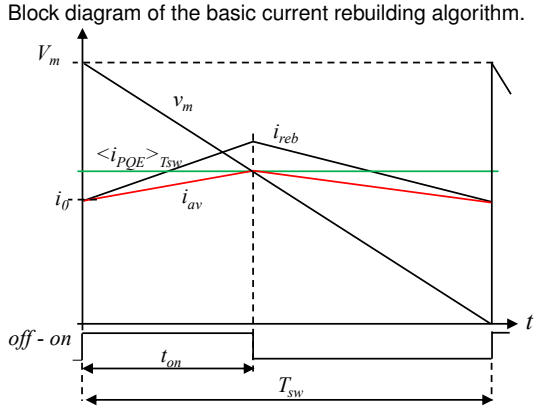

Fig. 6. Representation of the NLC variables.

Modulation (PWM). A variable $i_{av}(t)$ is calculated during each switching period, $0 \leq t \leq T_{sw}$, from $i_{reb}(t)$, which is the output of the current rebuilding algorithm [51] shown in Fig. 5 and i_0, which is the current at the beginning of the switching period. The carrier signal, v_m, and i_{av} are compared to set the duty cycle, d.

$$i_{av}(t) = \frac{i_{reb}(t) + i_0}{2}, \tag{24}$$

It is assumed that $i_{av}(dT_{sw})$ represents the average current over the switching period when the estimation errors are properly compensated i.e.

$$i_{av}(dT_{sw}) = \langle i_{PQE} \rangle_{T_{sw}} \tag{25}$$

To derive the *sinPFC* NLC for the PQE PFC, $\langle i_{PQE} \rangle_{T_{sw}}$ is firstly assumed sinusoidal, so that

$$\langle i_{PQE} \rangle_{T_{sw}} = \frac{P^{in}_{PQE}}{V_{PCC,1}} \sqrt{2} \sin(\omega t) \tag{26}$$

The controller with $k = 0$ results in an input current i_{PQE} , i.e. $\langle i_{PQE} \rangle_{T_{sw}}$, proportional to v_{PCC} using the NLC technique as shown in Fig. 6 and summarized with the expression

$$\langle i_{PQE} \rangle_{T_{sw}} = \frac{V_{DC}}{R_{eq}} (1 - d), \tag{27}$$

with the duty cycle $d = t_{on}/T_{sw}$ and the carrier signal v_m, whose amplitude, V_m, is proportional to the input power, P^{in}_{PQE}, and also represents the inverse of the emulated resistance R_{eq}.

$$v_m = V_m \left(1 - \frac{t}{T_{sw}}\right), 0 \leq t \leq T_{sw} \tag{28}$$

with

$$V_m = R_s \frac{V_{DC}}{R_{eq}} = R_s \frac{V_{DC}}{V_{PCC,1}^2} P_{PQE}^{in}, \tag{29}$$

where R_s is a fictitious sensing resistance, which gives consistency to the units of the variables in the rebuilding algorithm.

Considering a distorted AC line voltage at the PCC according to (3), (26) can be rewritten as a function of $v_{PCC,1}$

$$\langle i_{PQE} \rangle_{T_{sw}} = \frac{v_{PCC,1}}{R} = \frac{v_{PCC} - v_{PCC,H}}{R} \tag{30}$$

where R provides proportionality between the input current i_{PQE} and the fundamental component of the voltage v_1.

Assuming that the converter operates in the Continuous Conduction Mode (CCM), the ideal quasi-static conversion characteristic of the PWM-controlled Boost converter with duty cycle d is given by

$$v_{PCC} = V_{DC}(1-d) \tag{31}$$

and introducing (31) into (30) results in

$$\langle i_{PQE} \rangle_{T_{sw}} = \frac{1-d}{R} V_{DC} - \frac{k}{R} v_{PCC,H} \tag{32}$$

Around the AC line zero crossing, where the converter operates in the Discontinuous Conduction Mode (DCM), a little distortion in the input current occurs as is explained in detail in [34] for the traditional NLC controller, affecting this low THD_I controller in the same way. In CCM, the NLC control achieves power factor correction through a comparison of signals (Fig. 6) that finds an easy implementation in a digital circuit.

The output voltage is approximated in (31) and (32) by its DC value (small ripple approximation) at the specified reference level $V_{DC} = V_{DC}^{ref}$. The first term in (32), $V_{DC}(1-d)/R$, is similar to the NLC control law shown in [34] or the Linear Peak Current-Mode (LPCM) control in [52]. The second term, $v_{PCC,H}/R$, corresponds to line harmonic voltage distortion and factor k allows the THD_V to be considered. The duty cycle command is obtained by comparing the digitized signals $i_{av}(t)$ and a leading-edge saw-tooth carrier signal $v_m(t)$, redefined as

$$v_m(t) = V_m \left(1 - \tfrac{t}{T_{sw}}\right) - k \tfrac{v_{PCC,H}}{R} R_s, \quad 0 \le t \le T_{sw} \tag{33}$$

where $V_m = R_s V_{DC}/R$. For the current sensorless application, $R_s = 1\ \Omega$ is arbitrarily adopted, where the value R changes with the load and is set by the outer voltage loop with V_m [43]. The second term in (33), $kR_s v_{PCC,H}/R$, offsets the carrier signal in each switching period, meaning a low-frequency harmonic content in the carrier signal. With the factor k defined in the previous section, the operation mode of the PFC is selected. Fig. 7 shows the waveforms defined in (33) and the lowest harmonics over a half line cycle, for an input voltage with a $THD_V = 6\ \%$ with harmonics $v_{PCC,3} = 0.05\sqrt{2}\sin(3\omega t)$, $v_{PCC,5} = 0.03\sqrt{2}\sin(5\omega t + \pi)$ and $v_{PCC,7} = 0.01\sqrt{2}\sin(7\omega t)$. For clarification purposes, T_{sw} has been depicted much longer than the actual implemented switching period.

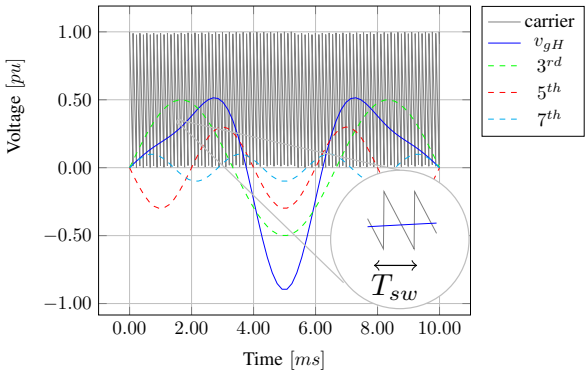

Fig. 7. Carrier and $v_{PCC,H}$ in an example of input voltage with $THD_V = 6\%$.

In order to obtain the second term in (33), an Analog-to-Digital Converter (ADC) digitizes the input voltage, v_{PCC}, and a sinusoidal pattern is synchronized with the utility line-to-neutral voltage using a digital Zero-Crossing Detector (ZCD). An input voltage peak detector is used to approximate the value of $v_{PCC,1}$ to $v_{PCC,1} \approx V_{PCC,peak}\sin(\omega t)$. Different approaches, such as the zero-phase detector circuit in [53] or PLLs can be applied here, the last one being the preferred approach to achieve immunity to input voltage distortion [54], [55], as is included in certain PFC proposals [56], [57]. Hence, (30) is rewritten as

$$\langle i_{PQE} \rangle_{T_{sw}} = \frac{V_{PCC,peak}}{R} \sin(\omega t), \tag{34}$$

where ω is evaluated on a period-to-period basis and, assuming slow harmonic variations, their effect on ω are negligible. Estimation errors occur due to the phase displacement of $\sin(\omega t)$ and the fundamental in v_{PCC}, which are caused by the relative phase and magnitude of the voltage harmonics in v_{PCC}. Replacing the ZCD by a PLL avoids such effects, however, it must be considered that the THD_V in residential feeders is usually in the range (1%,3%) [58], which limits the potential phase errors to less than a maximum 3.3 degrees. The effects of the voltage harmonic distortion on the estimation of $V_{PCC,peak}$ are mitigated by the outer voltage control loop of the PQE, which adjusts the amplitude of i_{PQE}.

If i_{PQE}, which is purely sinusoidal according to (30), is initially different to the one required by the load, then the outer voltage loop modifies V_m, and therefore R, to set the input current according to the required power.

A block diagram of the Boost rectifier with the low THD_I controller and its connection to the operation mode selector is shown in Fig. 1. The proposed circuit obtains a signal that represents the input voltage distortion with $|v_{PCC,H}| \approx |v_{PCC}| - v_{PCC,peak}\,|\sin(\omega t)|$.

The calculation of the voltage distortion can be improved using a specific algorithm implemented in a digital device, i.e. a microcontroller or an Field Programmable Gate Array (FPGA), the Fast Fourier Transforms (FFT) is a good choice to obtain the harmonic content of a variable, with dedicated blocks to compute this, like in [59], [60], but this requires

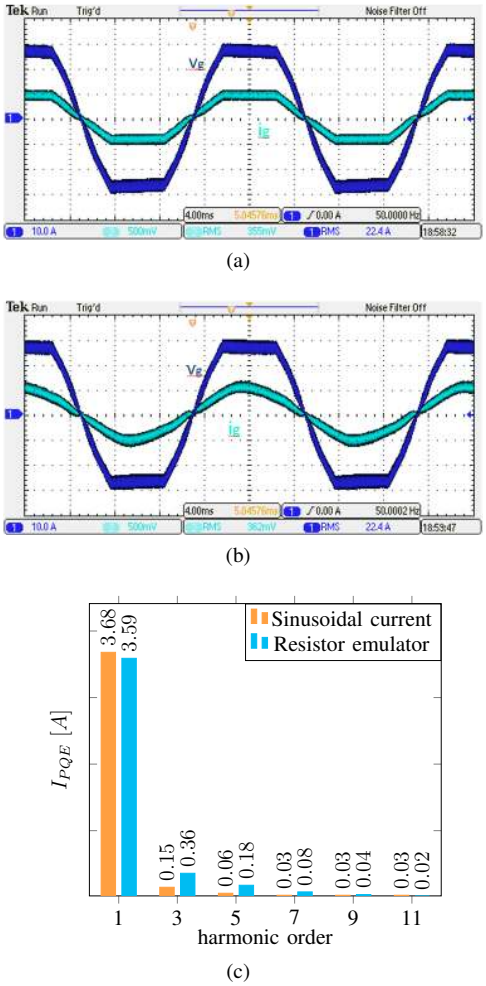

Fig. 8. Experimental results of PQE PFC at $50\ Hz$. Voltage and current waveforms in a) resistor emulator mode ($k = 0$), b) sinusoidal current mode ($k = 1$) and c) measured spectra in both operation modes.

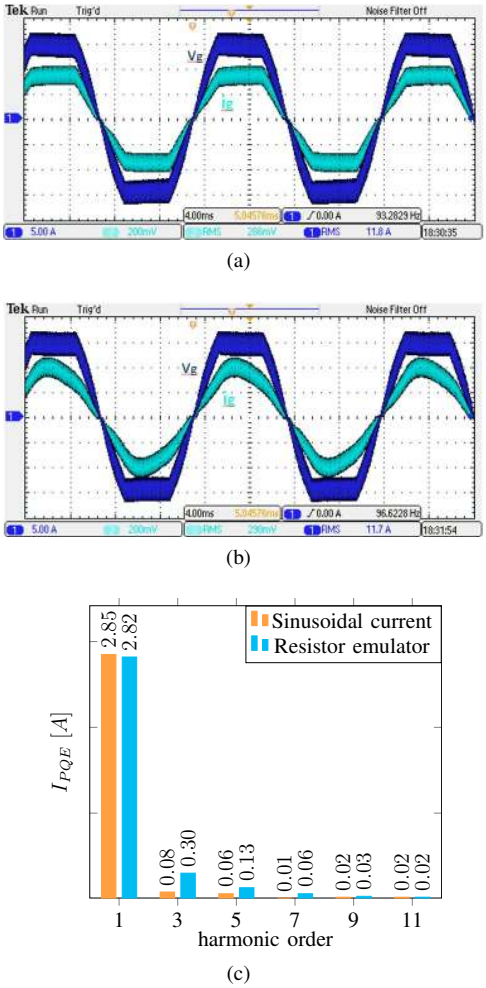

Fig. 9. Experimental results of PQE PFC at $60\ Hz$. Voltage and current waveforms in a) resistor emulator mode ($k = 0$), b) sinusoidal current mode ($k = 1$) and c) measured spectra in both operation modes.

lots of resources. On the other hand, the outer loop makes an accurate calculation of the distortion term unnecessary and the value of each harmonic voltage is not needed, so the total harmonic voltage $v_{PCC,H}$ is computed, with the outer voltage loop setting the value of V_m. In steady-state, R automatically defines the amplitude $< i_{PQE} >_{T_{sw}}$ [46].

Note that with the PQE controller, the load viewed by the grid, R_{eq}, is now a function of the input voltage phase. In steady state, and for a defined input power P^{in}_{PQE}, the input current in (26), and (34) yields an expression for R

$$R = \frac{V_{PCC,peak} V_{PCC,1}}{P^{in}_{PQE}\sqrt{2}} \tag{35}$$

From (35), it is possible to obtain the expression for the equivalent resistance R_{eq}

$$R_{eq} = R\frac{v_{PCC,1}}{v_{PCC}} \tag{36}$$

IV. Experimental Results

With the addition of the proposed modification to the NLC controller, the parameter k selects the preferred behavior depending on the application, either resistor emulator or low THD_I.

To experimentally validate this proposal, the Boost converter has been tested under two input voltages (120 V_{rms} and 230 V_{rms}) and three input frequencies (50 Hz, 60 Hz and 400 Hz), with 12 % harmonic distortion, for two different power levels (around 330 W and 800 W), and 96 kHz switching frequency. These situations have been tested with the PQE controller in both pure sinusoidal and resistor emulator behavior modes, and the results are summarized in Table I. A Pacific 345-AMX AC power source is used to supply the front-end stage with a distorted voltage. Different templates of distorted voltages are predefined. The THD_I results, which include all the harmonics required by the standards, are also provided by the AC power source. Comparing the results presented in Table I, it can be observed that the highest power factor values are obtained, as expected, with the resistor emulator behavior, with a THD_I similar to the THD_V of the input voltage; obtaining a power factor similar to the obtained with pure sinusoidal grid voltage. On the other hand, with the new proposal, the current harmonics are lower (above all 3^{rd}

TABLE I
EXPERIMENTAL RESULTS UNDER DISTORTED LINE VOLTAGE

	V_{PCC} $[V]$	I_{PQE} $[A]$	P^{in}_{PQE} $[W]$	f $[Hz]$	THD V_{PCC} [%]	THD I_{PQE} [%]
Resistance behavior (traditional PFC controller approach)						
Fig. 8.a	226.2	3.64	820	50	12	11.5
Fig. 9.a	117.3	2.85	329	60	12	10.8
Fig. 10.a	225.5	3.6	800.9	400	12	11.33
Sinusoidal input current						
Fig. 8.b	226.1	3.7	823	50	12	4.2
Fig. 9.b	117.3	2.88	329	60	12	3.4
Fig. 10.b	225.5	3.6	800	400	12	2.93

and 5^{th} harmonics) than the voltage ones and therefore the THD_I is also lower than the THD_V.

Fig. 8.a and 8.b show the voltage and current waveforms of the PQE PFC in resistor emulator and sinusoidal current modes respectively at $50\ Hz$. In resistor emulator mode the current waveform is proportional to the voltage one and, hence, current harmonics (the blue bars in Fig. 8.c) will generate voltage harmonics at the PCC due to Z_g in Fig. 1. By changing the operation mode to sinusoidal current one, the THD_I reduces from $11.5\ \%$ to $4.2\ \%$ and the current waveform in Fig. 8.b is almost sinusoidal but the zero crossing. Since the EPQ PFC active power is almost constant ($\approx\ 820\ W$) in both operation modes, the fundamental input current must increase to compensate for the active power transferred by the current harmonics in the resistor emulator mode.

The proposed PQE PFC performance has also been evaluated in $60\ Hz$ EPS, as it is shown in Fig. 9.a and 9.b. The results are similar to the $50\ Hz$ case. Input current ripple is higher because the DC output voltage is intentionally lower in these tests to verify that the PQE controller performance does not depend on the output voltage level. As it is shown in Fig. 9.c, the input current spectra in both operation modes follow the behavior observed in the $50\ Hz$ case.

Finally, in order to show the applicability of this approach to airplane EPS, the PQE PFC has been connected to a $400\ Hz$ grid voltage and the obtained results are shown in Fig. 10. Again, the performance of the PQE PFC is consistent with the previous cases (Fig. 10.c). The results of all the cases are summarized in Table I.

The lower distortion observed as the line frequency increases is a consequence of the applied technique without current sensor [46]. This technique compensates for the current estimation errors acquired around the zero line crossing and therefore the accumulated error during half the line period becomes lower as the line frequency increases.

V. CONCLUSION

The consequence on the electrical power quality of connecting household appliances to the grid through PFC stages has been assessed considering different THD_V scenarios. As has been shown in (17) and (23), there are conditions under which sinusoidal current consumption results in better PF at the PCC than with resistor emulator behavior, commonly assumed to be ideal for PFC stages. A modification of the carrier signal of NLC controllers applied to PFC stages is designed to impress sinusoidal input current despite the input voltage distortion.

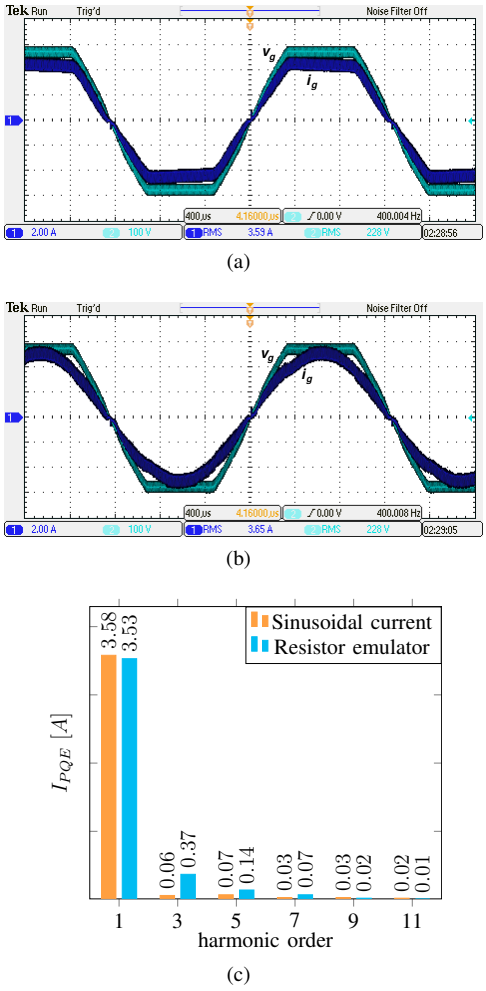

Fig. 10. Experimental results of PQE PFC at $400\ Hz$. Voltage and current waveforms in a) resistor emulator mode ($k = 0$), b) sinusoidal current mode ($k = 1$) and c) measured spectra in both operation modes.

The line current estimation with no interaction with the power stage implements the NLC with high noise immunity. The digital implementation of the non-linear controller is appropriate to define the carrier and to include additional reduction of the current distortion depending on the application. The PQE controller can be applied to mitigate the effect of nonlinear loads within household appliances on residential electrical grids. The operation mode of the digital controller can be autonomously adjusted through the locally measured THD_V, without extra circuitry. The user or a THD_V threshold detection selects the convenient behavior (either resistor emulator or pure sinusoidal current). Experimental results obtained with high THD_V (above $5\ \%$) confirm the feasibility of the PQE controller in both sinusoidal current and resistive emulator modes.

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