POWER ROUTER BASED ON A FRACTIONALLY-RATED BACK-TO-BACK (FR-BTB) CONVERTER

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POWER ROUTER BASED ON A FRACTIONALLY-RATED BACK-TO-BACK (FR-BTB) CONVERTER

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To

my parents,

Vani and Prakasa Rao Kandula.

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LIST OF ABBREVIATIONS

PR	Power router
VAR	Volt-ampere reactive
FR-BTB	Fractionally-rated back-to-back
LTC	Load tap changing
FACTS	Flexible alternating-current transmission systems
UPFC	Unified power-flow controller
BTB	Back-to-back converter
VSC	Voltage source converter
CNT	Controllable network transformer
CEF	Controlled energy flows
RPS	Renewable portfolio standards
DoE	Department of energy
HVDC	High voltage DC
TSC	Transformer-side converter
LSC	Line-side converter
IPP	Independent power provider

TRANSCO	Transmission company
ISO	Independent system operator
RTO	Regional transmission operator
EPA	Energy policy act
TLR	Transmission loading relief
OTC	Operating transfer capacity
ISO	Independent system operator
NERC	National American electric reliability conference
SVC	Static Variable Compensator
TSR	Thyristor Switched Reactor
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
FC-TCR	Fixed Capacitor-Thyristor Controlled Reactor
STATCOM	Static Synchronous Compensator
GTO	Gate turn-off
TSSC	Thyristor-switched Series Capacitor
SSR	Sub-synchronous resonance
TCSC	Thyristor-controlled Series Capacitor

SSSC	Static Synchronous Series Compensator
SSR	Sub-synchronous resonance
TC-PAR	Thyristor Controlled-Phase Angle Regulator
PAR	Phase-angle regulators
VFT	Variable Frequency Transformer
D-FACTS	Distributed-FACTS
DSSC	Distributed Static Series Compensator
DSI	Distributed Series Impedance
NPC	Neutral point clamped
IGBT	Insulated gate bipolar transistor
SCR	Silicon controlled rectifier
FPGA	Field programmable gate array
DSP	Digital signal processor
SOA	Safe operating area
DSF	Disturbance sensitivity function
ATS	Automatic transfer switch
CVR	Conservation voltage reduction

SUMMARY

The objective of the proposed research is to develop a low-cost power router, capable of dynamic, independent control of active- and reactive-power flows on meshed grids. A power-flow solution with the aforementioned characteristics would enhance electric-grid utilization, leading to thermal and economic efficiency. Increasing load demand and growth of wind generation have significantly increased the stress on the transmission grid. The low investment in transmission infrastructure necessitates adoption of methods for efficient use of existing resources. Power-converter-based flexible alternating-current transmission systems (FACTS), capable of dynamic power-flow control, have been the preferred solution to maximize utilization of existing infrastructure.

Traditional FACTS solutions for power-flow control, such as unified-power-flow controller (UPFC) and back-to-back high-voltage direct-current (BTB HVDC) converter, are based on two unique features. First, a BTB converter forms the core of the power-flow controller. BTB converters based on the voltage-source converter (VSC) technology are commercially available up to 70 kV. But realizing a BTB converter at transmission-level voltages (> 138 kV) requires low-frequency step-down transformers. Also, the DC-link capacitor is typically implemented with electrolytic capacitors to reduce the cost of the converter. The electrolytic capacitor requires frequent maintenance and has a limited lifetime. Because of the large converter, low-frequency transformers, and DC capacitors, building high-power converters at transmission voltages is complex and cost prohibitive. The other essential characteristic of the traditional FACTS solutions is the centralized approach, with a single controller responsible for the entire control range. The centralized approach results in a single point of failure negatively impacting the grid reliability.

Controllable network transformer (CNT), an alternative approach based on direct AC-AC converters, obviates the need for DC capacitors. The CNT based solution reduces the

required rating of low-frequency transformers compared to the traditional FACTS solution. Also, implementation through a fractionally-rated converter provides a low-cost solution. But the practical implementation of CNT is limited by challenges such as reliable commutation, voltage scaling, and lack of freewheeling path, which are yet to be addressed satisfactorily.

The proposed research aims to develop a power router (PR), also called as power-flow controller, that combines the advantages of BTB and CNT while overcoming the limitations of both approaches. The proposed PR consists of a fractionally-rated BTB converter (FR-BTB) connected across the taps of a transformer. A fail-normal switch is connected in shunt with the converter to bypass the converter during faults. The proposed implementation, as in the case of a CNT, reduces the low-frequency transformer requirement compared to traditional FACTS solutions. At the same time, since the converter is based on a standard BTB converter, it avoids the commutation and free-wheeling path issues associated with direct AC-AC converters. The fractionally-rated converter and reduced transformer rating lead to a low-cost solution, while the BTB-based approach ensures a scalable, reliable, and market-ready solution.

As a part of this research, the power-flow-control range of the proposed PR is evaluated. The control architecture of the PR is developed and the criterion for selection of controller parameters is determined. The operation of the proposed PR and the controller design is verified through system simulations. Fault handling of series-connected controllers can have a significant impact on the network reliability. In the proposed research, the coordination between the converter and the fail-normal switch, for reliable operation under different types of faults, is analyzed through simulation studies. System-level studies for determining the feasibility, rating, and location of power routers will need reduced-order power-router models. As a part of this research, small-signal and frequency-domain models of the proposed PR are developed. Also, the functionality of the proposed PR is experimentally demonstrated at 13 kV, 1 MW.

The concept of controlled energy flows (CEFs) was introduced to lower the cost of accommodating the variability of stochastic renewable-energy sources and ensure the benefits of transmission investment to the investor. Implementation of the CEF concept, based on power routing through a given path, will require small power routers to be installed on multiple transmission lines, which can be short, medium, and long. In comparison, traditional FACTS devices are implemented only on long tie-lines, which require large control range. Even for tie-line solutions, a distributed solution, consisting of multiple power routers connected in series, will provide higher availability and flexibility compared to a centralized solution. But mutual interactions between multiple power routers, located in an electrically-close region, can lead to network instability. A controller design, to ensure stable operation of multiple power routers, is presented and verified through simulations.

Achievement of the research objectives will provide a reliable and economical solution for independent, dynamic control of active- and reactive-power flows. Through optimum utilization of the existing electric grid, the resulting technology can reduce required transmission investment and facilitate cost-effective integration of wind generation.

CHAPTER 1

INTRODUCTION

1.1 Problem Statement and Background

An electric transmission grid is an extensive, interconnected network of high-voltage power lines that transport electricity from generators to consumers. In the United States (U.S.), the electric transmission grid is almost 125 years old and presently consists of about 372,340 miles of lines [9]. In earlier years, transmission lines were isolated and radial in nature, with each consumer group serviced by not more than a single generating unit. But with the start of the regulation era in 1934, the electric utilities joined together under a vertically-integrated monopoly to share the peak load and backup power. The interconnection of utilities led to meshed systems that provided reliability, allowing utilities to provide service even under contingencies to an extent. The deregulation in 1990s resulted in a complex system of independent power providers (IPPs), transmission companies (TRANSCOs), independent system operators (ISOs), regional transmission organizations (RTOs), and retailers. IPPs sell the service to retailers through the transmission network, owned and operated by TRANSCOs. ISOs and RTOs are independent regulators, responsible for ensuring non-discriminatory services, and safe and reliable operation of the grid. With deregulation, the economics of the electric grid dominated the physics of the grid, pushing the grid towards an unsustainable state. A few of the problems associated with the present day electric grid are discussed here.

1.1.1 Increasing Electrical Load

The electrical energy delivered through the transmission networks has been increasing at about 2% per year for the last two decades, as shown in Figure 1.1. It increased from 2800 TWH in 1990 to 4000 TWH in 2010 and is expected to reach 4400

TWH by 2030 [1]. The electrical-energy demand is driven primarily by consumption growth in residential and commercial sectors [2, 3]. The growth in the residential sector is because of the population and economic growth, and continued population shifts to warmer regions with greater cooling requirements. The growth in the commercial sector is driven by the increasing demand from service sectors. Penetration of electric vehicles is not sufficient to reverse the slowing trend of electrical-energy demand in the transportation sector [3]. The electrical-energy demand of the industrial sector increases by only three percent from 2008 to 2035 because of the efficiency gains and the slow growth in industrial production.

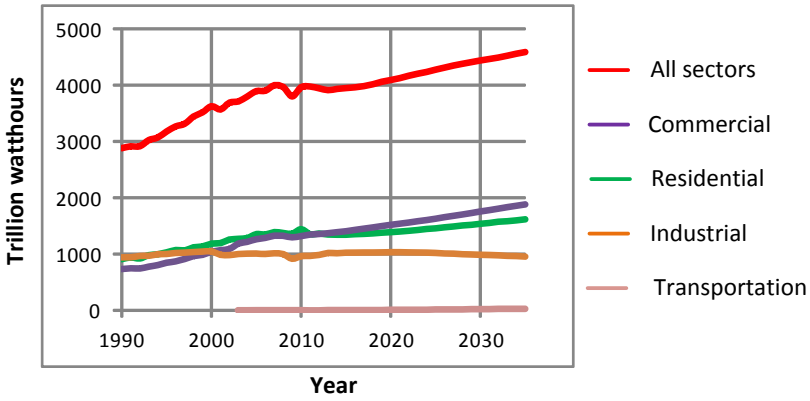


Figure 1.1: Electrical energy delivered through the electric-power sector. (Projected data: 2010-2035).

1.1.2 Increasing Renewable Energy

Renewable-energy sources provided about 13% of the total U.S. utility-scale electric energy generation, in 2011. Wind energy is the second largest contributor of the total renewable generation, with 23%. The growth of wind energy in the electric-power sector in the last 20 years and the projected growth till 2035 is shown in Figure 1.2 [4, 5]. Wind-energy generation increased from 6 TWh in 2000 to 120 TWh in 2011. Increase of wind-energy generation is driven by renewable portfolio standards (RPS). As of May 2012, 29 states have enacted the RPS programs that resulted in creation of one-third of the current U.S. non-hydro renewable electricity. A number of states without the RPS policies have also seen a significant increase in renewable generation because of federal incentives,

state programs, and market conditions [6]. Wind energy is expected to reach about 30% of the total renewable energy and 12% of the total energy sources by 2035 [4].

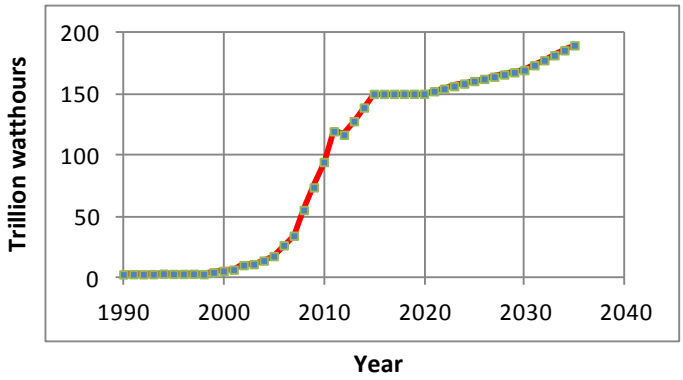
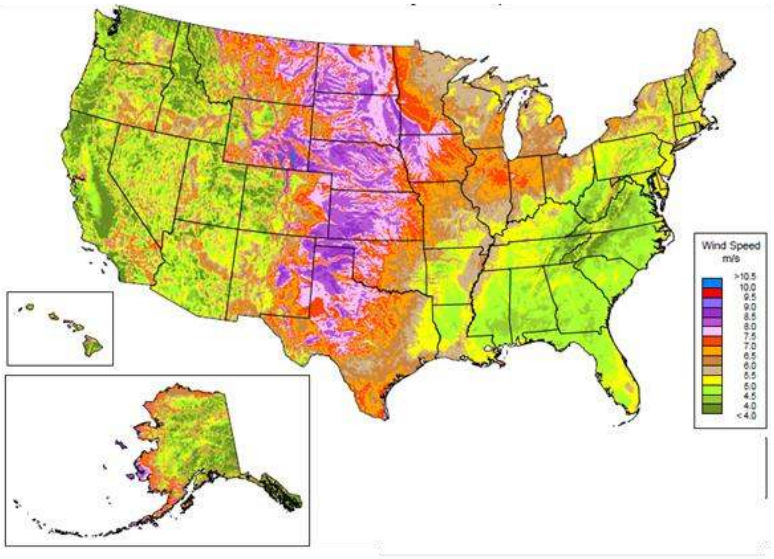


Figure 1.2: Wind energy delivered through the electric-power sector. (Projected data: 2011-2035).

Wind-energy integration will require a capable transmission system to deliver the energy from the generation centers to the load centers. As of 2012, most of the wind generation was installed in locations where there has been adequate transmission capacity to deliver the wind energy to the loads [7]. In Figure 1.3, the potential wind resources in U.S. [8] and wind generation installed as of 2012 [9] are shown. Wind potential, shown in Figure 1.3(a), matches with installed locations, shown in Figure 1.3(b), where there has been adequate transmission capacity to interconnect the new wind generators and deliver their electricity to loads [7]. A number of published reports indicate that a large number of wind projects are held up due to the lack of transmission infrastructure [7, 10, 11].

(a)



(b)

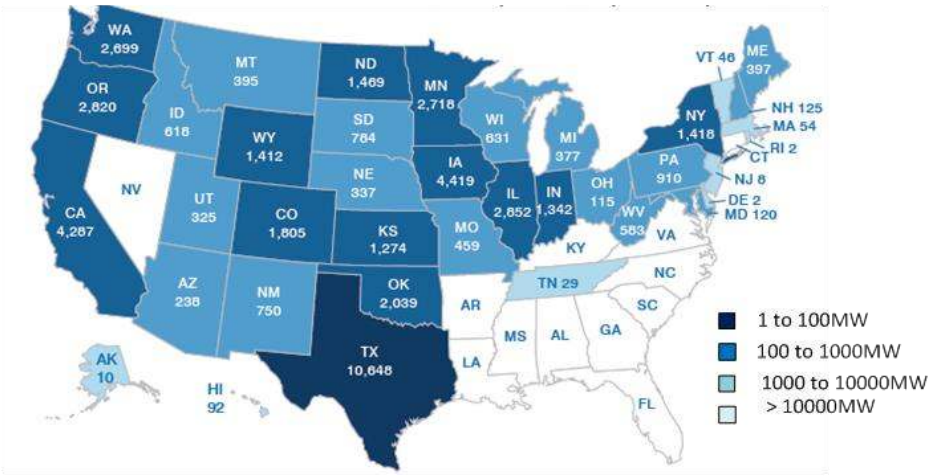


Figure 1.3: (a) Wind resources and (b) wind installed-generation in US.

1.1.3 Investment in Transmission Infrastructure

After two decades of low investments, the investment in the electric transmission sector has increased in the last decade. For the period 1988-2010, the comparison of the investment in the transmission lines [12, 13] and the investment in the generating sector [1] is shown in Figure 1.4. Fuelled by the load growth, there was a bump in the investment in the generating capacity during 2000-2005. After 2005, the investment in the generating sector slowed down and much of the investment started flowing into the transmission sector.

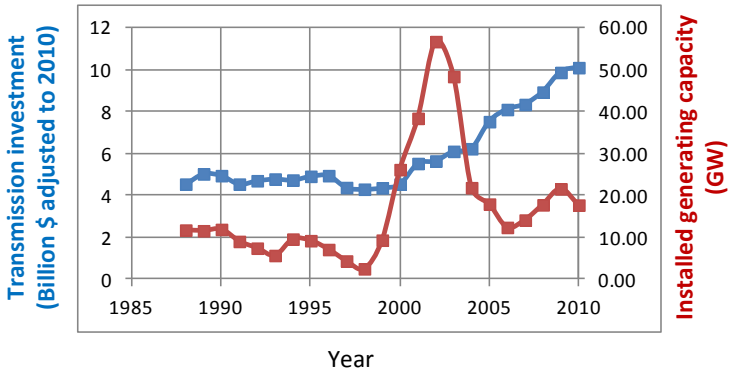


Figure 1.4: Historical investment in the transmission lines (> 100 kV) and generating capacity.

The major support for the transmission investment came from the Energy Policy Act (EPA) of 2005 and federal transmission-pricing policies [13]. The investment in transmission sector is expected to add 30,000 circuit-miles of transmission lines over the period 2010-2017, in addition to the existing capacity of 372,340 circuit-miles as of 2009, as shown in Figure 1.5[1]. It is primarily driven by reliability concerns and for facilitating renewable integration, as shown in Figure 1.6 [14].

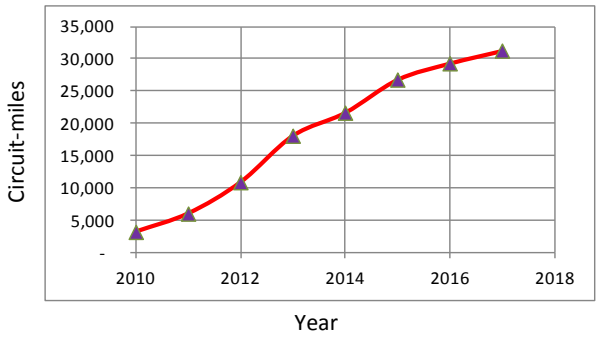


Figure 1.5: Expected addition to the transmission capacity.

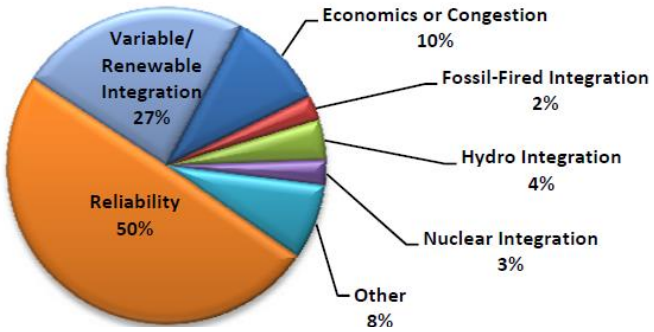


Figure 1.6: Drivers for growth in transmission capacity.

Though transmission additions are increasing, they are not sufficient yet. The Brattle Group estimates that $298 billion transmission investment is needed between 2010 and 2030 to maintain reliable service [15]. Another study indicates an investment need of $55 billion over the period 2013-2025, just to meet the existing RPS mandates [15]. The requirement increases to $100 billion if a hypothetical 20% federal RPS mandates are considered [16]. But the planned investment is only approximately $56 billion for the period 20011-2015 [17]. A large number of transmission projects are being delayed because of right of way, cost allocation, and other environmental issues [18].

1.1.4 Network Congestion

Congestion occurs on electric transmission facilities when actual or scheduled flows of electricity across a line or a piece of equipment are restricted below desired levels [7]. These restrictions may be imposed either by the physical or electrical capacity of the line, or by operational restrictions created and enforced to protect the security and reliability of the grid. Because power purchasers typically try to buy the least expensive energy available, when transmission constraints limit the amount of energy that can be delivered into the desired load center or exported from a generation-rich area, these constraints (and the associated congestion) impose real economic costs upon energy consumers.

There are number of commonly used metrics for determining congestion and are region dependent [7]. The metric for eastern interconnection is the number of Transmission Loading Relief (TLR) issued in an area, while for western interconnection it is the number of lines operating above Operating Transfer Capacity (OTC). A TLR is a NERC developed procedure for a transmission operator when a transmission path is at or beyond the operating limits [7]. TLRs have five levels depending on the severity of congestion, with the 5^{th} level being the most critical state requiring major generation rescheduling. OTC is defined as the amount of power that can be transferred in a reliable

manner, meeting all NERC contingency requirements, considering the current or projected operational state of the system.

The history of TLRs logged by the transmission operators for the last decade is shown in Figure 1.7(a) [19]. The increasing number of TLRs, indicating increasing congestion, has a growing pattern from 1998 to 2008, and then starts decreasing. The decreasing trend is because of various initiatives by the transmission operators such as building new transmission lines, moderate economic growth, new generation close to the load centers, demand side management and others. [20]. Still, level 5 TLRs, shown in Figure 1.7(b), are increasing every year indicating the need for efforts to contain congestion. Similarly, in the western interconnection the number of lines operating above OTC has reduced in the last 8 years, as shown in Figure 1.8. But, this does not give the complete picture as only 23 major paths are considered for analysis. As of 2009, DOE has identified a number of congested areas that are not reflected in this figure [7].

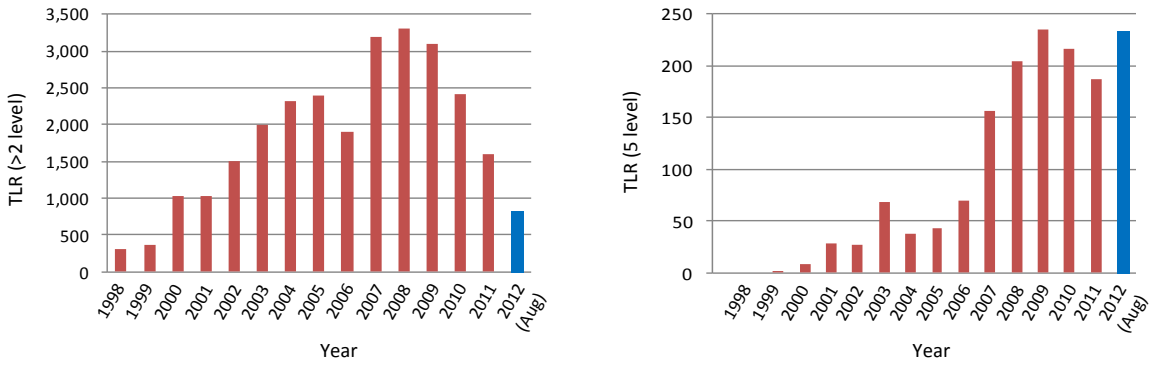


Figure 1.7: Number of logged TLRs in the eastern interconnection.

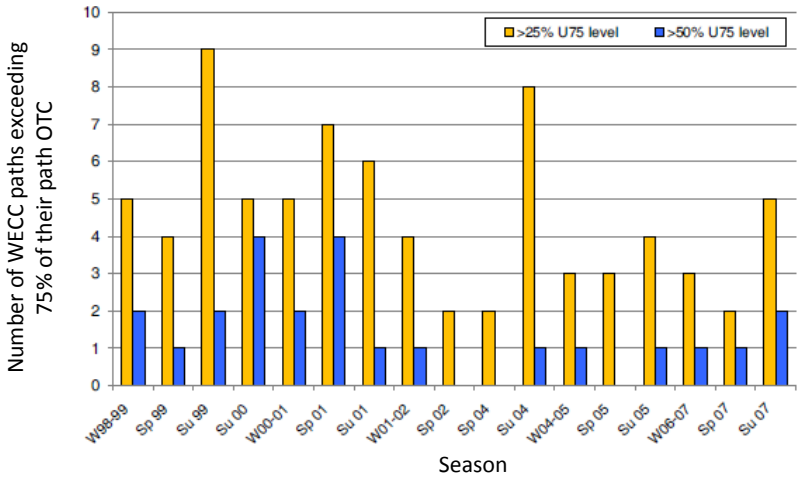


Figure 1.8: Path utilization trend in western interconnection, US.

1.1.5 Efficient Utilization of Existing Transmission Grid

Considering the uncertainties in the development of the transmission infrastructure, it is necessary to adopt methods for efficient utilization of existing grid. Besides demand-side management, distributed generation, and energy efficiency, DOE also advocates the use of high-impact advanced technologies to address transmission bottlenecks [21]. The high-impact technologies include flexible alternating-current transmission systems (FACTS), high-temperature superconductor cable, and superconducting magnetic energy storage. Among various solutions, FACTS have reached technological maturity [22], but are hampered by high installation and maintenance costs. Recent advances in semiconductor technology and reducing prices of switching devices have rekindled interest in FACTS technologies. FACTS together with wide-area measurement systems (WAMS) can enable better control of electricity over existing lines [23].

Capability of FACTS devices for relieving congested networks and reducing energy price for consumers is discussed in large number of publications. Studies discussing the technical aspects are mainly related to the algorithms for choosing optimal location and ratings of FACTS devices [24-26]. Application of FACTS devices, specifically, for alleviating wind-penetration related congestion while satisfying transient stability constraints, is also shown [27-29]. Economic aspects such as cost allocation for FACTS

devices [30] and overall economic gains, accrued as a result of reduced generation from conventional generators and reduced congestion costs [31-36], are also discussed.

Recently, the concept of controlled energy flows (CEFs) based on delivering energy from source to destination along a desired path is proposed [37-39]. Implementation of CEFs will require a power-flow controller at each of the intersecting node along the designated path, as shown in Figure 1.9.

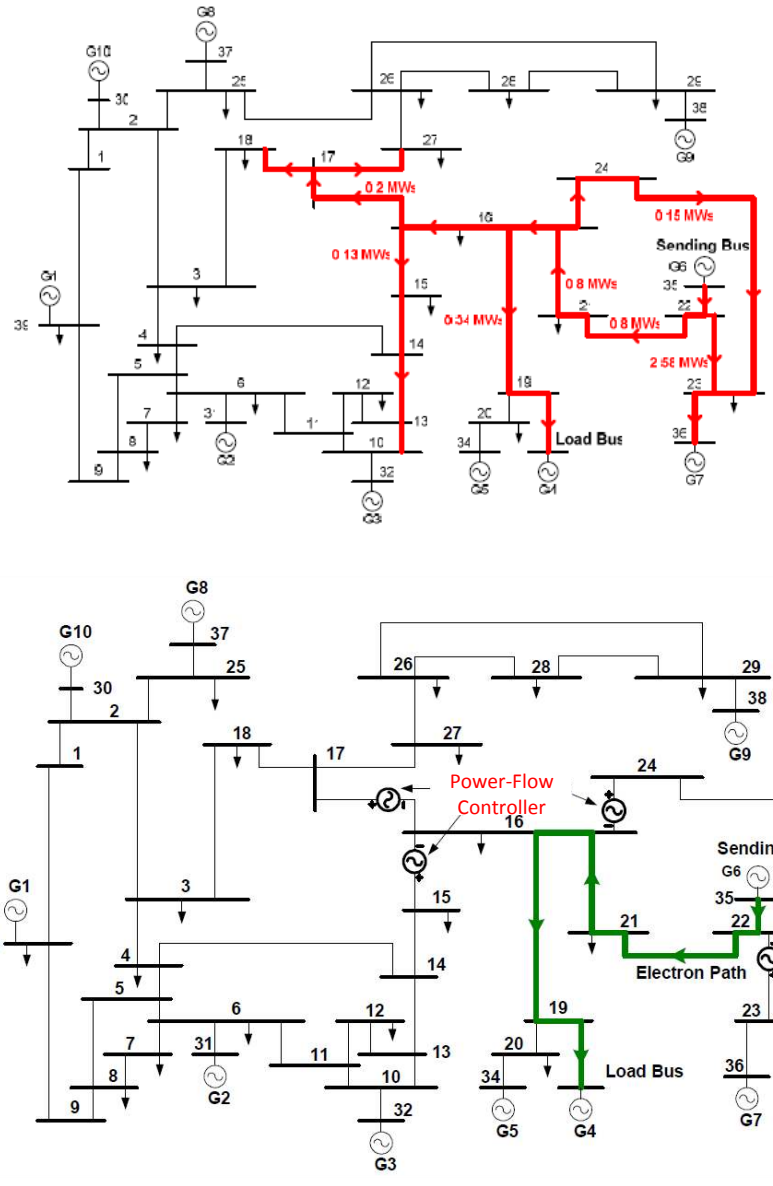


Figure 1.9: Line flows associated with dispatch of 3.4 MW from Gen 6 to load bus (a) without CEF and (b) with CEF [37].

The power-flow controller will inject an incremental voltage to direct the flow of electrons along the desired path. The required control effort is only a fraction of the total controlled power [37]. The same concept can be extended to multiple transactions using the superposition principle. CEF concept relieves congestion through improved asset utilization and can create a parallel market for renewable generation, providing higher returns on investment [38].

Implementation of power-flow control, for relieving congestion by enabling efficient utilization of infrastructure, will need a cost-effective and reliable power-flow controller.

1.2 Research Scope

This research presents a low-cost power router (PR) for meshed systems, which is capable of dynamic, independent control of active- and reactive-power flows. The proposed PR consists of a fractionally-rated, back-to-back converter (FR-BTB) connected across the taps of a transformer. A fail-normal switch is connected in shunt with the converter to bypass the converter during faults. The proposed implementation provides a cost effective solution compared to traditional power-routing solutions. The fractionally-rated converter and the reduced transformer rating lead to a low-cost solution, while the standard BTB-based approach ensures a scalable, reliable, and market-ready solution. Implementation of the power-flow control to alleviate congestion may require multiple PRs installed on the network. But mutual interactions between multiple PRs can lead to network instability. The research aims to develop a controller design to ensure stable operation of multiple power routers.

The primary objectives of this research are:

1. To present operating principle, various possible configurations and control range of the proposed power router.
2. To present control architecture that is necessary to achieve power flow control with the proposed power router.

3. To verify the control algorithm through simulation and low power prototype.
4. To develop small-signal and frequency-domain models from basic time domain equations.
5. To identify various fault modes and develop a protection system for realible operation of the proposed power router.
6. To verify the proposed protection scheme through simulation studies.
7. To analytically evaluate the reason for intercations between multiple power routers.
8. To develop controller design that can ensure stable operation of multiple power routers and verify through system level studies.
9. To develop a full-scale 13 kV, 1 MVA prototype and validate the proposed power router functionality.

1.3 Outline of Chapters

Chapter 2 will review various existing technologies for implementation of power-routers. The features and shortcomings of various power routers are presented, explaining the need for a need a better power-routing solution.

Chapter 3 will introduce the proposed power-routing solution for meshed systems. The detailed power-router configuration, various possible implementations and salient features of the power router are presented. The operating principle, control range and control architecture are presented. The verification of the control scheme through simulations and low power prototype is presented. Small-signal and frequency-domain modles of the proposed power router are derived.

Chapter 4 will discuss the fault management aspects of the proposed power-router. Various fault modes are identified and a protection scheme to avoid single point-of-failure is presented. In this chapter, the simulation results for verification of the protection scheme are discussed.

Chapter 5 introduces the problem of interactions between multiple power routers, which may lead to instability. An analytical method to analyze stability of a system with multiple power routers is presented and verified. Controller-design conditions to ensure stable operation of multiple power routers are proposed and verified on a IEEE 39-bus system through simulation studies.

Chapter 5 presents the various possible applications and associated challenges of the power router in distribution systems.

Chapter 7 presents the work performed to demonstrate the power router functionality at 13 kV, 1 MVA. The design of the test setup, selection of various components and fabrication of the power router is discussed. The experiment results at 13 kV, 1 MVA, validating the power router functionality are presented.

Chapter 8 delineates the contributions, presents suggestions for future work, and summarizes the research.

CHAPTER 2

PRIOR ART

FACTS are power-electronic based systems capable of controlling one or more transmission parameters. They were developed as an alternative to slow moving mechanical power-flow controllers to provide fast response and increased availability [40]. The biggest advantage of FACTS is that the base technology is similar to HVDC, where converters up to the rating of 3.0 GVA, +/- 500kV are commercially built [41]. Though the FACTS technology has reached a stage of maturity, the market penetration has not reached expected levels. This section reviews various FACTS devices for power-flow control, enumerating the advantages and limitations of each technology.

2.1 Power-flow Controllers

Consider a simplified two-bus system connected through a loss-less transmission line, as shown in Figure 2.1. The power-flow in the line is given by Equations (1)-(3).

$$P = \frac{V_1 * V_2}{X} \sin\delta\,, \tag{1}$$

$$Q_s = \frac{V_1}{X}(V_1 - V_2 * \cos\delta)\,, \tag{2}$$

$$Q_r = \frac{V_2}{X}(V_2 - V_1 * \cos\delta)\,, \tag{3}$$

where P is the active power, Q_s is the sending-end reactive power, Q_r is the receiving-end reactive power, V_1 is the sending-end voltage, V_2 is the receiving-end voltage, X is the line impedance, and δ is the phase angle between V_1 and V_2.

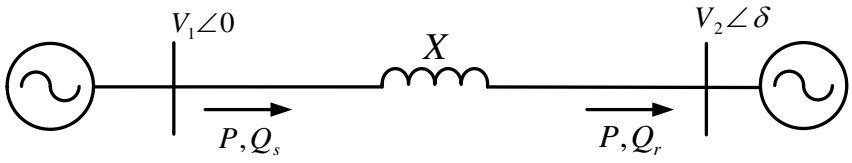


Figure 2.1: Simplified two-bus system.

From Equation (1), it is evident that the active power can be controlled by varying one or more of the following three parameters: line voltage, impedance, and phase angle. Power-flow controllers can be classified based on the parameter the device can control [40].

- Shunt controllers – control line voltage.
- Series controllers – control effective line impedance and/or phase angle.
- Combined series and shunt controllers – control line impedance, phase angle and line voltage.

2.1.1 Shunt Controllers

In principle, shunt controllers inject current at the point of interconnection with the primary objective of providing voltage support. From Equation (1), it can be seen that any increase in bus voltage directly impacts the power flow. But regulations limit the line-voltage variation to +/- 10% of the nominal voltage. Hence, shunt controllers cannot provide a greater degree of active-power-flow control. Also, any attempt to vary the active-power flow through shunt compensation is associated with an even greater change in reactive-power flow. Though shunt compensation is ineffective for active-power-flow control, it can improve the power-transfer capability of a transmission line. Midpoint shunt compensation can double the power-transfer capability [42]. With midpoint voltage, V, controlled to be the same as sending- and receiving-end voltages, the new active-power-flow equation, P, is given by Equations (4).

$$P = \frac{2V^2}{X}\sin\frac{\delta}{2}. \tag{4}$$

Comparing Equation (4) with Equation (1) indicates that with midpoint compensation the maximum active-power flow has doubled. Similarly, further line segmentation, achieved by applying shunt compensation at appropriate points, can further increase

power-transfer capability. With sufficient dynamic control, shunt compensation can also aid in improving transient stability and power-oscillation damping [40].

Fixed shunt capacitors/reactors can be used to provide the required shunt compensation, but because of the adverse response at non-nominal loading levels, switched capacitors/reactors are preferred. Mechanically switched capacitors/reactors have slow response, and hence lack dynamic control, limiting the additional power transfer capability that can be achieved. FACTS technology, by providing a faster response time and continuous control, has enabled realizing the full potential of shunt compensation. FACTS devices for shunt compensation are mainly divided into two categories. The controllers in the first category are commonly termed as Static Variable Compensator (SVC), based on semiconductor devices with no forced turnoff capability. Devices such as Thyristor Switched Reactor (TSR), Thyristor Controlled Reactor (TCR), Thyristor Switched Capacitor (TSC), and Fixed Capacitor-Thyristor Controlled Reactor (FC-TCR) come under this category. The second category consists of static converter based controllers, based on switches with forced turnoff capability, such as a Static Synchronous Compensator (STATCOM).

2.1.1.1 Static Voltage Compensator (SVC)

SVC is usually implemented as a combination of one or more of the following: TSR, TCR, TSC, and FC-TCR. A brief introduction of each of these devices is given below.

TCR, as shown in Figure 2.2 (a), consists of a reactor connected in shunt with the line through a bi-directional switch, realized by two anti-parallel thyristors. By controlling the thyristor firing delay angle, defined as the angle between the instant of crest voltage and the instant of thyristor, the effective inductive impedance can be varied. The operating region of a practical TCR is shown in Figure 2.2 (b), with the boundaries determined by the ratings of the thyristor and the reactor. TCR can only provide inductive compensation and the maximum compensation is voltage dependent.

Thyristor switching introduces unwanted odd harmonics in the system, the significant being the 3rd, 5th, 7th and 9th. Usually, the triple-n harmonic currents are blocked from the system by employing a delta connected TCR, and a 12-pulse arrangement is employed to eliminate 5th and 9th harmonics. Because the thyristor turns off only when the current decays to zero naturally, the response time of a 3-ph TCR cannot be smaller than T/3, T being the time period of the fundamental frequency. If the firing angle of the TCR is fixed, usually at 0 deg, then it is termed as Thyristor Switched Reactor (TSR). TSR does not introduce any harmonics but can only provide on/off control.

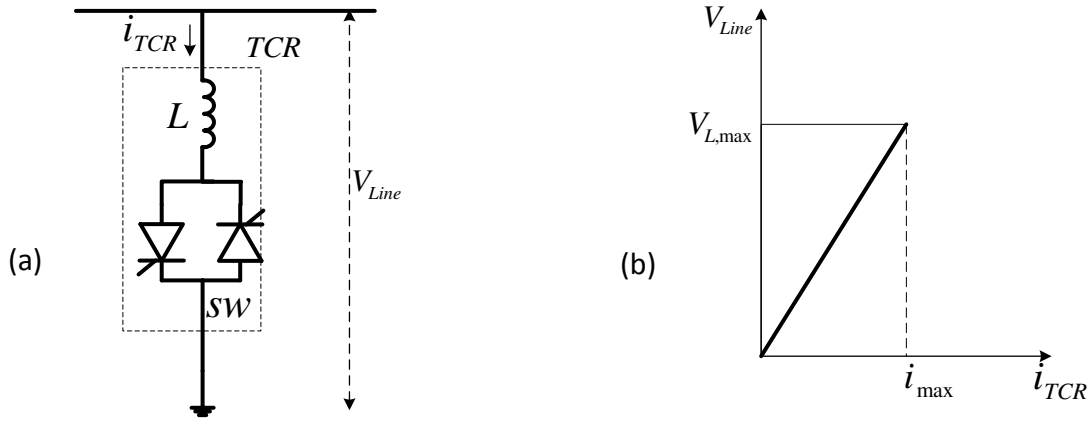


Figure 2.2: (a) Schematic of TCR. (b) V-I characteristics of TCR

TSC, shown in Figure 2.3(a), consists of a capacitor connected in shunt with the line through a thyristor. A small reactor is also connected in series to limit the surge currents during transients. To limit the transients, the capacitor can be switched on only at a particular instant in a cycle when the voltage across the switch is zero. Hence, firing delay angle control is not possible with TSC. Since a single TSC module can only provide fixed step control, a number of TSCs are connected in parallel to approximate continuous control. Typical V-I characteristics of a TSC are shown in Figure 2.3(b).

FC-TCR, shown in Figure 2.4(a), consists of a fixed capacitor connected in shunt with a TCR. The capacitor provides the fixed part of the compensation while the TCR provides the variable component. Typical V-I characteristics of a FC-TCR are shown in

Figure 2.4(b). The capacitor, while providing the compensation at fundamental frequency, will also act as a filter for the dominant harmonics generated by the thyristor switching in the TCR. Though FC-TCR can provide continuous capacitive and inductive VAR control, the presence of TCR limits the dynamic response time to one third of a cycle. Also, the thyristor switching introduces undesirable harmonics in the system.

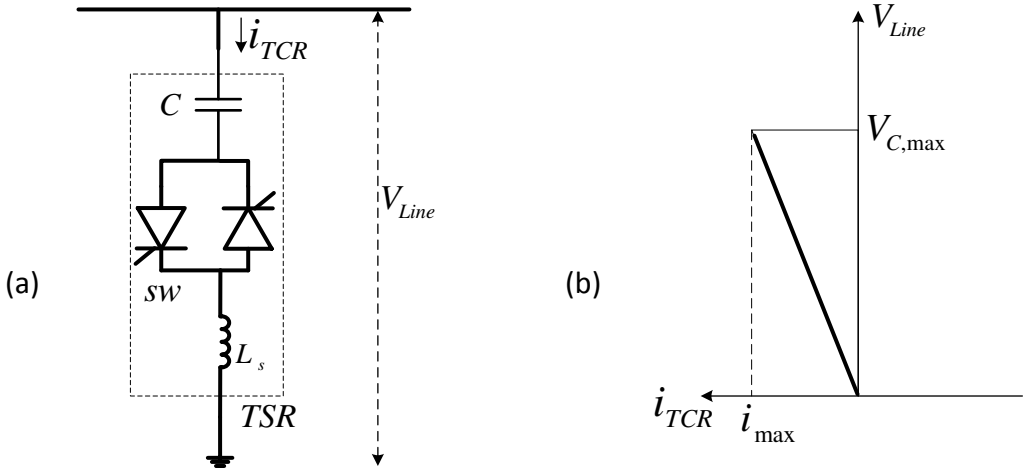


Figure 2.3: (a) Schematic of TSC. (b) V-I characteristics of TSC.

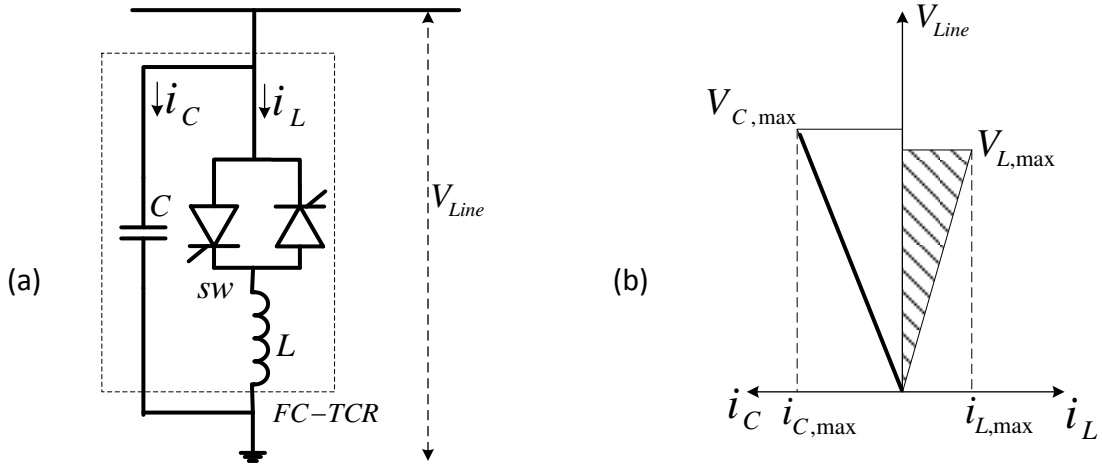


Figure 2.4: (a) Typical implementation of FC-TCR. (b) V-I characteristics of FC-TCR.

SVC, commercially available since 1974 for industrial applications, is the popular device among FACTS devices. For power system applications, the first installation in U.S. was a 40 MVAR SVC, installed in 1978 at Shannon substation [43]. In the next 10

years, 41 compensators with an installed capacity of 9710 MVAR have been added to the transmission system [43]. Photograph of 500 kV, -145/+575 MVAR at Rawlings, Maryland, one of the largest SVC installed, is shown in Figure 2.5.

Figure 2.5: 500 kV, -145/+575 MVAR at Rawlings, Maryland, U.S. (Courtesy: ABB)

2.1.1.2 STATCOM

Gyugyi introduced the concept of using switching converters for reactive power control, in 1976. Static Synchronous Compensator (STATCOM) is one such device based on the principle of generating reactive power by circulating currents in the phases through a switching converter. As shown in Figure 2.6 (a), it consists of a Voltage Source Converter (VSC) connected in shunt with the line through a relatively small reactance (0.1-0.15 p.u.). On the input side of the converter is a DC capacitor, essential to maintain the equality of the instantaneous input and output powers. The converter is usually an array of semiconductor switches with forced turnoff capability (GTO thyristors or IGBTs).

STATCOM, much like a synchronous generator, operates by generating a voltage in phase with the line. By controlling the magnitude of the in-phase voltage, the reactive current can either be generated (capacitive) or absorbed (inductive). As shown in Figure 2.6 (b), that the reactive power generated by STATCOM is not voltage dependent, an

advantage over SVC. Also, STATCOM has much faster response time than SVC, as both the turn-on and turn-off instants of the switches can be controlled in STATCOM, while only turn-on instant is controllable in SVC.

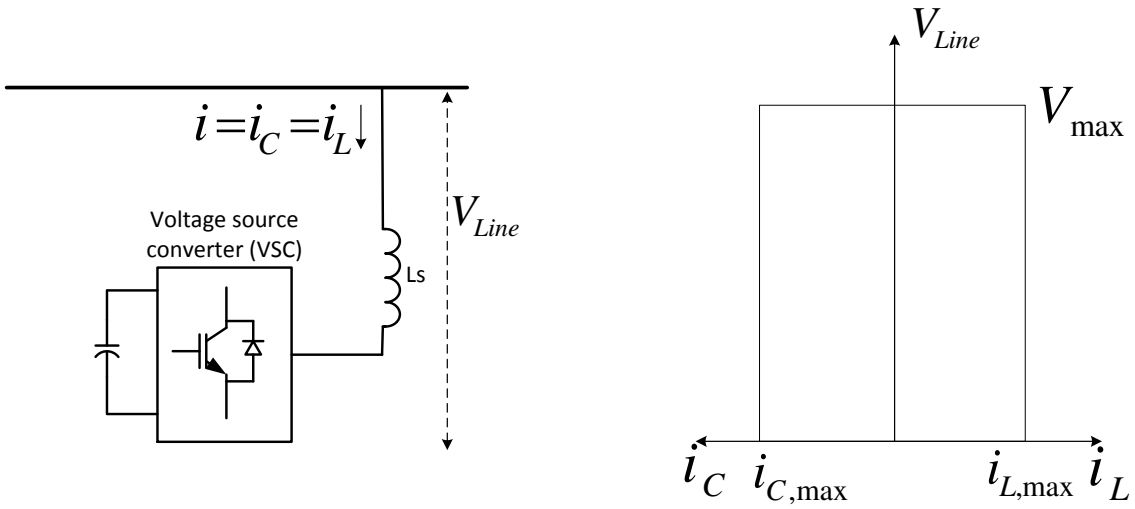


Figure 2.6: (a) Schematic of STATCOM. (b) V-I characteristics of STATCOM.

The first STATCOM in U.S. was a +/- 100 MVAR installation at Sullivan substation of Tennessee Valley Authority (TVA), in 1995, for regulating the 161 kV bus voltage [44]. Other prominent U.S. installations are as follows: +/- 86 MVAR, 115kV STATCOM at Essex substation, in 2001 [45]; +/- 100 MVAR STACOM at Talega, in 2002 ; the +/- 95 MVAR STATCOM at Holly substation in 2004, shown in Figure 2.7.

The improvement of power transfer capability by providing shunt compensation through SVC and STATCOM has been proved in practice. But, as mentioned in the introduction for shunt controllers, shunt compensation is ineffective for controlling the active power-flow. Still, in active power-flow control applications, shunt controllers are used along with series controllers to provide the requisite reactive power support.

Figure 2.7: 138 kV, +/- 95 MVAR STATCOM at Holly substation, U.S. (Courtesy: ABB)

2.1.2 Series Controllers

Series controllers are of two types: variable-impedance and phase-angle controllers. In principle, both types of series controllers inject a series voltage to control the line current. The transmission line impedance is usually very low (0.001-0.002 pu per mile) and so is the voltage drop across the line. Hence, a small voltage injected by the series controller can have a significant impact on the line current. It also implies that the volt-ampere (VA) rating of the series controller would only be a small fraction of the throughput power rating of the line.

The series-voltage injection can be either in-phase or out-of-phase (quadrature) or both. As shown in Figure 2.8(a), the quadrature-voltage injection (V_{series}) has a significant impact on the active-power flow. Phase-angle controllers control the active power directly by injecting quadrature voltage. Variable-impedance controllers control the line impedance, which effectively implies controlling the magnitude of the voltage drop across the uncompensated line as shown in Figure 2.8(b). Variable-impedance controllers have no controllability at zero phase-angle. Typical variable-impedance controllers are thyristor-switched series capacitor, thyristor-controlled series capacitor, and static synchronous series compensator, while phase-angle regulator is a phase-angle controller.

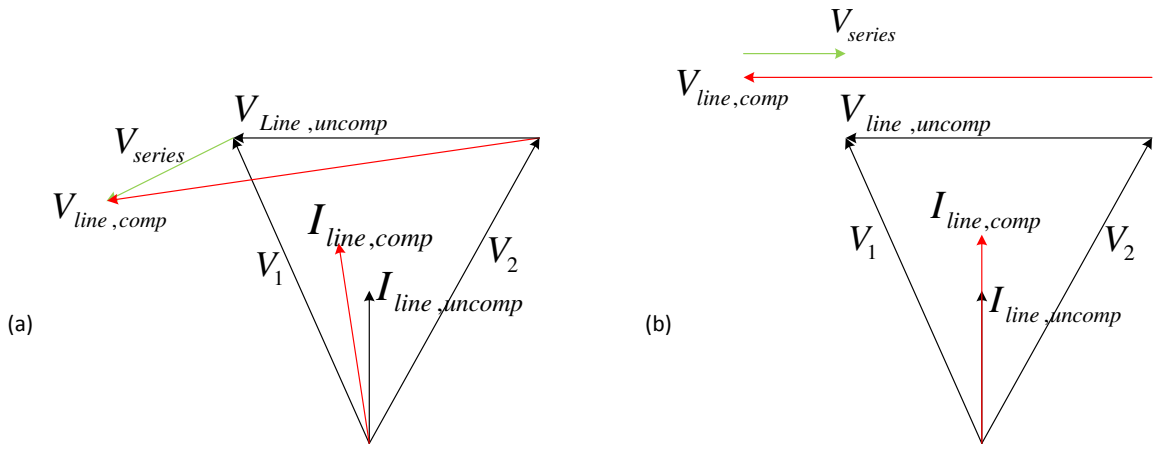


Figure 2.8: Phasor diagram for compensation of (a) Phase-angle type compensators and (b) Impedance type compensators.

2.1.2.1 Thyristor-switched Series Capacitor (TSSC)

The concept of variable series compensation was first proposed as a means to improve transient stability [46]. Implementation of variable capacitance through thyristor-switched capacitors was later introduced by Karady, in 1991 [47]. A typical implementation of a TSSC is shown in Figure 2.9, and it consists of a string of switched capacitors in series, each one added or bypassed by an anti-parallel thyristor in shunt. The capacitive impedance is varied by switching the capacitors.

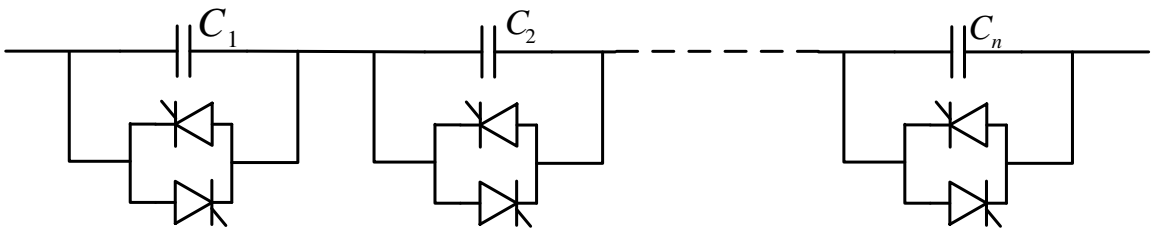


Figure 2.9: A typical implementation of TSSC.

TSSC can be operated either in voltage compensation mode or in impedance compensation mode. Typical V-I characteristics of TSSC in voltage compensation mode and impedance compensation mode are shown in Figure 2.10(a) and Figure 2.10(b), respectively [48]. The operation in either mode is differentiated by the value of line current (I_{min}, I_{max}) at which the maximum compensation is provided. Any further increase in current will result in reduced compensation.

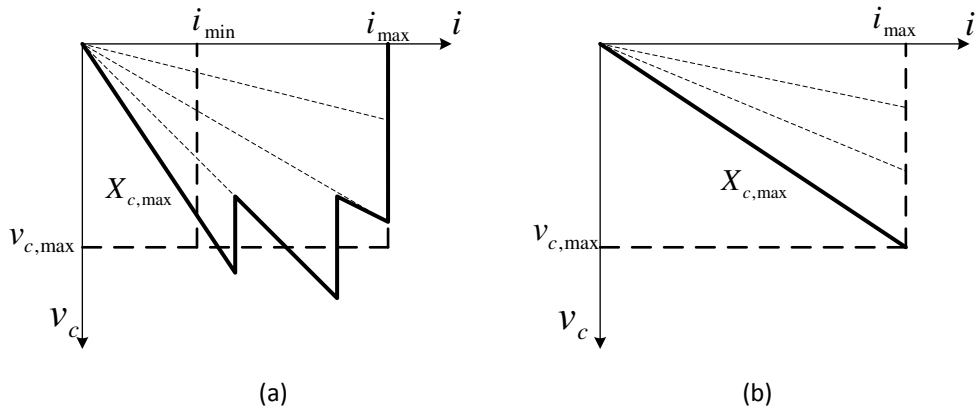


Figure 2.10: V-I characteristics of TSSC [48]. (a) Voltage compensation mode. (b) Impedance compensation mode

The only known TSSC installation was on a 345 kV transmission line, at Kanawa River Substation in West Virginia, U.S. [49]. Essentially an experiment to the test the TSSC hardware, a thyristor valve was applied across one phase of a capacitor module. Siemens installed a number of thyristor-protected series capacitors (TPSC) worldwide [50]. The TPSC technology is available up to 500 kV and 400 MVAR. TPSC is structurally similar to TSSC, but the thyristor is switched on only to bypass the capacitor during faults.

The TSSC can only add capacitive impedance to the line in discrete steps. Also, the capacitor can be inserted only at the zero-current crossing, where the thyristor naturally turns off. The capacitor can only be bypassed at the capacitor-voltage zero-crossing to avoid initial surge currents in the valve. The thyristor-switching constraints limit the minimum response time to one fundamental cycle, making it ineffective for mitigating sub-synchronous resonance (SSR) at higher frequencies [48]. In practical conditions, an inductor in series with the thyristor is required to address the $\frac{di}{dt}$ limitations of the thyristor. The use of the TSSC was limited because of the above mentioned limitations.

2.1.2.2 Thyristor-controlled Series Capacitor (TCSC)

Thyristor-based implementation of continuously-variable series impedance, known as TCSC, was proposed in 1986 by Vithayathil et al. [51]. A typical implementation and operating characteristics of the TCSC are shown in Figure 2.11. As shown in Figure 2.11 (a), the TCSC consists of a series capacitor in shunt with a thyristor-controlled reactor (TCR). To obtain variable impedance, the TCR is controlled by varying the thyristor firing-angle. The compensation provided by TCSC is given by the Equation (5).

$$X_{TCSC}(\alpha) = \frac{X_C X_L(\alpha)}{X_L(\alpha) - X_C}, \tag{5}$$

where $X_L \leq X_L(\alpha) \geq \infty$, $X_L(\alpha)$ is the effective inductive impedance of the TCR, $X_L$is the impedance of the inductor, X_c is the impedance of the capacitor, and α is the thyristor firing-angle. Typically, the ratio X_L/X_c is in the range of 0.1-0.3 [48]. X_L is small to provide a low impedance path for surge currents during faults. As shown in Figure 2.11(b), the operation is prohibited over a small range of α to avoid resonance.

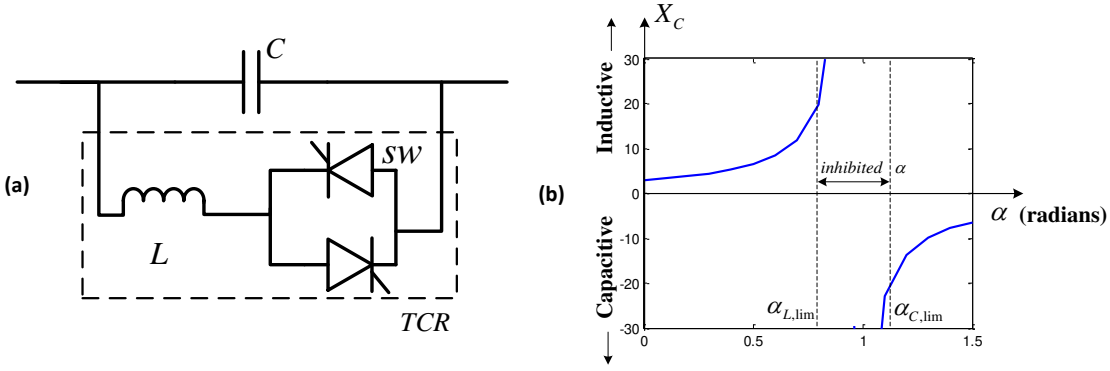


Figure 2.11 (a) Typical implementation and (b) operating characteristics of TCSC.

Like TSSC, TCSC can be operated in either voltage compensation mode or impedance compensation mode. The V-I characteristics for either modes are shown in Figure 2.12[3]. Unlike TSSC, TCSC can provide continuous control in both inductive and capacitive regions.

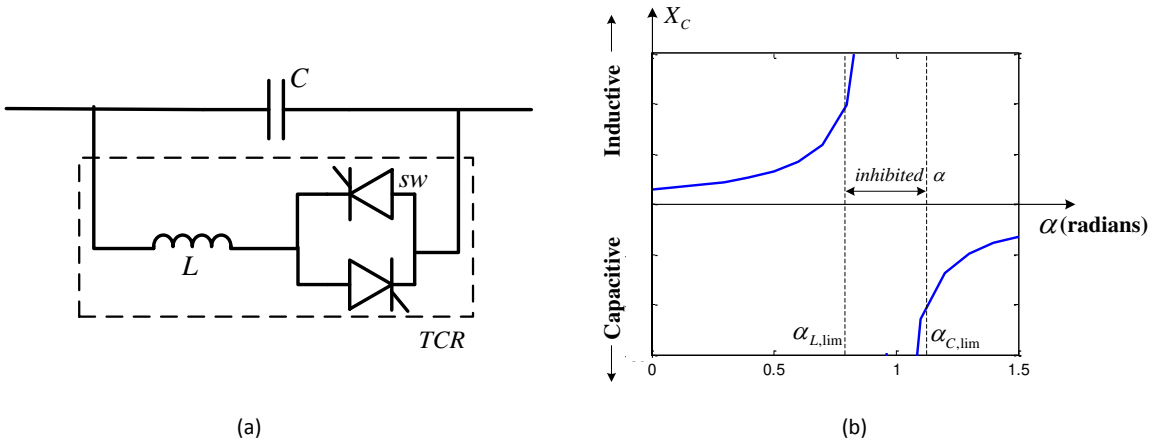


Figure 2.12: (a) Schematic of TCSC. (b) TCSC compensation as a function of thyristor firing delay angle.

The world's first three-phase TCSC was installed at Kayenta substation, Arizona, USA in 1990, with the objective of improving the power-transfer capability of the transmission system [48]. The picture of the 230 kV, 100 MVA TCSC at Kayneta is shown in Figure 2.13. Also, a 202 MVAR TCSC system in U.S. was installed on the 500 kV Bonneville Power Administration (BPA) transmission system, in 1993 [52, 53]. The 440 MVAR TCSC at Purnea-Gorakhpur, India is the largest installation in the world [54].

Figure 2.13: Image of 230 kV, 330 MVAR TCSC at Kayenta, U.S. (Courtesy: ABB).

The TCSC cannot provide independent control of active- and reactive-power flows. The uncontrolled reactive power can lead to additional line losses and also limit the power transfer capability. Because of these limitations, the application of TCSC, in majority of cases, is restricted for damping the SSR caused by fixed series capacitors.

2.1.2.3 Static Synchronous Series Compensator (SSSC)

SSSC is based on the concept of synchronous voltage sources [55]. A typical implementation and V-I characteristics of an SSSC are shown in Figure 2.14. As shown in Figure 2.14(a), a typical implementation of an SSSC consists of a VSC connected in series with the transmission line through a series coupling transformer [56]. It can provide continuous, dynamic, capacitive- and inductive-impedance control, as shown in Figure 2.14(b).

An SSSC will act as a capacitor only at fundamental frequency, and at all other frequencies only the leakage inductance of the series transformer is presented to line. Hence, the SSSC inherently does not ignite any SSR [56], and additionally it can provide damping for SSR caused by other capacitors on the line. The SSSC can also compensate for the real part of the line impedance by inducing a voltage in phase with the line current. Compensation of the real part of the line impedance will involve exchange of active power with the line, and hence the need for an energy source/sink

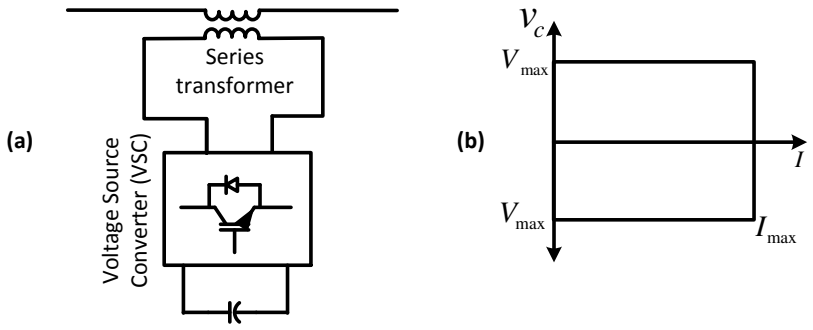


Figure 2.14: (a) Schematic and (b) operating characteristics of SSSC.

An SSSC with an energy source/sink can provide dynamic, independent control of active- and reactive-power flows. But realizing a separate energy source/sink is not economically viable, and hence there are no standalone implementations of SSSC till date. The SSSC is usually implemented as a part of UPFC, where the energy is sourced from the line through a shunt converter [57, 58].

2.1.2.4 Thyristor Controlled-Phase Angle Regulator (TC-PAR)

Phase-angle regulators (PARs) are being used for static power-flow control since 1930s [59]. As shown in Figure 2.15, a typical implementation of a PAR consists of an exciter unit and a regulator unit. The exciter unit is a shunt transformer, with the primary connected between the line and the neutral. The regulator unit is a series transformer, with the primary connected to the secondary of the exciter unit in such a way that it is effectively connected across the line-to-line voltage. The regulator unit injects a quadrature voltage by appropriate selection of line-to-line voltages. The power flow in the line is controlled by varying the series-voltage injection through the taps on the secondary.

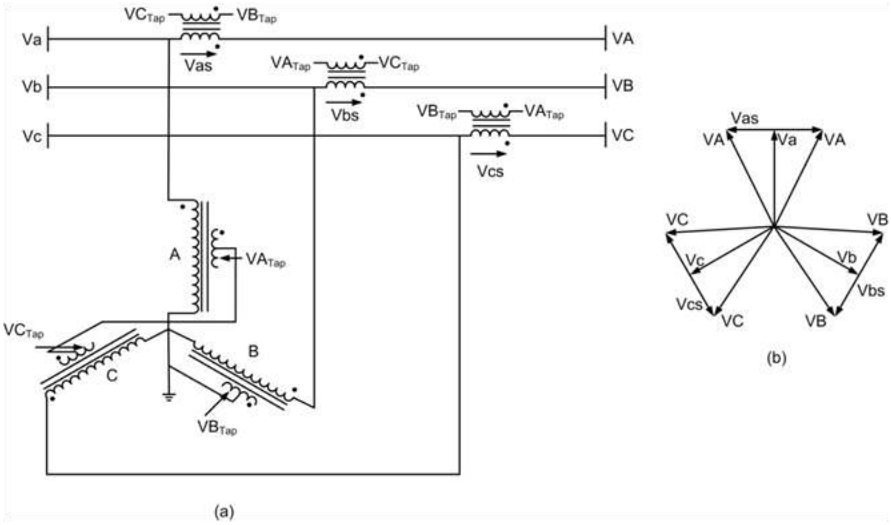


Figure 2.15: Schematic and phasor diagram of phase-angle regulator [59].

TC-PAR is an implementation of the PAR with the mechanical contacts replaced by thyristors [60, 61]. In a simple and direct approach, the thyristors directly replace the mechanical switches. But this approach can only provide step control and requires eight thyristors per phase [62]. In another approach, the thyristors are controlled to achieve continuous control, but the thyristor control generates undesirable harmonics. Inherently, a TC-PAR cannot provide independent control of active- and reactive-power flows. Also, the inter-phase coupling can lead to challenges with respect to fault identification [59].

The quadrature voltage injected by the TC-PAR interacts with the line current resulting in exchange of reactive power with the grid. Since the TC-PAR cannot source/sink the requisite reactive power, a separate shunt volt-ampere-reactive (VAR) source has to be used in conjunction. So far, there are no practical implementations of the high-power TC-PAR because of the above mentioned limitations.

2.1.2.5 Variable Frequency Transformer (VFT)

VFT is essentially a continuously variable phase shifting transformer that can operate at an adjustable phase angle [63]. As shown in Figure 2.16, VFT consists of a rotary transformer with three phase windings on both rotor and stator. One power grid is connected to the rotor side of the VFT and another power grid is connected to the stator side of the VFT. Power transfer through the rotary transformer is a function of the torque applied to the rotor by a drive motor. The rotor inherently orients itself to follow the phase angle difference imposed by the two asynchronous systems, and will rotate continuously if the grids are at different frequencies. The VFT is designed to continuously regulate power-flow with drifting frequencies on both grids. Reactive power-flow through the VFT is determined by the series impedance of the rotary transformer and the difference in magnitude of voltages on the two sides.

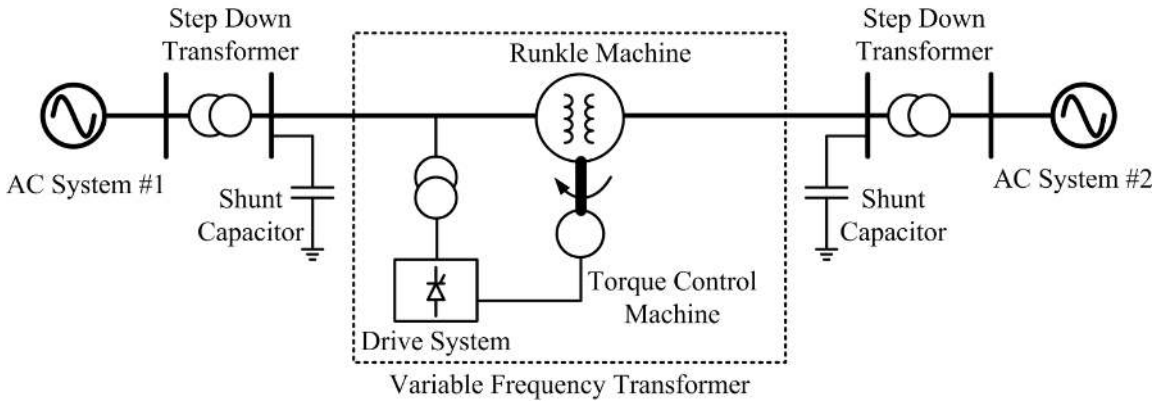


Figure 2.16: Schematic of variable frequency transformer [64].

The VFT has the advantage that, unlike power electronic alternatives, it produces no harmonics and does not cause undesirable interactions with neighboring generators or other equipment on the grid. On the other hand, the VFT being essentially a slow rotating transformer has a very large time constant of the order of 1-2 seconds. The transformer of the VFT has to be rated for full system power and also has to handle the worst case fault current. Since the rotor of the VFT has to be designed for rotational motion, it is difficult to achieve high reliability. The design of VFT becomes complicated and expensive for power levels exceeding 100 MVA, requiring multiple VFTs in parallel for higher power ratings. Till date, there are three VFT installations: 100 MW, Hydro Quebec Langlois, Canada-USA, in 2004 [65], picture shown in Figure 2.17; 100 MW, AEP Laredo, Mexico-Texas, in 2007 [66]; and 300 MW (3 units), Linden, New Jersey–New York, U.S., in 2009 [64].

Figure 2.17: Image of 100 MW VFT at Langlois, Canada-USA. (Courtesy: GE)

2.1.3 Combined Series-Shunt Controllers

Combined series-shunt controllers are capable of providing both series and shunt compensation for independent control of active- and reactive- power flows.

2.1.3.1 Unified Power-flow Controller (UPFC)

UPFC, proposed in 1992 by Gyugi et al. [67], is an effective implementation to achieve the combined functionality of a STATCOM and an SSSC. A typical implementation of a UPFC consists of two VSCs connected back-to-back, as shown in Figure 2.18 [68]. The series inverter provides the basic functionality of the UPFC by injecting a series voltage, and thereby controlling the power flow in the line. The injected voltage can be of any phase and magnitude, limited only by the rating of the converter. Thus, a UPFC can provide independent control of active - and reactive-power flows [68]. The series voltage injection results in exchange of active power between the series inverter and the transmission line. The shunt inverter is controlled to compensate the active power exchanged by the series inverter. In addition, the shunt inverter can also act as a shunt compensator to provide VAR support.

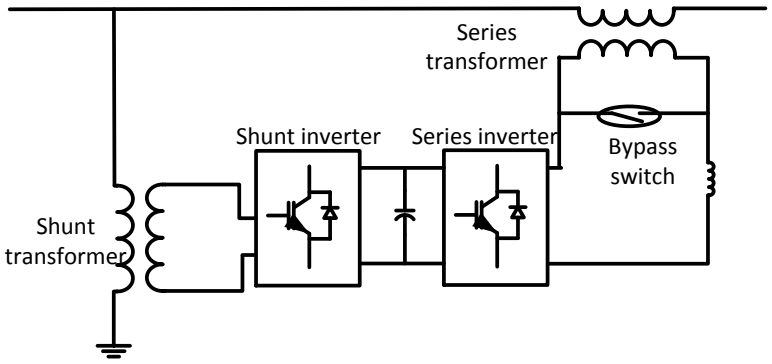


Figure 2.18: Schematic of UPFC.

The first UPFC is installed in 1998, at Inez substation in eastern Kentucky, U.S. [57]. A picture of the Inez UPFC is shown in Figure 2.19. In Inez UPFC, the series and the shunt inverters are rated for 160 MVA each and the DC bus is at 24 kV. To enable operation at 138 kV, both the inverters are connected to the line through step-up transformers, rated for 160 MVA. A set of 80 MVA intermediate transformers are used to achieve harmonic cancellation. A large converter and a number of low-frequency transformers resulted in an expensive implementation. The converter is rated for 2.0 p.u., the intermediate transformers are rated for 0.5 p.u., and the shunt transformer is rated for

1.0 p.u. To avoid saturation during startup, the series transformer is usually rated for at least 1.5 p.u. [69].

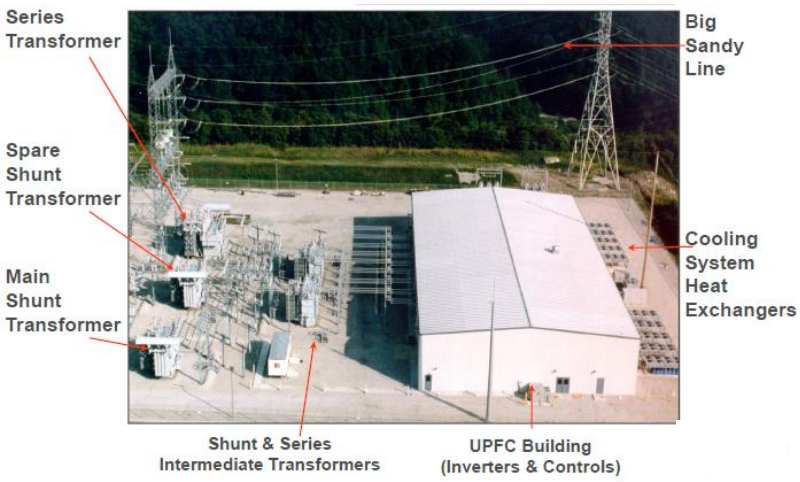


Figure 2.19: Image of 320 MVA UPFC installed at Inez substation, U.S. (Courtesy: Siemens).

A major problem with the UPFC is the fault-current handling. In case of faults, the shunt converter is turned off, but the series converter is kept on to avoid an open secondary on the series transformer. To protect the series converter from fault current, an electronic by-pass switch is connected as shown in Figure 2.18. A small inductor is connected between the series converter and the by-pass switch to avoid shorting the converter. But the inductor reduces the overall capacitive-compensation range. The high cost and the complexity has restricted the wide-scale implementation of the UPFC. Till date, there are only two other installations in the world [58, 70].

2.1.3.2 Back-to-Back High-voltage DC (BTB HVDC)

BTB HVDC system consists of two converters connected next to each other through an energy-storage element. It converts AC power at one terminal to DC and then converts back to AC at the other terminal. The intermediate DC stage allows complete decoupling of the two AC systems. In the VSC-based BTB HVDC systems, a DC capacitor is used for the intermediate DC stage, as shown in Figure 2.20 [71]. Typically, a VSC-based BTB HVDC system is connected in series with the line through coupling transformers to

allow operation at lower DC voltages. The VSC-based BTB HVDC system can provide dynamic bi-directional control of active- and reactive-power flows. Also, it can provide independent reactive-power support at both ends.

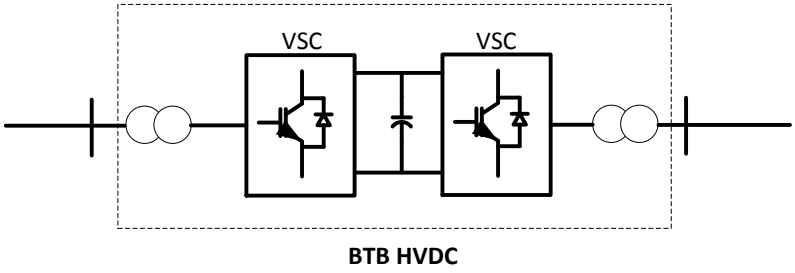


Figure 2.20: Schematic of VSC-based BTB HVDC system.

In U.S., the first VSC-based BTB HVDC system was installed at Eagle Pass substation, in 2001 [71]. The picture of the Eagle Pass BTB HVDC is shown in Figure 2.21. It is a 36 MVA VSC-based BTB tie, interconnecting two power systems to maintain a controlled bi-directional power transfer between them. It also provides reactive-power support for dynamic voltage control at the two ends of the BTB tie. The DC bus is maintained at +/- 15.9 kV. BTB HVDC technology is currently available up to 200 MW, 70 kV [72].

Figure 2.21: Image of BTB HVDC at Eagle Pass, U.S. (Courtesy: ABB)

Traditionally, BTB HVDC systems are used for interconnecting asynchronous systems. Conceptually, a BTB HVDC system can also be used for power-flow control applications in synchronous systems. A BTB HVDC is functionally similar to a UPFC

with 100% series-compensation capability, except the decoupling that only a BTB HVDC can provide. In most applications, the required series compensation is not greater than 20% because of the low line impedance (0.001-0.002 pu/mile). The economics associated with the large DC capacitor, fully rated VSCs, and decoupling transformers have made the BTB HVDC technology unjustifiable for power-flow-control applications in synchronous systems. The BTB HVDC to be installed at Mackinac, Michigan is the only BTB HVDC system for synchronous systems, in U.S. [72]. Even in Mackinac, requirement for islanded operation is the main reason for choosing BTB HVDC technology.

2.1.3.3 Sen Transformer

PAR can provide active power regulation while the Load Tap Changing Transformer (LTC) can provide voltage compensation. A combination of LTC and PAR will be able to provide both the compensations, and one such effective implementation called Sen Transformer has been proposed in 2003 [73]. As shown in Figure 2.22, the Sen Transformer (ST) consists of a three-phase primary winding and nine secondary windings. Among the 9 secondary windings, a1, a2, and a3 are on the same core as phase-A winding; b1, b2, and b3 are on the same core as phase-B; and c1, c2, and c3 are on the same core as phase-C. The phase-A line is connected in series with secondary windings a1, b1, and c1. As shown in the phasor diagram, Figure 2.22(b), the voltages across a1, b1, and c1 are 120 deg apart. By appropriately choosing the taps of the three windings (a1, b1, and c1), any voltage phasor can be derived from the phasor sum of the three voltages. Since both magnitude and phase of the resultant vector can be varied, both voltage and active power compensation can be achieved. Similar explanation holds for the other two phases. Like in case of TC-PAR, the mechanical tap changer can be replaced by electronic switches for dynamic control.

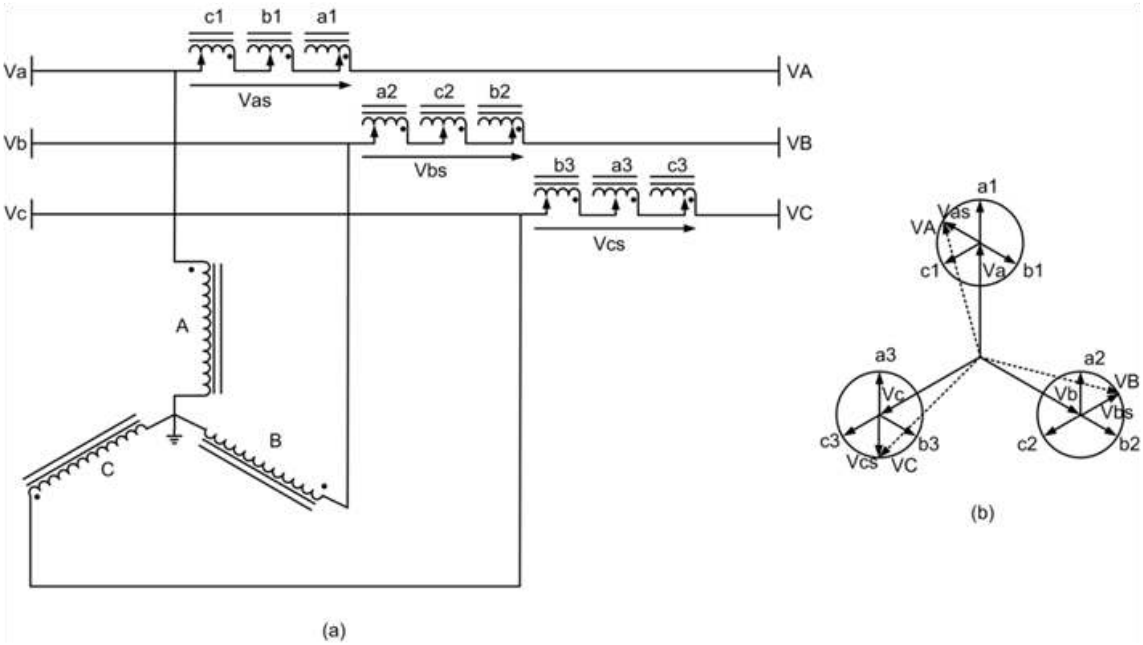


Figure 2.22: Schematic and phasor diagram of Sen Transformer

Sen Transformer is a cost effective and reliable implementation of both LTC and PAR functionality with a single transformer, but it has its own limitations. Each one of the nine secondary windings has to be rated for the line current, and hence, the magnetic rating of the ST has to be at least 2.0 p.u. [69]. The series winding of the ST exchanges active and reactive power with the system because of the interaction of the compensating voltage and the line current. The exchanged power, compensated by the shunt transformer, appears as a load on the system. A separate shunt compensator, such as SVC, is needed to reduce the additional stress on the system [69]. The cost effectiveness of ST is adversely affected by the 2.0 p.u. rating and the need for additional shunt compensation. Also, like in case of a PAR, the inter-phase coupling can lead to challenges with respect to fault identification and isolation. Still, the biggest drawback of the ST is the response time. Even with electronically switched taps, the response time is limited to T/6, T being the fundamental time period. Till date, there are no reported practical implementations of STs in U.S.

2.1.3.4 Direct AC-AC Converters

The concept of direct AC-AC converters was first introduced in [74] but rigorous theoretical analysis was developed by Venturini [75]. Direct AC-AC converter, also called as Matrix converter, is an alternative to three-phase VSC, obviating the need for bulky DC capacitor. As shown in Figure 2.23, it consists of nine switches arranged in rows of three such that any output phase can be connected to any of the input phases at any instant. The switches are controlled to generate voltage of required magnitude, phase, and frequency.

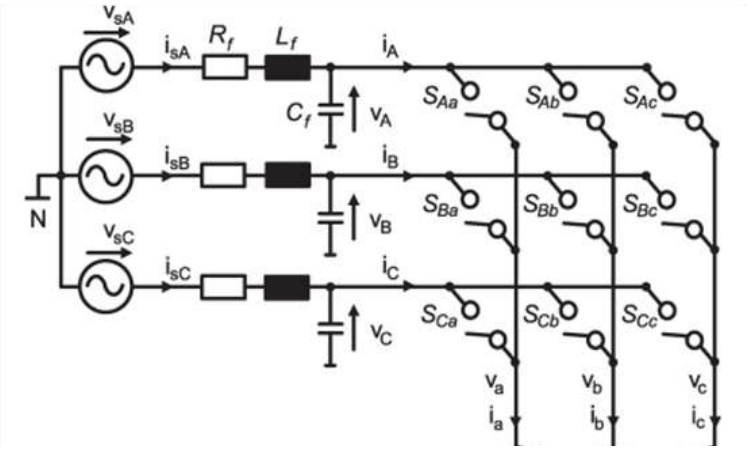


Figure 2.23: Basic schematic of Matrix converter.

The output voltage is limited to 86.6% of the input voltage by the constraint that the peak-to-peak output voltage has to be less than the minimum difference between any two input voltages [76]. Methods have been proposed to fully utilize the input voltage, but are associated with harmonics in both input and output [77]. One of the major issues of Matrix converters is the lack of free-wheeling path. To avoid an open or a short circuit during commutation, a 4-step commutation method was proposed [78] and further improved by a 2-step commutation method [79].

Matrix converters, proposed for power-flow applications, consists of the converter connected in series with line through a set of coupling transformers [80]. It was shown that for 1 p.u. of power-flow control, the converter rating has to be 2.0 p.u., which is

comparable to the BTB based UPFC. Still, the lack of freewheeling path for the fault currents is a major reliability constraint for matrix converters, especially for power-flow applications. Also, like in case of a PAR or a ST, the inter-phase coupling is undesirable, as it can lead to challenges with respect to fault identification and isolation.

2.1.3.5 Controllable Network Transformer (CNT)

The concept of controllable network transformer (CNT) was introduced in 2008 [81]. As shown in Figure 2.24, it consists of a tap-changing transformer augmented by a direct AC-AC converter to provide dynamic vernier control of voltage magnitude and phase angle simultaneously. The direct AC-AC converter, also called as a thin AC-AC converter (TAAC), consists of two AC switches connected to the two transformer taps. The switches can be controlled to connect the line to either of the taps.

The AC-AC converter in a CNT is implemented on per-phase basis to avoid inter-phase coupling. The concept of "Dual Virtual Quadrature Sources" [82] is applied to generate phase-angle control. Within the operating region, a CNT can provide independent control of active and reactive-power flows.

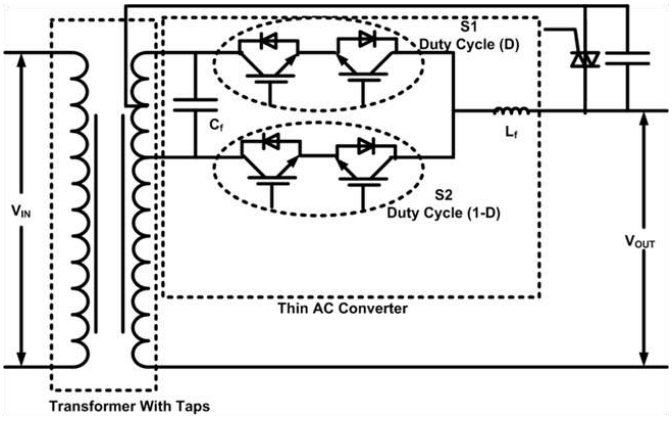


Figure 2.24: Schematic of controllable network transformer (CNT).

The biggest advantage of a CNT is the fractional power rating of the converter. Also, the elimination of DC capacitor implies increased reliability compared to a UPFC. Though the concept of CNT looks promising, it still has the problems associated with

direct AC-AC converters. One of the major issues of direct AC-AC converters is the lack of free-wheeling path. The lack of freewheeling path for the fault currents is a major reliability constraint for power-flow applications. Scaling of direct AC/AC converters for transmission voltages and reliable operation under complex fault modes is yet to be proved in practice.

2.1.4 Distributed Power-Flow Controllers

High costs and reliability concerns have restricted the use of FACTS for power-flow control. The concept of distributed-FACTS (D-FACTS) is introduced as a way to remove these barriers [83]. Two prominent devices under this category are distributed static series compensator (DSSC) and distributed series impedance (DSI).

2.1.4.1 Distributed Static Series Compensator (DSSC)

DSSC consists of multiple modules that attach to the transmission line, achieving power-flow control by varying the line impedance [83]. As shown in Figure 2.25, each DSSC module consists of a single-phase inverter, a single-turn transformer, control block, and communication system. The whole module is either mechanically clamped or suspended from the line and is self-powered.

The principle of power-flow control of a DSCC is similar to that of an SSSC, but the major advantage of the DSSC is the ease of implementation. The single-turn transformer of DSSC overcomes the limitation of series-transformer design for fault current. By choosing an appropriate turns ratio, the current on the converter side, even during faults, can be limited to within the ratings of the semiconductor switches. Also the single-turn transformer aids in saving footprint and isolation requirements. The distributed nature adds sufficient redundancy, improving the reliability and availability.

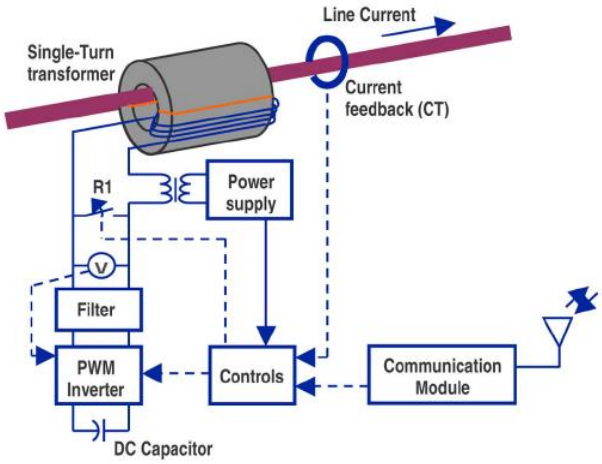


Figure 2.25: Implementation of distributed static series compensator (DSSC) [83].

The DSSC concept has introduced an effective way of implementing distributed controllers, but is limited by lack of independent control of active- and reactive-power flows. Since the module is powered form the line itself, the controller cannot operate at low currents. Also, the DC capacitor in the DSSC has a short life time, requiring frequent replacements. Since the installation cost is a significant component of the total system cost, frequent maintenance may not be cost effective over a long period [84].

2.1.4.2 Distributed Series Impedance (DSI)

As shown in Figure 2.26, a DSI consists of an inductor, a single-turn transformer and an AC capacitor [85]. The AC capacitor has a longer lifetime than a DC capacitor, and hence the DSI is more economically viable than the DSSC. The DSI controls power flow by adding a series impedance, either inductor or capacitor, in series with the line. The electrical characteristics of the DSI are similar to the characteristics of the TCSC. The DSI retains the same advantages as that of the DSSC, in terms of fault current ride-through and reduced isolation requirements. But like the DSSC, the DSI lack independent control of active and reactive powers and cannot operate at low currents.

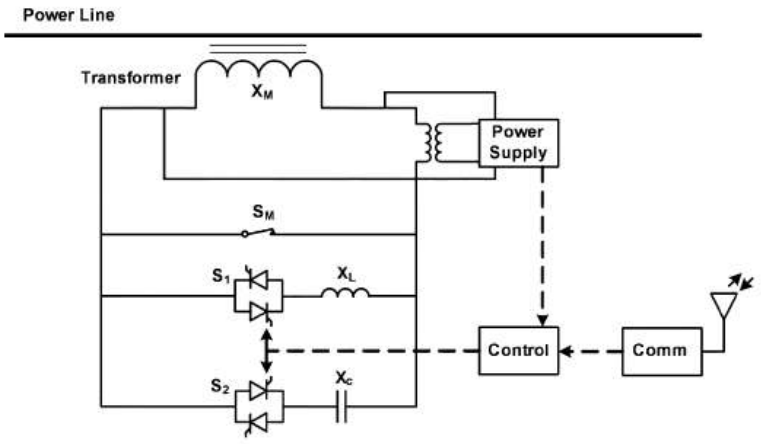


Figure 2.26: Schematic of distributed series impedance (DSI) [85].

2.2 Control of Multiple Power-flow Controllers

The number of FACTS devices on the system is increasing steadily over the years and is expected to increase at a much faster rate with the reducing prices of high-power semiconductor devices. The concept of D-FACTS seems promising and can lead to an even faster increase in the number of controllers on the network [83, 86]. Also, with the advent of faster semiconductor switches, the response time of the FACTS devices is decreasing. With multiple controllers installed on the network, each trying to control the system parameters to achieve its own objective, high-frequency interaction between different controllers can occur.

A possible occurrence of interaction between PARs is reported in [87]. It was shown that, without a carefully designed controller, even slow-responding PARs can counteract each other, leading to instability. With the advent of faster thyristor-based controllers, the issue of multiple-controller interactions at high frequencies is observed. A potential high-frequency interaction between a TCSC and a SVC is reported in [88], and the interaction between multiple SVCs is shown in [89].

Interactions between multiple controllers can be avoided by coordinated controller design, where the control parameters of all the controllers are tuned simultaneously [90]. A test case demonstrating the importance of coordinated controller design of multiple

TCSCs is shown in [91]. Though coordinated controller design is widely used in various system designs, it has its own limitations. The network configuration is not constant, and the controller parameters may not be optimal for all possible configurations. More significantly, with the advent of the concept of D-FACTS, the number of controllers can be large and coordinated controller design can become cumbersome, computationally intensive, and non-viable with constantly changing network conditions.

A simple method for coordinated control of multiple controllers is proposed in [92]. The method was demonstrated with multiple DSIs, but the same can be extended to any D-FACTS controller. In the proposed strategy, each DSI controller internally corrects itself, and controls the rate of injection by looking at the system state at each sampling instant. The self-correcting mechanism allows the controllers to adjust to the system dynamics and obviates the need for communication between controllers. The control strategy is given by Equation (6).

$$u_{exp} = \left(u_{inj} - u_{prev}\right) * \left(1 - exp^{-(t-t_0)}\right) + u_{prev}\,, \tag{6}$$

where $u_{inj} = f\left(I_{line}, I_{line}^{ref}\right)$, u_{exp} is the magnitude of injection for the next step, u_{prev} is the present value of injection, u_{inj} is the reference value for the sampling period, I_{line} is the present value of the line current, and I_{line}^{ref} is the final reference value of the line current. Based on I_{line} and I_{line}^{ref}, u_{inj}, either voltage or impedance in case of DSR, is calculated at the end of each sampling period. Within each sampling period, the controller tries to increase the injection from u_{prev} to u_{inj} in a decaying exponential manner. The decaying exponential approach damps any high-frequency interactions between controllers. Since the controller self-corrects and adjusts the rate of injection at each sampling period, the controller reaches the desired injection asymptotically over time.

The efficacy of the control strategy was demonstrated through simulations [92], but the criterion for selecting the control parameters is not discussed. Hence, there is no basis

to guarantee absolute stability for all system conditions. Ensuring stable operation of multiple controllers is a critical factor for achieving dynamic power-flow control.

2.3 Conclusions

The transmission grid, gradually developed over the last 125 years, is experiencing increasing stress levels. The electrical load increased by 40% in the last two decades and is expected to increase further, driven primarily by the consumption growth in residential and commercial sectors. In contrast, the investment in transmission infrastructure has only recently started. For an estimated requirement of $298 billion between 2010 and 2030, only $55 billion dollars has been planned for the period 2011-2015. A large number of transmission projects are being delayed because of the right of way, cost allocation and other environmental issues. Wind energy has increased dramatically in the past decade and is expected to reach 12% of the total energy delivered by 2035. So far, most of the wind generation is installed in locations with adequate transmission capacity. Further development of wind energy is hampered by the lack of transmission infrastructure. The increasing electrical load and limited transmission investments have led to increased electric-grid congestion. Congestion data from recent years indicate the need for either development of new infrastructure or efficient use of existing resources.

Considering the uncertainties in the development of transmission infrastructure, it is necessary to adopt methods for efficient utilization of the existing grid. Among available high-impact technologies, FACTS have reached technological maturity, but are hampered by high installation and maintenance costs. Recent advances in semiconductor technology and reducing prices of semiconductor switching devices have rekindled the interest in FACTS technologies.

Power-flow controllers, a class of FACTS devices, have been successfully implemented in practical application for relieving congested networks. Thyristor-based series controllers provide dynamic control, which is not possible with mechanically-

switched controllers (MSCs). TSSC is a thyristor-based controller, capable of providing capacitive compensation. Besides an experimental installation, there are no known commercial TSSC installations. TCSC can provide dynamic inductive and capacitive compensation. There are a number of TCSC installations worldwide, but usually it is installed to provide SSR damping. TC-PAR is proposed to improve the response time of a PAR, but there are no utility installations till date. In general, the thyristor-based controllers have faster response time than the MSCs, but the lower limit on response time is still above one-third cycle. Also, the thyristor-switched devices lack continuous control, while the thyristor-controlled devices generate undesirable harmonics. Significantly, TCSC, TSSC, and TC-PAR lack independent control of active and reactive powers.

VSC-based controllers have lower response time than the thyristor-based controllers. UPFC can provide three independent degrees of control: active power, reactive power, and voltage at one bus. But the large converter-rating and high count of low-frequency transformers makes the UPFC an expensive proposition. Till date, there are only three UPFC installations worldwide. SSSC can provide dynamic inductive and capacitive compensation, and with an energy source/sink, it can even provide independent control of active and reactive powers. But realizing a separate energy source/sink is not economically viable. BTB HVDC is the complete power-flow controller, capable of providing four degrees of control: active power, reactive power, and voltages at sending and receiving buses. But, as in the case of UPFC, the large converter rating and low-frequency transformer count has limited the application of BTB HVDC to asynchronous systems. Though VSC-based BTB technology is available up to 70 kV, the cost and the complexity has restricted widespread use of UPFC, SSSC or BTB HVDC. Also, the three-phase implementation can lead to issues with fault identification and isolation.

The CNT-based solution obviates the need for DC capacitors and reduces the required rating of low-frequency transformers compared to a UPFC or a BTB HVDC. Also, the

CTN implementation based on a fractionally-rated AC-AC converter provides a low-cost solution. But reliable commutation and voltage-scaling issues of direct AC-AC converters are yet to be addressed satisfactorily.

Distributed power-flow controllers, such as DSSC and DSI, are shown to be an effective approach for power-flow control. The modular approach enables redundancy, increased availability, and flexibility to adapt to the changing network conditions. The concept of CEFs is shown to be a cost effective method for implementing the RPS mandates. Implementation of either CEFs or distributed power routers will require multiple power routers installed in an electrically-close region. It is shown that the interactions between multiple controllers can lead to instability.

A reliable, cost-effective power router for dynamic, independent control of active and reactive powers is required. Controller design to ensure stable operation of multiple power routers is needed. Achievement of the research objectives will provide a solution for optimum utilization of existing transmission grid, which will reduce the need for immediate investments in transmission infrastructure and facilitate a cost-effective method for implementing the RPS mandates.

CHAPTER 3

PROPOSED POWER ROUTER AND LOW POWER VALIDATION

The objective of the proposed research is to develop a low-cost power router (PR), capable of independent control of active- and reactive-power flows. A power-routing solution with the aforementioned characteristics would enhance electric-grid utilization. In this chapter the basic topology, operating principle, and control architecture are introduced. A comparison of the proposed power router with existing technologies is provided. The simulation and experimental results verifying the PR functionality are presented.

3.1 Topology

The proposed PR consists of a transformer augmented with a fractionally-rated back-to-back (FR-BTB) converter. The single-phase, two-level implementation of the power router is shown in Figure 3.1. The converter is connected across the taps of an autotransformer, typically +/- 10%. A fail-normal switch, realized by two anti-parallel thyristors, is connected across the converter.

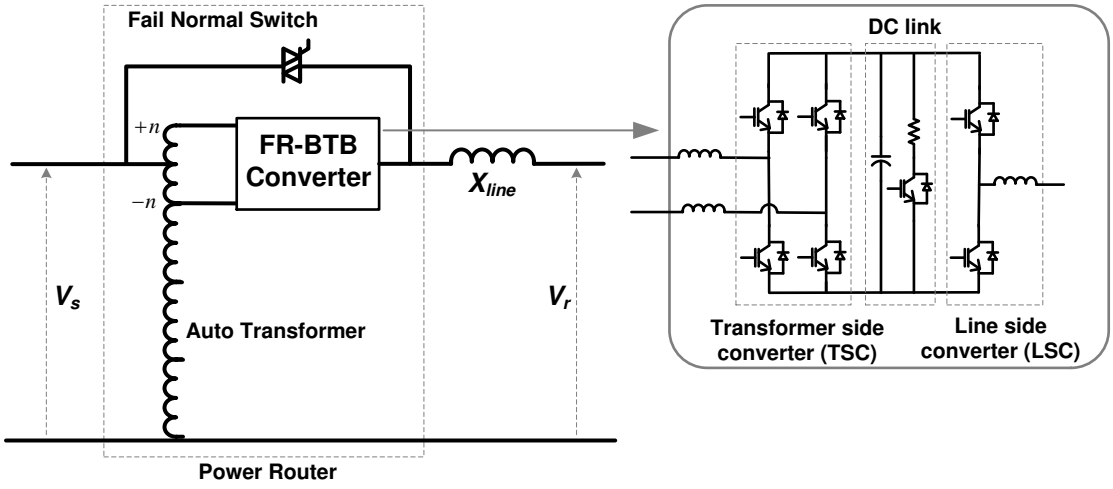


Figure 3.1: Single-phase, two-level implementation of the proposed power router.

The FR-BTB converter consists of a transformer-side converter (TSC) and a line-side converter (LSC), connected through a common DC-link capacitor. The TSC is a full-bridge converter, and the LSC is a half-bridge converter. Hence, the TSC is constructed using two IGBT poles while the LSC is achieved with one IGBT pole. To achieve uniform current ratings across all the poles, the LSC may also be fitted with two poles operating in phase-staggered mode. For retrofit applications, an existing load-tap-changing transformer can be substituted for the autotransformer as shown in Figure 3.2.

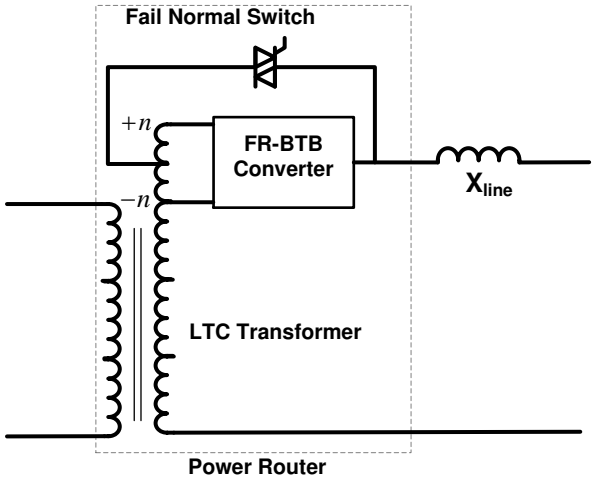


Figure 3.2: Implementation of the proposed system for retrofit applications using LTC transformers.

The main advantage of the proposed converter compared to traditional FACTS solutions is the fractional rating of the BTB converter. The converter rating is only a fraction of the total controlled power, as the switches handle a fraction of the transformer voltage. Typically, as the system power level increases, the line voltage increases proportionately. The FR-BTB configuration has a unique advantage since the converter achieves the fractional rating via fractional voltage rather than fractional current. At very high voltages (>138 kV), where series operation of IGBTs cannot be avoided, the converter can be easily scaled by implementing a multi-level converter. Neutral-point-clamped (NPC) approach is an industry standard to realize multi-level converter because of its advantages in reduced dv/dt, device voltage rating and lower losses compared to a two-level configuration [71]. IGBT-based NPC converter technology is commercially

available up to 150 kV showing ability of series device stack to scale [72]. The three-level NPC implementation of the FR-BTB converter is shown in Figure 3.3.

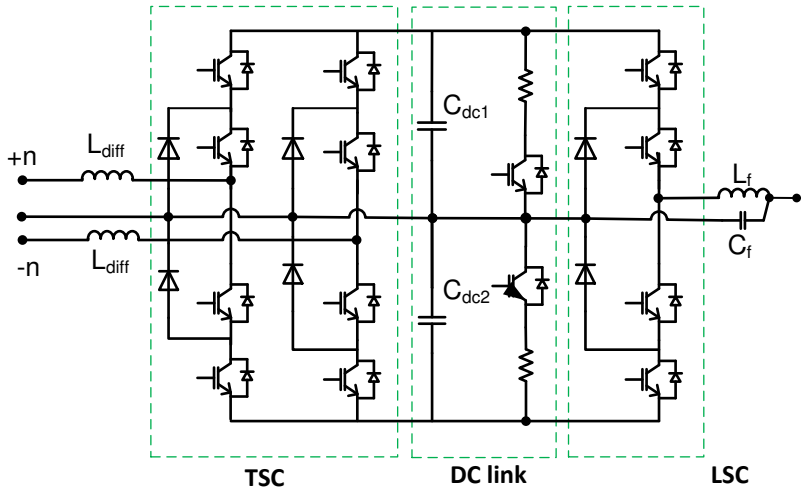


Figure 3.3: Single-phase, three-level implementation of FR-BTB converter.

As a series element, the power router could introduce a single point of failure. By providing a fail-normal feature, system reliability can be improved. The fail-normal feature is realized using an anti-parallel thyristor connected across the FR-BTB converter, as shown in Figure 3.1. For three-phase applications, three single-phase converters are required. The single-phase implementation avoids phase interactions, which can lead to problems with fault identification and fault isolation [93].

3.2 The Principle of Power-flow Control

In an elementary arrangement of two buses connected through a transmission line, the power flow in the line depends on the line impedance X_{line}, the sending-end voltage V_s, the receiving-end voltage V_r, and the phase angle between two buses δ. Active and reactive power in the line can be controlled through series compensation [56]. In the proposed power router, the FR-BTB converter injects a series voltage V_{conv} to provide the requisite series compensation. As shown in Figure 3.4, V_{conv} adds to V_s to generate an effective sending-end bus voltage V_{out}. By controlling V_{conv}, V_{out} can be controlled in magnitude and phase, and thereby active and reactive power in the line can be controlled.

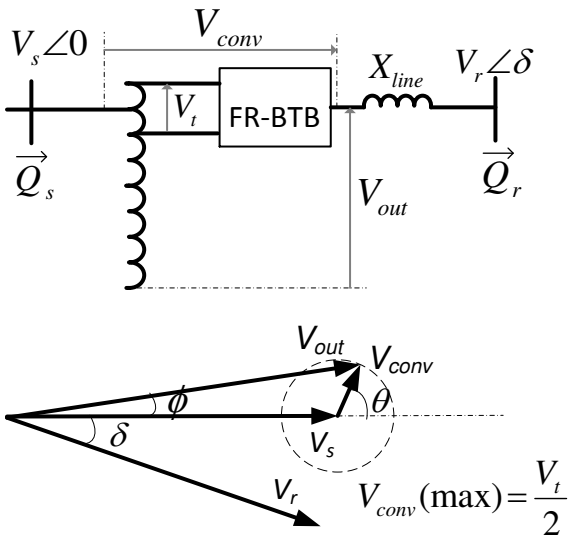


Figure 3.4: Principle of power-flow control of the proposed power router.

The equations for active power P, sending-end reactive power Q_s, and receiving-end reactive power Q_r with the proposed power router are given by Equations (7), (8) and (9), respectively.

$$P = \frac{V_{out} * V_2}{X_{line}} * \sin(\delta + \emptyset)\,, \tag{7}$$

$$Q_s = \frac{V_{out}}{X_{line}}(V_{out} - V_2 * \cos(\delta + \emptyset))\,, \tag{8}$$

$$Q_r = \frac{V_2}{X_{line}}(V_2 - V_{out} * \cos(\delta + \emptyset))\,, \tag{9}$$

where $V_{out} = \sqrt{(V_1^2 + V_{conv}^2)}$, $\emptyset = \tan^{-1}\left(\frac{V_{conv}*\sin\theta}{V_1 + V_{conv}*\cos\theta}\right)$, and θ is the phase angle of V_{conv}. The magnitude of V_{conv} is limited to half of the voltage across taps V_t while the phase can be varied over the entire range. The voltage V_{conv} can be independently controlled in magnitude and phase, thereby providing four-quadrant power-flow control.

3.3 Power-flow Modes

The control of FR-BTB converter is different than a standard BTB converter because of the difference in implementations. The power flow in a FR-BTB converter is controlled by two current components: common-mode and differential-mode. The

common- and differential-mode currents in a two-level FR-BTB converter and a three-level FR-BTB converter are shown in Figure 3.5 and Figure 3.6, respectively. The common-mode current I_{comm} is unique to the proposed system and is same as the line current I_{line}. The common-mode voltage V_{comm} is the series compensation provided by the converter, and it controls the power-flow in the line. The differential-mode current I_{diff} shuffles energy between the DC capacitor and the system, through the TSC.

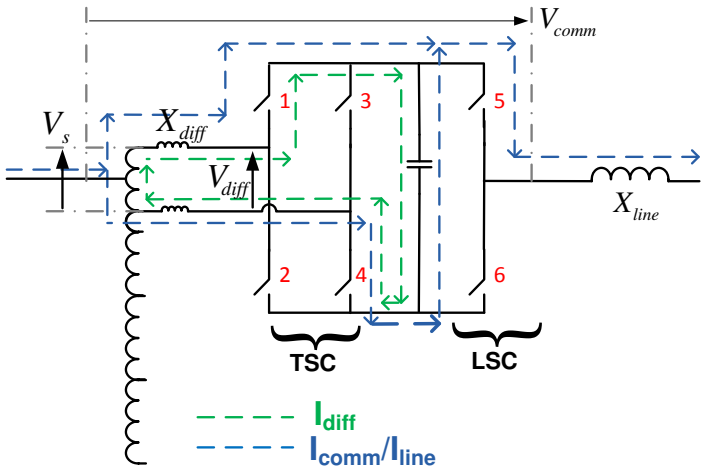


Figure 3.5: Common- and differential-mode currents in a two-level FR-BTB converter.

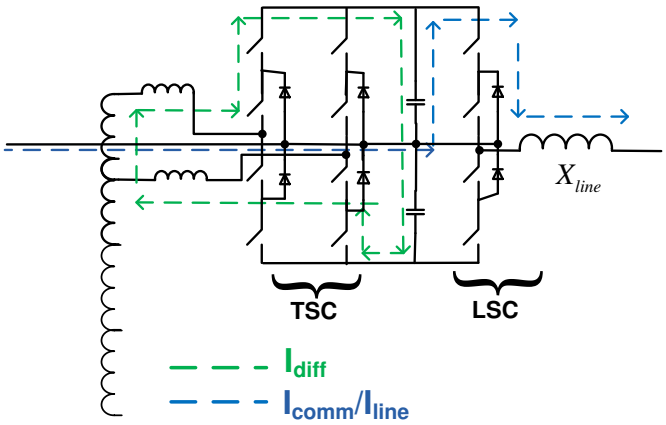


Figure 3.6: Common- and differential-mode currents in a three-level FR-BTB converter.

In a two-level FR-BTB converter, I_{comm} is shared equally between the two TSC poles, and only one half of it flows through the capacitor at any time. In a three-level converter, I_{comm} completely bypasses the TSC resulting in lower converter loss compared with the two-level configuration. Significantly, the transformer in a two-level

configuration has to carry I_{comm} and I_{diff}, while it carries only I_{diff} in a three-level configuration. Hence, the transformer in a three-level configuration will require smaller rating than the transformer in a two-level configuration. Except for the I_{comm} path, there is no major difference between the two configurations, and further analysis will use the two-level configuration.

At any time, the v_{comm} generated by the converter is independent of the status of TSC switches. As shown in Figure 3.7, v_{comm} depends only on the status of the LSC switches and is proportional to either the sum or the difference of the converter input voltage v_s and the DC-link voltage v_{dc}. Therefore, v_{comm} can be independently controlled by the LSC to generate the requisite line current. Similarly, v_{diff} is independently controlled by the TSC to generate I_{diff}. The current I_{diff} is controlled to maintain the DC-link voltage and, if required, to provide shunt-VAR support.

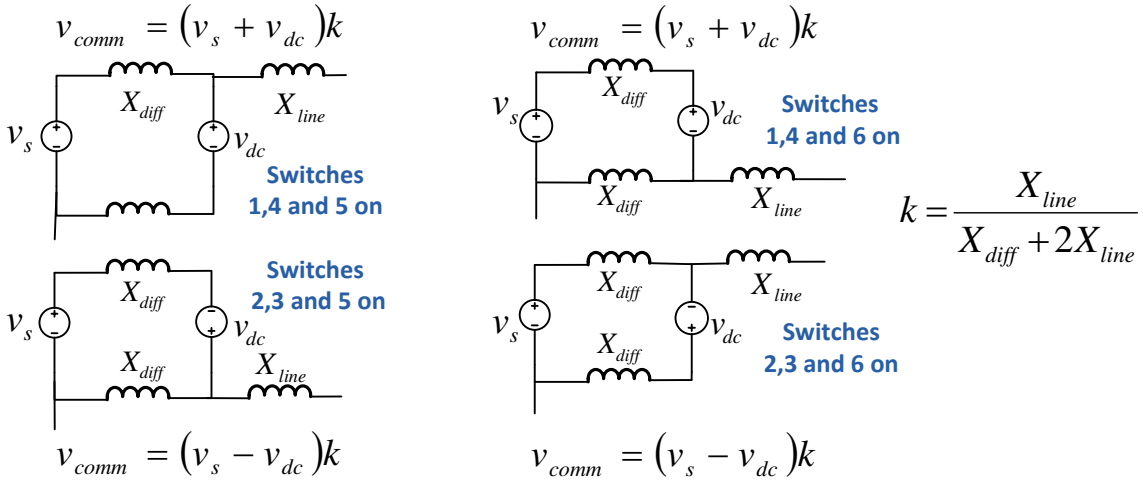


Figure 3.7: Common-mode voltage for different switching combinations of the FR-BTB converter.

3.4 Range of Power-flow Control

For complete controllability of the FR-BTB converter, the DC-link voltage must be higher than the instantaneous converter input voltage v_s at all times. Typically, the average DC-link voltage V_{dc} is maintained at 10 % higher than the peak v_s. For the given

v_s and v_{dc}, the maximum (v_{max}) and the minimum common-mode voltage (v_{min}) generated by the LSC are given by Equation (10) and Equation (11) respectively.

$$v_{max} = v_s + v_{dc} * \frac{X_{line}}{X_{line} + X_{diff}} \cong \frac{v_s + v_{dc}}{2}, \tag{10}$$

$$v_{max} = v_s - v_{dc} * \frac{X_{line}}{X_{line} + X_{diff}} \cong \frac{v_s - v_{dc}}{2}, \tag{11}$$

where X_{diff} is the differential-mode impedance. As shown in Figure 3.8, any voltage waveform that remains within the envelope of v_{max} and v_{min} can be synthesized by switching between the two extremes. The fundamental voltage $v_{comm,1}$ that the LSC can synthesize is given by Equation (12).

$$v_{comm,1} = \frac{V_{s,pk}+V_{dc}}{2} * \left(k_q Sin\theta + k_p Cos\theta\right), \tag{12}$$

such that $\sqrt{\left(k_q - 0.5\right)^2} + k_p^2 < 0.5$, where $V_{s,pk}$ is the peak of v_s. k_q, k_p, and θ are the reactive-power coefficient, active-power coefficient, and phase angle of the LSC-reference voltage, respectively.

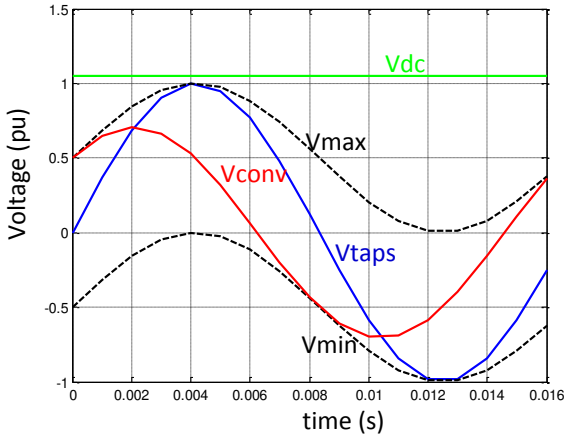


Figure 3.8: Synthesis of FR-BTB converter voltage.

As shown in Figure 3.9, the common-mode voltage, equivalent to the series compensation provided by the converter, can vary over the entire phase range within $(V_{s,pk} + V_{dc})/2$. The corresponding power range depends on system parameters (X_{line},V_1, V_2, and δ) and is given by Equations (7), (8), and (9).

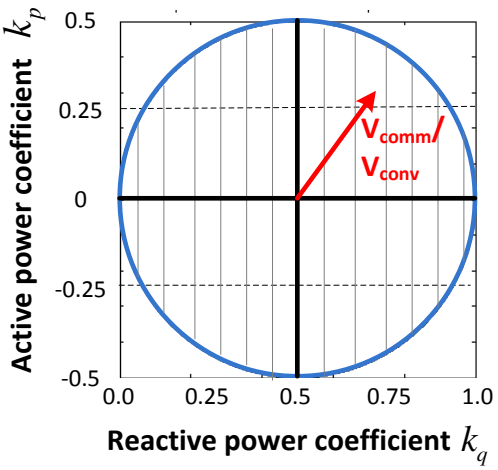


Figure 3.9: Series-voltage-compensation range of the proposed power router.

Consider the 138 kV two-bus system shown in Figure 3.10. A 30-mile line, with a typical impedance of 0.79 ohms/mile [94], was connected between the two buses. The FR-BTB converter was connected to the +/- 5% taps of the autotransformer at the sending end. The realizable power-flow-control range as a function of δ is shown in Figure 3.11. The PR provides up to +/- 38 MVA of control capability under all operating conditions.

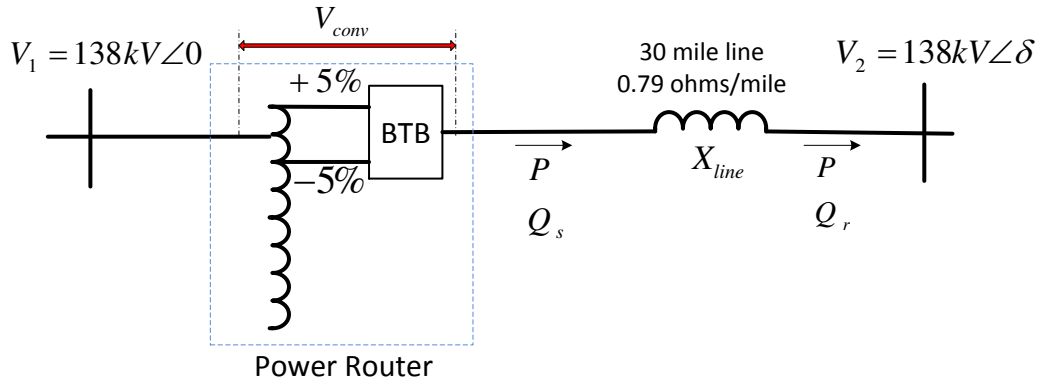


Figure 3.10: 138 kV example system with the proposed power router.

The power router tends to lose range of independent control of active power P and sending-end reactive power Q_s as δ increases, which implies that as δ increases any voltage injected to change P will result in an increasing change in Q_s. The loss of independent control is indicated by the increasing elliptical nature of the P versus Q_s plot

as δ increases. The relationship between δ and the amount of independent control of receiving-end reactive power is negligible. Though the power router provides a control range of +/- 38 MVA, the FR-BTB converter is rated only 6.8 MVA for $\delta = 2^{\circ}$, 18 MVA for $\delta = 10^{\circ}$, and 31 MVA for $\delta = 20^{\circ}$. As δ increases, the converter reduces its fractional-rating advantage, but most of the short to medium lines have $\delta < 10^{\circ}$.

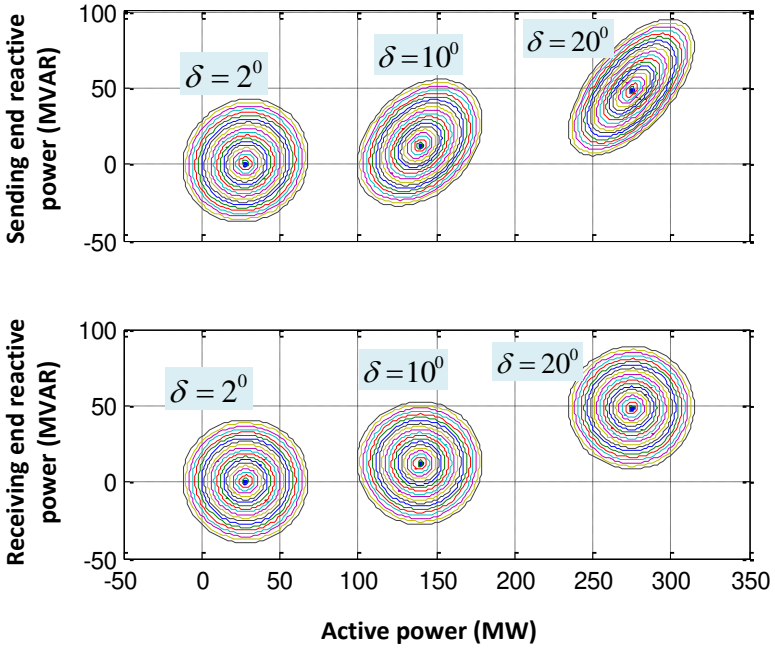


Figure 3.11: Control range of the proposed power router as a function of phase-angle difference.

3.5 Converter Control

The main objective of the control scheme is to control the current I_{comm}, and hence the line-power flow. The current I_{comm} flowing through the DC-link capacitor will result in active- and/or reactive-power flows in the capacitor. Since flow of active power will vary V_{dc}, another objective of the control scheme is to control the I_{diff} to maintain the V_{dc} at a set value. The converter-control scheme, shown in Figure 3.12, consists of common-mode control and differential-mode control in d-q synchronous-reference frame. The current references for common-mode control are calculated from desired active power and series volt-ampere-reactive (VAR). The desired line current I_{comm}^{ref} is then compared with the actual current I_{comm} and the error is sent to a proportional-integral

(PI) regulator. The PI regulator generates an output voltage reference V_{comm}^{ref} to minimize the error. V_{comm}^{ref} is then compared with the carrier wave to generate switching pulses for the LSC.

The objective of the differential-mode control is to maintain the voltage V_{dc} at a desired value and control the shunt VARs. The voltage V_{dc} is extracted with a low-pass filter and then compared with the DC-link-voltage reference $V_{dc,0}^{ref}$. The voltage error is sent to a PI regulator which generates the active component of the differential-current reference $I_{diff,d}^{ref}$. The reactive component of the differential-current reference $I_{diff,q}^{ref}$ is set by the desired shunt VARs. As in the common-mode control, the reference voltage is compared with a carrier wave to generate appropriate switching pulses for the TSC.

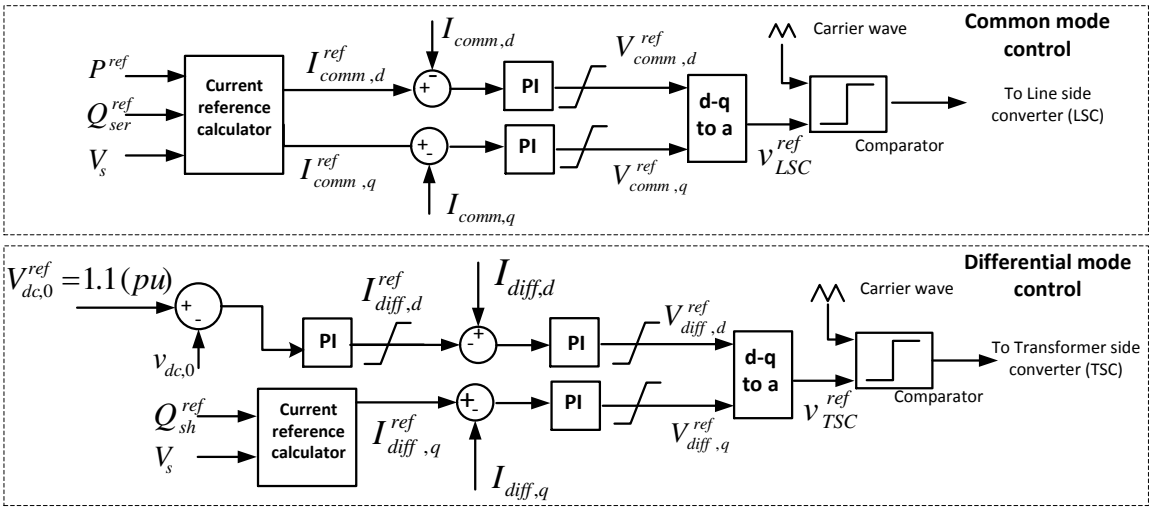


Figure 3.12: Converter-control scheme for the proposed power router.

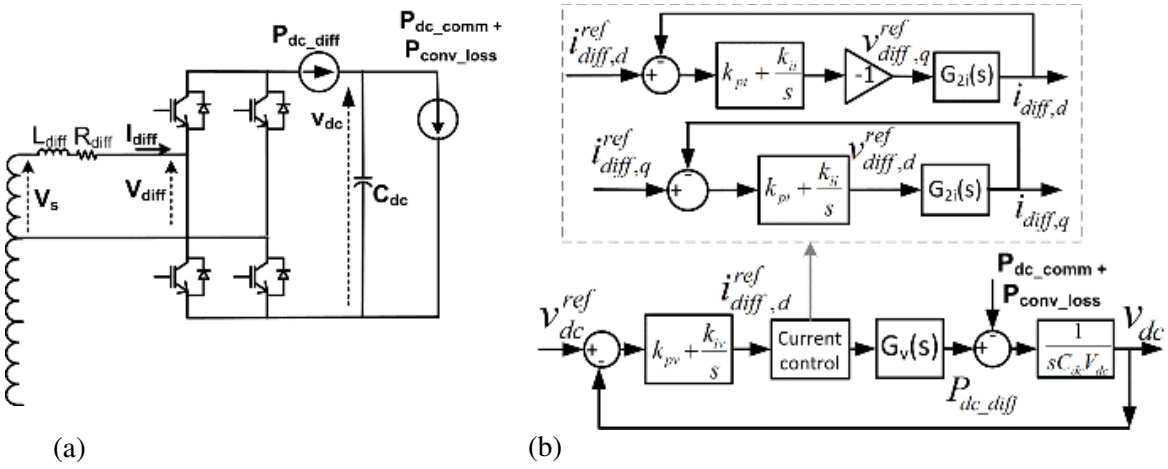
Controller design: The equivalent circuit for the differential-mode control is shown in Figure 3.13(a). The differential-mode control consists of a inner current control loop and an outer DC-bus control loop as shown in Figure 3.13(b).

The differential current dynamics are given by Equation (13). The impact of $G_{1i}(s)$ can be neglected by choosing the PI controller gains to have a time constant greater than L_{diff}/R_{diff} [95]. The current control block then reduces to the form shown in Figure 3.13(b) and the PI gains can be deduced by standard Bode-plot techniques.

$$\begin{bmatrix} I_{diff,d} \\ I_{diff,q} \end{bmatrix} = \begin{bmatrix} G_{1i}(s) & G_{2i}(s) \\ -G_{2i}(s) & G_{1i}(s) \end{bmatrix} \begin{bmatrix} V_{s,d} - V_{diff,d} \\ -V_{diff,q} \end{bmatrix}, \tag{13}$$

where $G_{1i}(s) = \frac{R_{diff} + s * L_{diff}}{L_{diff}^2 * s^2 + 2 * R_{diff} * s * L_{diff} + R_{diff}^2 + \omega^2 * L_{diff}^2}$ and

$G_{2i}(s) = \frac{\omega * L_{diff}}{L_{diff}^2 * s^2 + 2 * R_{diff} * s * L_{diff} + R_{diff}^2 + \omega^2 * L_{diff}^2}$.



(a) (b)

Figure 3.13 (a) Differential-mode equivalent circuit. (b) Differential-mode control scheme.

The DC-bus dynamics are described by Equation (14), and since they are non-linear, the equation is linearized around an operating point of I_{diff} and is given by Equation (15) [96]. Conditions to ensure stability at given operating point can be derived from the linearized equation and are given by Equation (16). The PI gains for the DC-voltage control are chosen so that the stability constraints are satisfied and also the time constant of the control loop is at least five times greater than the time constant of the inner current loop to ensure decoupling between the two control loops.

$$P_{dc_{diff}} - P_{dc_{comm}} - P_{conv_{loss}} = C_{dc} * v_{dc} * \frac{d}{dt}(v_{dc}), \tag{14}$$

$$\Delta v_{dc}(s) = \frac{1}{V_{dc} * C_{dc} * s}\left(V_{s,d} - 2 * R_{diff} * I_{diff,d} - s * L_{diff} * I_{diff,d}\right) * \Delta I_{diff,d}(s), \tag{15}$$

$$k_{pv} < \frac{V_{dc} * C_{dc}}{L_{diff} * I_{diff}}, \quad k_{iv} < \frac{V_{s,d} * k_{pv}}{L_{diff} * I_{diff}} - \frac{2R_{diff} * k_{pv}}{L_{diff}} \tag{16}$$

The controller design for the common-mode current control is similar to the differential-mode current control with L_{diff} and R_{diff} replaced by L_{line} and R_{line}, respectively.

3.6 Simulation Results

The two-bus 138 kV system, shown in Figure 3.10, was simulated to demonstrate the functionality of the proposed power router. The converter parameters used in the simulation are shown in Table 3.1. The control parameters, designed using standard Bode-plot techniques, are shown in Table 3.2**.**

Table 3.1: System parameters used for FR-BTB converter simulation.

Parameter	**Value**
FR-BTB source voltage, V_t	8.0 kV
DC-link voltage, V_{dc}	12.5 kV
DC-link capacitor	1 mF
Differential inductor, L_{diff}	4 mH
Filter inductor/capacitor, L_f / C_f	1 mH/50 µF
Phase angle, δ	2º

Table 3.2: Control parameters used for converter simulation.

Parameter	**Value**	**Parameter**	**Value**
Differential-mode		**Common-mode**	
V_{dc} (base)	12.5 kV	V_{conv} (base)	4 kV
I_{diff} (base)	500 A	I_{line} (base)	800 A
K_p , K_i (voltage loop)	4 A/V, 10 A/V^2 respectively.	K_p, K_i (current loop)	0.1 V/A, 0.5 V/A^2 respectively.
K_p , K_i (current loop)	0.05 V/A, 0.5 V/A^2 respectively.		

At $\delta = 2^0$, the power flow in the uncompensated line (without PR) was 28 MW. As shown in Figure 3.14, the power router can vary the power flow from 66 MW to -10 MW, thereby providing a control range of +/- 38 MW. The reactive power was held constant while the active power was varied, demonstrating independent control. Similarly, the reactive power was varied while the active power was constant. As the power is varied, the regulation of the DC-link voltage through differential-current control is shown in Figure 3.15. The converter input voltage V_t, the line current I_{line}, and the

converter injected voltage V_{conv} are shown in Figure 3.16. The maximum voltage V_{conv} that the converter can generate was half of V_t.

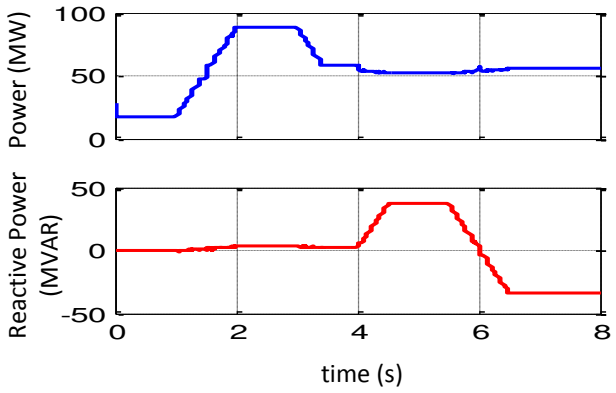


Figure 3.14: Simulation results showing dynamic control of active and reactive powers.

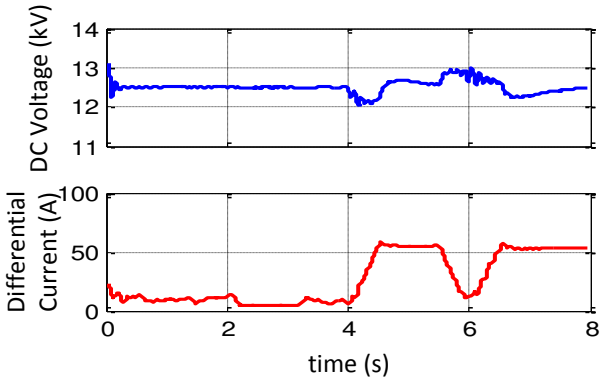


Figure 3.15: Simulation results showing the DC-link voltage and differential current (rms) variation under dynamic power-flow control.

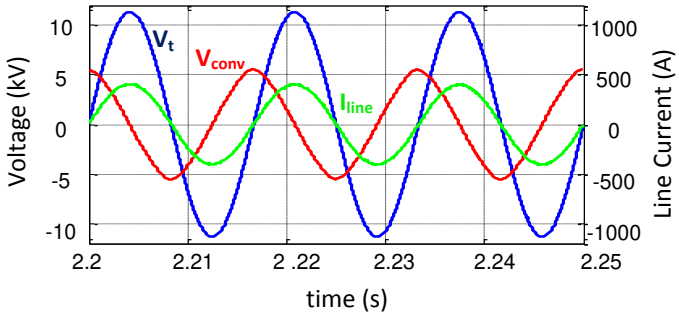


Figure 3.16: Simulation results showing the input voltage, output voltage, and line current of the FR-BTB converter.

Figure 3.17 shows the magnitude of the differential and common-mode currents over the entire control range for the simulation case. The worst case common-mode current

will be the same as the maximum line current, which occurs when the power router is injecting out-of-phase voltage It has been observed that the differential current is maximized when the power router is injecting in-phase voltage to control series VARs. In this operating condition the active power exchange between the LSC converter and the line is maximal. Hence the differential current, which compensates for the active power exchange, is at a maximum for this condition.

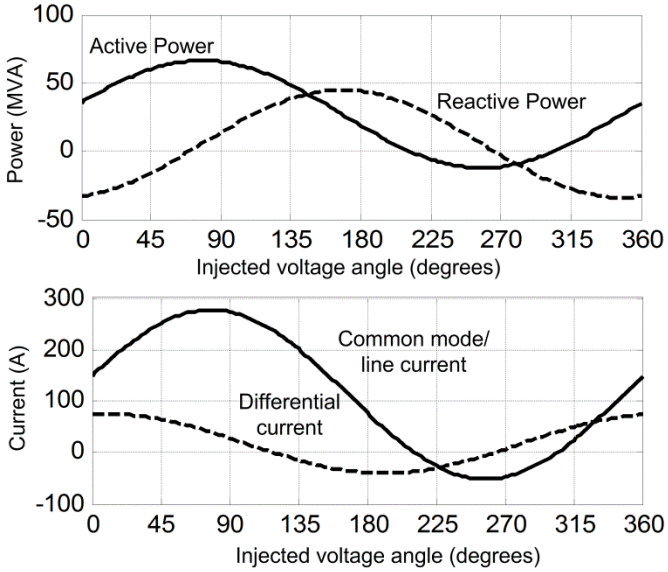


Figure 3.17: Simulation results showing the (a) active and reactive power; and (b) common and differential mode currents at 4 kV series voltage injection.

A controllability range of +/- 38 MW/MVAR was achieved with the FR-BTB converter rated for 6.6 MVA. Since the converter was connected between +/- 5 % taps, the FR-BTB converter was rated to handle a peak voltage of 12 kV. Realizing the same control range with a standard BTB converter would require a converter that can handle peak voltages of 200 kV or low-frequency step-down transformers, increasing the cost of implementation. The simulation results demonstrate the capability of the proposed FR-BTB based power router to independently control active- and reactive-power flows.

3.7 Comparison of the Proposed PR with UPFC and CNT

The UPFC [97] and CNT [98] are other converter-based solutions that can provide independent control of active and reactive power. In this section, the proposed power

router based on FR-BTB converter is compared with UPFC and CNT. The power routers are compared in terms of control range, component requirement, cost, implementation, and reliability. The configurations of the proposed power router, CNT, and UPFC used for comparison are shown in Figure 3.18. For the sake of uniformity, all the three controllers were designed to provide 5 % series quadrature-voltage compensation on the 138 kV system shown in Figure 3.10. Throughout the analysis, the bus voltages were held constant, and the phase angle across the uncompensated line was assumed to be 5^0. The assumptions resulted in an initial current and active power of 294 A and 70 MW respectively. With 5% quadrature-voltage compensation, the maximum current and the active power were 453 A and 107 MW, respectively.

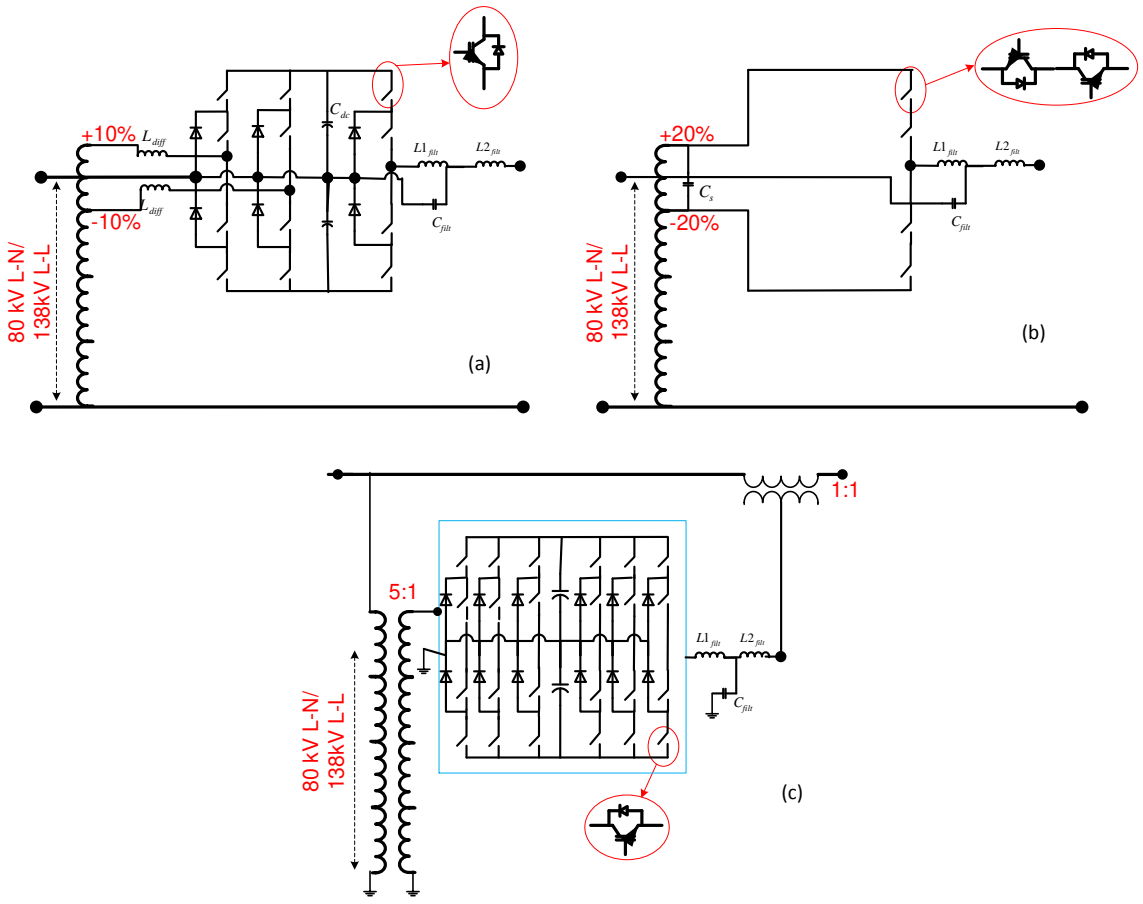


Figure 3.18: Power-router topologies for comparison study. a) Single-phase, three-level FR-BTB converter. (b) Single-phase, two-level CNT. (c) Three-phase, three-level UPFC.

3.7.1 Semiconductor Requirement

For the chosen converters, voltage scaling was achieved by series connecting devices in each pole, and multiple poles were connected in parallel to achieve the desired current rating. Dynex 1700V, 300A IGBT devices were used for this analysis. To provide margin of safety for voltage spikes during switching, the peak operating voltage of the 1700 V IGBT was limited to 1200 V. To account for derating under relatively high temperature operation, a current peak of 220 A was considered.

To provide 5 % quadrature-voltage compensation, the CNT was connected across +/- 10 % taps. Thus each IGBT pole has to withstand a peak of 22.5 kV and a peak current of 640 A. The CNT required 76 of the selected IGBTs per pole, connected in series. In addition, the CNT required three poles, operating in parallel, to carry 640 A. The total semiconductor VA rating for the CNT was 350 MVA for the three-phase implementation.

The FR-BTB converter was connected across +/- 5 % taps to provide 5 % quadrature-voltage compensation. For the chosen configuration each IGBT pole had to withstand a peak of 12.5 kV, resulting in 22 devices per pole. Given that the IGBT pole in the FR-BTB LSC had to withstand a peak of 640 A, three poles were connected in parallel. In addition, each pole of the three level converter would require two clamping diodes rated to carry the same pole current and block half the DC-link voltage. The semiconductor VA requirement of the LSC was 34 MVA for the IGBTs and 17 MVA for the clamping diodes. The differential current depends on the active power exchanged by the LSC with the line, which is the average of the product of the series-injected voltage and the line current. For the analysis, the peak active power absorbed/delivered by the LSC was 1.1 MW per phase, and the peak differential current of the TSC devices was 195 A. Hence, the TSC in the two-level FR-BTB converter required two poles with a VA requirement of 23 MVA per phase. The total VA requirement of the three-phase, three-level FR-BTB was 168 MVA for IGBTs and 84 MVA for clamping diodes.

For the UPFC, a transformation ratio of 5:1 was selected for the shunt transformer and a 1:1 transformation ratio was selected for the series transformer. Therefore, the FR-BTB converter poles were appropriate for the UPFC. However, the number of poles varied because the UPFC was implemented using a three-phase converter while the FR-BTB was implemented using three single-phase converters. The UPFC shunt converter required half the number of poles of the FR-BTB TSC. The UPFC series converter required the same number of poles as the FR-BTB LSC. The ratings of the three-level UPFC implementation were 202 MVA for IGBTs and 101 MVA for diodes.

3.7.2 Reactive Components

3.7.2.1 Transformers

The three-phase CNT requires three auto-transformers, connected either in star or delta configuration. The transformer VA rating was twice as that of the converter VA rating, which was rated for 5.4 MVA. In the FR-BTB, the transformer rating is the same as the TSC rating, which was 3.3 MVA. The UPFC has a shunt transformer and a series transformer. The shunt transformer contributes towards the active-power exchange of the series converter, as in the case of the FR-BTB TSC. Hence, the shunt transformer rating was 3.3 MVA. The series transformer was rated twice as large as the series converter, to achieve the same dynamic response as the FR-BTB and the CNT [69]. Since the series converter was rated for 5.4 MVA, the series transformer was 10.8 MVA.

3.7.2.2 Reactors

In case of a CNT, a third-harmonic voltage of the same magnitude as that of the fundamental compensating voltage is generated [98]. In a balanced three-phase system, the third-harmonic voltages in each phase cancel each other. But in unbalanced systems, a series third-harmonic filter is required to block the resultant third-harmonic current in the line [99]. For this analysis, the third-harmonic filter was designed for a 10 %

unbalance. The optimum value of the inductor is 10 % of the line impedance for 100 % third-harmonic compensation [99]. This analysis required ten percent third-harmonic compensation, so the filter inductor was set at one percent of the line impedance. Thus, the required filter inductor was 0.6 mH, 0.1 MVAR per phase.

For the UPFC, the significant reactors are the line reactors connected between the transformer and the converter. The UPFC line reactors are usually rated in the range of 10-15 % of the converter VA rating. Similarly, the differential inductors in the FR-BTB are chosen to be 10 % of the TSC rating.

3.7.2.3 Capacitors

The CNT configuration has two AC capacitors. One capacitor is connected across the taps to isolate the transformer windings from high-frequency ripple currents. The required capacitor is a function of the transformer leakage inductance. Assuming a 10% leakage inductance, a 5.0 μF capacitor was chosen to absorb the switching-ripple current at 2.0 kHz. At 16 kV, the capacitor was 0.5 MVAR per phase. The other AC capacitor in the CNT is a part of the third-harmonic series filter. With a 0.6 mH per phase filter inductor, the value of the capacitor was 1100 μF, 53 kVAR per phase.

The significant capacitor in the FR-BTB and the UPFC is the DC-link capacitor. The capacitor is chosen to provide energy during the transients and to limit the voltage ripple. The metric used for selecting the DC capacitor, for providing energy during transients, is called unit capacitance constant (UCC) [100]. It is typically in the range of 3000-6000 J/MVA for converters exchanging active power with the grid [101]. With a UCC of 4000 J/MVA, the FR-BTB required a 85 μF capacitor with an energy capacity of 7 kJ. But with a 85 μF capacitor, the second-harmonic ripple in the DC-link voltage was 10 kV (76%). To limit the ripple to be within +/- 10%, a 650 μF, 54 kJ DC capacitor was chosen for the single-phase FR-BTB implementation. In case of a UPFC, the ripple is at sixth harmonic,

as all the three phases share the same capacitor. A 255 μF, 18.5 kJ DC capacitor was chosen so that the UPFC had the same DC-link ripple as the FR-BTB.

3.7.3 Reliability

CNT has the same commutation issues associated with direct AC-AC converters. The lack of free-wheeling path in AC-AC converters is a major constraint. Also, scaling to high voltages requires series stacking of devices. It is important to ensure static- and dynamic-voltage sharing among series-connected AC switches. In principle, an active snubber can solve the commutation issues, ensure voltage sharing, and provide the free-wheeling path [102], but the active snubber is yet to be proved in practical application.

The FR-BTB and UPFC have BTB converter, which is based on VSC technology. VSC-based BTB technology is commercially available at 75 kV, and the technology for series stacking of IGBTs is well established [72]. The major reliability constraint in the FR-BTB and UPFC is the DC-link capacitor. Electrolytic capacitors are preferred for DC-link applications, as they are economical than film capacitors. But electrolytic capacitors have a limited life time of only 2000-10000 hours. Film capacitors, with a lifetime of 100,000 hours, may be used for DC-link applications at an additional cost.

3.7.4 Isolation Requirements

In case of the FR-BTB and CNT, the converter is connected across the taps of a transformer. The converter floating at line voltage requires sufficient isolation from ground level. Like in case of TCSC [40], a raised platform can be provided for isolation, but at an additional cost. Providing a raised platform for the FR-BTB can be more expensive than a CNT because of the bulky DC-link capacitor in FR-BTB. In case of UPFC, the shunt and the series transformers provide the required isolation. Hence, the converter and the DC capacitors can be installed at the ground level. Still, the series transformer, floating at line voltage, has to be provided with sufficient isolation.

3.7.5 Cost Assumptions

For the cost analysis, the costs of various components considered are shown in Table 3.3. In case of the CNT and the FR-BTB, the costs involved in providing elevated structure for ground isolation were not considered.

Table 3.3: Costs of various components used for comparative analysis of different power routers.

Parameter	Value	Remarks
Transformers	10 $/kVAR [103]	
AC reactors	20 $/kVAR [104]	
AC capacitors	10 $/kVAR [105]	
DC electrolytic capacitors	0.075 $/J [106]	
Film capacitors for DC storage	0.35 $/J [106]	
1700V IGBT device	0.75 $/A / 440 $/MVA	Retail cost is 1.0 $/A
1700V Diode	0.6 $/A /350 $/MVA	Retail cost is 0.75 $/A

3.7.6 Remarks

The comparison of the three power-routing technologies is shown in Table 3.4. The technologies are compared for providing 8.0 kV per phase series compensation on a 138 kV system. Unlike the CNT and UPFC, the FR-BTB three-level configuration is more economical than the two-level configuration. Comparing the three-level configurations, the FR-BTB and UPFC required half of the semiconductor requirement for the CNT. The low-frequency transformer required for FR-BTB was only a fraction of the requirement for CNT and UPFC. Though implementing the DC link with film capacitors increases the cost of the FR-BTB, it is still economical compared to the UPFC or the CNT. Thus, the proposed power router based on three-level FR-BTB offers a low-cost power-routing solution compared to a CNT or a UPFC.

Table 3.4: Comparison of power-router technologies.

Features		**CNT**		**UPFC**		**FR-BTB**	
			Cost (k$)		**Cost (k$)**		**Cost (k$)**
Line voltage		138 kV		138 kV		138 kV	
Series compensation		8 kV		8 kV		8 kV	
Converter peak voltage rating		22.5 kV		12.5 kV		12.5 kV	
Converter peak current rating		650 A		650 A		650 A	
Semiconductor VA rating-3level NPC converter	IGBT	350	154	202	89	168	76
	Diode	-	-	101	36	84	30
Reactors (MVAR)		0.3	9	0.54	11	0.3	6.6
Capacitors	AC (MVAR)	1.5	15	-	-	-	-
	DC-link (μF / kJ)	-	-	220/21.5	1.75	1950/112	8.5
	DC-link with film capacitors (μF / kJ)	-	-	220/21.5	7.5	1950/112	39
Transformers (MVA)	Shunt	17.1	171	5.4	54	3.3	33
	Series			10.8	108		
Total cost	**Three-level**		**349**		**298**		**154**
	Three-level with only film caps		**349**		**305**		**184**
Isolation	Converter	Floating		Ground level		Floating	
	DC bus	-		Ground level		Floating	
	Transformer	-		Floating series transformer		-	
Fault handling		Fail-normal switch		Fail-normal switch		Fail-normal switch	
Reliability limitation		Switch commutation, free-wheeling path and series operation of AC switches.		DC capacitor.		DC capacitor.	

3.8 Low Power Implementation

The control algorithm and functionality of the proposed power router was verified through a 50 KVA prototype.

3.8.1 Experimental Setup

To demonstrate the functionality of the proposed PR, the two-bus test-bed shown in Figure 3.19 was fabricated. It consists of a single-phase 240 V source and two sets of 240 V/1320V transformers. The inductor connecting the two transformers was replicating the line inductance. The two transformers, with taps at +/- 120 V, were representing the buses in a typical two-bus system. The FR-BTB converter was connected to one of the transformer sets between the +/- 120 V taps. The components used for the setup are shown in Table 3.5. The control algorithm, implemented on TI TMS320F2812 DSP, consists of grid synchronization, synchronous-frame control, three-level pulse-width-modulation (PWM) pulse generation, and dead-time control. Separate control boards were developed for implementing signal conditioning and protection logics. The complete control scheme and the developed control boards are shown in Figure 3.20.

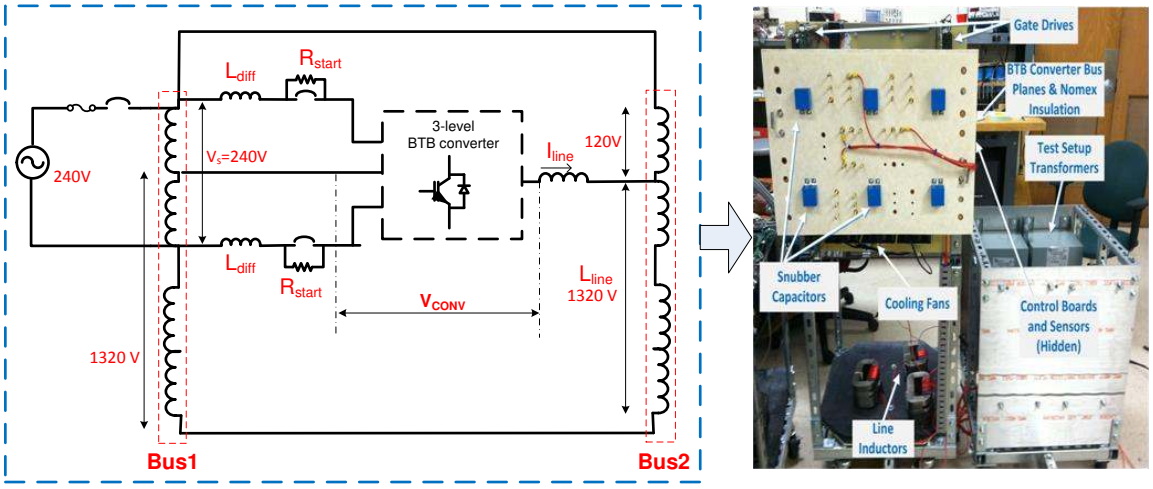


Figure 3.19: Schematic and implementation of the 50 kVA two-bus experimental system.

Table 3.5: Components for the 50 kVA power-router prototype.

Parameter	Value
Bus1,Bus2	240V/1200V, 100 kVA transformers
IGBT	1700V, 200A Dynex
Diodes	1700V, 60A Semikron
Line inductor	2 mH, 60A
Differential inductor	300 mH, 20A
DC capacitor	300 µF , 600V

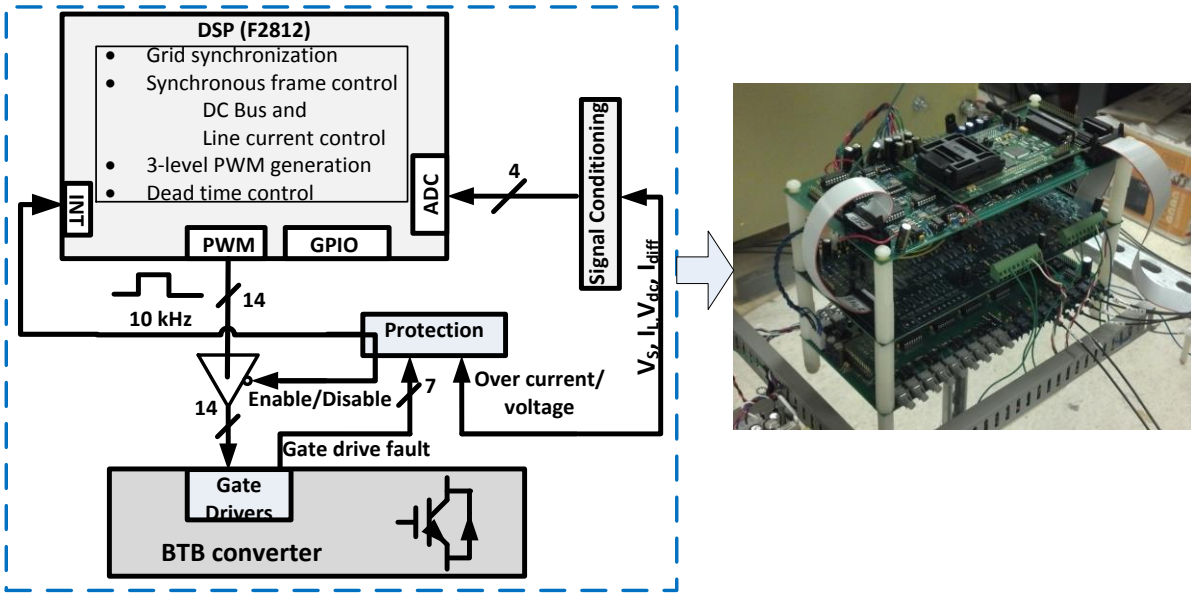


Figure 3.20: Control system implementation for the 50 kVA experimental prototype.

Table 3.6: PR-controller parameters for the 50 kVA experimental prototype.

Parameter	Value
Differential-mode	
Vdc (base)	300V
I_{diff} (base)	20A
K_p,k_i (DC-voltage loop)	0.5 A/V, 2 A/V^2 respectively
K_p,k_i (current loop)	0.05 V/A,0.5 V/A^2 respectively
Common-mode	
V_{conv} (base)	120V
I_{line} (base)	50A
K_p, k_i	0.24 V/A, 1.2 V/A^2 respectively

3.8.2 Results

Without the FR-BTB converter, the two buses have the same voltage, and hence no power flowed across the line. With the proposed PR, the effective voltage of Bus 1 was controlled in magnitude or phase or both, to induce power flow across the line. Four-quadrant-control results at 50 kVA are shown in Figure 3.21. The converter voltage V_{conv}, the voltage impressed by the LSC on the line inductor, induce a 35 A line current I_{line} at a bus voltage of 1320 V. The TSC is controlling the DC capacitor voltage at 400 V. The common-mode current and the differential current in the negative-real-power mode are shown in Figure 3.22. In the experiment circuit, the sending and the receiving end voltages are sourced from the same source, and hence the differential current is only supplying the losses in the converter and is therefore of a very low value.

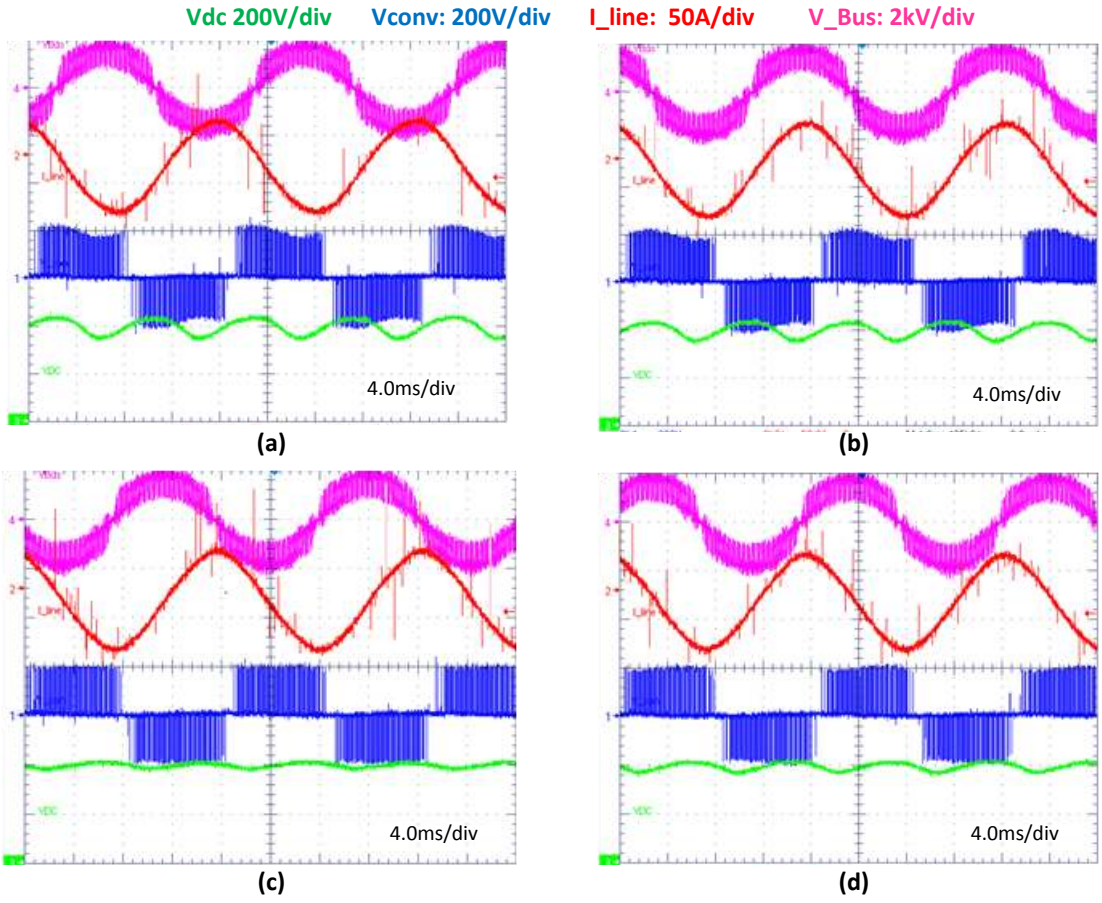


Figure 3.21: 50 kVA experiment results. (a) Positive power (b) Negative power (c) Lagging VAR (d) Leading VAR.

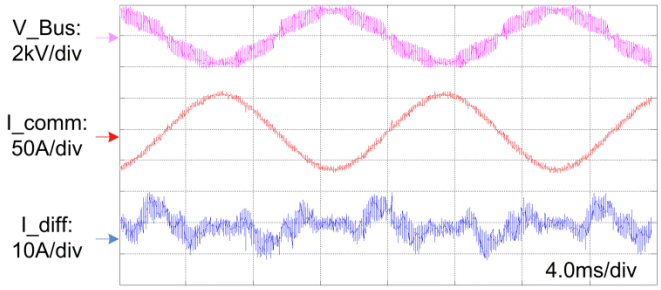


Figure 3.22: 50 kVA experiment results showing the common- and differential-mode currents in real power mode.

The dynamic-control results are shown in Figure 3.23. The current reference is varied to ramp the active power from 0 kW to 46 kW and then to -46 kW to demonstrate the dynamic controllability of active power. The corresponding changes in DC-link voltage and line current are shown in Figure 3.23(a). The active power calculated from voltage and current is shown in Figure 3.23(b). A controllability range of +/- 46 MW/MVAR was achieved with the 10 kVA converter. The advantage of the proposed PR in terms of fractional converter rating, leading to lower cost and reduced complexity, was experimentally demonstrated.

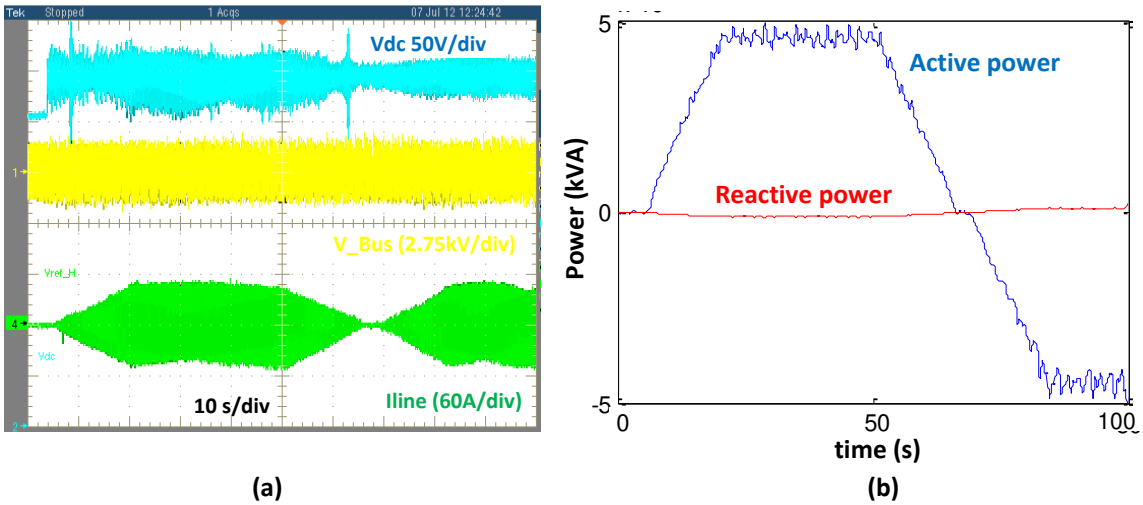


Figure 3.23: 50 kVA experiment results for dynamic control. (a) Vdc, V_bus, and I_line. (b) Active power.

3.9 Small-signal and Steady-state Models

Simplified models of the converter are necessary for system studies. The time-domain model for the proposed power router are derived using similar basic principles used in

UPFC model derivation [107]. The small-signal model is then derived from the time-domain model by averaging the switching dynamics. But it will retain the dynamics of the DC-link capacitor, which are necessary to understand the transient operating limits of the proposed PR. The small-signal model is useful for transient-stability studies and for the PR-controller design. The steady-state model will be derived by averaging the switching frequency dynamics and the DC-voltage dynamics. The steady-state model is useful for system-level studies such as load-flow analysis, and identification of optimum location and rating of the power router.

3.9.1 Time-Domain Model

Consider the implementation of the proposed power router shown in Figure 3.24. The compensating voltage injected by the power router for controlling the line current is given by Equation (17), and the corresponding line current dynamics are given by Equation (18).

$$v_{comm} = \frac{2n * v_1 + v_{dc}}{2} S_{comm} + \frac{2n * v_1 + v_{dc}}{2} S'_{comm} \ , \tag{17}$$

$$v_1 - v_2 + v_{comm} = \left(L_{line} + \frac{L_{diff}}{2}\right) * \frac{d(i_{line})}{dt} + \frac{R_{diff}}{2} * i_{line} \ , \tag{18}$$

Where $S_{comm} = 1$ if sw5 is on, $S_{comm} = 0$ if only sw6 is on, S'_{comm} is complimentary of S_{comm}, v_{comm} is common-mode voltage injected by the power router, v_1 is the sending-end voltage, $v_2 v_2$ is the receiving-end voltage, i_{line} is the line current, L_{line} is the line inductance, L_{diff} is the differential inductance, and R_{diff} is the line resistance.

The differential-mode voltage generated by the power router TSC is given by the Equation (19), and the corresponding differential-current dynamics are given by Equation (20). The DC-capacitor dynamics are given by Equation (21).

$$v_{diff} = v_{dc} * S_{diff} + v_{dc} * S'_{diff} \ , \tag{19}$$

$$2n * v_1 - v_{diff} = 2 * L_{diff} * \frac{d(i_{diff})}{dt} + 2 * R_{diff} * i_{diff} \ , \tag{20}$$

$$C_{dc} * \frac{d(v_{dc})}{dt} = i_{diff} * \left(S_{diff} - S'_{diff}\right) - \frac{i_{line}}{2} * \left(S_{comm} - S'_{comm}\right) , \tag{21}$$

where $S_{diff} = 1$ if sw1 and sw4 are on, $S_{diff} = 0$ if sw2 and sw3 are on, i_{diff} is the differential current, v_1 v_1 is the sending-end voltage, v_{diff} is the differential voltage, v_{dc} is the DC-link voltage, R_{diff} is the differential-mode resistance, L_{diff} is the differential-mode inductance, C_{dc} is the DC-link capacitor, and n is the tap ratio.

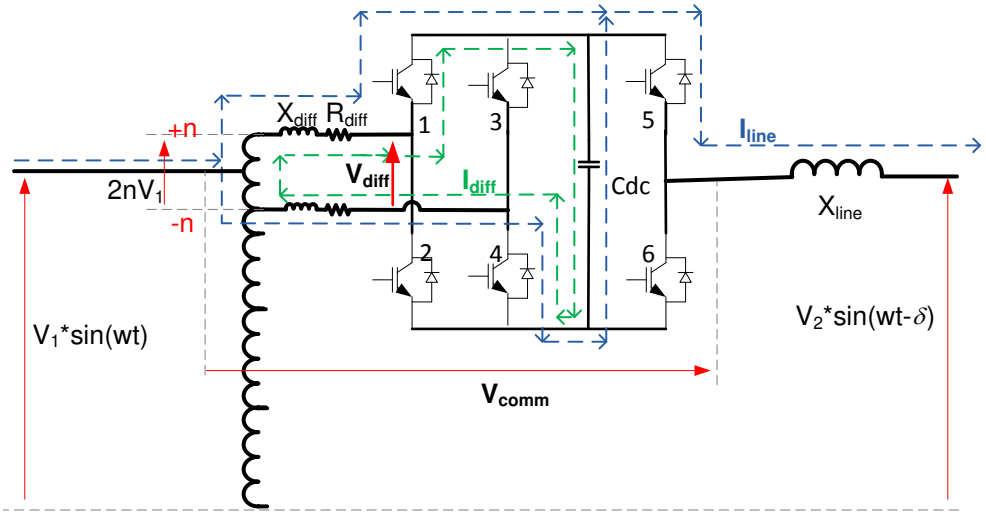


Figure 3.24: Schematic of proposed PR for deriving time-domain models.

3.9.2 Small-Signal Model

The small-signal model is obtained by averaging the switching-frequency dynamics. By replacing the switching functions ($s_{comm}, s'_{comm}, s_{diff}$, and s'_{diff}) in the time-domain model by their average models, the averaged switching functions are derived. The common-mode averaged switching function is given by Equation (22) and the differential-mode averaged switching function is given by Equation (23).

$$\begin{aligned} S'_{comm\_avg} &= 0.5 - 0.5 * mi_{comm} * \sin(\omega t + \emptyset_{comm}) , \\ S_{comm\_avg} &= 0.5 + 0.5 * mi_{comm} * \sin(\omega t + \emptyset_{comm}), \end{aligned} \tag{22}$$

$$S'_{diff\_avg} = 0.5 - 0.5 * mi_{diff} * \sin\left(\omega t + \emptyset_{diff}\right) , \tag{23}$$

$$S_{diff\_avg} = 0.5 + 0.5 * mi_{comm} * \sin(\omega t + \emptyset_{diff}) ,$$

where mi_{comm} is the magnitude of the reference for the common-mode voltage,

mi_{diff} is the reference function magnitude for generating differential-mode voltage,

$\emptyset_{comm}$ is the phase of the reference for the common-mode voltage,

and $\emptyset_{diff}$ is the phase of the reference for the differential-mode voltage.

The averaged switching functions are substituted in Equation (17) and (18) to derive the common- and differential-mode voltages of the small-signal model. The common-mode voltage of the small-signal model is given by Equation (24) and the differential-mode voltage given by Equation (25).

$$v_{comm\_avg} = mi_{comm} * \sin(\omega t + \emptyset_{comm}) * \frac{V_{dc}}{2}, \tag{24}$$

$$v_{diff\_avg} = mi_{diff} * \sin(\omega t + \emptyset_{diff}) * \frac{V_{dc}}{2}, \tag{25}$$

where v_{comm_avg} is the common-mode voltage of the power router small-signal model,

and v_{diff_avg} is differential-mode voltage of the power router small-signal model injected by the power router. Similarly, the capacitor dynamics of the small-signal model, given by Equation (26), are obtained by substituting the averaged switching functions in Equation (21). The capacitor dynamics can also be obtained in terms of common-mode power and differential-mode power and are given by Equation (27).

$$C_{dc}\frac{d(V_{dc\_avg})}{dt} = i_{diff\_avg} * mi_{diff} * \sin(\omega t + \emptyset_{diff}) - \frac{i_{line\_avg}}{2} * mi_{comm} * \sin(\omega t + \emptyset_{comm}) , \tag{26}$$

$$C_{dc}\frac{d(V_{dc\_avg})}{dt} = \frac{P_{dc\_diff} - P_{dc\_comm}}{v_{dc}}, \tag{27}$$

where $P_{dc\_comm} = \int 0.5 * v_{comm\_avg} * i_{comm\_avg}$,

$P_{dc\_diff} = \int v_{diff\_avg} * i_{diff\_avg}$,

V_{dc_avg} is the DC-link voltage of the small-signal model,

i_{line_avg} is the common-mode current of the small-signal model,

and i_{diff_avg} is the differential-mode current of the small-signal model.

For network analysis, the small-signal model can be represented by series- and shunt-controlled voltage sources, as shown in Figure 3.25. The equations governing the controlled voltage sources are given by Equations (24) - (27).

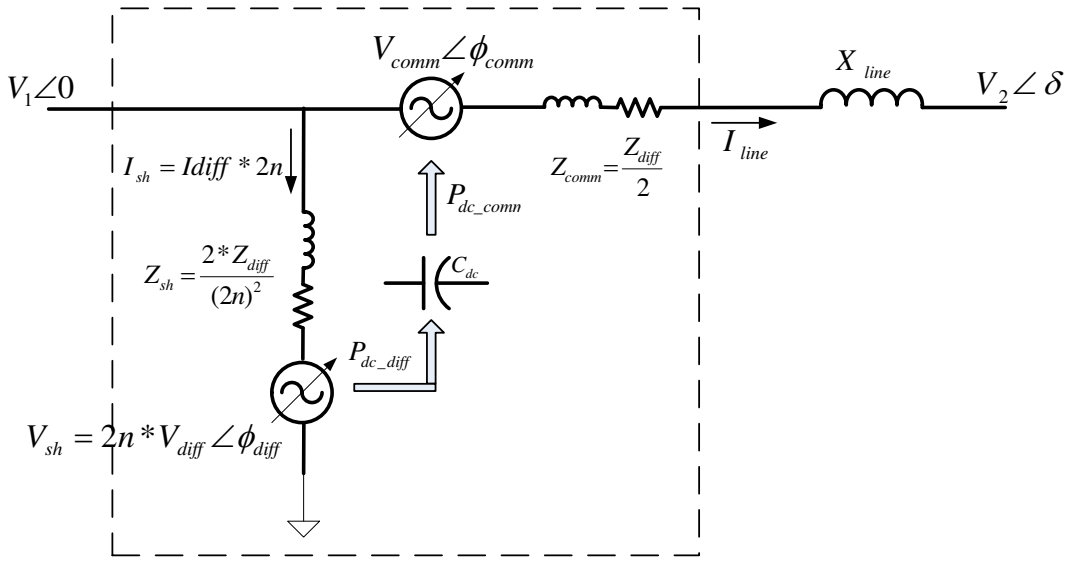


Figure 3.25: Small-signal model of the proposed power router.

The small-signal model is verified by comparing the results with the time-domain model. The results for the time-domain model are obtained by simulating the system in MATLAB/SIMULINK©, with the converter represented by ideal switches. For simulating the small-signal model, the converter is represented by the Equations (24) - (27). The line current and the differential currents, from time-domain and small-signal models, are compared in Figure 3.26. The switching-frequency ripple is not present in the small-signal model, as it is averaged. The dynamics of the DC-link voltage from time-domain and small signal models are compared in Figure 3.27. There is no second-harmonic ripple in the small-signal model, as it is averaged.

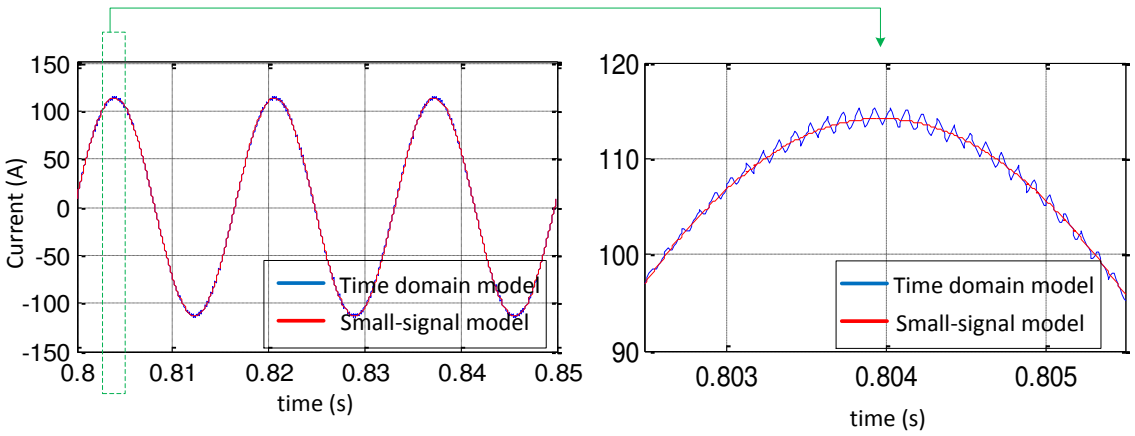


Figure 3.26: Comparison of line current from time-domain and small-signal models.

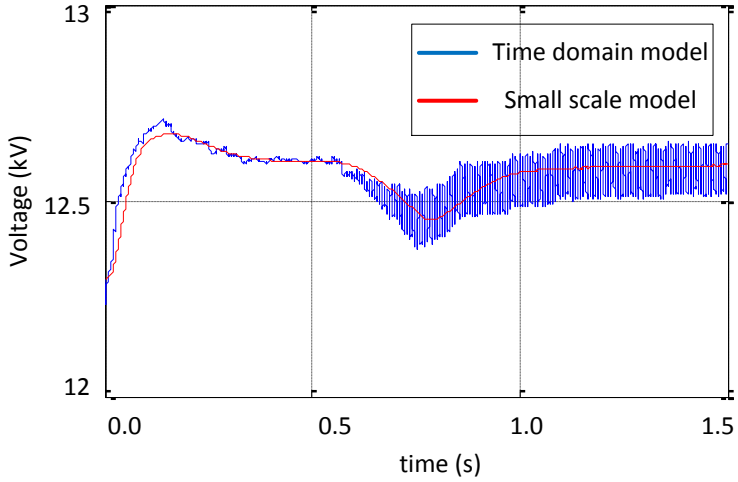


Figure 3.27: Comparison of DC-link voltage from time-domain and small-signal models.

3.9.3 Frequency-Domain Model

In the frequency-domain model, the power router is modeled as active and reactive power injection at either bus, as shown in Figure 3.28. In this model, the dynamics of the DC-link voltage are ignored. The active- and reactive-power equations of the model are given by Equations (28)-(30).

$$P_{ser} = \frac{V_{out} * V_2}{X_{line}} * \sin(\delta + \varphi) \tag{28}$$

$$Q_1 = Q_{1,ser} + Q_{1,sh} \tag{29}$$

$$Q_{2,ser} = \frac{V_2}{X_{line}}(V_2 - V_{out} * \cos(\delta + \varphi)) \tag{30}$$

where $Q_{1,ser} = \frac{V_{out}}{X_{line}}(V_{out} - V_2 * \cos(\delta + \varphi))$,

$Q_{1,sh} = \frac{2nV_1}{2X_{diff}}\left(2nV_1 - V_{diff} * \cos(\delta + \emptyset_{diff})\right)$,

$V_{out} = \sqrt{(V_1^2 + V_{conv}^2)}$,

$\varphi = \tan^{-1}\left(\frac{V_{conv} * \sin\theta}{V_1 + V_{conv} * \cos\theta}\right)$,

P_{ser} is the active power injection at sending-end bus,

Q_1 is the reactive power injection at sending-end bus,

$Q_{2,ser}$ is the reactive power injection at receiving-end bus,

V_1 is the sending-end voltage,

V_2 is the receiving-end voltage,

δ is the phase angle between the two buses,

V_{conv} is the magnitude of PR injected series voltage,

θ is the phase of PR injected series voltage,

X_{line} is the line impedance,

V_{diff} is the magnitude of power router differential voltage,

$\emptyset_{diff}$ is the phase of power router differential voltage,

X_{diff} is the differential impedance,

and n is the tap ratio.

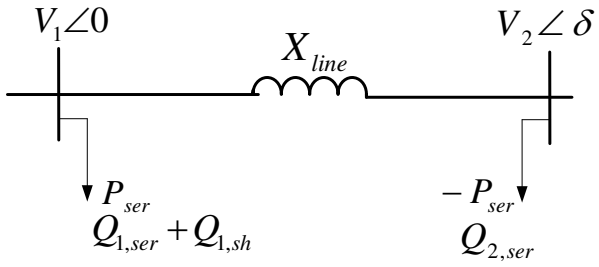


Figure 3.28: Frequency-domain model.

3.10 Conclusion

A power router for dynamic control of active/reactive power in a meshed network is presented. The controller structure, principle of operation, and control range are presented. The power-flow-control ability is demonstrated through simulation results. It was shown that the proposed PR can achieve power flow control at a fractional cost compared to the classical UPFC. A 50 kVA lab prototype is built, and results at 50 kW demonstrate the functionality and advantages of the proposed power router. The fractional rating of the converter obtained through its fractional voltage rating gives the proposed converter a unique advantage in scaling for transmission level voltages, providing a simplified, cost-effective method for power flow control.

CHAPTER 4

FAULT MANAGEMENT

Ensuring reliable operation of the proposed power router, which is designed for utility applications, is essential. In the proposed power router, unlike the UPFC or the SSSC, the semiconductor devices are directly connected in series with the line. The direct series connection of semiconductor devices exposes them to fault currents. The fault currents can be of the order of 20-40 kA for 10 cycles, which is the typical time period before the line protection acts. Available fast turn-off semiconductor devices, such as IGBTs, can handle ten times the rated current for 10 μs. Thus, a 1200 IGBT, the largest available, can handle a peak fault current of 12 kA for only 10 μs, which is not a sufficient time for the protection device to operate. To avoid converter damage, it is necessary to isolate the converter from the fault current. Similarly, the basic grid operation needs to be restored by isolating the grid from the converter faults.

In this section the converter response for various faults and the system parameters that can be used for fault detection are presented through simulation studies. A three-tier protection scheme to avoid single point-of-failure is proposed. The detailed design and operation of the protection mechanism is also presented.

4.1 Protection Philosophy

The proposed power router consists of a fail-normal switch that can provide a bypass path for the line current. The bypass path will isolate the FR-BTB converter from the grid faults and will also isolate the grid from any internal faults in the converter. The reliability of a converter based on active devices will typically be lower than the electric grid, which is predominantly a passive structure. Hence, by restoring the grid to its passive mode when the converter sees internal faults, the fail-normal switch assures that

the system reliability is not impacted even when a lower reliability converter is used to impact the system performance. This approach strikes a good balance between system reliability and performance at lowest cost. In addition, by isolating the converter from grid faults, the fail-normal switch will protect the converter elements from being stressed with sustained fault currents.

4.2 Protection System Description

The detailed schematic of the proposed power router, with the protection elements highlighted in bold, is shown in Figure 4.1. The two main protection elements are the fail-normal switch and the DC-link voltage limiting chopper. The DC-link can accrue additional energy during the flow of line fault currents. The DC-limiting chopper dissipates the excess energy in the DC-link capacitor and limits the voltage across the devices. Also the chopper is used to discharge the DC-link capacitors during the shutdown.

The fail-normal switch is connected in shunt with the power converter and it consists of an antiparallel SCR and a passive switch. In case of a fault either in the system or in the converter, the fail-normal switch provides the bypass path for the line current, thereby isolating the converter from the network. The SCR will provide the fast response time in the range of μs and will carry line/fault current for the initial few cycles. The passive switch, which has a response time of few cycles, will provide the bypass path on a steady state basis. The impedance of the passive switch is substantially less than that of the SCR, and hence will provide a low-loss path for continuous operation. Effectively, the combination of SCR and passive switch will provide fast dynamic response, low-loss operation capability, and redundancy to assure safe bypass operation. The filter capacitor C_f will also act as a SCR snubber capacitor to limit the dv/dt of the SCR. The filter capacitor discharges into the SCR when the SCR is turned on. The inductor L_{SCR}

connected in series with C_f will limit the SCR di/dt. The combination of C_f and L_{SCR} can resonate and hence a resistor R_{SCR} is connected in series to provide damping.

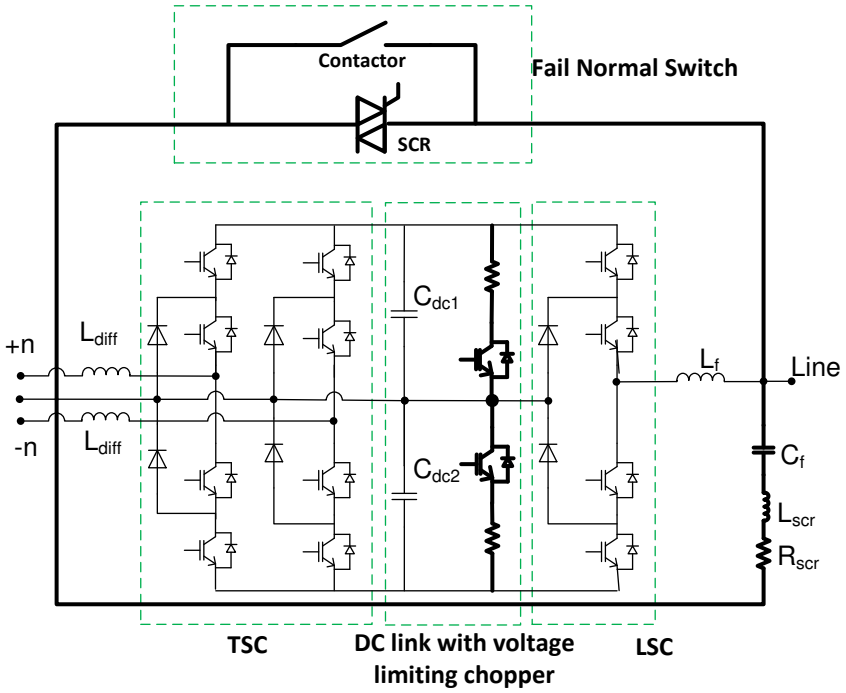


Figure 4.1: FR-BTB converter with protection elements highlighted.

4.3 Protection Scheme

The protection scheme for the proposed power router is shown in Figure 4.2. It consists of three-tier monitoring and protection systems. The three systems interact with each other but are also designed to act independently. The reason for multiple and independent protection schemes is to avoid single point-of-failure. The three schemes have some common monitoring variables, but are prioritized by choosing increasingly higher limits for the protection scheme to act.

The first one is the main controller which can be implemented on a FPGA or the DSP. The main controller monitors the bus voltage, line current, the DC-bus voltage, the filter inductor current and the filter capacitor current. On detection of fault, which is indicated by abnormal current or voltage, the main controller disables the converter switches and also sends a command to the SCR gate drive. In case of an overvoltage on

the DC-link, the main controller will activate the limiting chopper. The main controller also monitors the SCR current to evaluate the SCR status. If the SCR is turned on at any time, except the initial startup period, the main controller turns the converter pulses off.

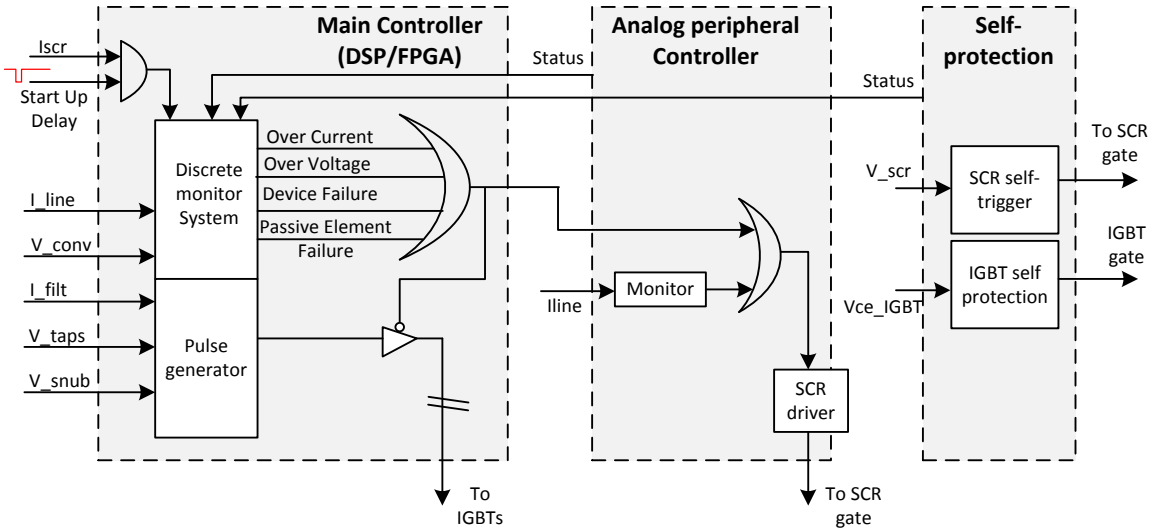


Figure 4.2: Power-router protection scheme

The second controller in the three-tier protection system is the peripheral controller. It is an analog based system which is powered by the voltage across the taps. The peripheral protection system is designed to act in case of failure of the main controller to detect a fault. The peripheral protection system monitors the filter inductor current and on detection of fault issues a command to turn on the SCR. The set point on the filter current fault detection is chosen to be at a higher value than the main controller to accord a higher priority to the master controller.

The third element in the three-tier protection system is the self-monitoring circuit for the active devices. The IGBTs are provided with a fault monitoring circuit, which would turn off the IGBT on detection of higher than nominal IGBT current. Similarly, the SCR is provided a self-triggering circuit, which would turn on the SCR on detection of abnormally higher voltages across the SCR. The third tier protection system is independent of the other two systems and have higher set points compared to the main and the peripheral protection systems.

The intercommunication between each of the protection system is based on active low logic, which will make the protection unit assume a fault in the case of interconnection failure. The three-tier protection system will avoid a single point-of-failure of the protection scheme by providing a backup for failure of each critical element in the protection scheme. The critical elements and the protection logic in case of element failure are shown in Table 4.1. As it is not possible to design for multiple cascaded failures, the table shows the backup plans considering one failure at a time. The protection logic to be implemented in the three-tier protection scheme is shown in Figure 4.3. The protection logic is chosen in such a way that any catastrophic failure will not result from any one failure at a time.

Table 4.1: Backup protection plans for failure of protection and sensing elements.

Failure	Backup action
Sensor for Line current/ Bus voltage/ filter voltage	Peripheral controller will continue to monitor line faults while the algorithm on the main controller can detect feedback failure and shutdown the system.
Filter inductor current sensor	Main controller can continue monitoring faults
Power supply for main controller	The peripheral controller turns on the FN switch to enter by-pass mode.
Power supply for the peripheral controller	The SCR gate drive turns on the FN switch to enter by-pass mode.
Power supply for IGBT gate drives	Main controller detects a converter fault and enters by-pass mode.
Control software delay/failure	Peripheral control will provide protection against faults.
SCR command from the main controller to the peripheral controller	Peripheral controller will detect fault.
SCR command from peripheral controller to SCR gate drive	SCR gate drive will act to enter by-pass mode.
Feedback failure from IGBT gate drives	Main controller assumes a fault and enters by-pass mode.
SCR gate drive	SCR self-triggering circuit will continue to monitoring faults while the main controller detects the gate drive failure.

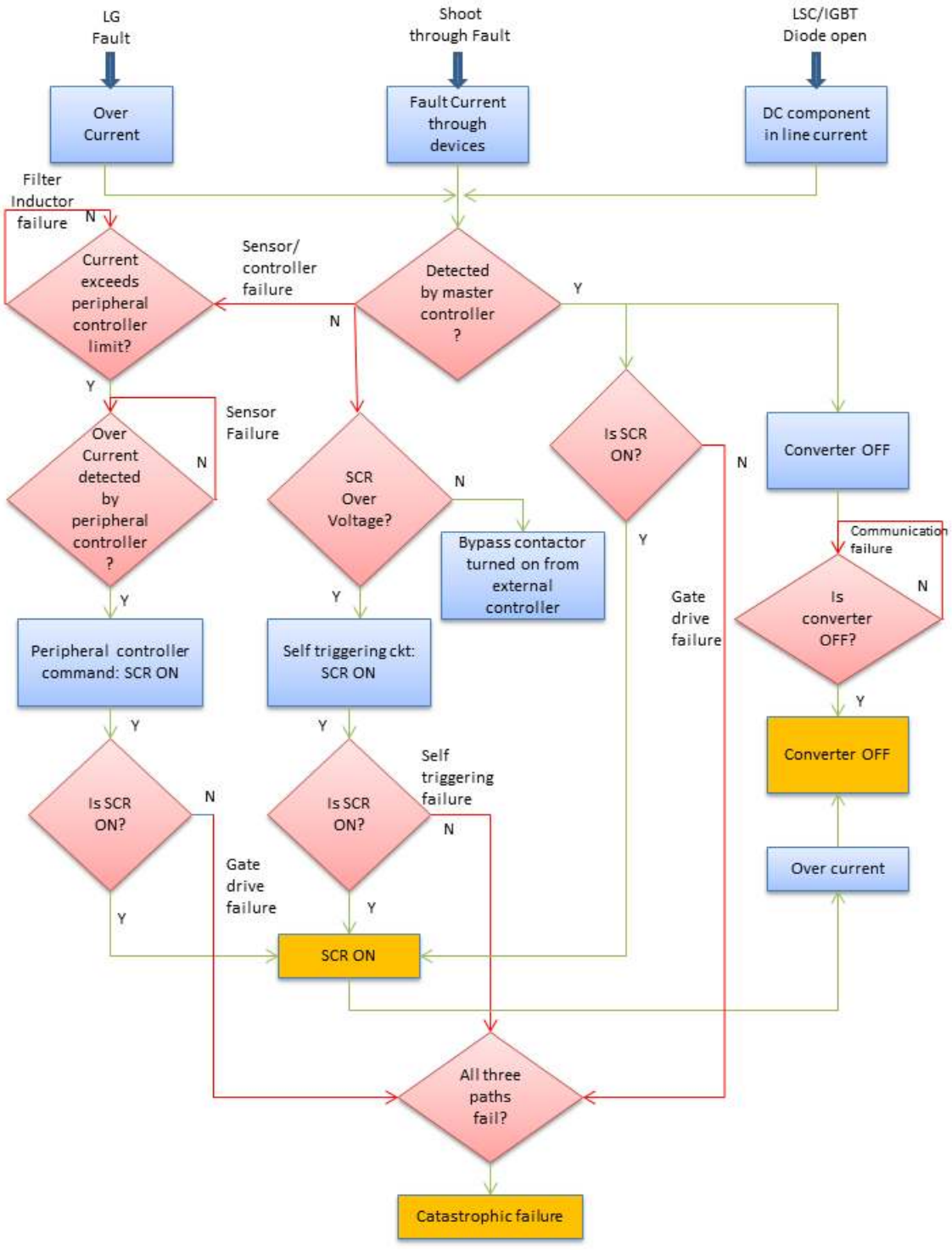


Figure 4.3: Fault protection logic to avoid catastrophic failure.

4.4 Fail-Normal Switch Design

The fail-normal switch is a critical element in the power-router protection scheme, requiring robust design. The selection of individual components of the fail-normal switch is described below.

4.4.1 SCR Selection

SCRs are capable of handling large fault currents. The popular application of SCRs for handling large fault currents is in a series-type, solid-state fault-current limiter (SS-FCL) [108]. In an SS-FCL, the thyristors are used to carry peak fault currents up to 40 kA for 8 ms [109, 110]. The typical response time, from the time of fault initiation to the time of device activation, is in the range of 40-60 μs [109, 110]. SCR was also used as bypass switch in TCSC and TPSC applications [111].

The SCR selection is primarily determined by the current and the voltage rating. In the fail-normal switch application, the SCR carries the fault current for a few cycles and hence the SCR selection can be based on transient current rating. The SCR should be electrically, thermally, and mechanically capable of handling the peak fault current for a duration determined by the turn-on delay time of the mechanical switch. The SCR should also be capable of handling the peak voltage across the converter filter capacitor, which also acts as a SCR snubber capacitor.

4.4.1.1 Filter/ Snubber Capacitor Selection

The filter capacitor which is connected in shunt with the SCR also acts as a snubber capacitor for the SCR. As a snuber capacitor, C_f limits the dv/dt stress on the SCR. As will be explained in the line-ground fault analysis, the fault current initially flows through C_f leading to increase in voltage across it. The minimum value of C_f is limited by the maximum allowable voltage across C_f as given by Equation (31).

$$C_{f,min} = \frac{V_{Bus,pk} * (\Delta t)^2}{2 * \left(V_{cf,pk} - V_{conv\_inj,pk}\right) * L_{flt}}, \tag{31}$$

where $\Delta t = \frac{L_{flt} * I_{flt,lmt}}{V_{Bus,pk}}$,

$V_{Bus,pk}$ is the peak bus voltage,

L_{flt} is the fault line impedance,

$V_{cf,pk}$ is the maximum allowed voltage across C_f,

$V_{conv\_inj,pk}$ is the peak voltage injected by the FR-BTB converter,

$I_{flt,lmt}$ is the fault current limit at which the SCR is triggered to turn on.

A small capacitor value will result in a higher voltage rating for both the capacitor and the SCR, while a large value will result in large current in the SCR. When the SCR is turned on, C_f is shorted through the SCR resulting in a large current. The selection criterion for the capacitor is given by Equation (32a).

$$C_{f,min} = \frac{I_{flt,pk} * \Delta t}{\Delta V_{Cf}}, \tag{32a}$$

$$C_{f,max} = \frac{L_{scr} * I_{scr,pk}^2}{\left(V_{cf,nom} + \Delta V_{Cf}\right)^2}, \tag{32b}$$

where $I_{flt,pk}$ is the peak fault current expected,

Δt is the time between the fault incidence and fail-normal switch turn on,

L_{scr} is the SCR di/dt limiting inductor,

$I_{scr,pk}$ is the peak SCR current allowed,

ΔV_{Cf} is the voltage rise allowed on C_f, and

$V_{cf,nom}$ is the nominal voltage across C_f.

4.4.1.2 SCR Inductor Selection

The function of the SCR inductor is to limit the di/dt across the SCR. Hence, the minimum value of L_{SCR} is determined by the maximum di/dt capability of the SCR as given by Equation (33).

$$L_{scr,max} = \frac{V_{cf,pk}}{\frac{di}{dt}, max}, \tag{33}$$

where $V_{cf,pk}$ is the maximum allowed voltage across C_f,

and $\frac{di}{dt}, max$ is the maximum di/dt stress on the SCR. The maximum value of the SCR inductor is determined by its impact on the converter filter performance. The SCR inductor, which is in series with the filter capacitor, can impact the filter capability to absorb high frequency currents. Hence, by choosing $L_{scr} << L_{filt}$, the impact of L_{scr} on filter performance can be minimized.

4.4.1.3 SCR Resistor Selection

The function of the SCR resistor is to damp oscillations caused by the L_{scr} and the C_f when the SCR is turned on. The minimum value of R_{scr} is determined by the value of L_{scr} and C_f as shown in Equation (34).

$$R_{scr} >= 2\sqrt{\left(\frac{L_{scr}}{R_{scr}}\right)}. \tag{34}$$

The value of R_{scr} is limited on the higher side by the steady state losses in resistor because of the capacitor current. The losses in R_{scr} are given by

$$R_{scr,loss} = V_{conv,inj}^2 \omega_1^2 C_f^2 R_{scr} + \left(\frac{V_{dc}/2}{4\sqrt{3}L_f F_{sw}}\right)^2 R_{scr} \tag{35}$$

where $R_{scr,loss}$ is the loss in the SCR resistor,

$V_{conv,inj}$ is the maximum converter injection,

ω_1 is the fundamental frequency in radians,

V_{dc} is the DC bus voltage,

L_f is the filter inductor, and

F_{sw} is the switching frequency in Hz.

4.4.2 SCR Self-Triggering Circuit Design

In the protection scheme it was stated that the self-triggering circuit for the SCR is the final mode of protection when the main controller and the peripheral protection system fails. Hence, to ensure robust operation of the self-triggering scheme it is designed to have the following features:

- Self-powered, thereby, avoiding dependence on external power sources.
- Self-triggered at a preset value.
- Minimal components and simplistic design to reduce probability of failure.

A number of self-powered and self-triggered gate drives are available, with each one specific to the application [112]. Of particular significance is the SCR gate drive scheme suggested in [113, 114], which is self-powered, uses minimal number of components, but is triggered externally. The gate drive scheme has been modified to implement the self-triggering feature. The proposed gate drive scheme for each SCR in the fail-normal switch is shown in Figure 4.4. It consists of a self-powered block and self-triggered block.

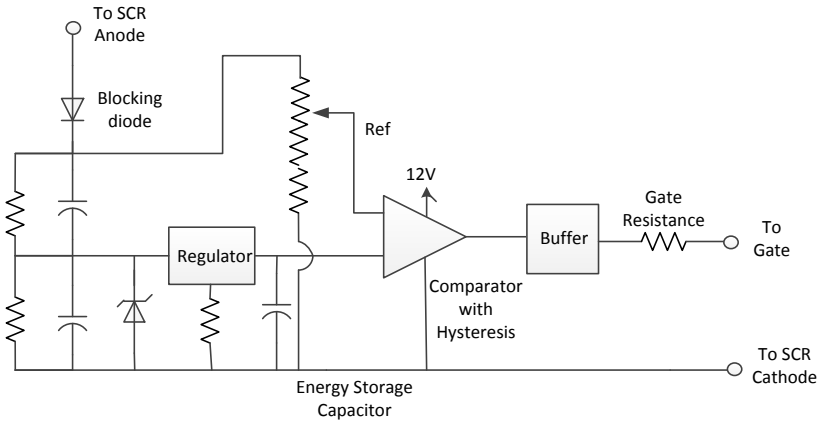


Figure 4.4: SCR self-powered and self-triggering gate drive.

In the self-powered block, the gate drive draws power from the SCR blocking voltage. The SCR blocking voltage is stepped down to control voltage by using a voltage divider. In the self-triggering block the SCR voltage is compared with a preset reference

value to detect a fault and trigger the SCR. The selection criterion for various components of the proposed SCR self-powered and self-triggering gate drive is given below:

4.4.2.1 Capacitor Divider

The capacitor divider consists of two capacitors, C_l and C_h, with voltage sharing resistors, R_l and R_h, connected across the capacitors. The value of C_l and C_h are selected to meet the following design criterion:

- The voltage across C_l is always greater than the control voltage (5 V/12 V) by a sufficient margin (2 V) for all voltages greater than half the set point voltage at which the self-triggering circuit is set to turn the SCR on.
- The effective capacitance of C_l and C_h is much lower than C_f to ensure the most of the fault current flows through C_f and not C_l and C_h.

The value of R_l and R_h are chosen in such a way that the current in the resistors is at least five times the leakage current in the capacitors to ensure static voltage sharing between both the capacitors. The leakage current of the capacitors will be different and for choosing the R_l and R_h, the higher of the two leakage currents should be used. The criterion for selecting C_l, C_h , R_l and R_h are given below.

$$\frac{C_h}{C_l + C_h} * \frac{V_{scr,set}}{2} = V_{ctrl} + 2\ V \tag{36}$$

$$\frac{C_l C_h}{C_l + C_h} \ll C_f \tag{37}$$

$$\frac{R_h}{R_l} = \frac{C_l}{C_h} \tag{38}$$

$$\frac{V_{scr,set}}{R_h} \gg I_{leakage,C} \tag{39}$$

where C_l is the lower capacitor in the voltage divider,

C_h is the higher capacitor in the voltage divider,

R_l is the voltage sharing resistor across C_l ,

R_h is the voltage sharing resistor across C_h ,

$V_{scr,set}$ is the voltage at which the SCR is triggered on by the gate drive, and

$I_{leakage,C}$, is the leakage current of the C_h and C_l, whichever is higher.

4.4.2.2 Voltage Regulator

The function of the voltage regulator is to maintain a steady control voltage to the self-triggering circuits, irrespective of load and supply fluctuations. A linear regulator is better suited to this application because of the relatively lower load (10 mA), less noise and higher reliability compared to switching regulators. The power rating of the linear regulator can be calculated by Equation (40).

$$P_{loss,LVR} = \frac{V_{scr,set}}{2} * I_{el,off\_state} \tag{40}$$

where $P_{loss,LVR}$ is the power loss in the linear voltage regulator,

$V_{scr,set}$ is the voltage at which the SCR is triggered on by the gate drive, and

I_{el,off_state}, is the current drawn by the electronic load in the self-triggering circuit with the gate off. The linear regulator is protected from high voltage transients by a voltage clamp at its input. The voltage clamp is typically implemented with a zener regulator.

4.4.2.3 Energy Storage Capacitor

The function of the energy storage capacitor is to deliver the required transient energy at the time of SCR gate turn on without resulting in significant drop in gate voltage. The linear regulator has a time delay in responding to the load fluctuations and hence the energy storage on the regulator output is used to absorb the load fluctuations. The value of capacitor C_{ES} to supply gate energy at turn on with the gate voltage dropping down by not more than 1 V is given by Equation (41).

$$C_{ES} = \frac{2V_G^2}{R_G} * T_{pulse} \tag{41}$$

where C_{ES} is the energy storage capacitor,

R_G is the gate resistor,

V_G is the gate driving voltage, and

T_{pulse} is the SCR turn-on pulse width. The value of R_G is typically chosen to deliver gate current, which is more than five times the minimum gate trigger current of the SCR.

4.4.2.4 Self-Triggering Gate Drive

The function of self-triggering gate drive is to turn on the SCR when the SCR voltage exceeds a predetermined value. It consists of a comparator and a buffer. The comparator compares the SCR voltage with a reference value to generate on/off signal. The comparator output is then fed to a buffer, which is rated to drive the SCR gate.

Since the proposed SCR driving scheme is a self-powered circuit, it is necessary to optimize gating energy. Gating energy depends on the pulse width, required gate voltage and the gate current. While the gate voltage and gate current are available directly from the data sheet, the gate pulse width can be calculated from the SCR turn-on delay time and rise time. Once the SCR current rises above the latching current, the SCR will stay on without the gate supply.

4.4.3 Experimental Evaluation of Self-Triggering SCR Gate Drive

The functionality of the proposed self-powered and self-triggering gate drive is experimentally evaluated. The schematic of the experimental setup to test the proposed gate drive is shown in Figure 4.5 (a) and the picture of the experimental setup is shown in Figure 4.5 (b). The experiment setup consists of 1 kV 1-ph source, 1700 V 400A SCR and the proposed gate drive. The gate drive is designed to power form the SCR blocking voltage and trigger the SCR when the voltage exceeds 600 V. The current in the SCR at turn on is limited by a load resistor of 100 Ω.

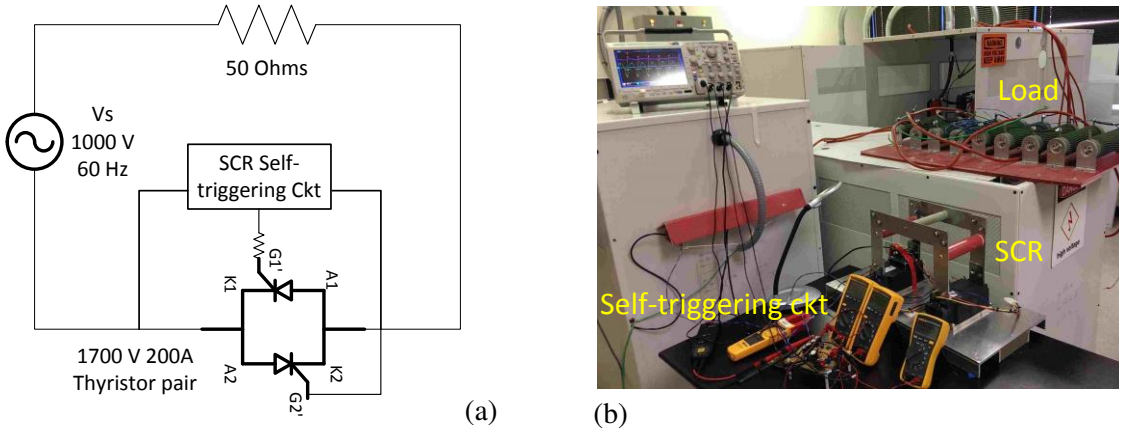


Figure 4.5: (a) SCR self-triggering circuit test schematic. (b) Picture of SCR self-triggering experimental setup.

The experimental results of the SCR voltage, current are shown in Figure 4.6. The results show that the SCR self-triggering circuit turns the SCR on when the voltage exceeds 600 V as designed. The self-triggering and self-powered circuit behavior at gate turn on is shown in Figure 4.7. The 12 V bus of the self-powered circuit drops by 1 V because of the gate current at SCR turn on and remains stable thereafter.

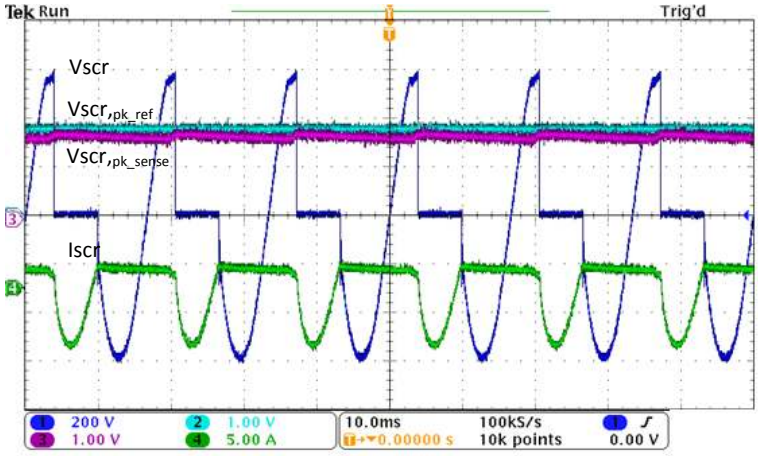


Figure 4.6: SCR self-triggering test results

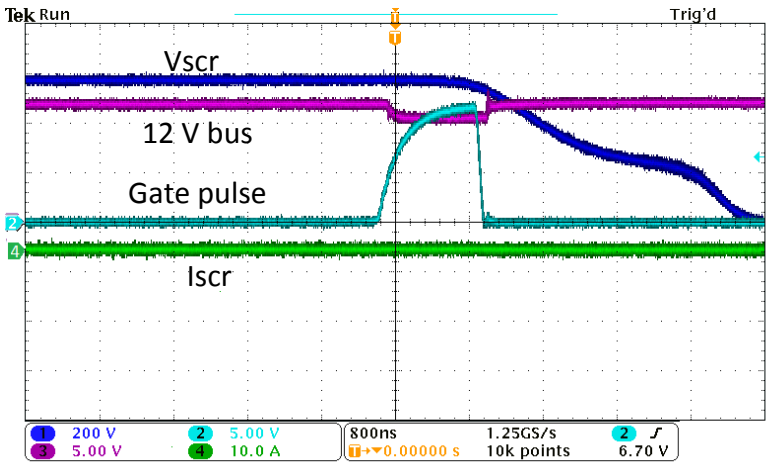


Figure 4.7: SCR gate self-powered circuit results.

4.5 Fault Analysis

4.5.1 Line-Ground (L-G) Fault Analysis

The test system used to simulate the converter and the fail-normal switch operation under line-to-ground fault is shown in Figure 4.8. The test system consists of a 138 kV 2-bus system connected by a 30 mile line (0.17+j0.79 Ω/mile). The power router, which has a control range of +/- 4 kV, is installed at the midpoint of the line. The system is simulated for a zero impedance L-G fault next to the converter for different system conditions such as bus voltage, injected voltage, and the line current. The results presented here correspond to the worst case response time before which the protection mechanism should operate to limit the stress on the converter.

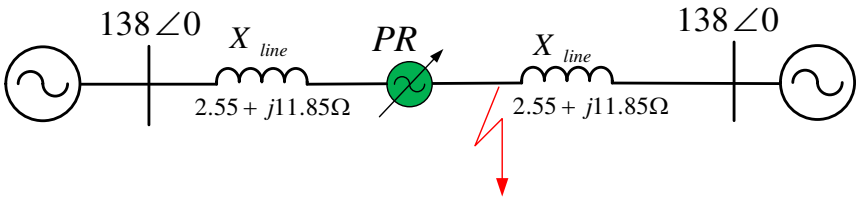


Figure 4.8: Test system for L-G fault analysis

4.5.2 Fail-Normal Switch Operation

The FR-BTB converter and the fail-normal switch response for the line fault are shown in Figure 4.9. The fault has occurred at t= .204 s and on detection of fault the

converter switches are turned off and the fail-normal switch is turned on. Once the SCR turns on, the fault current is now transferred to the SCR. The passive switch gets turned on after a cycle and the fault current in the SCR is now transferred to the passive switch. The fault current will flow through the passive switch till it is cleared by the external breakers on the line. The process ensures that there is a continuous path for the fault current at all instants and also the converter is not stressed with large line-fault currents.

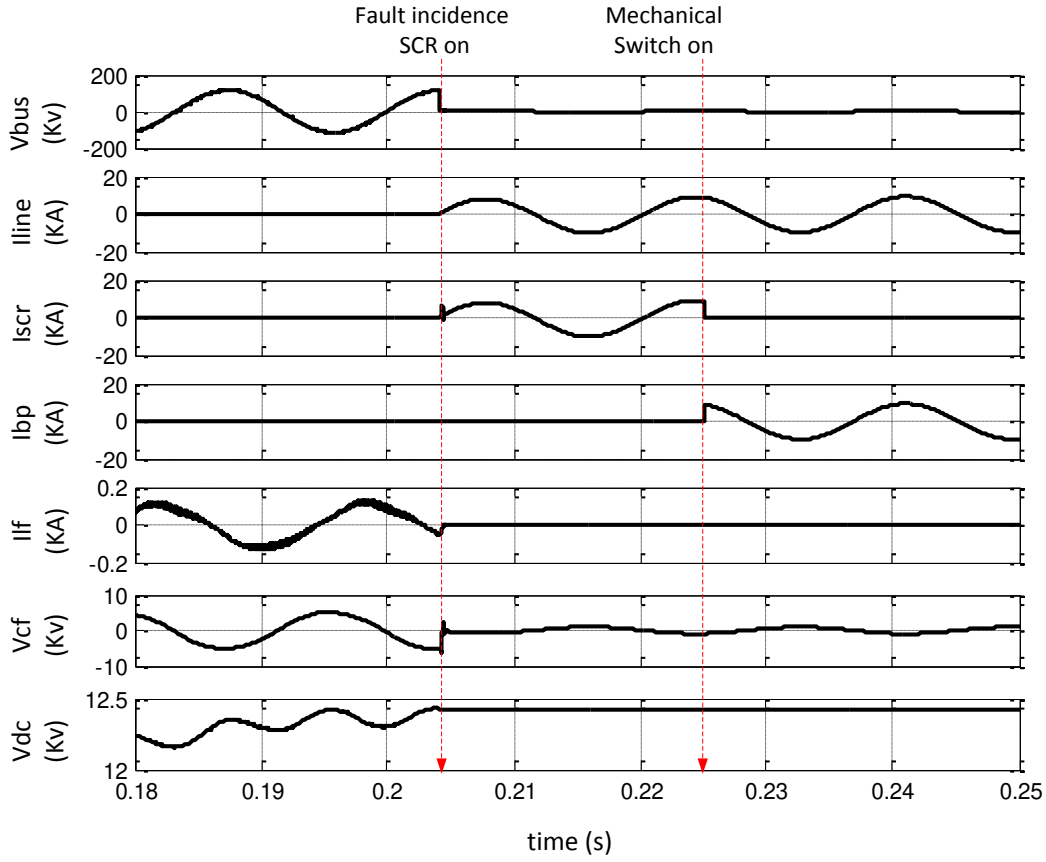


Figure 4.9: Fail-normal switch operation for L-G fault.

On fault incidence, the PR transient response depends on the three-tier protection system. Three test cases for the transient analysis are presented here. In Case 1, the main controller is assumed to detect the fault, turn off the converter and turn on the SCR. In Case 2, the main controller detects the fault and turns off the converter, but fails to turn on the SCR. The SCR is turned on by the self-triggering circuit. The Case 3 is similar to Case 2 except that the main controller turns off the converter after the SCR is turned on.

4.5.2.1 Case 1

The transient response of the converter and the SCR during the fault is shown in Figure 4.10. The fault has occurred when the bus voltage is at its positive peak and the converter injected voltage is at its negative peak. On fault occurrence, the line current starts to increase at a rate determined by the line impedance. The protection circuit gets triggered by either the over current or the over voltage. In this case, the protection mechanism is triggered when the current reaches 500 A, which is twice the nominal current peak. The fault current initially flows through the filter capacitor because for the transient currents the capacitor will provide low impedance compared to the inductor as shown in Figure 4.11. It implies that the converter switches are not stressed by the fault current. The flow of fault current will result in increase of the capacitor voltage.

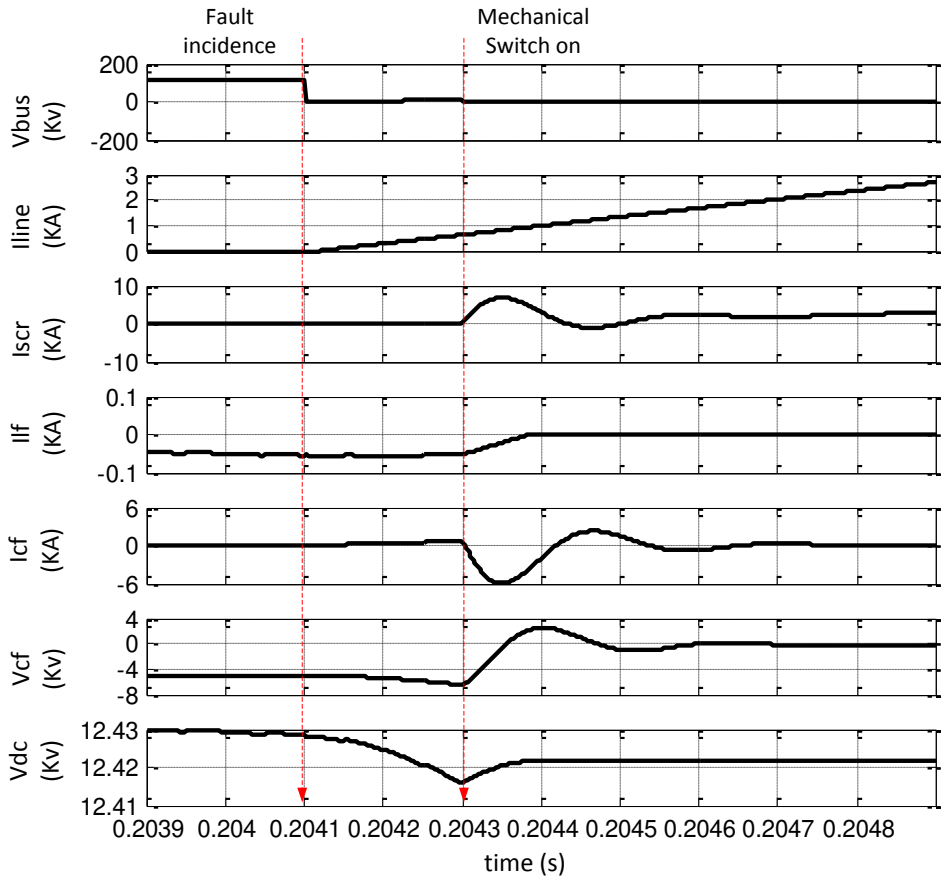


Figure 4.10: L-G Fault Case 1: Power router response with the converter turned off and the SCR turned on by the main controller.

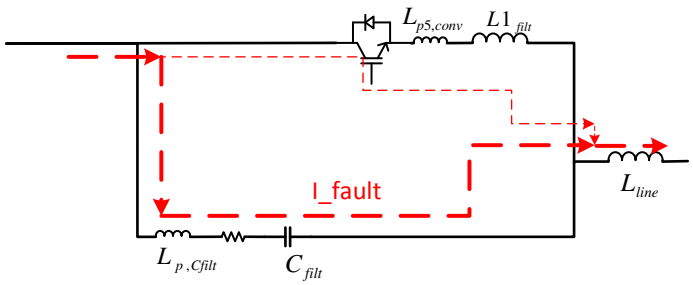


Figure 4.11: Initial transient flow of L-G fault current through the FR-BTB converter

The fault is detected 200 µs after the occurrence of the fault. The capacitor voltage has increased by 1 kV to 6.5 kV because of the flow of the fault current through it for 200 µs. On detection of fault the converter switches are turned off and the fail-normal switch is turned on. The SCR is assumed to turn on after a delay of 20 µs, which accounts for the sensor delay, controller delay, and gate drive delay. Once the SCR turns on, the fault current is now transferred to the SCR. Simultaneously, the energy in the filter capacitor and the L_{scr} is dissipated in the SCR and the damping resistor. The L_{scr} will limit the di/dt stress on the SCR caused by the filter capacitor discharge.

Isolation of the converter from line faults is critical, and hence it is necessary to consider all protection mechanism failure modes. In this case, the protection mechanism failure can be any or all of the following: current sensor failure, current sensor to controller communication failure, controller to SCR gate drive communication failure, and SCR gate drive failure. In all the above cases, the SCR will not turn on even when a fault has occurred. As described in the fail-normal design, the last line of protection in this case would be the SCR self-triggering circuit. The SCR self-triggering circuit monitors the SCR voltage, which is the same as the filter capacitor voltage, and when it exceeds the limit, the SCR is turned on. The converter can either be turned off on detection of fault or wait till the SCR is turned on. Case 2 and Case 3 show the converter response in each case.

4.5.2.2 Case 2:

In Figure 4.12, the case where the converter is turned off on detection of fault irrespective of the SCR status is shown. As in the above case, the fault current flows through the filter capacitor resulting in an increase in the capacitor voltage. The converter is turned off once the fault current exceeds 500 A. The self-triggering circuit turns on the SCR when the filter capacitor voltage exceeds 9 kV, which is 50 % more than the nominal voltage of the filter capacitor. Significantly, the converter is not stressed by the large fault current even though the master controller fails to turn the SCR on.

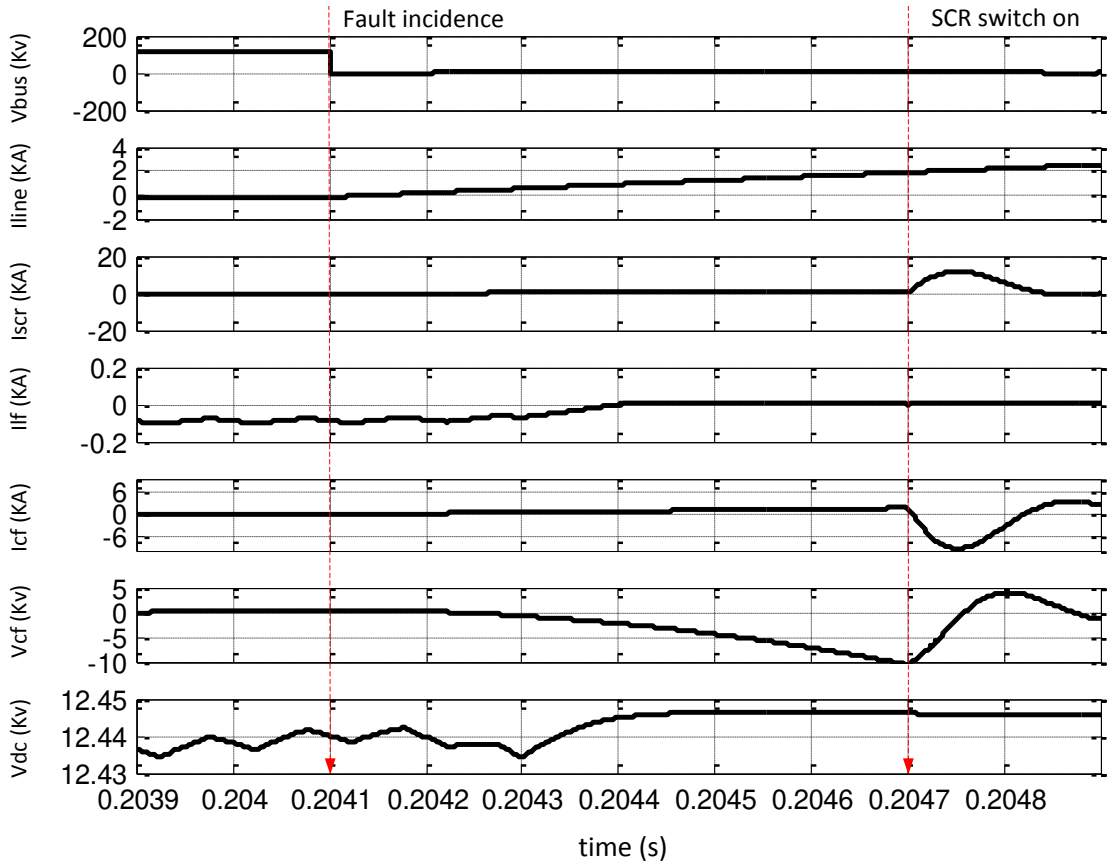


Figure 4.12: L-G Fault Case 2: Power router response with the converter turned off by the main controller before the SCR is turned on by the self-triggering circuit.

4.5.2.3 Case 3:

In Figure 4.13, the case where the converter is turned off only on detection of SCR turn on is shown. The fault current flows through the filter capacitor resulting in an

increase in the capacitor voltage. But now the fault energy is also transferred to the filter inductor indicated by the increasing current in the filter inductor. It implies that in this case, the converter switches are stressed unlike the above cases. Also the filter inductor is not rated to handle such high currents and hence will saturate resulting in device short circuit. The comparison of the Case 2 and Case 3 shows that turning off the converter devices irrespective of the SCR status avoids additional stress on the devices.

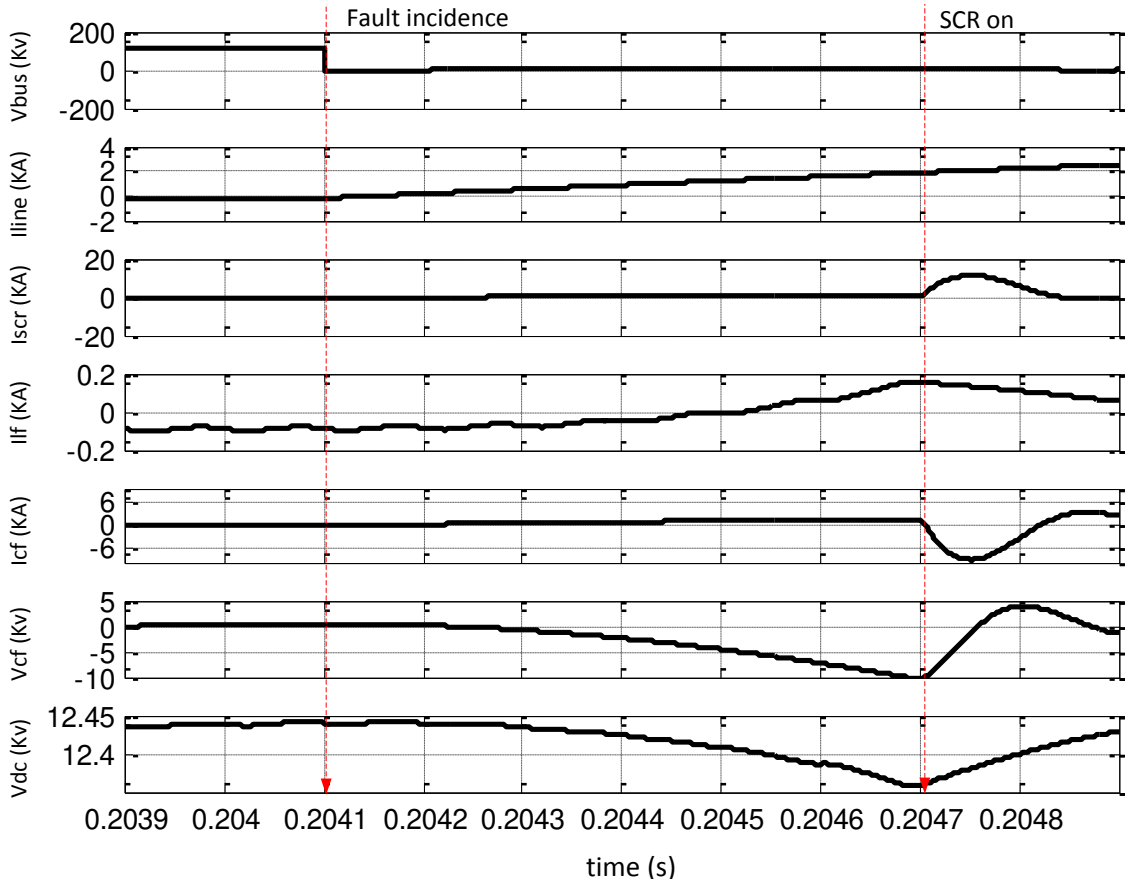


Figure 4.13: L-G Fault Case 3: Power router response with the converter turned off by the main controller after the SCR is turned on by the self-triggering circuit.

4.5.3 Shoot-Through Fault Analysis

In case of an IGBT or a diode short, the DC bus will be shorted and would result in a large current, which is limited only by the parasitic inductance. This type of fault is typically termed as shoot-through fault. A short in the filter capacitor, the filter inductor or any of the differential inductors will also result in a similar fault. The shoot-through

fault can occur because of either the device failure or incorrect switching. In both cases, the healthy device has to be turned off to avoid sustained fault currents, which can destroy the devices and the DC bus. Sustained shoot-through fault currents may also result in fire hazard. As with any fault protection, the shoot-through fault protection scheme also consists of fault detection, fault management, and fault recovery. The shoot through fault can be detected by the following methods:

- Fault sense resistor connected in the load current path.
- Current transformer.
- Desaturation (desat) detection which includes monitoring voltage across the collector and the emitter in the IGBT on state.

The fault sense resistor has the advantage of simple implementation to provide an analog feedback of the current. But the parasitic inductance of the resistor can impact the transient response and significantly, the sense resistor is not isolated from the main power circuit. The current sensor can provide current measurement with required isolation between control and power circuits. But it is difficult to design a current transformer with wide bandwidth sufficient enough to measure fundamental frequency currents and also fast rising fault currents. The desat detection circuit monitors the collector to emitter voltage to detect a fault. In the IGBT on state, the collector-emitter voltage V_{CE} will be low on-state voltage (< 3 V). But when the fault occurs, the device voltage tries to reach the supply voltage resulting in high V_{CE} even in the IGBT on state. The rise in voltage V_{CE} in IGBT on state is used to detect the shoot-through fault. The desat detection circuit is fast because of low inductance, has high bandwidth, and is inexpensive to integrate. The desat circuit is not isolated from the power circuit, and hence the fault management circuit has to be implemented locally.

4.5.3.1 Shoot-Through Fault Management

On detection of fault, the gate voltage can be removed at the fastest rate possible to break the fault current. But a steep fall in IGBT current during turnoff can result in a large voltage across the IGBT because of the parasitic inductance in the circuit. If the di/dt at turnoff and the parasitic inductance is sufficiently high then the resultant voltage can permanently damage the device. In addition, if the gate pulse is turned off even before the IGBT voltage reaches its clamp, the device physics can result in a condition called latch up, leading to permanent damage. To avoid the above two conditions, a two-step approach is usually followed on short circuit detection. In the first step, the gate voltage is reduced to a value where the peak current is limited to be just within the safe-operating area (SOA) of the device. The gate voltage is held at this value till the device voltage reaches the full DC-link voltage. The duration of this period depends on gate resistance, device construction, and device capacitances. It is difficult to calculate this value and it is usually chosen to be the maximum short-circuit withstand time, which is available from the datasheet. Since the current is within the SOA, the device will be able to turn off without any permanent damage. In the second step, the gate voltage is reduced gradually at a much slower rate compared to the first step. The gradual decrease in the gate voltage limits the di/dt of the fault current at the IGBT turnoff. The two step process can be implemented using simple RC circuits either as two decaying exponentials or as a single exponential as shown in Figure 4.14(b). Most commercial gate drives implement a desat detection circuit and make provision for a soft turnoff at a desired rate on fault detection.

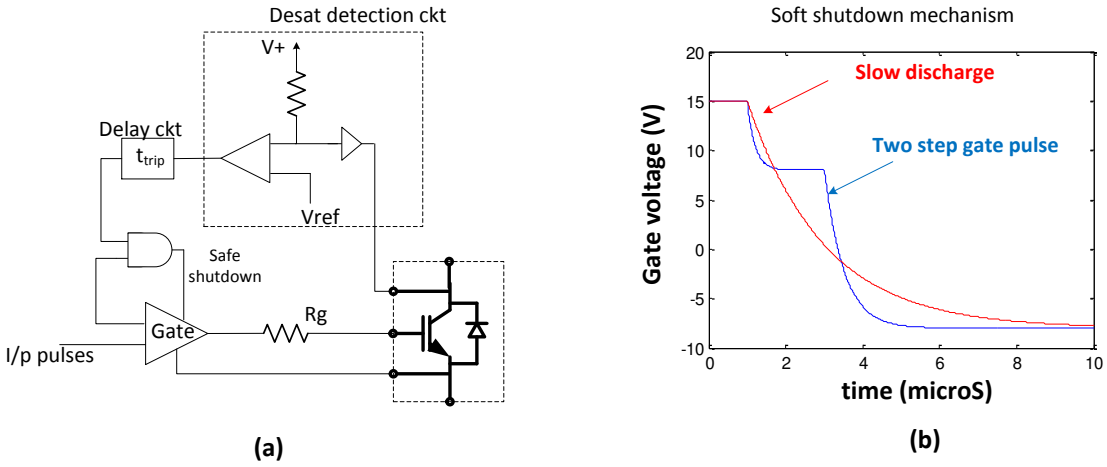


Figure 4.14: (a) Desat detection circuit. (b) IGBT soft turn-off mechanism.

The two step process for fault management is simulated in SABER™ for a typical 17000 V, 200 A IGBT. The test system used for simulation, consisting of a half-bridge converter is shown in Figure 4.15. The parasitic inductances of the switches and the capacitor are assumed to be 100 nH and 1.0 µH respectively.

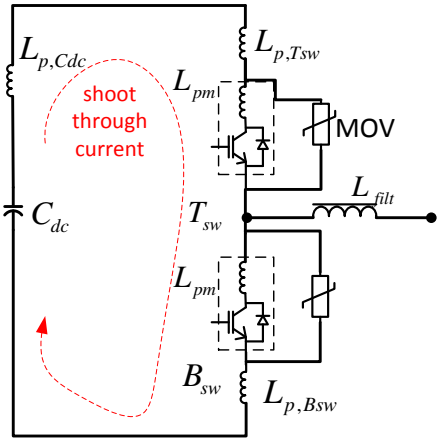


Figure 4.15: Test system for simulating shoot-through fault.

The simulation results for the shoot through fault at device level are shown in Figure 4.16. Before the fault, the top switch T_{SW} is conducting and is carrying a load current of 150 A. At t=2.5 µs, the bottom switch B_{SW} is turned on even with the T_{SW} in on state, resulting in a shoot through fault. The fault current rises at a rate determined by the parasitic inductances. At t=3.9 µs, the desat is detected on the top switch and the gate voltage is reduced to 8 V from 15 V. The reduction in gate voltage reduces the peak

current in the circuit to 500 A. The gate voltage is maintained in this period for 1 µs during which the top switch voltage $V_{CE}\_T_{SW}$ has reached its clamp. The gate voltage is then reduced gradually to a negative bias of -8.0 V to limit the fault current di/dt. By limiting the di/dt of the current, the voltage spike on the $V_{CE}\_T_{SW}$ is controlled to be within the device blocking capability. After the T_{SW} is completely turned off the load current continues to flow though the free-wheeling diode in the B_{SW}.

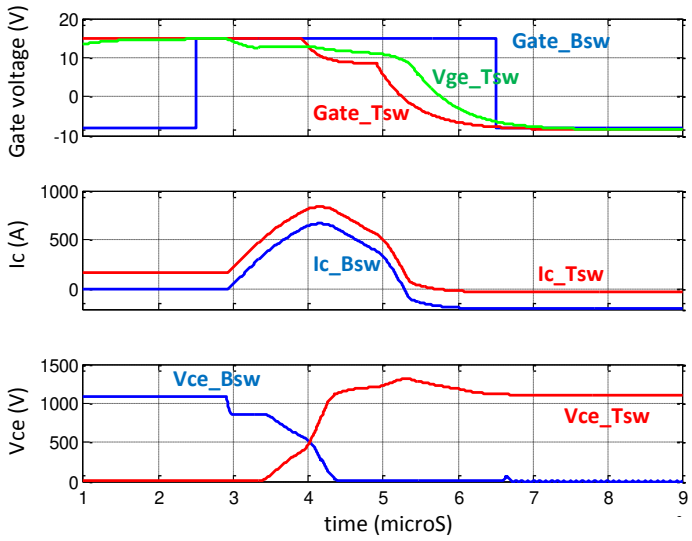


Figure 4.16: Shoot-through-fault protection results.

4.5.3.2 Impact of Shoot-Through Fault at System Level

The same two-bus system described in the previous section is used to simulate the impact of converter shoot-through fault on the grid. The simulation results are shown in Figure 4.17. Without the power router the current in the system was 40 A. With the PR enabled at t = 0.1 s, the line current was increased to 60 A. A converter shoot-through fault is assumed to occur at t=0.305 s. The impact of fault can be seen in the increased DC-bus current. The desat protection scheme of the IGBTs is assumed to safely turnoff the converter and the fail-normal switch is turned on within 10 µS. With the power router bypassed the line current reduces to its earlier value of 40 A without the power router. For the duration of fault, no significant currents or voltage drops are observed on the system. The simulation results have shown that the impact of the converter-shoot through

fault on the system is not significant with the desat protection and fail-normal feature enabled.

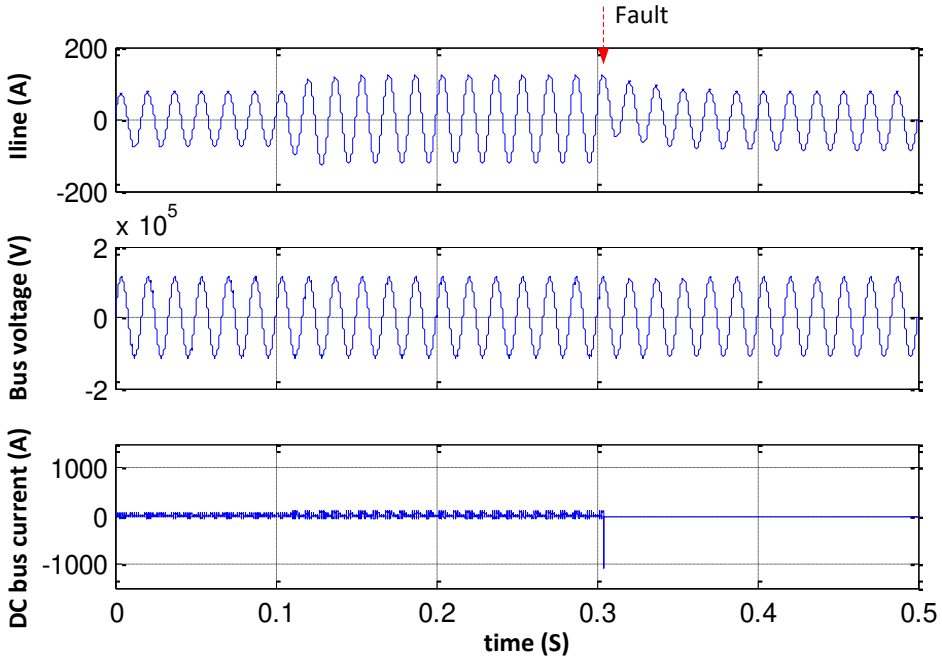


Figure 4.17: Power router response for shoot-through fault on the FR-BTB converter.

It is necessary to consider the case where the main controller fails to turn on the SCR. In this condition, the filter capacitor is connected in series with the line inductor and the equivalent circuit is similar to the fixed series capacitor (FSC) application. The line current will tend to flow through the filter capacitor and depending on the system conditions, the filter capacitor voltage can raise enough for the SCR self-triggering circuit to act. The system conditions determining the filter capacitor voltage in this condition are the line inductance, filter capacitance, and the voltage difference between the two buses. In case the capacitor voltage does not increase enough to trigger the self-triggering circuit of the SCR, then the system will continue to work as in a FSC application. To avoid this situation, a provision to turn on the bypass contactor from an external control circuit, such as the SCADA™ system, has to be implemented.

4.5.4 LSC IGBT/Diode Open

The simulation results for the case where any IGBT on the line-side-converter (LSC) is open either because of the device failure or the gate-drive failure are shown in Figure 4.18. With the IGBT open, the generated LSC injected voltage is non-sinusoidal because of the uneven positive- and negative-voltage injection. The uneven injection will result in a DC component and unwanted harmonics in the injected voltage leading to a DC component in the line current. The line current DC component will lead large fluctuations at fundamental frequency in the DC bus voltage. The large fluctuations in the DC bus voltage will also result in DC injection and harmonics in the differential current. The main controller can detect the LSC IGBT failure by monitoring the DC component in the injected voltage, the DC component in the line current, and the fundamental ripple in the DC bus voltage. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation. In case the main controller fails to detect the fault, the peripheral controller will sense the increasing line current and will turn on the fail-normal switch.

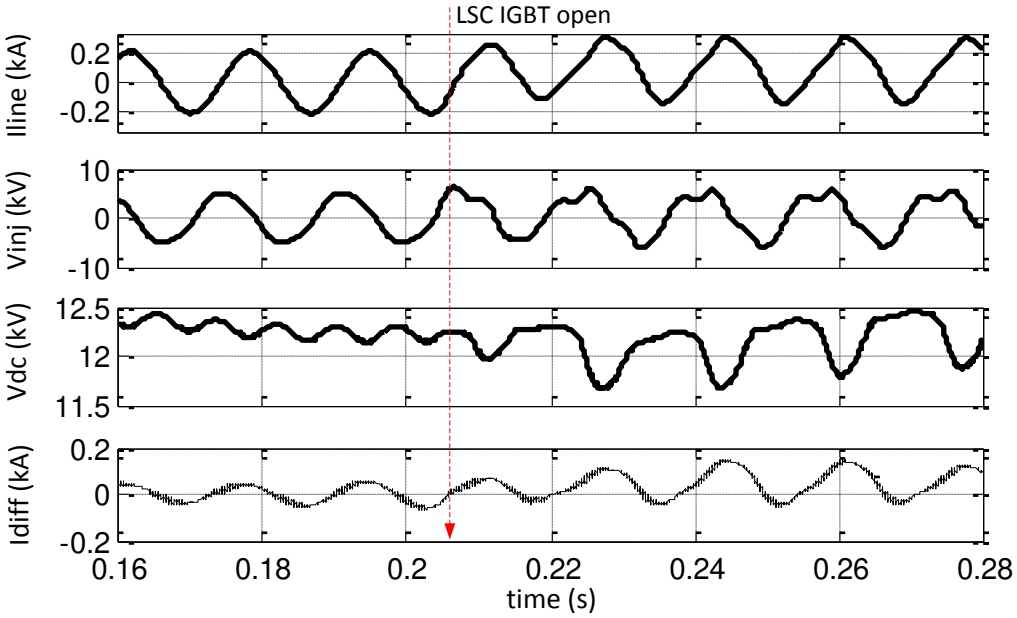


Figure 4.18: Power-router response for the LSC IGBT open fault.

The impact of LSC diode failure is similar to that of the LSC IGBT failure, resulting in DC injection in the line current. The simulation results for the LSC diode failure case are shown in Figure 4.19. As in the case of the LSC IGBT failure, the main controller can detect this type of fault by monitoring the converter injection voltage and the line current. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation.

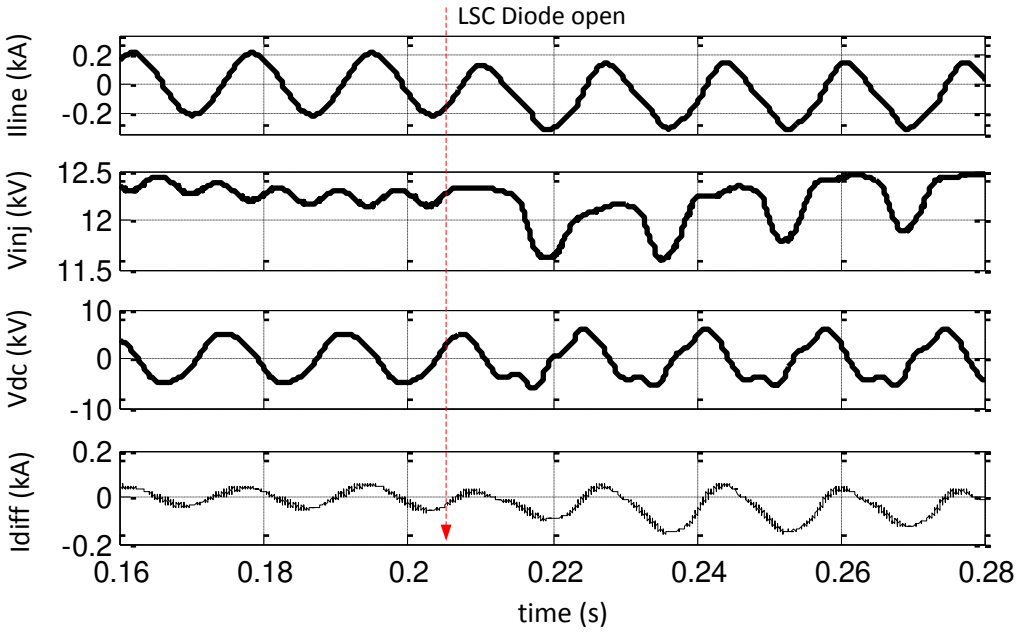


Figure 4.19: Power-router response for the LSC diode open fault.

4.5.5 TSC IGBT/Diode Open

The simulation results for the case an IGBT on the TSC is open either because of the device failure or the gate drive failure are shown in Figure 4.20. With the IGBT open, the TSC generated voltage is not sinusoidal and will result in a DC component and unwanted harmonics in the differential current. The TSC loses DC bus control resulting in either increase or decrease in the DC bus voltage depending on the system conditions. The impact on the LSC converter depends on the DC bus voltage. If the DC bus voltage drops by a significant value, then the maximum voltage injected by LSC will also decrease and the LSC may lose power-flow controllability. The main controller can detect the TSC

IGBT failure by monitoring the DC-bus voltage and the DC component of the differential current. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation. In case the main controller fails to detect the fault, the DC bus voltage will continue to either increase or decrease. In either case, the increased differential current is detected by the peripheral controller, which will turn on the fail-normal switch.

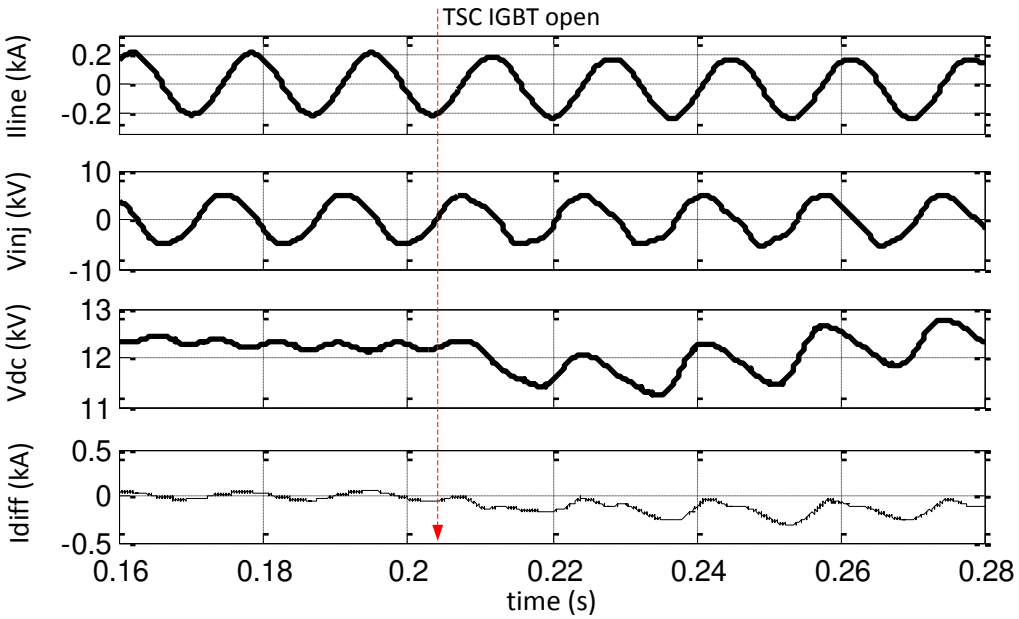


Figure 4.20: Power-router response for the TSC IGBT open fault.

TSC diode failure has a similar impact to that of the TSC IGBT failure, causing loss of DC-bus voltage control resulting in increase or decrease of DC-link voltage. The simulation results for the TSC diode failure case are shown in Figure 4.20. The main controller can detect this type of fault by monitoring the DC-bus voltage and the differential current.

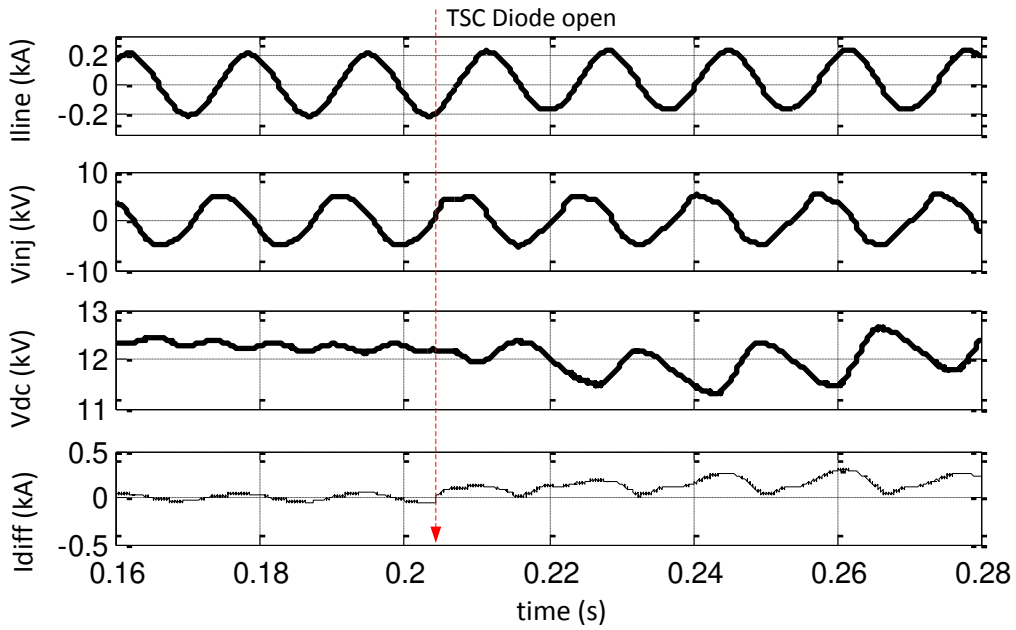


Figure 4.21: Power-router response for the TSC diode open fault.

4.5.6 Open Filter Inductor

The simulation results for the case where the filter inductor fail open are shown in Figure 4.22. With the filter inductor open, the converter cannot inject any voltage in the line. In this condition, the filter capacitor, effectively, acts as a series capacitor as in a FSC application. The voltage across the filter capacitor will now depend on system conditions such as line inductance and voltage difference between two buses. The main controller can detect this type of fault by monitoring the filter inductor current and the filter capacitor voltage. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation. In case the main controller fails to detect the fault, the filter capacitor voltage monitored by the SCR self-triggering circuit will protect the system from over voltages. If the filter capacitor voltage does not exceed the SCR self-triggering circuit set point, then the system will continue to work as in a FSC application until it is bypassed by the contactor, which has to be operated from an external control circuit.

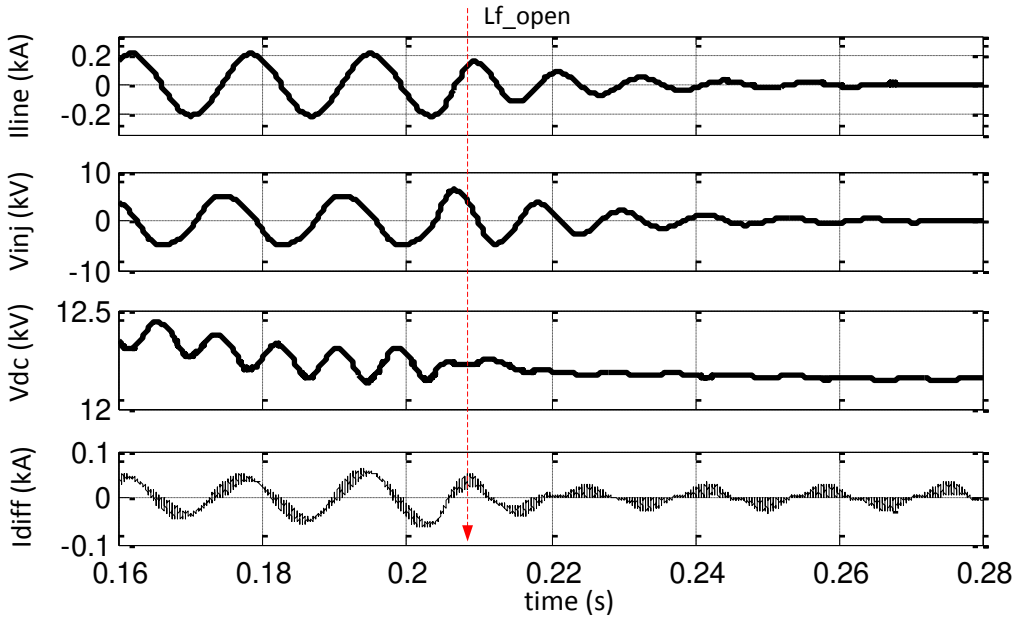


Figure 4.22: Power-router response for the filter inductor open fault.

4.5.7 Open Differential Inductor

The simulation results for the case where the differential inductor fail open are shown in Figure 4.23. With the differential inductor open, the converter loses DC-bus control resulting in increase or decrease of DC-bus voltage. The resulting DC-bus voltage will cause increased differential current through the working converter leg. As in case of the LSC IGBT failure, the impact of differential inductor fail open on the LSC converter depends on the DC-bus voltage. If the DC-bus voltage decreases, then the maximum voltage injected by LSC will also decrease and the LSC may lose power flow controllability. The main controller can detect the differential inductor fail open by monitoring the DC-bus voltage and the DC component of the differential current. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation. In case the main controller fails to detect the fault, the DC-bus voltage will continue to either increase or decrease. In either case, the increased differential current is detected by the peripheral controller, which will turn

on the fail-normal switch. The device will be protected from overvoltage on the DC bus by the DC-limiting chopper.

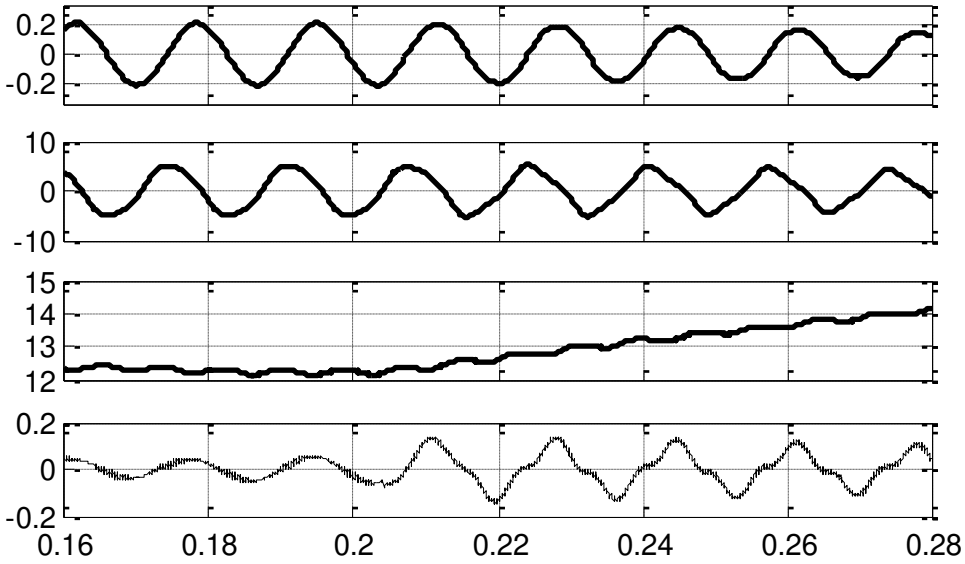


Figure 4.23: Power-router response for the differentail inductor open fault.

4.5.8 Open Filter Capacitor

The simulation results for the case where the filter capacitor fail open are shown in Figure 4.24. The loss of filter capacitor will result in injection of increased voltage and current harmonics in the line. In addition, the high frequency switching harmonics, which are no longer filtered, will stress the SCR with high dv/dt. The main controller can detect the differential inductor fail open by monitoring the increased switching frequency ripple in the line current and the filter voltage. On detection of fault, the converter will be turned off and the fail-normal switch will be turned on to enter the bypass mode of operation. In case the main controller fails to detect, the PR will continue to operate with increased current harmonic injection in the line until it is bypassed by the contactor, which has to be operated from an external control circuit.

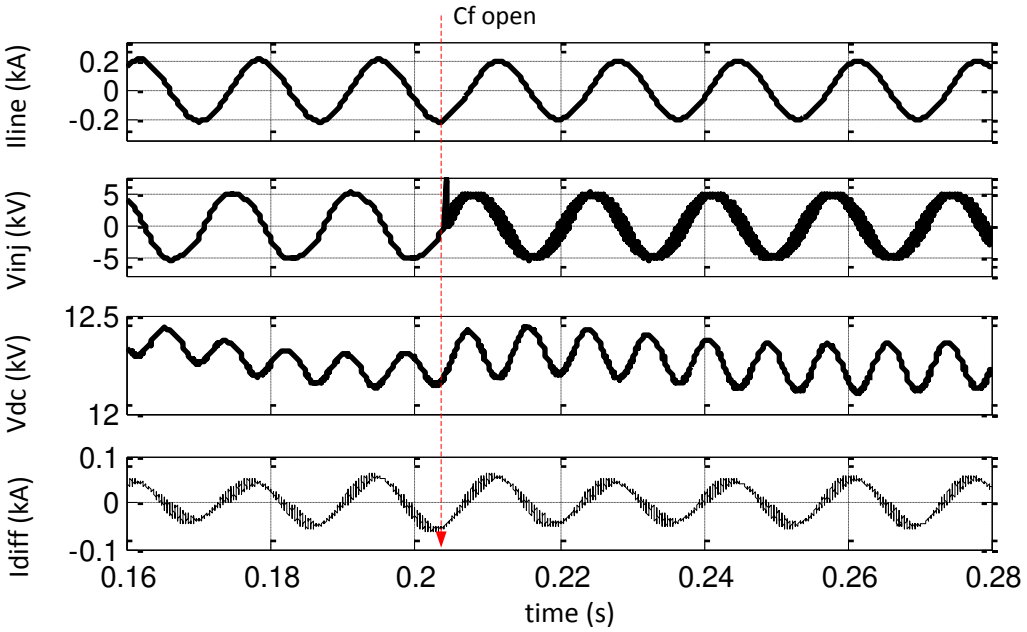


Figure 4.24: Power-router response for the filter capacitor open fault.

4.6 Conclusion

In this section the protection system based on a fail-normal switch, which is critical in isolating the converter from the grid faults, is presented. The detailed design of the various protection elements is presented. A three-tier protection scheme to avoid single point-of-failure is proposed. The converter response for various faults and the system parameters that can be used to detect the faults are presented through simulations. The operation of proposed protection system in isolating the converter and the grid in the event of faults is verified through simulation.

CHAPTER 5

CONTROL OF MULTIPLE POWER ROUTERS

5.1 Introduction

Power routing on a meshed grid may require operation of multiple power routers (PRs). It is important to show how stable operation can be obtained under steady state, dynamic and fault conditions with multiple power routers. Also, as units are geographically dispersed, communication latencies and failure can cause instability and poor controllability. This has not been addressed before. A main objective of the proposed research is to evaluate the PR-controller requirements to ensure stable operation of multiple power routers.

With multiple power routers installed on the network, each trying to control the system parameters to achieve its own objective, high-frequency interaction between different controllers may occur. Consider the four-bus 138 kV system shown in Figure 5.1. The system has two power routers controlling the power in Line 1-2 and Line 3-2.

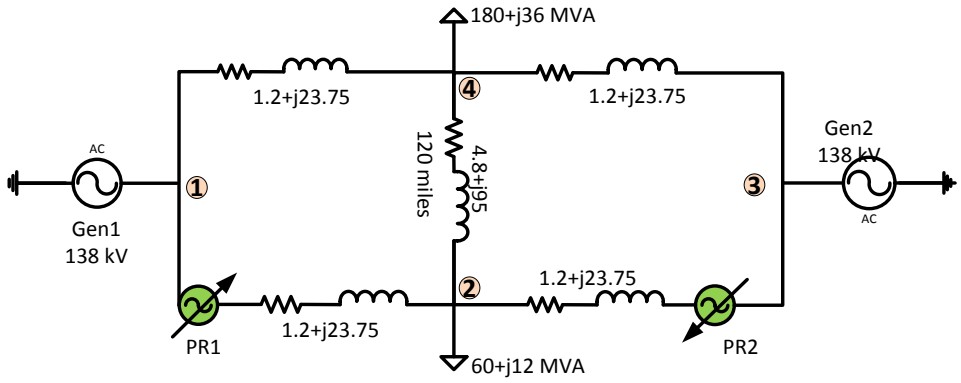


Figure 5.1: Four-bus test system with multiple power router devices.

The system was simulated in PSCAD^{TM} using fourth-order generator models to mimic the system dynamics accurately. The simulation results are shown in Figure 5.2. With neither controller enabled, the power in Line 1-2 was 44 MW and 20 MW in Line 3-2. PR1, enabled at 40 s, injected a 12 kV voltage to increase the power in Line 3-2 to

82 MW. The change in power in Line 1-2 caused a change in power in Line 3-2 from 20 MW to -4 MW, indicating the electrical coupling between Line 1-2 and Line 3-2. PR1 was disabled at 50 s, and PR2 is enabled at 60 s to reduce the power in Line 3-2 to 0 MW. Again, the change in power in Line 3-2 caused a change in power in Line 3-2, indicating the electrical coupling between both lines. When enabled individually, both power routers reached steady state within one second after initial oscillations. But when PR1 is enabled in presence of PR2 at 70 s, the power routers entered into oscillation mode, also called 'hunting'. In the example case, the system had a damped oscillatory response, but under certain conditions can be unstable. In the following sections, the impact of system conditions leading to hunting or instability between multiple power routers is discussed.

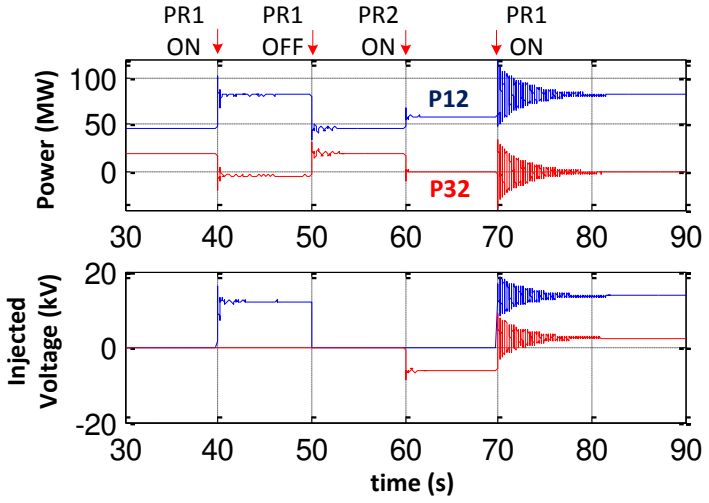


Figure 5.2: Power-flow control with multiple power routers.

5.2 Stability Analysis with a Single Power Router

The first step to understand the interactions between multiple power routers is to study the controller design of a single power router and identify the factors influencing power-router stability. Consider the same four-bus system shown in Figure 5.1, but with just PR1. Since a power router only re-routes the active power, the system in Figure 5.1

can be reduced to the system shown in Figure 5.3. The equivalent network is valid under the following assumptions:

- Only active-power-flow control is considered.
- The generator dynamics are much slower than the control dynamics of the power router.
- The change in bus voltage and the corresponding change in load are negligible.

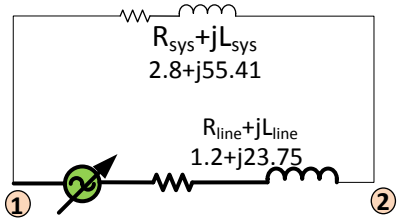


Figure 5.3: Equivalent system for the power-router controller design

The plant model is the sum of the compensated-line (line with power router) impedance, $Z_{line} = R_{line} + jX_{line}$, and the equivalent impedance of the rest of the system, $Z_{sys} = R_{sys} + jX_{sys}$. The corresponding power-router controller model, with cross-coupling control in synchronous reference frame $(d-q)$, is shown in Figure 5.4 [95].

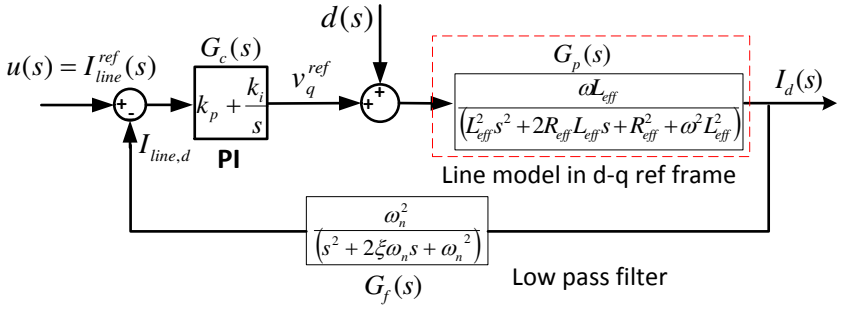


Figure 5.4: Power-router controller in synchronous (d-q) reference frame.

The network stability is analyzed by evaluating the phase margin of the loop-gain transfer function. The loop-gain transfer function is a product of the plant model $G_p(s)$ the low-pass filter model $G_f(s)$ and the PI-regulator model $G_c(s)$. With constant line impedance Z_{line} and constant control parameters k_p, k_i, the phase margin of the

controller decreases as the system impedance Z_{sys} decrease. Reducing phase-margin implies that the system is moving towards instability. The impact of system impedance on the system stability is shown in Figure 5.5. The step response of the system indicates increasing oscillations with decreasing system impedance.

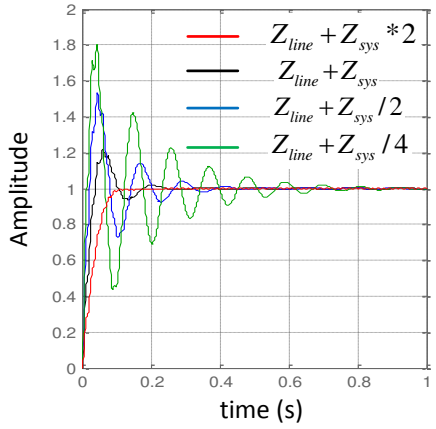


Figure 5.5 Impact of system impedance on the step response of the power-router controller.

The analysis showed that besides the controller parameters, the controller performance is also influenced by the equivalent system impedance seen by the controller. Even though the controller is designed for a non-oscillatory response for a specific network condition, the varying system impedance can result in instability.

5.3 Proposed Stability-analysis Technique for a System with Multiple PRs

In the presence of 'n' multiple controllers, PR1-PRn, the stability of PR1 is analyzed by replacing the rest of the compensated lines, the lines with PR2-PRn, with their respective equivalent impedances. A disturbance sensitivity function (DSF) is used to derive the equivalent impedance of a compensated line. In general, DSF defines the controller response for a disturbance. For a compensated line with active-power control, the DSF is defined as the change in in-phase line current $\Delta I_d(s)$ for a change in quadrature voltage between the buses $\Delta V_q(s)$. For an nth compensated line, with a power router PR_n controlling the active power, the DSF given by Equation (42).

$$\frac{\Delta I_d(s)}{\Delta v_q(s)} = \frac{G_{p,PRn}(s)}{1 + G_{c,PRn}(s) * G_{f,PRn}(s) * G_{p,PRn}(s)}, \tag{42}$$

For an uncompensated line, the DSF is just the plant model $G_{p,PRn}(s)$ which is same as the line model. For the stability analysis, a compensated line can be replaced by equivalent frequency-dependent impedance, which is derived by comparing the equivalent uncompensated-line DSF with the compensated-line DSF. At frequency ω the equivalent resistance of the n^{th} compensated line $R_{line,PRn}(\omega)$ is given by Equation (43) and the equivalent reactance of the compensated line $X_{line,PRn}(\omega)$ is given by Equation (44).

$$x_{line,PRn}(\omega) = \frac{\omega * \omega_s}{\omega_s^2 - \omega^2} * Re\left(\frac{\Delta V_q(j\omega)}{\Delta I_d(j\omega)}\right) - x_{sys}(\omega), \tag{43}$$

$$R_{line,PRn}(\omega) = \frac{\omega_s}{2\omega} * Im\left(\frac{\Delta V_q(j\omega)}{\Delta I_d(j\omega)}\right) - R_{sys}. \tag{44}$$

Using Equations (43) and (44), the equivalent impedance for each compensated line (PR2-PRn), at a given frequency ω is derived. The network is reduced to a system with single power router (PR1) by replacing the rest of the compensated lines with their respective equivalent impedances. Now, the stability of PR1 is analyzed using the same procedure described in the preceding section. To determine the stability of the network, the stability analysis is repeated for PR2-PRn.

5.4 Demonstration of the Proposed Stability-Analysis Technique

The four-bus system, shown in Figure 5.1, was used to demonstrate the proposed stability-analysis technique. The example system had power routers PR1and PR2 on Line 1-2 and Line 3-2, respectively. The proposed stability-analysis technique was used to find the control parameters of PR1 at which the system will be quasi-stable, in presence of PR2. The proposed stability-analysis technique was demonstrated by verifying the control parameters derived through analytical methods with simulation results.

The line parameters, plant model for the PR2 controller, PI block for chosen control parameters, and the chosen low-pass filter are given by Equations (45), (46), (47), and (48), respectively. The low-pass filter has a cutoff frequency of 62.8 rad/s.

$$Z_{line,PR2} = 1.2 + j23.75, Z_{sys,PR2} = 2.8 + j55.71, \tag{45}$$

$$G_{p,PR2}(s) = \frac{79.5}{0.0445s^2 + 1.68s + 6336}, \tag{46}$$

$$G_{c,PR2}(s) = 23 * \left(0.1 + \frac{150}{s}\right), \tag{47}$$

$$G_{f,PR2}(s) = \frac{62.8^2}{s^2 + 88.8s + 62.8^2}. \tag{48}$$

Figure 5.6: DSF of compensated ($k_p = 2.3\ V/A, k_i = 3.45\ kV/A^2$) and uncompensated Line 1-2.

The stability of PR1 was analyzed by replacing the compensated Line 3-2 by its equivalent impedance as shown in Figure 5.7. The equivalent impedance is calculated using Equations (43) and (44). Since the equivalent impedance of Line 3-2 is frequency dependent, the plant model of PR1 was recalculated at each frequency. The low-pass filter of the PR1 controller and the proportional constant of the PR1-controller block were the same as that of PR2. The integrator constant K_i of the PR1-controller was the variable to be calculated at which the system will be quasi-stable. The loop-gain equation $G_{c,PR1}(s)G_{f,PR1}(s)G_{p,PR1}(s) = -1$ is satisfied at 63.0 rad/s with $k_i = 4.64$ kV/A^2, indicating quasi-stability.

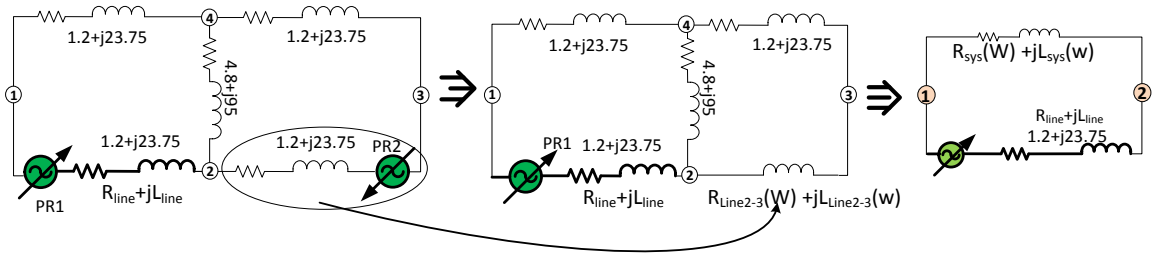


Figure 5.7: The equivalent circuit for evaluation of stability of PR1 in presence of PR2.

The four-bus system shown in Figure 5.1 was simulated in PSCAD^{TM}. The simulation results are shown in Figure 5.8. The control parameters for PR1 and PR2 were same as the ones used in the preceding analysis, except k_i for PR1. The quasi-stable state is

achieved by trial-and-error method by varying the gain k_i for PR1. PR1 and PR2 had stable response when enabled individually at 40 s and 60 s, respectively. But at 70 s, the power routers entered quasi-stable state when PR1 was enabled in presence of PR2. Both the power routers oscillate at 62.8 rad/s around their respective reference powers.

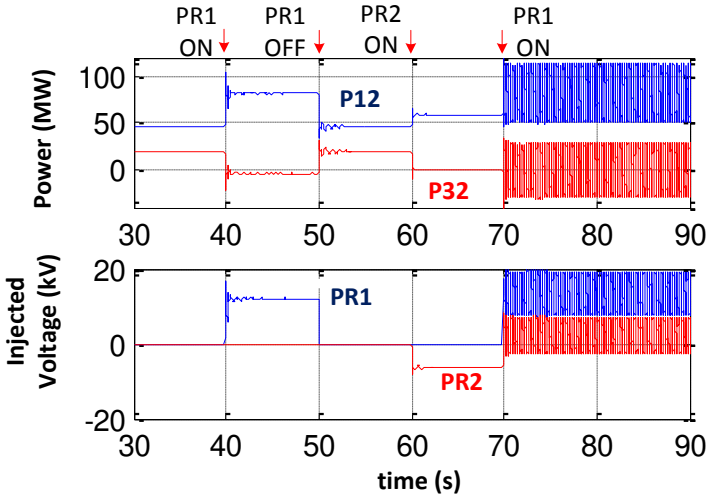


Figure 5.8: Quasi-stable results for the four-bus system with $k_p = 2.3\ V/A$ and $k_i = 4.64\ kV/A^2$.

The proposed analytical method is tested for two other conditions and the results are shown in Table 5.1. The condition for quasi stability obtained through analytical method closely matches with the results from simulation study, verifying the proposed stability-analysis technique. The results also show that an improperly designed power-router controller acts as negative impedance at certain frequencies and degrades the performance of the other power routers on the network at those frequencies. This can be a serious problem in the operation of multiple power routers.

Table 5.1: Verification of proposed stability-analysis technique.

Test Condition						**Analytical**		**Simulation**	
Case	$k_{p,PR2}$ **(V/A)**	$k_{i,PR2}$ **(kV/A^2)**	$f_{cutoff,PR2}$ **(rad/s)**	$k_{p,PR1}$ **(V/A)**	$f_{cutoff,PR1}$ **(rad/s)**	$k_{i,PR1}$ **(kV/A^2)**	f_{osc} **(rad/s)**	$k_{i,PR2}$ **kV/A^2)**	f_{osc} **(rad/s)**
1	2.3	3.45	62.8	2.3	62.8	4.64	63	4.5	62.8
2	2.3	2.3	62.8	2.3	62.8	5.49	63.25	5.37	62.8
3	2.3	3.45	62.8	2.3	75.4	5.86	75.5	5.53	75.4

5.5 Impact of Negative Impedance on System Stability

Consider Case 1, shown in Table 5.1, the parameters for which are shown to result in a quasi-stability state. For the chosen gains, the DSF of the compensated Line 3-2 is compared with the uncompensated line in Figure 5.6. The DSF of uncompensated Line 3-2 is calculated using Equation (46), and the DSF of the compensated system is evaluated using Equation (42). At around 62 rad/s, the compensated system has a higher gain than the uncompensated system. The DSF represents the equivalent admittance of the line, and hence a higher gain implies effective negative impedance at these frequencies. It is inferred that the negative impedance introduced by PR2 reduces the effective system impedance for PR1 and hence causes oscillations in PR1 response.

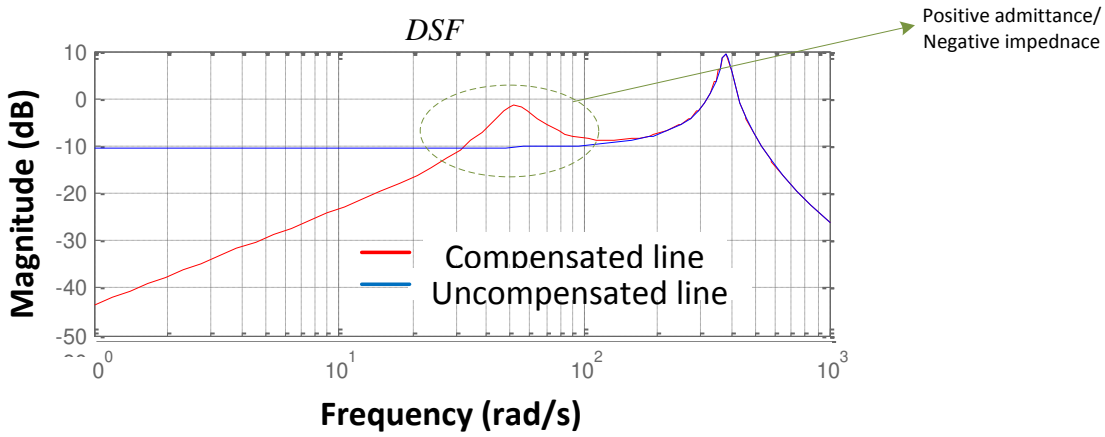


Figure 5.9: Comparison of DSF of compensated Line 3-2 (line with power router PR2) with DSF of uncompensated Line 3-2 (line without power router).

To show the impact of negative impedance, the system is now designed so that no negative impedance is introduced. PI gains for PR2 are chosen to be $k_{p,PR2} = 2.3\,V/A$ and $k_{i,PR2} = 46\,V/A^2$ to achieve an over damped response. For the chosen gains, the DSF of the compensated Line 3-2 has lower gain than the uncompensated Line 3-2 at all frequencies, as shown in Figure 5.10. Similarly, PI gains for PR1 are chosen to be $k_{p,PR1} = 2.3\,V/A$ and $k_{i,PR1} = 46\,V/A^2$. Since the network is symmetrical for Line 3-2 and Line 1-2 and both controllers have same gains, the DSF for Line 3-2 is same as DSF for Line 1-2.

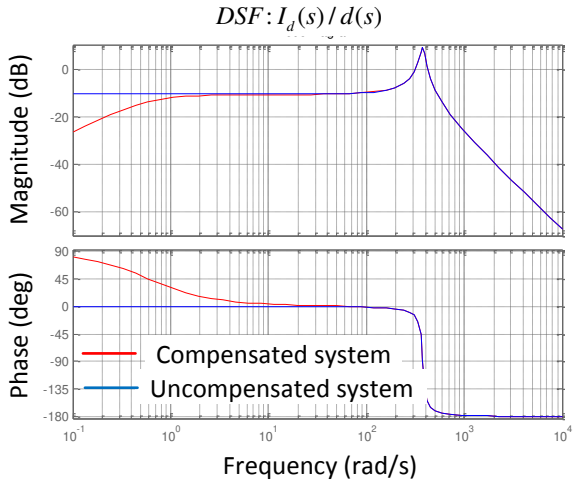


Figure 5.10: DSF of compensated Line 3-2 ($k_{p,PR2} = 2.3\ V/A$, $k_{i,PR2} = 46\ V/A^2$) and uncompensated Line 3-2.

The simulation results with the chosen control gains are shown in Figure 5.11. The response of the power routers when enabled individually is damped and stable. The response of PR1, with PR2 enabled, was still over damped and there was no hunting between the controllers. The results when compared with the earlier design, where the PR2-controller introduced negative impedance, shows that an improperly designed power-router controller acts as negative impedance at certain frequencies and degrades the performance of the other power routers on the network, at those frequencies.

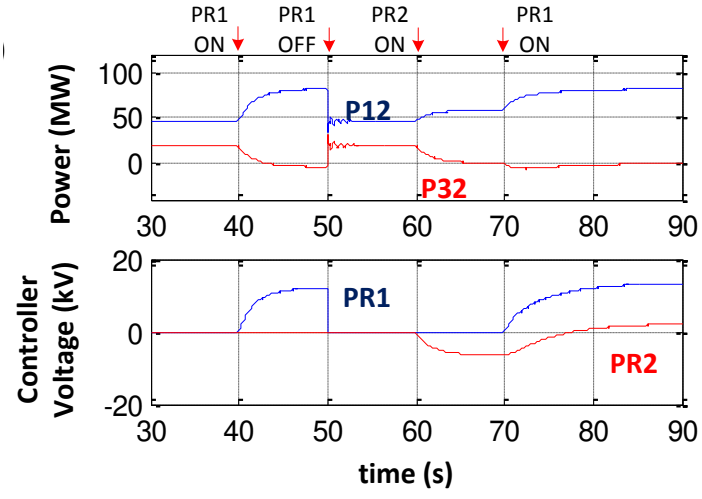


Figure 5.11: Simulation results for the four-bus system with gains $k_{p,PR1} = 2.3\ V/A$, $k_{i,PR1} = 46\ V/A^2$, $k_{p,PR2} = 2.3\ V/A$, and $k_{i,PR2} = 46\ V/A^2$.

5.6 Design Conditions for Guaranteeing Stability and Avoiding Hunting

In the previous section, it was shown that an improperly designed power-router controller introduces negative impedance at certain frequencies and degrades the performance of the other power routers on the network, at those frequencies. Based on the observations, the condition for guaranteeing stability and the condition for avoiding hunting are stated below.

Condition for stability: The interactions between multiple power routers in a given network will be stable if, at all frequencies, each power router is designed to be stable, and if the DSF of each compensated line has less gain than the corresponding uncompensated-line DSF.

Condition for avoiding hunting: The hunting between multiple power routers will be avoided if, at all frequencies, each power router is designed to have an over-damped response, and if the DSF of each compensated line has less gain than the corresponding uncompensated-line DSF.

5.7 Stability Analysis on IEEE 39-Bus System

In this section, the proposed controller design to ensure stable operation of multiple power routers is demonstrated on an IEEE-39 bus system. The chosen IEEE-39 bus system is shown in Figure 5.12 and the system parameters are given in Appendix B [115]. The system is divided into four hypothetical regions each connected by assumed tie-lines. Four power routers are installed on some of these imaginary tie lines as shown in Figure 5.12. The four power routers control the power flow in their corresponding tie lines by injecting an appropriate series voltage. The mutual coupling between the power routers is shown in Figure 5.13, where a 100 MW change in Line 4-14 caused by PR1 results in a 25 MW decrease in Line 18-17, a 30 MW decrease in Line 3-4, and a 35 MW decrease in Line 17-16.

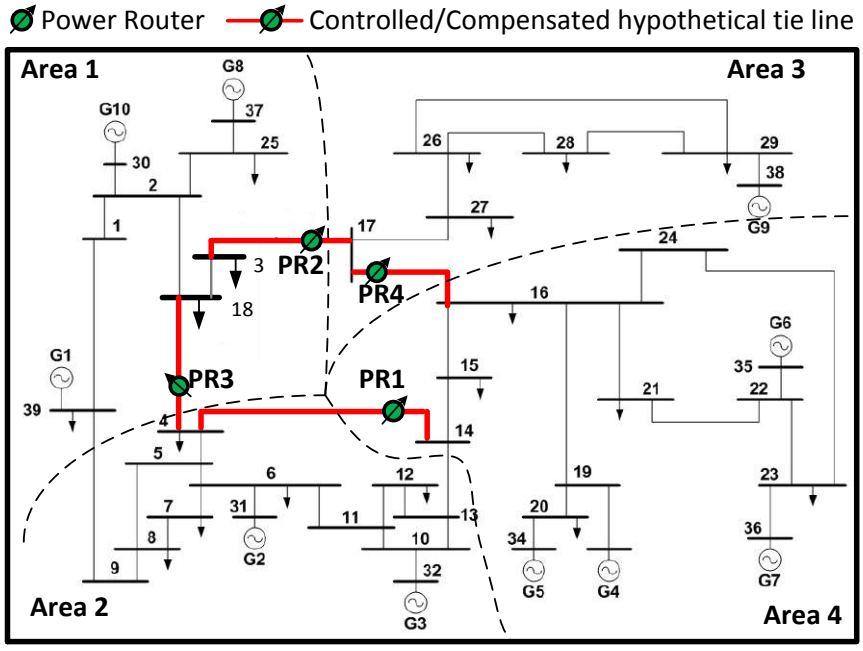


Figure 5.12: Schematic of IEEE 39-bus system with multiple PRs installed on assumed tie-lines.

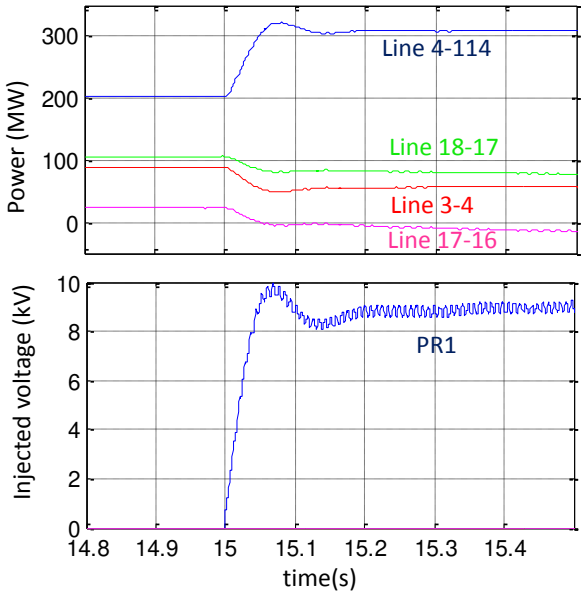


Figure 5.13: Electrical coupling between chosen controlled lines.

To verify the proposed controller design, two test cases are simulated on the chosen IEEE-39 bus system. In the first case, the controllers for the power routers are designed without considering negative impedance while in the second case the power routers are designed as per the proposed requirements to ensure guaranteed stability.

Case 1: In the first case, all the four power-router controllers are designed in the standard method, where each power-router controller is designed through Bode-plot techniques without considering the proposed stability constraints. The PI gains of the power-router controllers are designed to get the fastest response while ensuring that overshoot is less than 10%. For example, the step response of the PR1 controller with the chosen gains, $k_p = 5.6\ V/A\ , k_i = 1.2\ kV/A^2$, is shown in Figure 5.14. The controller parameters for the power routers are given in Table 5.2.

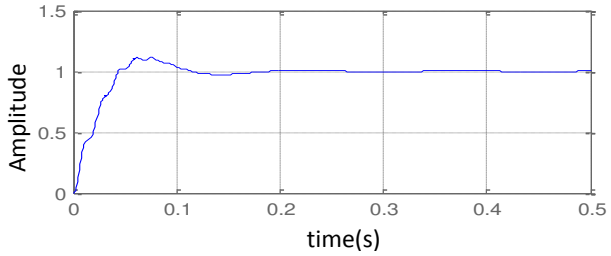


Figure 5.14: Step response of PR1 with traditional controller design.

Table 5.2: System and controller parameters for Case 1.

	R_{eff} (ohms)	L_{eff} (mH)	$k_{p,PR2}$ (V/A)	$k_{i,PR2}$ (kV/A^2)
PR1	3.5	125	5.6	1.34
PR2	6	191	5.6	1.8
PR3	6.2	224	5.6	1.9
PR4	7.8	264	5.6	2.3

The traditional controller design has resulted in reduced impedance, as shown in Figure 5.15. For the chosen gains, the DSF of the compensated Line 4-14 has higher gain in the region 25-100 rad/s compared to the uncontrolled line. The corresponding impedance of the Line 4-14, calculated using Equation (43) and (44) is shown in Figure 5.16. The impedance plot indicates that an effective peak negative impedance of 15 Ω is introduced by the PR1 controller. Similarly, the remaining power-router controllers introduce negative impedance.

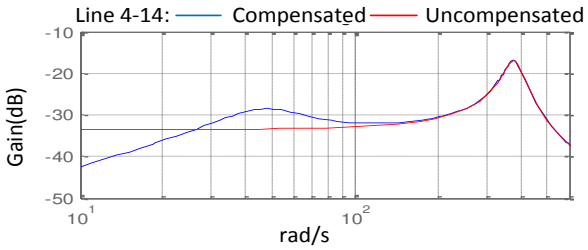


Figure 5.15: DSF of uncompensated and compensated Line 4-14 for Case1.

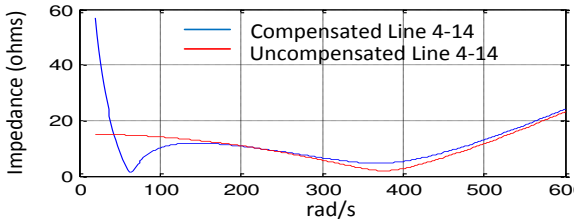


Figure 5.16: Impedance of uncompensated and compensated Line 4-14 for Case 1.

The performance of the PR controllers when enabled individually and collectively is simulated in PSCAD™. The performance of the four power routers when enabled individually at 15 s is shown in Figure 5.17.

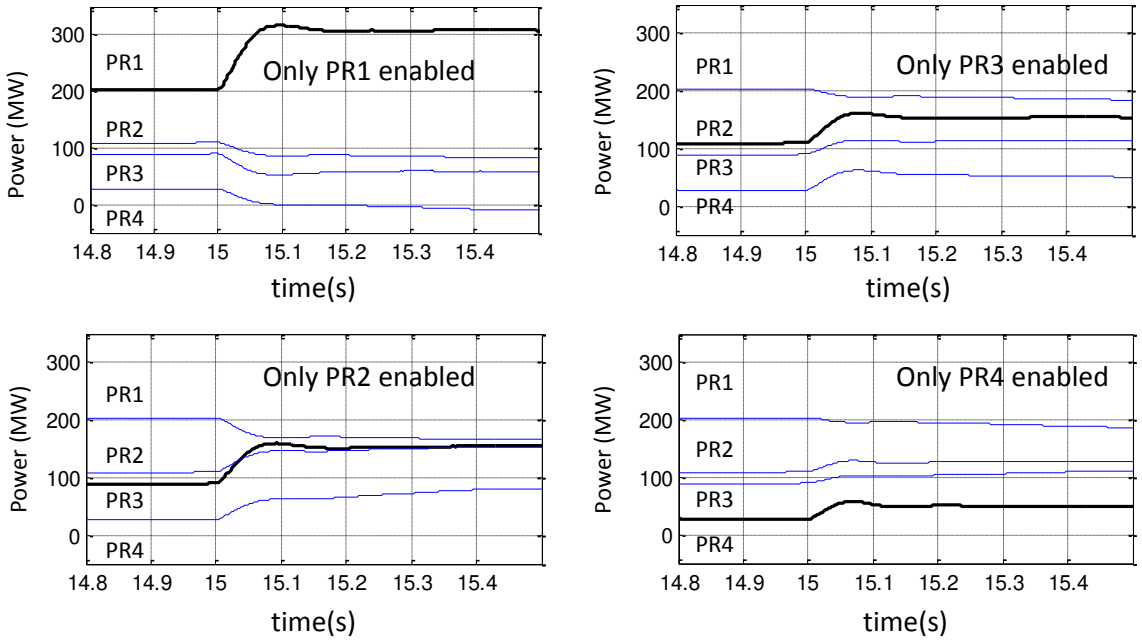


Figure 5.17: Response of power routers when enabled individually for Case 1.

PR1, PR2, PR3, and PR4 are controlling the power flow in corresponding lines at 310 MW, 150 MW, 150 MW, and 50 MW, respectively. As shown in the plot, the power

routers when operating individually have a stable and non-oscillatory response with an overshoot less than 10%. The response of the power routers when enabled collectively is shown in Figure 5.18. All the four power routers now have oscillatory response compared to when each of them is enabled individually. The frequency of the oscillations also indicates that the power routers are oscillating against each other i.e. hunting.

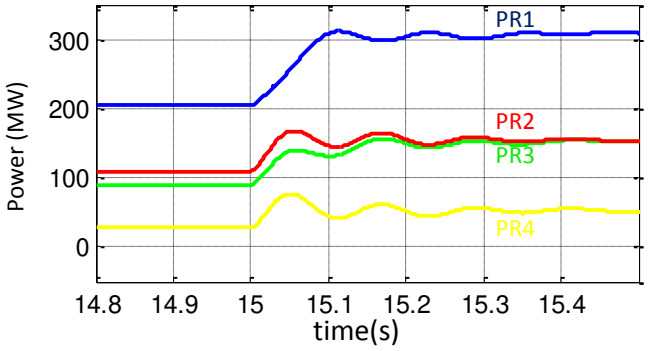


Figure 5.18: Response of power routers when enabled together for Case 1.

Case 2: In the second case the controllers of all four power routers are designed to meet the proposed stability conditions. For example, the PI gains of PR1 controller $k_p = 5.6\ V/A\ , k_i = 112\ V/A^2$ are chosen so that the system has a damped response and no negative impedance is introduced. This is illustrated in the DSF plots and the impedance plots shown in Figure 5.19 and Figure 5.20 respectively. The integral gain k_i for PR2, PR3 and PR4 is 168 V/A^2, 224 V/A^2 and 281 V/A^2 respectively.

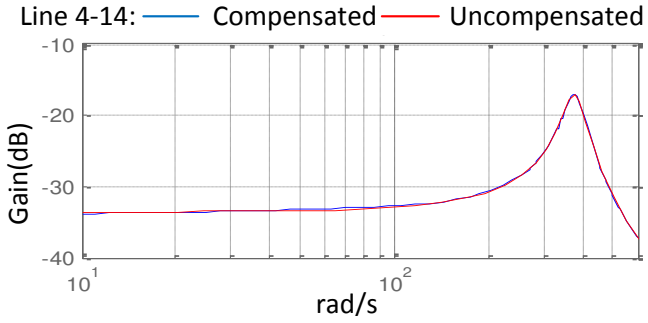


Figure 5.19: DSF of uncompensated and compensated Line 4-14 for Case 2.

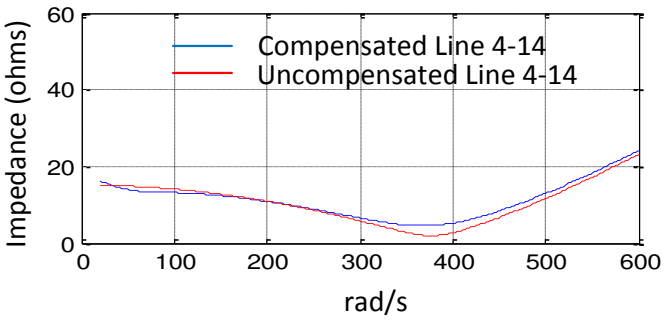


Figure 5.20: Impedance of uncompensated and compensated Line 4-14 for Case 2.

The performance of the four power routers when enabled individually at 15 s is shown in Figure 5.21. PR1, PR2, PR3, and PR4 are controlling the power flow in corresponding lines at 310 MW, 150 MW, 150 MW, and 50 MW, respectively. As shown in the plot, the power routers when operating individually have a stable and damped response. The response of the power routers when enabled together is shown in Figure 5.22. All the four power routers still have damped response unlike in Case 1.

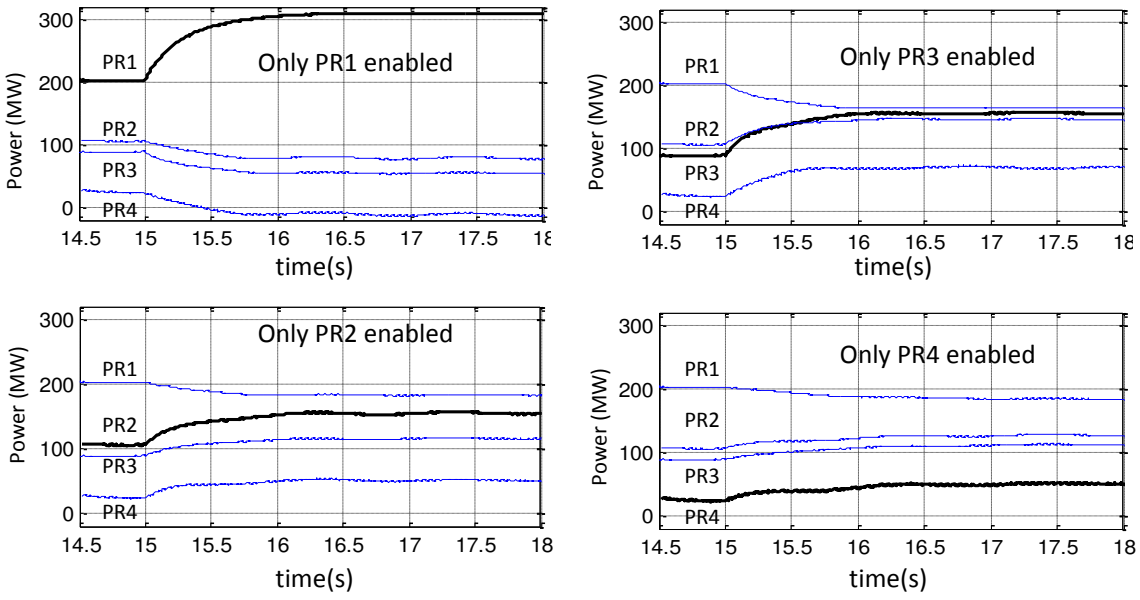


Figure 5.21: Response of power routers when enabled individually for Case 2.

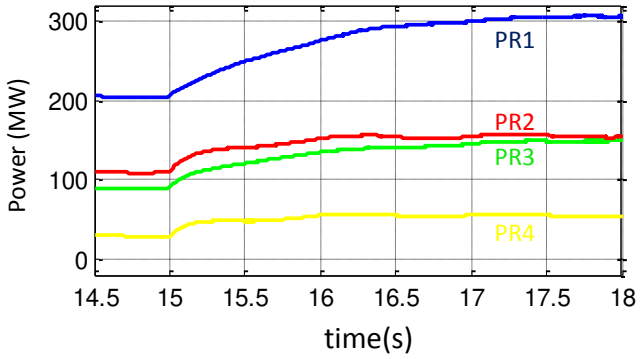


Figure 5.22: Response of power routers when enabled together for Case 2.

The proposed conditions to guarantee stable operation of multiple power routers are verified through simulation results. It is important to note that the proposed design is decentralized in nature: the controller design does not need information of other power routers in the system.

5.7.1 System Response for Transients

In this section, the response of the power routers for system transients such as line switching is compared for the tradition design and the proposed design. The controller gains for the traditional design and the proposed design case are the same as defined in the previous section for Case 1 and Case 2, respectively. A hypothetical test case of a new parallel line across Line 3-18 is considered. Because of the new parallel line, the impedance of Line 3-18 has reduced from 400 mH to 200 mH. The response of PR1 in presence of other power routers for Case1 is shown in Figure 5.23. The response of the power router before the line switching is shown in blue and the response after the line switching is shown in red. As shown in Figure 5.23, the response has become more oscillatory because of the new line. The response of PR1 in presence of other power routers for Case 2 is shown in Figure 5.24. There is no deterioration in response of PR1 even though the effective impedance is reduced because of the additional line.

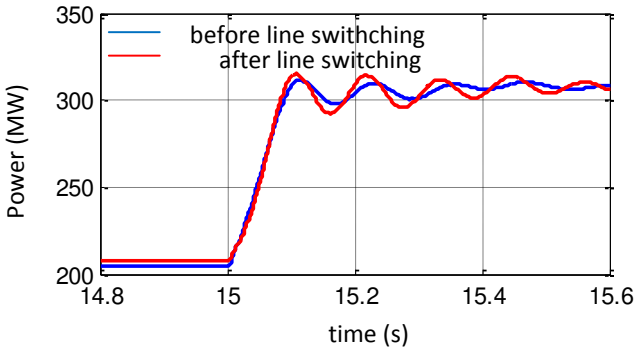


Figure 5.23: Response of PR1 before and after line switching for Case 1.

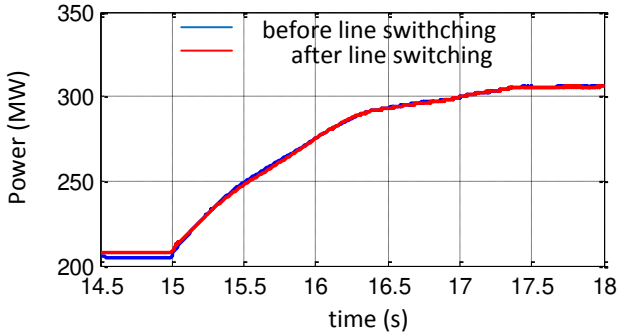


Figure 5.24: Response of PR1 before and after line switching for Case 2.

The results for the two simulated cases have shown that though the each power-router controller is designed to have non oscillatory behavior, the response could degrade to become oscillatory in presence of other power routers. But when the power-router controllers are designed as per the proposed constraints, the power routers response is unaffected by the presence of other power routers.

5.8 Conclusions

This research proposes conditions for power router controller design that can ensure stability even in presence of other power-router controllers. In contrast with the coordinated controller design, the proposed approach is independent of other controllers even at the design stage. An analytical method to evaluate the stability of a system with multiple power routers is proposed. The analytical method is used to show that an improperly designed controller acts as negative impedance at certain frequencies, and

hence degrades the performance of other controllers in the network. Based on the stability analysis, the necessary conditions for the PR-controller design to ensure stable operation of a system with multiple power routers are proposed. These necessary conditions are verified through simulation studies on a four-bus system with two power routers. The proposed conditions to ensure stable operation of multiple controllers are verified on the IEEE 39-bus system with four power routers. Also, the system stability is evaluated for system disturbances such as line switching. Though intuitively it is known that lower gains can lead to lower interactions between multiple power routers, this research provides an analytical basis to choose the controller gains that can ensure stable operation of multiple power routers. The analysis is equally applicable for any series voltage injection controllers like UPFC, SSSC, BTB etc.

CHAPTER 6

APPLICATIONS IN DISTRIBUTION SYSTEMS

This chapter describes the potential applications of proposed power router in distribution system and the associated challenges in implementation. The applications can be categorized into two main groups: power-flow control and voltage regulation. The power-flow control is achieved by out-of-phase voltage injection and the voltage regulation is achieved by in-phase voltage injection.

6.1 Power-Flow-Control Applications

6.1.1 Main-tie-main Arrangements

In a typical distribution system, two transformers are sited at a substation to serve the feeders. The arrangement, called as main-tie-main, has the two transformer buses connected with a normally-open (N.O) switch, as shown in Figure 6.1. Under normal conditions, the transformers share the load. If one transformer fails, the healthy transformer can serve the total load, thereby avoiding disruption of service.

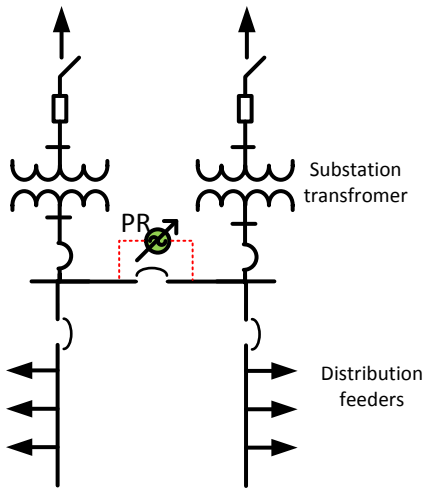


Figure 6.1: Replacing a N.O switch with a power router in a typical main-tie-main arangment.

The N.O switch is controlled manually or through an automatic transfer scheme (ATS). The manual transfer has a delay of 20 minutes, while the ATS scheme will switch to alternate transformer within three seconds [116]. As shown in Figure 6.1, by replacing the N.O switch with a power router, the disruption time could be reduced to a sub-cycle period. During normal operation, the power router will control the power from each transformer, thereby, balancing transformer loading. In case of faults, the service to the faulted feeder can be quickly restored, improving the reliability considerably.

6.1.2 Feeder Supply from an Alternate Path

In a typical radial system, a N.O switch is provided at the feeder ends. In case of fault on one feeder, the N.O switch is closed to allow supply of loads downstream of the fault using the second feeder. As in case of main-tie-main switch, the N.O switch is either manually controlled or through ATS [117].

A normally-closed (N.C) switch will improve the reliability of the system, but the implementation results in operational issues. The major issue is the loading of the two feeders. Different possible configurations of the radial system with feeder-end support are shown in Figure 6.2. With both the feeders supplied from the same transformer, the impact of N.C switch on loading levels is not significant [118]. But feeding from different transformers (b) or from different substations (c), can result in overload of the feeders [118]. Connecting two feeders supplied from different substations (c), can form a parallel path for the transmission system, resulting in unnecessary loop flows. As shown in Figure 6.2, the proposed power router can replace the N.C switch. The power router can limit the loop flows in normal conditions and can reduce the disruption time to a sub -cycle period under fault conditions.

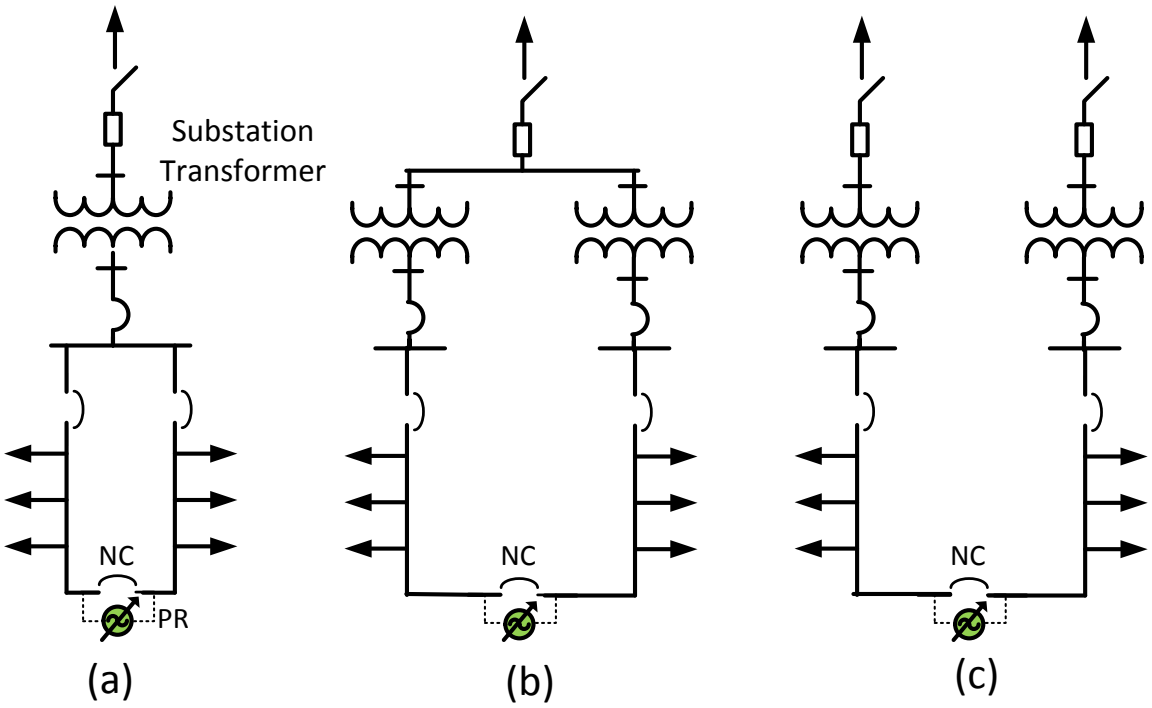


Figure 6.2: Radial systems with feeder-end support through a power router. (a) Feeders supplied from same transformer. (b) Feeders supplied from different transformers in the same substation. (c) Feeders supplied from different substations.

6.1.3 Mesh Grid Enabler

The advantage of meshed systems over radial systems is their increased reliability. If a single line in a meshed system goes out-of-service, other lines in the mesh compensate to satisfy the load that is unable to be fed by the faulted line. In a radial system if one line goes out-of-service, all loads downstream of the line experience an outage. Distribution systems in other countries such as in the United Kingdom and in specific areas such as the downtown areas in some US cities are meshed. However, most distribution systems are radial because it is hard to control power flows within a meshed system. The power router, by providing the power-flow controllability, can enable conventional radial distribution systems to be configured as meshed systems.

6.1.4 Load Balancing

In the proposed power router each phase is controlled independently, and hence there is an opportunity to correct for inherent imbalances in a distribution system. A number of

anomalies, such as increased power losses, misfiring of power converters and ill-tripping of protective relays, have been traced to the existence of power flow imbalances. The power router would be controlled to balance the three phases by slightly adjusting the power flow in each phase. Balancing the phases in a distribution system would be greatly beneficial as it will contribute to less current flowing in the neutral wire.

6.2 Voltage Regulator Applications

6.2.1 Mitigation of LTC Operation on Feeders with High PV Penetration

Photovoltaics (PV) are being integrated more and more into power systems at the distribution level. High penetration of PV increases the variability of voltages in the distribution system because the energy production from PV is itself variable. The increased variation of voltage levels in the distribution system can have dire consequences. Load-tap-changing (LTC) transformers located in these distribution systems have been experiencing an increase in the number of operations up to 30 times more than normal, due to these increased voltage fluctuations, and have caused premature deterioration of LTC transformers. A power router can be used to reduce LTC degradation by providing enhanced voltage regulation, which would effectively filter high PV-associated voltage variability.

6.2.2 Voltage Regulation in Distribution Systems

Voltage regulation is an important function in radial distribution systems. This is due in part because the voltage in radial distribution systems tends to drop along the feeder. To compensate for low voltages at the end of the feeders, the voltage can be regulated at certain points within the distribution system to set points that ensure that the voltage does not sag beyond specified limits at the end of the feeder. The power router can be used to regulate the voltage because it can control both the amplitude and phase of the voltage it inserts into the line.

6.2.3 Conservation Voltage Reduction (CVR)

Conservation voltage reduction (CVR) is the practice of lowering the voltage supplied to a distribution system in order to reduce the demand of the system, specifically during peak load hours. CVR is effective in the distribution systems with lots of constant impedance or constant current loads. Such loads decrease their power consumption when their input voltage is decreased. The power router could be used to target certain loads identified for energy conservation. The power-router power flows could then be adjusted to levels that the utility operator is comfortable supplying at that instance of time. If all three phases are present at the service drop, distribution transformers used to service households could even use power-router technology to precisely control power conservation down to the household.

6.3 Implementation Challenges

6.3.1 Fault Current

The protection system in the traditional radial distribution system is designed for power flowing from a single source to the load in one direction. With the power router installed, the peak fault current in the system can increase and affect the existing protection mechanism. For example consider the case where the power router is connected between two substation transformers to balance the load between the transformers. As shown in Figure 6.3, without the power router, the load is sourced from a single transformer and the peak fault current is 10 kA. The power router installed between the transformers will bypass the line faults, and hence the peak fault current increases to 20 kA. The existing protection system designed for 10 kA will now have to handle 20 kA.

The power router may be fitted with breakers on either side, but then the breakers will add to additional cost. Also the breakers operation should be coordinated with the

breakers down the radial line, requiring modification of the entire feeder protection scheme.

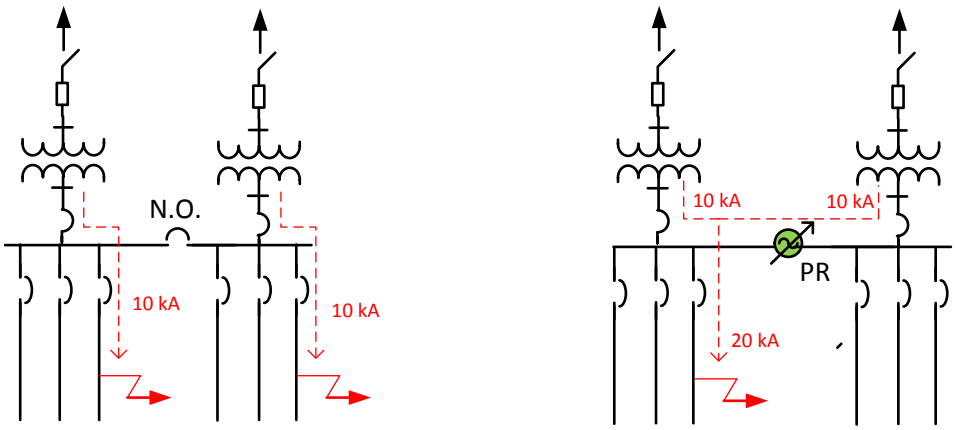


Figure 6.3: Impact of power router on fault current in distribution applications.

6.3.2 Differential Voltage Between Buses

The fractional-rating advantage of the power router is based on the fact that the power flow in a line can be controlled by injecting a fractional voltage in series in the line. This assumption is applicable for meshed systems where the voltage difference between the two buses δ is typically < 10°. In tie-line applications, where the two feeders are fed from different points in the transmission system as shown in Figure 6.4, the δ may be of large value. At large δ, the power router will have to be rated at relatively higher value to create any significant impact on the line power flow.

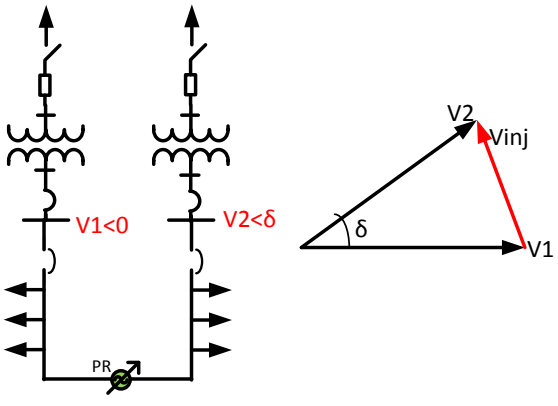


Figure 6.4: Significance of δ on power router rating in distribution applications.

6.4 Conclusion

In this chapter a number of applications of the proposed power router in distribution system are presented. The power router can be used as out-of-phase voltage injection device in tie-line power flow control or transformer/feeder load balancing application and as an in-phase voltage injection device for voltage magnitude control applications. The main constraint for power router in distribution applications is its impact on the fault current. The power router can increase or alter the flow of fault currents, the scenarios for which the radial distribution system might not have been designed. In addition, the fractionally rated power router might be ineffective for interconnecting systems with significant voltage difference between the buses, which is a possibility in interconnecting systems sourced from different sources in the transmission system. The application of proposed power router in distribution systems is system specific and requires detailed system analysis.

CHAPTER 7

HARDWARE IMPLEMENTATION AT 13 KV, 1 MVA

The primary application of the proposed power router (PR) is to achieve power flow control on meshed networks, which are typically found at transmission (> 69 kV) and sub transmission (> 39 kV) levels. The demonstration of the proposed concept at reasonably high voltage and power will be a more realistic approach to reflect on the challenges associated with high voltage and high power applications. As a part of this research, the functionality of the proposed power router is experimentally demonstrated at 13 kV, 1 MVA. In this chapter, the 13 kV 1 MVA experimental test setup built to test the power router is presented. The operation of the power router and the salient features of the power router are demonstrated through experimental results.

7.1 Test Setup Design

The schematic of the 1-ph, 13 kV, 1 MW setup to test the proposed power-router functionality is shown in Figure 7.1. The test setup consists of a two-bus system with the interconnecting line represented by a 4 mH inductor. The two buses are built using 167 kVA, 13 kV/ 1.3 kV transformers connected in auto transformer mode. The low voltage windings of both the transformers are excited from a 0-1.3 kV powerstat through an isolation transformer. The isolation transformer isolates the two-bus system from the power source, thereby, providing the freedom to choose the ground on the two-bus system at a desired terminal. With isolated grounds, the FR-BTB converter can be grounded by connecting the converter terminal to the system ground. The grounded converter provides a safer and convenient platform, especially in the initial part of the converter testing and debugging. Once the controls are established the converter can be floated at 13 kV, similar to a real application, by moving the ground to the lower terminal

of the transformers as shown in the Figure 7.1. The FR-BTB converter is connected across the +/- 650 V taps of the Bus1 transformer, and hence can inject a maximum voltage of 650 V. The transformer at Bus1 and the FR-BTB converter together represent the proposed power router, with the ability to control the Bus1 voltage magnitude and phase. Without the FR-BTB converter the line current will be zero because both the buses are at same voltage level as they are fed from the same supply. The proposed power router can demonstrate the power flow controllability by injecting a series voltage and controlling the line-inductor current. The rating and selection criterion for major components are given below.

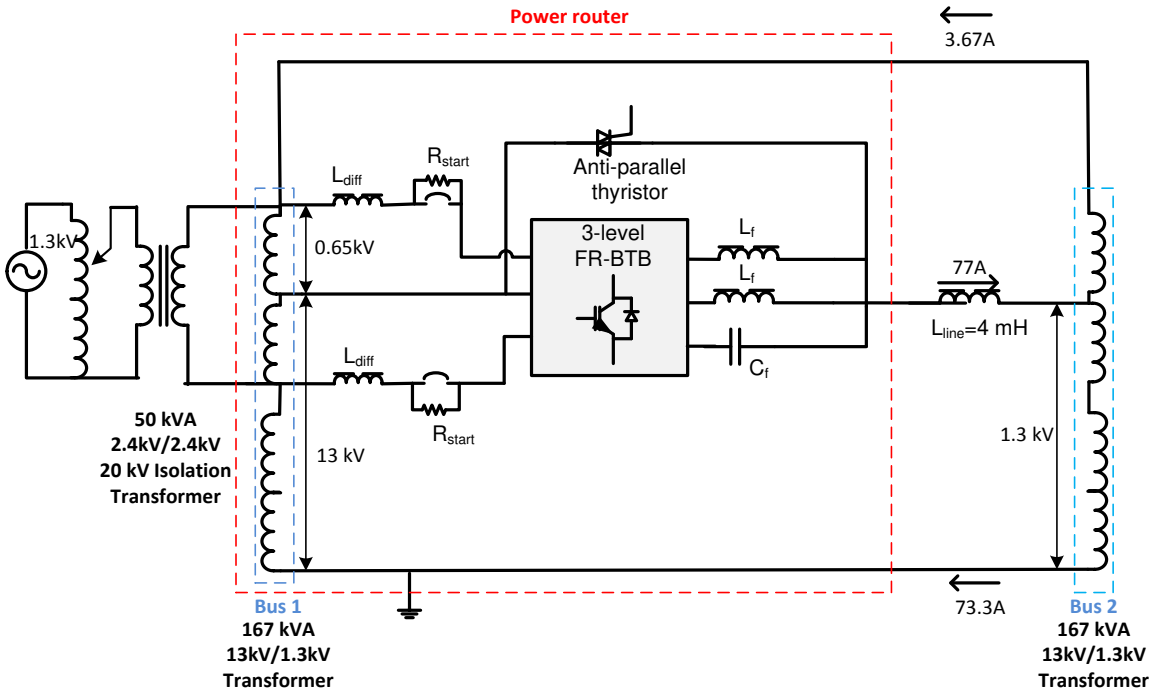


Figure 7.1: 1 MVA two-Bus Experimental Setup for FR-BTB-based power router

7.1.1 Component Selection

7.1.1.1 Bus Transformers (Bus1, Bus2)

Power flow of 1 MVA in the 13 kV two-bus system will result in a current of 77 A in the 1.3 kV winding of the transformer. Hence, the transformer has to be rated to handle at

least 100 kVA (74 A * 1.3 kV). The transformers selected are rated for 167 kVA, 13/1.3 kV with center tapped secondary.

7.1.1.2 Isolation Transformer

A 2.4 kV/ 2.4 kV transformer was chosen to provide isolation between the power source and the two-bus system. Since the power source only provides for the loss in the two-bus system, the power rating of the isolation transformer can be determined by the Equation (49).

$$\mathrm{KVA_{Iso\_Xmer}} >= \mathrm{n_{Xmer}} \times \mathrm{KVA_{Xmer}}(1-\eta_{\mathrm{Xmer}}) + \mathrm{KVA_{line\_ind}}(1-\eta_{\mathrm{line\_ind}}) \quad (49)$$

where KVA_{Iso_Xmer} is the kVA rating of the isolation transformer,

η_{Xmer} is the efficiency of the transformer,

KVA_{Xmer} is the kVA rating of the transformer,

$\mathrm{n_{Xmer}}$ is the number of bus transformers,

η_{line_ind} is the efficiency of the line inductor, and

KVA_{line_ind} is the kVA rating of the line inductor. The bus transformer efficiency, the converter efficiency and the line inductor efficiency is assumed to 98 %, 95 % and 99 % respectively. Based on the assumptions, a 10 kVA 1.3 kV/ 1.3 kV isolation transformer is sufficient for the application. A readily available 2.4 kV/ 2.4 kV 50 kVA isolation transformer was used for the application.

7.1.1.3 Powerstat

The powerstat provides a variable supply to enable testing the converter at lower voltages before ramping up to the final 13 kV voltage level. As in the case of the isolation transformer, the power rating of the powerstat is chosen to provide the loss in the 2-bus system. A 10 kVA, 0 – 1.3 kV powerstat is used in the test setup.

7.1.1.4 Line Inductor

The line inductor L_{line} represents the transmission line in an electric network. The inductor should be rated to handle 77 A corresponding to 1 MVA power flow at 13 kV. The maximum voltage across the inductor is equal to the maximum voltage the converter can inject, which is 650 V. Ideally, the inductance value should be such that a current of 77 A flow at 650 V across it. In this application a 4 mH inductor is chosen to optimize cost and space.

7.1.1.5 FR-BTB Converter

The detailed schematic of the 3-level FR-BTB converter is shown in Figure 7.2. It consists of a 1-ph 3-level converter with four half-bridge legs. Two of the legs constitute the transformer-side converter, which will be working in full-bridge mode. The other two legs constitute the line side converter and are operated in phase-staggered mode. The DC bus is chosen to operate at 10 % higher than the peak of the converter input voltage. Since the FR-BTB converter is connected across +/- 650 V taps, the DC bus is regulated at 2100 V. The chosen semiconductor devices should be able to block the DC voltage and carry the full line current. The FR-BTB converter also consists of a DC capacitor, output filter, differential inductors, DC-limiting chopper, and starting resistors. The selection of each individual component is described below.

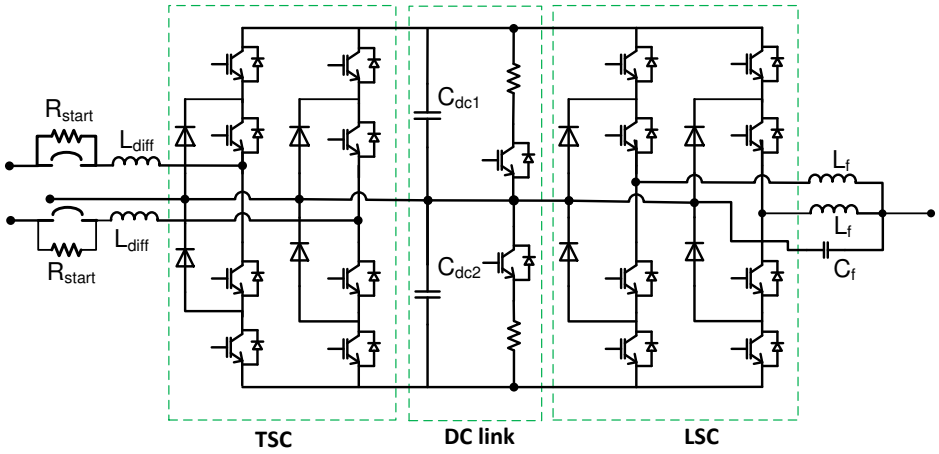


Figure 7.2: Schematic of the FR-BTB converter used for 13 kV, 1 MVA experimental evaluation.

7.1.1.6 Semiconductor Devices

The IGBTs are selected to handle a nominal voltage of 1100 V and a nominal current of 110 A. The neutral-clamped diodes are selected to handle a nominal voltage of 1100 V and an average current of 60 A. The IGBTs for the DC-limiting chopper are chosen to be the same as the IGBTs for the main converter to maintain uniformity. The semiconductor devices chosen for this application are given below.

- IGBTs: 1700 V, 200 A Dynex DIM200MHS17 IGBT module.
- Neutral clamped diodes: 1600 V, 60 A Semikron SKKD60F17 module.

7.1.1.7 DC Capacitor (C_{dc})

The primary purpose of the DC capacitor C_{dc} is to maintain a firm DC voltage and to limit the DC-voltage ripple to be within acceptable limit. In addition, the grid connected inverters choose the DC capacitor as an energy storage element to ride through the grid transients. Accordingly, the DC capacitor is chosen to meet the following criterion:

$$\frac{0.5 * C_{dc} * V_{dc}^2}{MVA_{conv}} >= 5000 \text{ J/MVA} \tag{50}$$

$$\frac{I_{line.pk}/2}{2 * \omega_f * C_{dc}} >= 0.05 * V_{dc} \tag{51}$$

where MVA_{conv} is the converter rating in MVA,

$I_{line.pk}$ is the peak line current,

ω_f is the fundamental frequency,

V_{DC} is the DC-link voltage. The DC capacitor should also be rated to carry continuous current $0.5 * I_{line.rms}$. A 730 µF, 3200 V DC-capacitor bank built using 16 numbers of 730 µF, 800 V capacitors was selected for this application.

7.1.1.8 Filter Inductor (L_f)

The value of the filter inductor L_f is designed to limit the worst case line current peak-to-peak ripple to < 10%. In the chosen FR-BTB converter configuration, there are two filter conductors, one per each phase leg of the LSC. Since the two LSC legs are operated in phase-staggered mode, the effective current ripple will be at twice the converter switching frequency and would reduce by half in magnitude. Hence, each filter inductor is designed to achieve a maximum of 20% current ripple and handle half of the fundamental line current. The value of the inductor for the chosen current ripple, DC-link voltage, and switching frequency can be calculated by Equation (52).

$$L_{filt} = \left(\frac{V_{dc}}{2}\right) * \frac{1}{2 * F_{sw} * \Delta i_{max}} \tag{52}$$

where V_{dc} is the maximum DC-link voltage which is 2100 V with the converter,

F_{sw} is the switching frequency, and

$\Delta i_{\max}$ is the maximum current ripple allowed. For the setup, an inductor of 10 mH is chosen, which can limit the ripple to < 10% at 10 kHz switching frequency and 2100 V DC-link voltage. The core material for the inductor is chosen such that it has low core loss even at switching frequencies. The inductor specifications are given below:

- Inductance: 10 mH, built using Finemet AMCC 1000
- Current: 38 A (rms) at 60 Hz and 11 A (pk-pk ripple) at 10 kHz
- Losses: < 100 watts

7.1.1.9 Differential Inductor (L_{diff})

The differential inductors L_{diff} act as an energy exchange medium between the transformer taps and the TSC phase legs. In such applications, the inductors are usually rated at 10 % of the exchanged power. In the power-router application, the power exchange by the TSC depends on the load on the DC bus. In the chosen test setup, the only load on the DC bus is the loss in the transformers, the FR-BTB converter, and the

line inductor. Hence the differential inductors are rated to be at least 10 % of the sum of the transformer, converter, and the line loss, which is calculated to be 4.5 kVA. The other function of the differential inductors is also to limit the differential current peak-to-peak ripple to <10 %. The specifications of the chosen differential inductor are given below.

- Inductance: 35 mH each (Built using Finemet AMCC 1000 cores)
- Current: 5 A (rms) at 60 Hz and 1 A (pk-pk ripple) at 10 kHz.
- Losses: < 20watts

7.1.1.10 Starting resistor (R_{start})

Initially when the supply is turned on, the DC-link capacitor, which is effectively a short, will see a large current and it can be detrimental for the transformers, inductors, and the capacitor. To limit the current at the startup, a resistor is connected in series with the supply as shown in Figure 7.1. The DC-link capacitor slowly charges to the peak of the input supply. After the capacitor is completely charged the resistor is bypassed by a contactor. The value of the resistor will determine the peak current during charging and also the charging time constant. The peak charging current should be less than the rated current of the differential inductor and the DC capacitor. With a 50 kΩ resistor connected in series with each leg of the TSC, the peak current is limited to 65 mA and the time constant for charging is 15 s. The power rating of the resistor can be calculated using the peak current. The specifications of the chosen starting resistor are given below:

- Resistance: 100 Ω each for a maximum current of 2 A.
- Power: Maximum of 400 watts for 0.2 s.

7.1.1.11 DC-limiting Chopper and Resistor (R_{chop})

During the fault conditions or transient conditions energy can accumulate in the DC-link capacitor and can result in overvoltage conditions. To avoid the DC-link overvoltage, a chopper and a resistor are connected in shunt with the capacitor. The chopper helps in transferring excessive energy in the capacitor to the resistor for dissipation. The chopper

is controlled like a buck converter in voltage control mode, with a reference value set at maximum allowed DC-link voltage. The reference voltage for the chopper is chosen to be well within the capacitor rating and also to avoid chopper interfering with the normal operation of the converter. The value of the resistor should be as low as possible to have a small time constant ($R_{chop} * C_{chop}$) and is only limited by the peak current capability of the chopper switch.

- DC-limiting chopper: IGBT of the same rating as that of the main switches in the converter
  (1700V, 200A).
- DC-limiting resistor: 22 Ω at 2.5 kW for 0.1 s.

7.1.1.12 Laminated Busbar

Parasitic inductance between the DC capacitor and the semiconductor devices can lead to significant voltage spikes across the device leading to device failure. The industrial practice for minimizing parasitic inductance is to use a laminated busbar for interconnecting the DC-bus capacitors, IGBTs, and diodes. The laminated bus bar consists of conductions planes interleaved with insulating material. It provides the shortest path between the interconnecting elements. The parallel path for the forward and the return currents cancel the flux of each conductor, thereby, reducing the parasitic inductance. The design of the laminated busbar should provide enough clearance and creepage distances between different buses to avoid flashover at transient voltage peaks. The laminated busbar should also be rated to handle the DC-bus voltage and the line current. The temperature rise on the busbar because of the line current should be well within the temperature ratings of the capacitor and the semiconductor devices. The specifications for the laminated busbar built for this application are as follows:

- Maximum voltage: 2*2.1 kV (nominal) + 1 kV = 5 kV.
- Maximum current: 100 A (rms).
- Temperature rise at nominal current: 20 degC.

7.1.1.13 Snubber Capacitor (C_{snub})

In addition to the large DC-link capacitor, the DC link usually consists of small (< 1 μF) snubber capacitors with very low inductance. The function of the snubber capacitor is to provide a path for the current in the DC-capacitor leakage inductance and the patristic inductance between the capacitor and the switches. While the main DC-link capacitors provide energy storage, the snubber capacitors absorb the switching noise and protect the devices from high $\frac{dv}{dt}$ noise. The value of the snubber capacitance is dependent on the estimated patristic inductance and is given by Equation (53).

$$C_{snub} = \left(\frac{V_{dc}}{2}\right) * \frac{L_p * I_{device,pk}^2}{2 * \Delta V * V_{dc,nom}} \tag{53}$$

where L_p is the estimated patristic inductance between the DC link and the devices,

$I_{device,pk}$ is the peak current in the devices,

$V_{dc,nom}$ is the nominal DC bus voltage, and

ΔV is the maximum voltage spike allowed. The specifications of the snubber capacitor built for this application are as follows:

- Maximum voltage: 1600 V.
- Maximum current: 100 A (rms).
- Parasitic inductance: < 1 nH.

7.1.1.14 IGBT Gate Drives

In addition to providing the required energy to drive the IGBT, the gate drive should also provide desat protection to protect the device from shoot through faults. Also the gate drive should provide isolation between the power and the control circuits.

The specifications of the IGBT gate drives selected built for this application are as follows:

- Gate drive voltage: +15 V/-8 V
- Peak current: 5 A
- Isolation: 5000 V
- Desat detection and protection

7.1.1.15 Passive Cooling System

One of the important factors affecting the life of converters is the cooling system. Traditional cooling systems typically involve fans or other moving parts that could limit the life of the system. In this test setup a passive cooling system that does not use any moving parts was used. The design inputs for the cooling system are the estimated loss in the converter and the acceptable temperature rise. The loss in converter for a given operating condition can be estimated from the device characteristics [120]. The device characteristics are obtained from the datasheet and are modeled to develop loss models. Using the device loss models and the converter operating waveforms the converter loss is calculated. The device loss models for the selected IGBTs and diodes are described below.

The turn-on loss (E_{on}), turn-off loss (E_{off}), and diode recovery loss data (E_{rec}) gathered from the device data sheet were modeled by 2nd order polynomial as seen in Equation (54).

$$Loss\,(V,I,T) = \frac{T}{T_{nom}} * \frac{V}{V_{nom}} * (a_1 + a_2 I * a_3 I^2) \tag{54}$$

where V is the voltage,

V_{nom} is the voltage at which the actual data is available from the datasheet,

T is the temperature,

T_{nom} is the temperature at which the actual data is available from the datasheet,

I is the current,

a_1, a_2 and a_3 are the model coefficients. The temperature and voltage dependence of loss was modeled linearly. The linear relationship does not exactly represent the actual temperature dependence of the devices. But the main concern will be the worst case

condition at the device maximum operating temperature and voltage. The modeled loss data and the data obtained from the datasheet are compared in Figure 7.3.

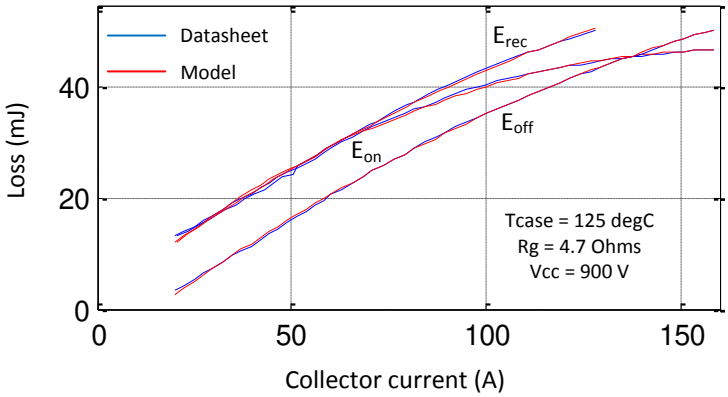


Figure 7.3: Dynex 1700V, 200 A IGBT loss model evaluation.

The on-state voltage drop of the IGBT (V_{CE}), free-wheeling diode (V_{FWD}), and neutral-clamping diode ($V_{NPC,Diode}$) is similarly modeled using a second-order polynomial. The diode drop is divided into two regions for the lower currents and the higher currents and two separate polynomials are used to model the data. Conduction loss can be calculated from the product of the on-state voltage and the device current. The modeled on-state voltage data and the data obtained from the datasheet are compared in Figure 7.4. The values for each coefficient of the developed models are given in Appendix.

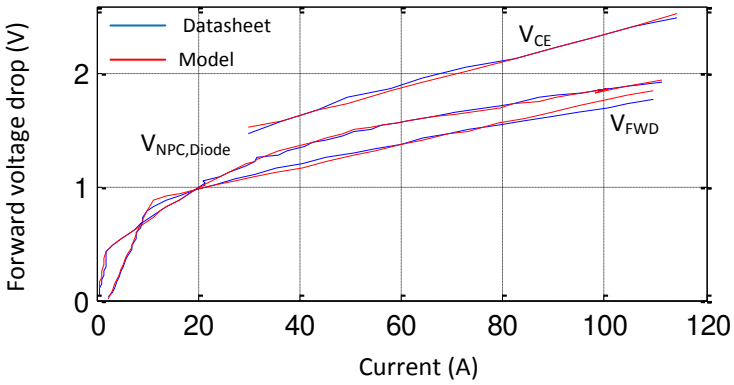


Figure 7.4: Dynex 1700V, 200 A IGBT and Semikron 1700 V, 60 A on-state voltage model evaluation.

The device loss models are then used to calculate the converter loss for different operating conditions, as shown in Figure 7.5. The passive cooling system was designed to limit the device temperature to be < 110 °C at a peak loss of 1800 watts. The details of the passive cooling technology are presented in [119]. The front and rear views of the passive cooling system rated to dissipate 2500 watts while maintaining device junction temperature below 125°C are shown in Figure 7.6.

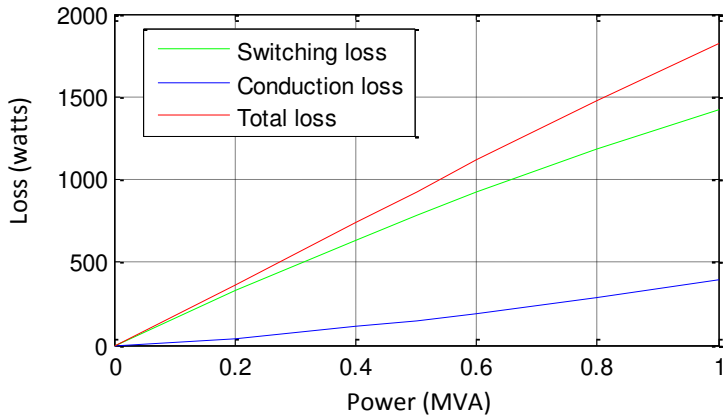


Figure 7.5: Estimated converter loss for the 13 kV, 1 MVA power router.

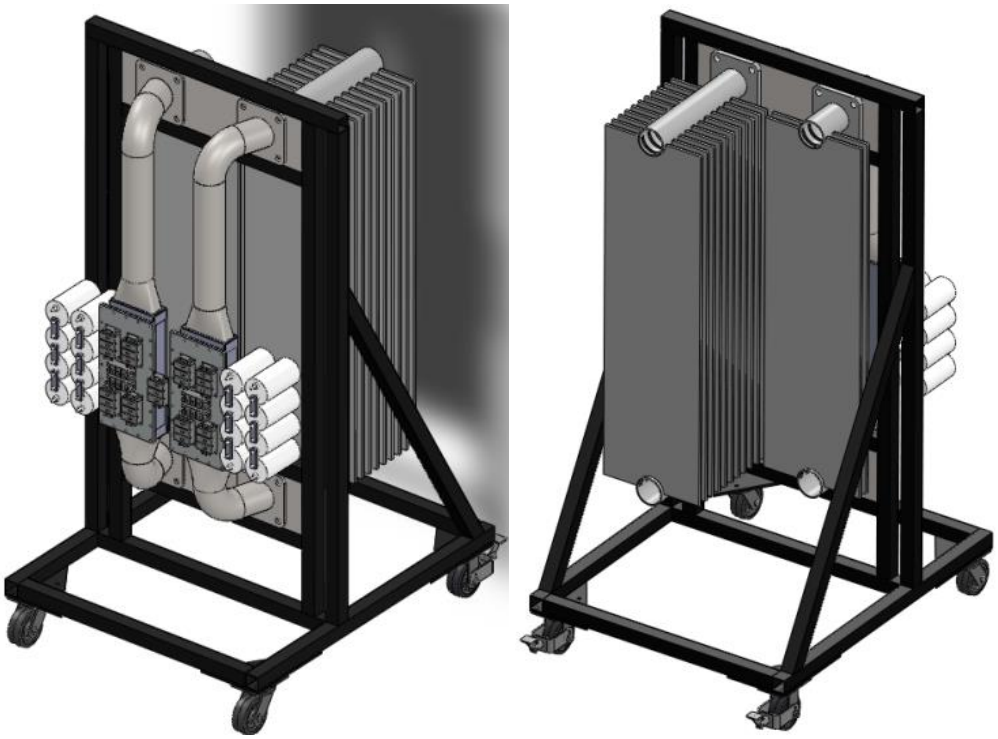


Figure 7.6: Front and rear images of the passive cooling system rated to dissipate 2.5 kW.

7.1.1.16 Controller

The controller that was developed and used in the 50 kVA lab prototype was used for the 1 MVA test setup. The controller implements the algorithm for controlling the grid synchronization, DC-bus voltage, line current/power, generating PWM pulses for the three-level converter, and protection logic. The controller code is shown in Appendix B.

The major components, ratings and prices are listed in Table 7.1.

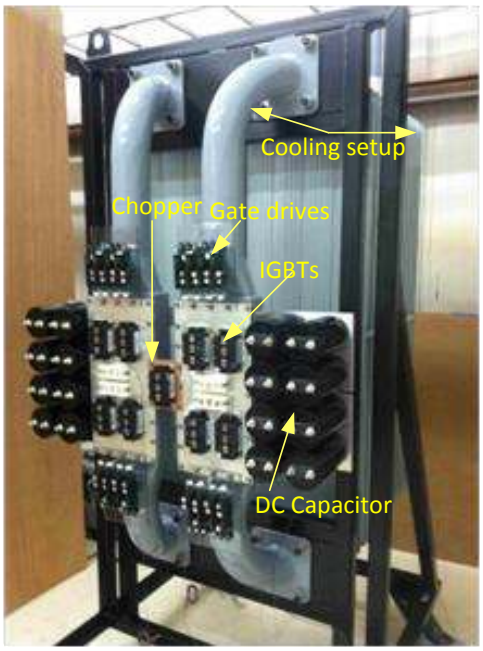
Table 7.1: Major components used for 13 kV, 1 MVA test setup.

Component	Ratings	Part Number	Manufacturer	Quantity	Cost ($)
Transformers	167 kVA, 13 kV/ 1300 V, taps at +/- 650V	--	Florida transformer	2	4300
Isolation transformer	2200V/2200V, 50 kVA	--	Hammond	1	2500
IGBTs	1700V, 200A	DIM200MHS17	Dynex	8	250
Freewheeling diodes	1600V, 100A	SKKD60F17	Semikron	4	80
Laminating bus bar	5 kV, 100 A		Eldre	1	2500
Line inductor	4 mH, 120A	--	Hammond	1	1400
Differential inductor	35 mH, 15A High frequency	AMCC 1000 cores	Assembled on Metglass cores	2	400
DC-bus capacitor	730 µF, 800V	947C731K801C DMS	Cornell Dubilier	16	75
Starting resistor	10k, 50 watts	--	Ohmite	2	5
Braking resistor	22 Ohms, 2500 watts	--	--	4	40
Gate drives	12 A(pk), 2500V isolation, +15V/-8V o/p	Based on VLA 500-01	Powerex	9	60
IGBT for braking chopper	1700V, 200A	DIM200MHS17	Dynex	1	270
Voltage sensor	1500V (rms)	AV100-1500/SP3	LEM	3	400
Current sensor	200A (rms)	LF 205-S	LEM	3	45
Control board	1.5 MHz Fixed point DSP	TMS320F2812	TI	1	1000

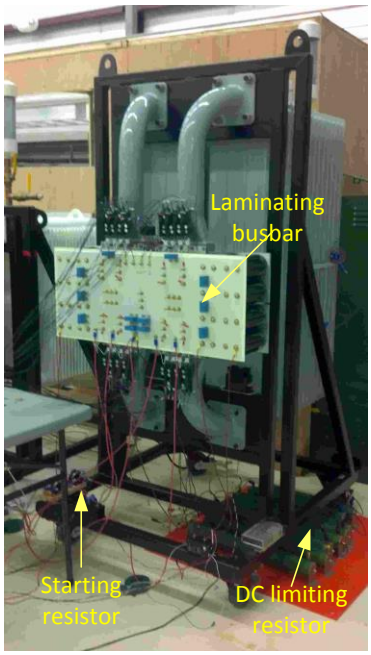
7.1.1.17 Assembled Test Setup

The images of the partially assembled FR-BTB converter are shown in Figure 7.7 (a), and the completely assembled FR-BTB converter is shown in Figure 7.7 (b). The partially assembled converter shows the passive cooling system, IGBTs mounted on the cold plate, and the DC capacitors at either end forming the DC bus. The fully assembled

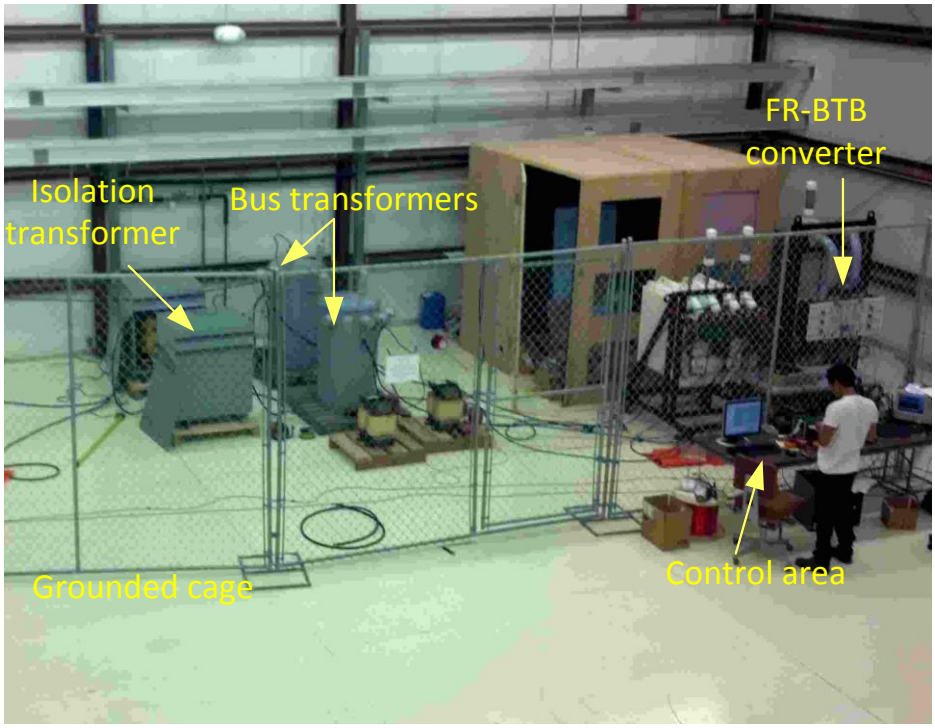
converter image shows the laminated busbar interconnecting the IGBTs and the DC capacitors. The image of the entire test setup is shown in Figure 7.7 (c). The power block is partitioned from the control region by a grounded framework to ensure operator safety.



(a)



(b)



(c)

Figure 7.7: (a) Semi-assembled FR-BTB converter. (b) Fully assembled FR-BTB converter. (c) 13 kV, 1 MVA power router test setup.

7.2 13 kV, 1 MVA Test Results

7.2.1 Active-Power Control

Without the FR-BTB converter, the two buses of Figure 7.1 had the same voltage, and no power flowed across the line. With the FR-BTB converter, the effective voltage of Bus1 was controlled in magnitude, or phase, or both, to induce power flow across the line. Figure 7.8 shows the power router successfully injecting the appropriate voltage to generate 1 MW of active power flow in the line. The top two waveforms show the bus voltage and line current, which is in-phase with the voltage indicating active power flow. The third waveform shows the differential current while the fourth and fifth waveforms show the TSC and the LSC 10 kHz switching voltage, respectively. The relatively low differential current was proportional to the losses of the converter, and can be seen to be small compared to the line current. The 13 kV, 1 MVA power router results for active power flow in reverse direction, leading reactive power and lagging reactive power are shown in Figure 7.9, Figure 7.10 and Figure 7.11, respectively. The results demonstrate the four-quadrant power-flow controllability of the proposed power router.

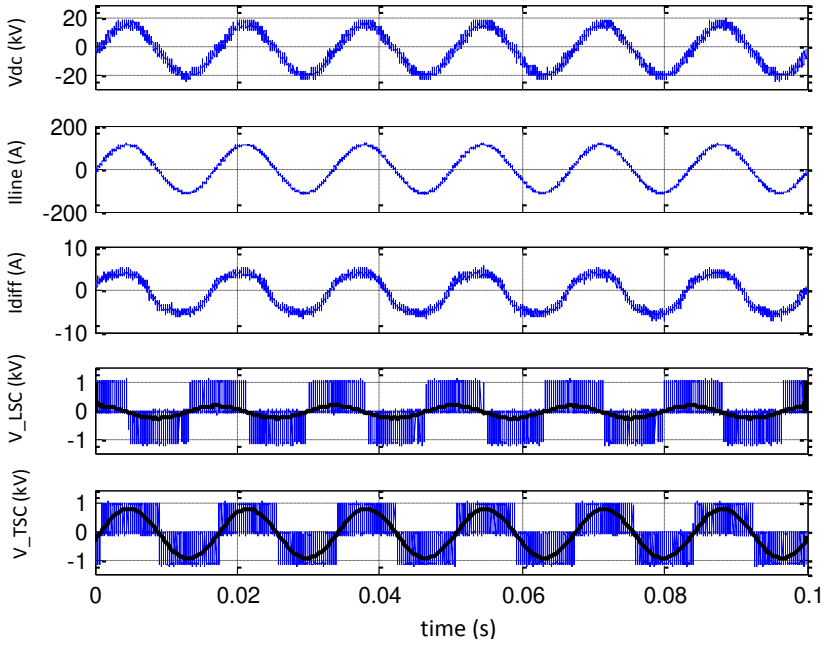


Figure 7.8: Power router active-power-flow control at 13 kV, 1 MW in forward direction.

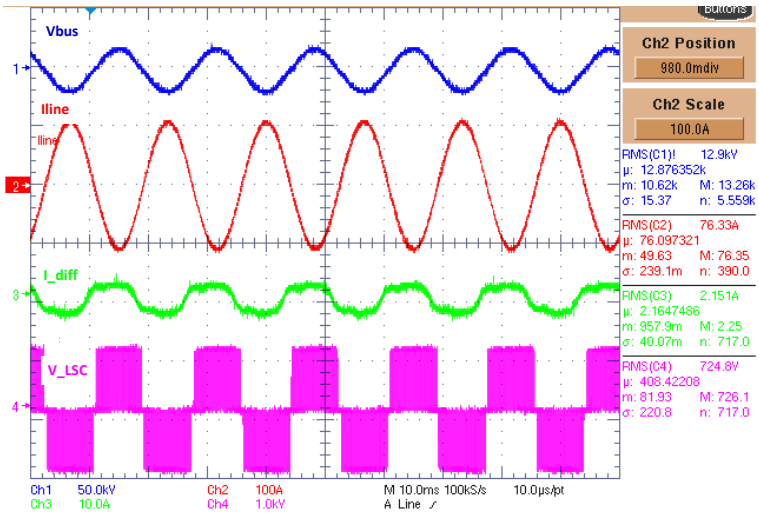


Figure 7.9: Power router active-power-flow control at 13 kV, 1 MW in reverse direction.

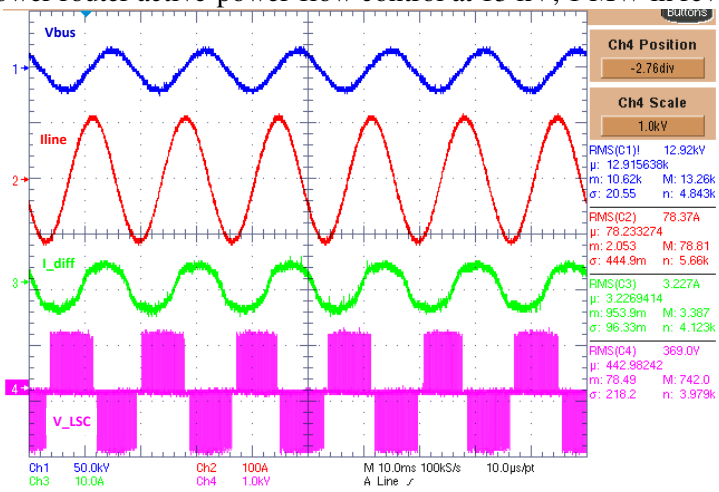


Figure 7.10: Power router leading reactive-power-flow control at 13 kV, 1 MVA.

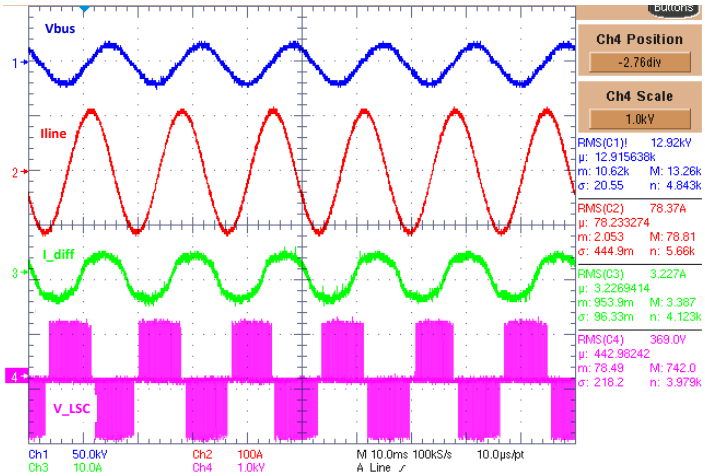


Figure 7.11: Power router lagging reactive-power-flow control at 13 kV, 1 MVA.

7.2.2 DC-Bus Control

In Figure 7.12 the startup procedure and DC-bus control for the power router is shown. The DC bus was initially charged to the peak of the converter input voltage. The transformer-side converter was then enabled to charge the DC bus to 10% above the peak voltage. After the DC-bus voltage reached its reference value, the line-side converter was enabled, and the line current was ramped up to the final desired value. As the line current ramped up, the increasing energy in the line inductor was supplied from the DC bus. Consequently, the DC-bus voltage tended to drop. The DC-bus control acted to maintain the DC-bus voltage at its reference value, as seen by the oscillations in the DC-bus voltage around the reference value.

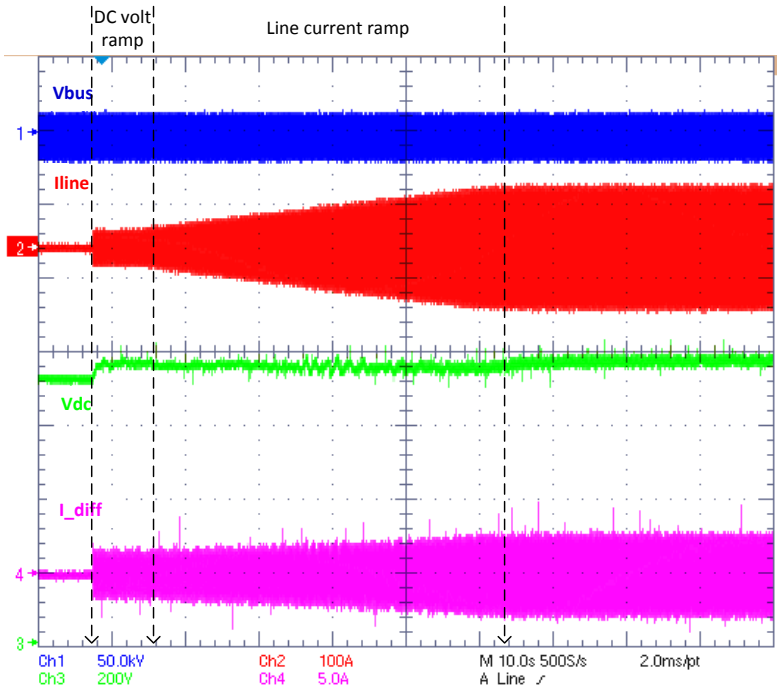


Figure 7.12. Startup results for the 1 MVA power-router prototype.

7.2.3 Dynamic Control

Figure 7.13 demonstrates the dynamic power-flow-control capabilities of the power router. Over the course of 100 s, the real power through the line was decreased to near zero, and it was then ramped up in the negative direction. The blue plot shows the line

voltage at 13 kV. The red plot shows the line current varying in proportion to the line power. The differential current shown in pink is controlling the dc-bus voltage, shown in green, at its reference value. The average power is evaluated from the bus voltage and the line current and is shown in Figure 7.13 (b). The voltage and current waveforms at positive active-power flow and negative active-power flow are shown in Figure 7.13 (c) and Figure 7.13 (d), respectively

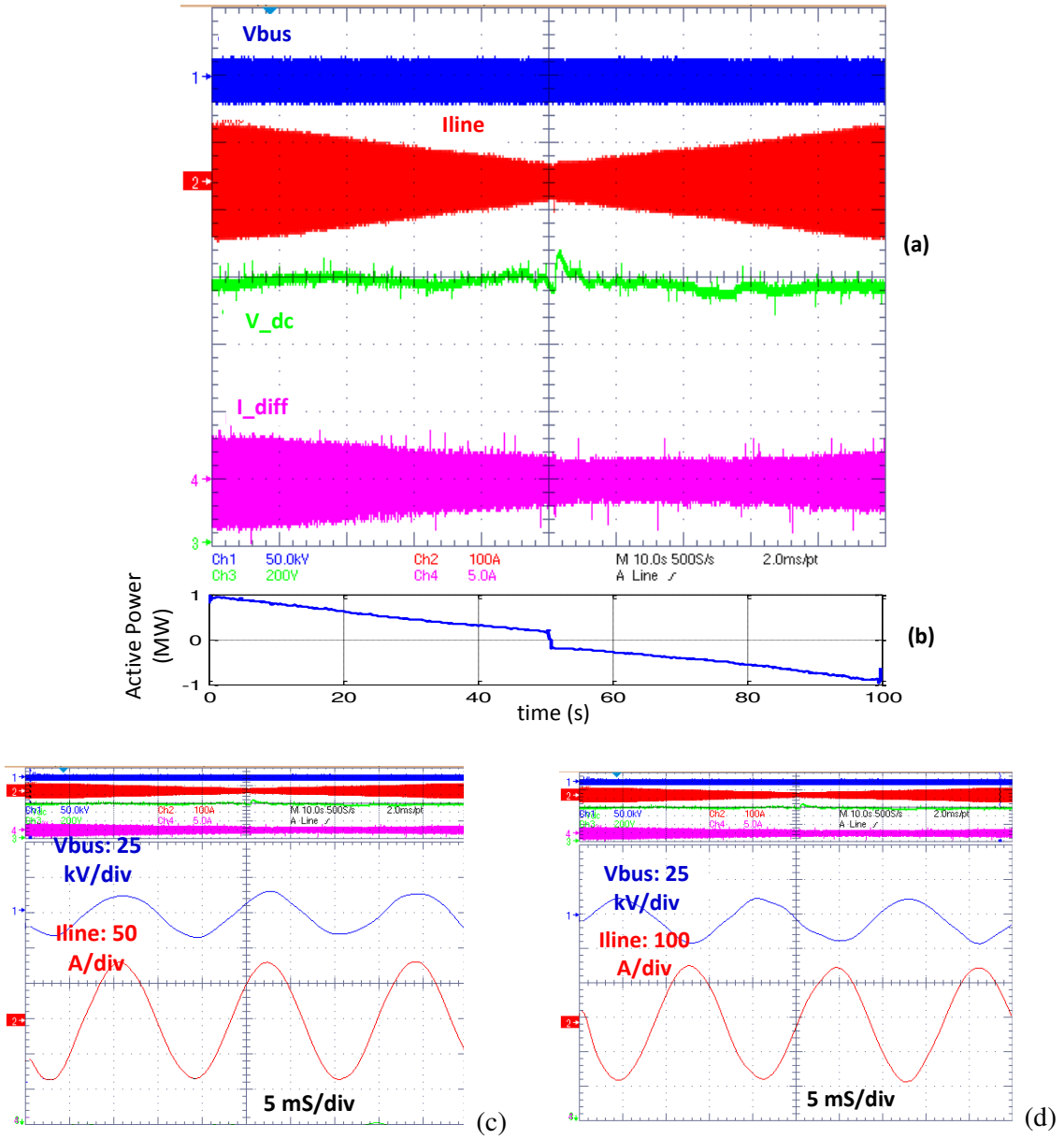


Figure 7.13. (a) 13 kV, 1 MW dynamic power-flow-control with the FR-BTB based power router: (b) Power flow calculated from oscilloscope data via Matlab, (c) Active power flow at t = 5 s, (d) Active power flow in opposite direction at t = 85 s.

In the experiment, the active is varied from 1 MW to -1 MW in 100 s. When the line power is varied, the transient energy is supplied form the dc bus. By either choosing a large dc capacitor or an adequately rated LSC that can compensate the DC bus variations, the response of the system can be improved further.

7.2.4 Efficiency Estimation

The losses for the 1 MVA setup were calculated by measuring the difference between the input and the output powers of the converter. The measurements for estimating the power loss are shown in Figure 7.14.

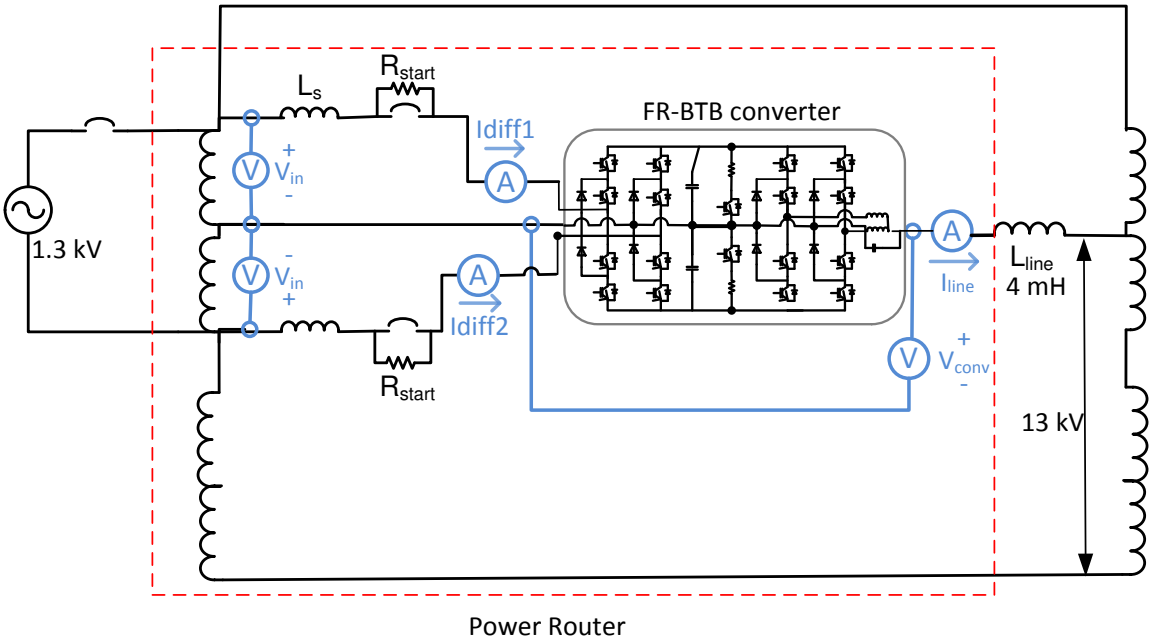


Figure 7.14: Measurements for converter loss estimation.

The converter input power was calculated from the bus voltage and the differential current flow. The converter output power was calculated from the converter output voltage and the line current. The voltage and the current waveforms at 1.0 MW power level are shown in Figure 7.15. The losses calculated by this method included the losses in all semiconductor devices, the losses in the DC-bus capacitor parasitic resistance, loss in filter inductor, and the losses in the differential inductors.

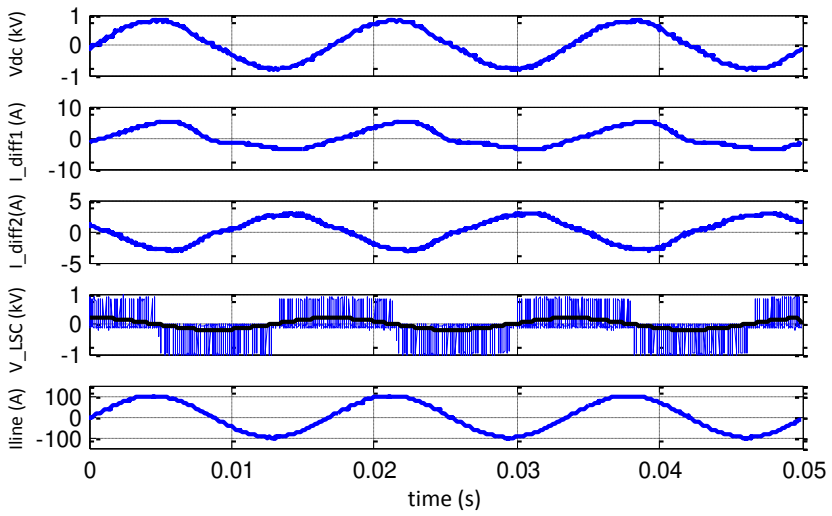


Figure 7.15: BTB Converter voltage and current waveforms for loss calculations at 1 MW.

The transformer efficiency could not be calculated experimentally because of the circulating-power nature of the test setup chosen. A conservative efficiency value of 98 % is assumed for the transformer loss calculations. Because the converter is connected across the +/- 5 % taps, the transformer loading will be 10 % of the controlled power in the line. So a 100 kVA transformer loading is assumed when the line power is 1 MVA, and is similarly calculated for other loading levels. The efficiency of the PR is calculated by the standard equation given by (55).

$$\eta_{PR} = \left(1 - \frac{Loss_{convereter} + Loss_{transformer}}{S_{line}}\right) * 100 \tag{55}$$

where η_{PR} is the efficiency of the power router,

$Loss_{convereter}$ is the loss in the converter calculated from the experiments,

$Loss_{transformer}$ is the transformer loss , and

S_{line} is the controlled power in the line.

The power router loss and the efficiency levels for different power levels are shown in Figure 7.16. The estimated power router efficiency is greater than 99.5% over a wide range of controlled power of 600 kVA to 1000 kVA.

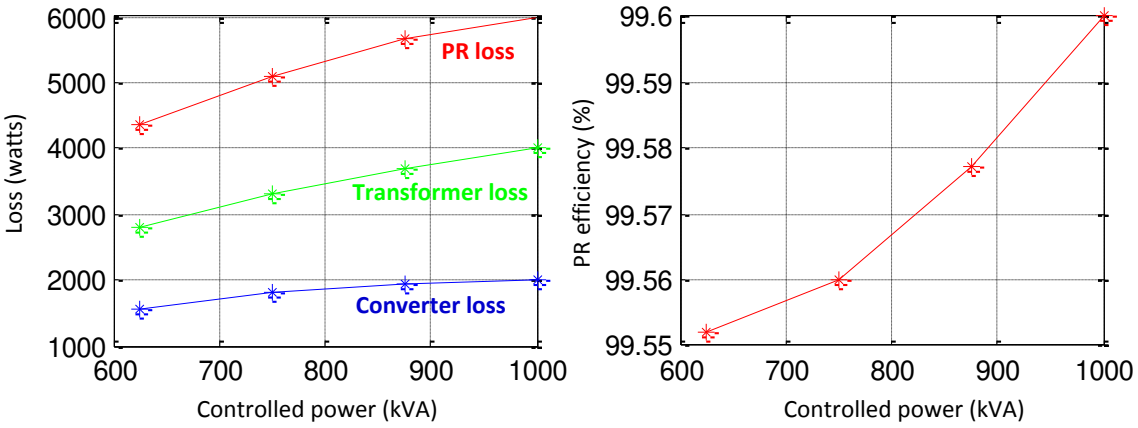


Figure 7.16: FR-BTB based power router efficiency.

7.3 Conclusion

The dynamic power flow controllability of the proposed power router was demonstrated at 13 kV, 1 MVA. Power-flow control of 1 MVA is achieved with a converter rated for 50 kVA. Significantly, the converter was rated to handle 1.3 kV while controlling the power flow at 13 kV. The fractional converter rating advantage of the proposed power router is experimentally demonstrated. The neutral-point-clamped three-level converter and the phase staggered approach used in the experimental prototype demonstrate the voltage scaling and current scaling methodology, respectively. The effectiveness of the proposed control algorithm in achieving power flow control is experimentally proved. The power router efficiency was determined to be at least 99.6 % at 1.0 MVA, again demonstrating the advantage of fractionally rated converter in achieving lower loss per controlled power compared to the standard BTB system. The 1.0 MVA experimental prototype also demonstrated passive cooling without fans, which can ensure longer operating life and less maintenance compared to actively cooled systems.

CHAPTER 8

CONCLUSIONS AND RECOMMENDED FUTURE WORK

8.1 Conclusions

This work has presented a low-cost power router (PR), capable of dynamic, independent control of active- and reactive-power flows on meshed grids. The proposed power router consists of a transformer augmented with a fractionally-rated back-to-back (FR-BTB) converter. The converter is connected across the transformer taps. The main advantage of the proposed converter compared to traditional FACTS solutions is the fractional rating of the BTB converter. The FR-BTB configuration has a unique advantage since the converter achieves the fractional rating via fractional voltage rather than fractional current. At very high voltages, the converter can be easily scaled by implementing a multi-level converter based on neutral-point-clamped (NPC) approach, which is an industry standard. The proposed power router consists of a fail-normal switch connected across the converter. The fail-normal switch assures that the system reliability is not impacted even when a lower reliability converter is used to impact the system performance.

The proposed power router achieves power flow control by injecting a series voltage like in a traditional UPFC or a BTB based solution. But because of the difference in implementation, the control of FR-BTB converter is different from traditional FACTS implementations. The various operating modes and the control structure to achieve the desired objective of power flow control are presented in detail. The control architecture is verified through simulations and hardware implementation. Starting from basic time-domain equations, detailed small-signal and frequency-domain models are developed, which are necessary tools for system-level studies.

Ensuring reliable operation of the power router, which is designed for utility applications, is essential. In the proposed power router, unlike the UPFC or the SSSC, the semiconductor devices are directly connected in series with the line, which exposes the devices to line fault currents. To avoid converter damage the fail-normal switch is used to isolate the converter from the line faults. The protection system based on the fail-normal switch and the detailed design of the various protection elements are presented. A three-tier protection scheme to avoid single point-of-failure is proposed. The converter response for various faults and the system parameters that can be used to detect the faults are presented through simulations. The operation of proposed protection system in isolating the converter and the grid, in the event of faults, is verified through simulation.

Power routing on a meshed grid may require operation of multiple power routers. It is important to show how stable operation can be obtained under steady state, dynamic and fault conditions with multiple power routers. This research proposed conditions for PR-controller design that can ensure stability even in presence of other power-router controllers. In contrast with the coordinated controller design, the proposed approach is independent of other controllers even at the design stage. An analytical method to evaluate the stability of a system with multiple power routers is proposed. The analytical method is used to show that an improperly designed controller acts as negative impedance at certain frequencies, and hence degrades the performance of other controllers in the network. Based on the stability analysis, the necessary conditions for the PR-controller design to ensure stable operation of a system with multiple power routers are proposed. These necessary conditions are verified through simulation studies. Though intuitively it is known that lower gains can lead to lower interactions between multiple power routers, this research provides an analytical basis to choose the controller gains that can ensure stable simultaneous operation of multiple power routers. The analysis is equally applicable for any series voltage injection controllers like UPFC, SSSC, BTB etc.

The proposed power router is designed for power flow control on meshed networks. Though the meshed networks are primarily present in transmission and sub transmission networks, there are some applications in distribution systems where the power router can be implemented. This research describes the potential applications of proposed power router in distribution system and the associated challenges in implementation. The power-router can be used either for power-flow control or for voltage control. A main constraint for power router in distribution applications is its impact on the fault current. It was shown that the application of proposed power-router in distribution systems is system specific and requires detailed system analysis.

The dynamic power flow controllability of the proposed power router was demonstrated at 13 kV, 1 MVA. Power-flow control of 1 MVA is achieved with a converter rated for 50 kVA. Significantly, the converter was rated to handle 1.3 kV while controlling the power flow at 13 kV. The fractional converter rating advantage of the proposed power-router is experimentally demonstrated. The NPC and the phase staggered approach used in the experimental prototype demonstrate the voltage scaling and current scaling methodology, respectively. The control algorithm, device gate signal generation, and protection mechanism were implemented on a DSP based platform. The effectiveness of the proposed control algorithm in achieving power flow control is experimentally demonstrated.

8.1.1 Summary of contributions

To summarize, this work has made the following contributions:

- Presented a low-cost power router (PR), capable of dynamic, independent control of active- and reactive-power flows on meshed grids.

- Presented the operating principle, detailed schematics, and various possible implementations of the proposed power router.

- Various operating modes are identified and a control algorithm has been proposed and verified through simulations.
- Developed small-signal and frequency-domain models of the power router from basic time-domain equations.
- Presented a three-tier protection system based on the fail-normal switch to avoid single point-of-failure.
- Verified the operation of proposed protection system in isolating the converter and the grid in the event of faults through simulation.
- Proposed an analytical method to evaluate the stability of a system with multiple power routers.
- Proposed necessary conditions for the PR-controller design to ensure stable operation of a system with multiple power routers. These necessary conditions are verified through simulation studies.
- Presented potential applications of proposed power router in distribution system and the associated challenges in implementation.
- Experimentally demonstrated the functionality and advantages of the proposed power router at 13 kV, 1 MVA.

8.2 Recommended Future Work

8.2.1 Experimental demonstration of stable operation of multiple PRs

This research has developed an analytical method to evaluate the stability of a system with multiple power routers and proposed controller design conditions to ensure stable operation of multiple power routers. The stability conditions have also been verified through simulation studies. It would be beneficial to experimentally validate the proposed stability conditions. The proposed stability conditions have been validated only for active power-flow control. It would be desirable to extend the analytical analysis to reactive power-flow control.

8.2.2 Impact of communication latency on operation of multiple PRs

In the proposed control architecture, each power router has local controller, which acts to control the power flow in the line at the desired value. But the desired value itself might be set from a remotely located central controller. In case of communication failure, the power-router controller will operate at the most recently updated power reference. It would be beneficial to simulate the impact of the communication failure on the system stability. In addition, it is necessary to understand the impact of any power-router failure on the operation of the rest of the power routers in the system.

8.2.3 Economic benefit of power routers

This research has demonstrated the technical advantages of the proposed power router compared to other power-flow-control solutions. It has also shown the cost advantage of the proposed power router compared to UPFC and CNT. It would be beneficial to show the economic advantages by evaluating the pay-back period for the investor.

8.2.4 Implementation of floating converters at very high voltages

In this research, the proposed power router was demonstrated at 13 kV. The actual implementation of the power-router will be at transmission and sub transmission levels, which is > 69 kV. The implementation of floating converters at such high voltages is associated with its own challenges. Though similar challenges have been addressed in case of FACTS devices like TCSC, which have been practically implemented with floating converters at voltages up to 369 kV, the challenges unique to the proposed system would be more apparent when it is implemented at higher voltages. Of importance would be the implementation of low power electronics at floating voltages. Also interesting would be to evaluate the cost involved in designing the power router to meet the appropriate basic-insulation-level (BIL) requirements.

APPENDIX A: PUBLICATIONS, PATENTS AND TECHNOLOGY TRANSFER

Publications

1. Kandula R.P, Rohit Moghe, Amrit Iyer, Jorge Hernandez, and Deepak Divan, “Power Router for Meshed Systems Based on a Fractionally-Rated BTB Converter”, IEEE Transactions on Power Electronics, 2013.

2. Kandula, R.P.; Iyer, A.; Divan, D., "Stable operation of multiple power routers," *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* , vol., no., pp.1435,1442, 15-19 Sept. 2013.

3. Iyer, A.; Kandula, R.; Moghe, R.; Hernandez, J.; Lambert, F.; Divan, D., "Validation of the Plug-and-Play AC/AC Power Electronics Building Block (AC-PEBB) for Medium Voltage Grid Control Applications," *Industry Applications, IEEE Transactions on* , vol.PP, no.99, pp.1,1

4. Hernandez, J.E.; Kandula, R.P.; Lambert, F.C.; Divan, D., "A Practical Directional Third Harmonic Hybrid Active Filter for Medium-Voltage Utility Applications," *Industry Applications, IEEE Transactions on* , vol.49, no.6, pp.2674,2683, Nov.-Dec. 2013.

5. Iyer, A.; Moghe, R.; Kandula, R.; Hernandez, J.; Divan, D., "Validation of the plug-and-play AC/AC power electronics building block (AC-PEBB) for medium voltage grid control applications," *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* , vol., no., pp.2544,2551, 15-19 Sept. 2013.

6. Iyer, A.; Moghe, R.; Kandula, R.; Hernandez, J.; Divan, D., "Plug-and-play AC/AC power electronics building blocks (AC-PEBBs) for grid control," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.1354,1361, 15-20 Sept. 2012.

7. Moghe, R.; Kandula, R.P.; Iyer, A.; Divan, D., "Loss comparison between SiC, hybrid Si/SiC, and Si devices in direct AC/AC converters," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.3848,3855, 15-20 Sept. 2012.

8. Kandula, R.P.; Iyer, A.; Moghe, R.; Hernandez, J.E.; Divan, D., "Power flow controller for meshed systems with a fractionally rated BTB converter," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.4053,4060, 15-20 Sept. 2012.

9. Hernandez, J.E.; Kandula, R.P.; Lambert, F.; Divan, D., "A practical directional third harmonic hybrid active filter for medium voltage utility applications," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.219,226, 15-20 Sept. 2012.

10. Moghe, R.; Kreikebaum, F.; Hernandez, J.E.; Kandula, R.P.; Divan, D., "Mitigating distribution transformer lifetime degradation caused by grid-enabled vehicle (GEV) charging," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* , vol., no., pp.835,842, 17-22 Sept. 2011.

11. Kandula, R.P.; Hernandez, J.E.; Divan, D., "Directional Triplen Hybrid Active Filter for radial systems," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* , vol., no., pp.4058,4065, 17-22 Sept. 2011.

12. Das, D.; Kandula, R.P.; Harley, R.; Divan, D.; Schatz, J.; Munoz, J., "Design and testing of a medium voltage Controllable Network Transformer Prototype with an integrated hybrid active filter," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* , vol., no., pp.4035,4042, 17-22 Sept. 2011.

Patents

1. D. Divan, and Kandula R.P, Anish Prasai, "Power-Flow Controller with a Fractionally Rated Back-to-Back Converter," US 20140009980 A1 patent pending.

2. D. Divan, Kandula R.P, "Directional Triplen Hybrid Active Filter for Radial Systems," U.S. Provisional patent filed.

ARPA-E Grant

The research has been partly funded by DoE through an ARPA-e grant under the Agile Delivery of Electrical Power Technology (ADEPT) program (Grant # DE-FOA-0000288).

Technology Transfer

The technology developed as a part of this research has resulted in a US patent (US 2014/0009980 A1) and has been transferred under “Technology transfer program” to Varentec Inc.

APPENDIX B

Device Loss Model Coefficients

$I_{nom} = 100\ A, E_{nom} = 40\ mJ$	a1	a2	a3
IGBT turn-off loss	-0.19	1.3365	-0.2649
IGBT turn-on loss	0.0347	1.388	-0.4233
IGBT reverse recovery loss	0.0447	1.3208	-0.2851

Device On-State Voltage Model Coefficients

$I_{nom} = 100\ A, V_{nom} = 3\ V$	a1	a2	a3
IGBT	0.3833	0.4014	0.0
Free-wheeling diode	0.26	0.3275	0.0
NPC diode	0.1203	1.2387	-0.9916

IEEE 39 Bus data

Generators:

Unit No.	**H**	**Ra**	**x'd**	**x'q**	**Xd**	**Xq**	**T'do**	**T'qo**	**xl**
1	500.0	0	0.006	0.008	0.02	0.019	7.0	0.7	0.003
2	30.3	0	0.0697	0.170	0.295	0.282	6.56	1.5	0.035
3	35.8	0	0.0531	0.0876	0.2495	0.237	5.7	1.5	0.0304
4	28.6	0	0.0436	0.166	0.262	0.258	5.69	1.5	0.0295
5	26.0	0	0.132	0.166	0.67	0.62	5.4	0.44	0.054
6	34.8	0	0.05	0.0814	0.254	0.241	7.3	0.4	0.0224
7	26.4	0	0.049	0.186	0.295	0.292	5.66	1.5	0.0322
8	24.3	0	0.057	0.0911	0.290	0.280	6.7	0.41	0.028
9	34.5	0	0.057	0.0587	0.2106	0.205	4.79	1.96	0.0298
10	42.0	0	0.031	0.008	0.1	0.069	10.2	0.0	0.0125

Line/Transformers:

Line Data					Transformer Tap	
From Bus	**To Bus**	**R**	**X**	**B**	**Magnitude**	**Angle**
1	2	0.0035	0.0411	0.6987	0.000	0.00
1	39	0.0010	0.0250	0.7500	0.000	0.00
2	3	0.0013	0.0151	0.2572	0.000	0.00
2	25	0.0070	0.0086	0.1460	0.000	0.00
3	4	0.0013	0.0213	0.2214	0.000	0.00
3	18	0.0011	0.0133	0.2138	0.000	0.00
4	5	0.0008	0.0128	0.1342	0.000	0.00
4	14	0.0008	0.0129	0.1382	0.000	0.00
5	6	0.0002	0.0026	0.0434	0.000	0.00
5	8	0.0008	0.0112	0.1476	0.000	0.00
6	7	0.0006	0.0092	0.1130	0.000	0.00
6	11	0.0007	0.0082	0.1389	0.000	0.00
7	8	0.0004	0.0046	0.0780	0.000	0.00
8	9	0.0023	0.0363	0.3804	0.000	0.00
9	39	0.0010	0.0250	1.2000	0.000	0.00
10	11	0.0004	0.0043	0.0729	0.000	0.00
10	13	0.0004	0.0043	0.0729	0.000	0.00
13	14	0.0009	0.0101	0.1723	0.000	0.00
14	15	0.0018	0.0217	0.3660	0.000	0.00
15	16	0.0009	0.0094	0.1710	0.000	0.00
16	17	0.0007	0.0089	0.1342	0.000	0.00
16	19	0.0016	0.0195	0.3040	0.000	0.00
16	21	0.0008	0.0135	0.2548	0.000	0.00
16	24	0.0003	0.0059	0.0680	0.000	0.00

17	18	0.0007	0.0082	0.1319	0.000	0.00
17	27	0.0013	0.0173	0.3216	0.000	0.00
21	22	0.0008	0.0140	0.2565	0.000	0.00
22	23	0.0006	0.0096	0.1846	0.000	0.00
23	24	0.0022	0.0350	0.3610	0.000	0.00
25	26	0.0032	0.0323	0.5130	0.000	0.00
26	27	0.0014	0.0147	0.2396	0.000	0.00
26	28	0.0043	0.0474	0.7802	0.000	0.00
26	29	0.0057	0.0625	1.0290	0.000	0.00
28	29	0.0014	0.0151	0.2490	0.000	0.00
12	11	0.0016	0.0435	0.0000	1.006	0.00
12	13	0.0016	0.0435	0.0000	1.006	0.00
6	31	0.0000	0.0250	0.0000	1.070	0.00
10	32	0.0000	0.0200	0.0000	1.070	0.00
19	33	0.0007	0.0142	0.0000	1.070	0.00
20	34	0.0009	0.0180	0.0000	1.009	0.00
22	35	0.0000	0.0143	0.0000	1.025	0.00
23	36	0.0005	0.0272	0.0000	1.000	0.00
25	37	0.0006	0.0232	0.0000	1.025	0.00
2	30	0.0000	0.0181	0.0000	1.025	0.00
29	38	0.0008	0.0156	0.0000	1.025	0.00
19	20	0.0007	0.0138	0.0000	1.060	0.00

DSP Code For Controller

```
#include "DSP281x_Device.h"        // DSP281x Headerfile Include File (chose device)
#include "DSP281x_Examples.h"      // DSP281x Examples Include File (Set CPU clock)
#include "math.h"                  // ANSI C Include File
#include "stdlib.h"
#include "IQmathLib.h"
#define N 256                      // Number of Samples per period
#define pi 3.14159265358979        // PI
#define  Conv_Start                GpioDataRegs.GPFDAT.bit.GPIOF8
#define  PLL                       GpioDataRegs.GPBDAT.bit.GPIOB15
#define  FMain                     GpioDataRegs.GPDDAT.bit.GPIOD1
#define  START_CONT                GpioDataRegs.GPBDAT.bit.GPIOB13
#define  Sys_Healthy               GpioDataRegs.GPBDAT.bit.GPIOB14
#define  Spare_op                  GpioDataRegs.GPFDAT.bit.GPIOF10
#define   EGPIO1                   GpioDataRegs.GPFDAT.bit.GPIOF4
/* --- Start: Prototype statements for functions found within this file. --- */
        void init_ev(void);
        void InitGPIO(void);
        void spi_init(void);
        void dac_send(double x,double xmin, double xmax, int channel);
        interrupt void t1uf_isr(void);
        void filter( _iq *flt_ip, _iq *flt_op_stg1,_iq *flt_op, int ctr1);
/* ----- end: Prototype statements for functions found within this file. --- */
/* ---------- Start: Global variables used in this example ---------------- */
        int     Tp=3720;                  // updown counting mode, 75MHz/Tp = 10 kHz
        int     Tp_EVB=7440;
        _iq     sine[N];                  // sine table
        // 2nd order filter constants, f(cutoff) = 10 Hz. F(samp) = 10 KHz
        _iq     flt_coeff_b[3] = {_IQ(0.00000983),_IQ(0.00001965),_IQ(0.00000983)};
        _iq      flt_coeff_a[3]                    =                    {_IQ(1.0),_IQ(-
1.991114292201654),_IQ(0.991153595868935)};
```

```
// sine wave generator for PLL testing
Uint16   theta, delta_theta = 6;
_iq      sinetheta;
// PI compensator constants
_iq      freq = _IQ(1.0), theta_pll=_IQ(45), pll_gain = _IQ(2.0);       // Initial freq and theta
_iq      Ki_pll = _IQ(0.00005), Kp_pll = _IQ(0.1);                      // PI loop constants
_iq      Vdc_Ref = _IQ(0.24);
_iq      Vdc_max = _IQ(0.75);
_iq      MI  = _IQ(0.065), mi_act = _IQ(0.0);
_iq       Ki_Vdc = _IQ(0.000005), Kp_Vdc = _IQ(0.1), Id_lmt = _IQ(0.02);      // Vdc PI
loop constants
_iq      Ki_Id = _IQ(0.00001), Kp_Id = _IQ(0.1);                        // Id loop constants
_iq      Ki_Iq = _IQ(0.00001), Kp_Iq = _IQ(0.1);                        // Iq loop constants
_iq      Vdc_temp;
int      Vdc_flt_flag = 0;
// PI compensator variables
_iq      e_pll, iop_pll , temp2;
_iq      e_Vdc, iop_Vdc, Id_Ref;
_iq      e_Id, iop_Id, Vq_Ref;
_iq      e_Iq, iop_Iq, Vd_Ref;
// PLL Variables
_iq      S,C, CS;
Uint16  theta_index;                          // for debugging
int     check;
// Filter variables
_iq      pll_flt_ip[3], pll_flt_op_stg1[3], pll_flt_op[3];
_iq      Vdc_flt_ip[3], Vdc_flt_op_stg1[3], Vdc_flt_op[3];
_iq      Vin_flt_ip[3], Vin_flt_op_stg1[3], Vin_flt_op[3];
_iq      Id_flt_ip[3], Id_flt_op_stg1[3], Id_flt_op[3];
_iq      Iq_flt_ip[3], Iq_flt_op_stg1[3], Iq_flt_op[3];
// ADC signals
```

```
 _iq      Vin=0.0, Vdc = _IQ(0.0), Vcap = _IQ(0.0), Pwr_Ref = _IQ(0.0);
_iq      Iline = _IQ(0.0), Idiff1 = _IQ(0.0), Idiff2 = _IQ(0.0);
_iq      Idiff;
int      Phi_Ref = 0, Phi_act = 0;
int      index_i =0,temp;
long     temp3;
// PLL variables
_iq D_rect, D_inv;
// Counters
Uint16   i=0,ctr1=0,ctr2=0,a=0;
int16    k=0;
// Flags
int Flt_flag;
int Start_flag;
// get_sign() variables
int max_count=5,counter1=0;
int aS1=1;
/* ---------- End: Global variables used in this example ---------- */
// Start. For Flash loading
extern Uint16 RamfuncsLoadStart;
extern Uint16 RamfuncsLoadEnd;
extern Uint16 RamfuncsRunStart;
// End. For Flash loading
void main(void)
{
/* ------------------------------------------------------------------
          Initialize System Control: PLL, WatchDog, enable Peripheral Clocks
          This example function is found in the DSP281x_SysCtrl.c file.
------------------------------------------------------------------ */
          InitSysCtrl();
/* --------------------Initalize GPIO:--------------------------------- */
```

```
        InitGPIO();
/* ------Clear all interrupts and initialize PIE vector table:---------- */
        DINT;                           // Disable CPU interrupts
/* --------------------Flash Initialization---------------------------- */
        // MemCopy(&RamfuncsLoadStart, &RamfuncsLoadEnd, &RamfuncsRunStart);
        // InitFlash();
/* ---------------------------------------------------------------------
        Initialize PIE control registers to their default state.
        Default state: PIE interrupts disabled and all flags cleared.
        This function is found in the DSP281x_PieCtrl.c file.
--------------------------------------------------------------------- */
        InitPieCtrl();
/* Disable CPU interrupts and clear all CPU interrupt flags:*/
        IER = 0x0000;
        IFR = 0x0000;
/*  ---------------------------------------------------------------------
         Initialize the PIE vector table with pointers to the shell Interrupt
        Service Routines (ISR).This will populate the entire table, even if
         the interrupt is not used in this example. This is useful for debug
         purposes. The shell ISR routines are found in DSP281x_DefaultIsr.c.
         This function is found in DSP281x_PieVect.c.
 --------------------------------------------------------------------- */
        InitPieVectTable();
/* --------------ISR functions found within this file.------------------ */
        EALLOW;                 // This is needed to write to EALLOW protected register
        PieVectTable.T1UFINT = &t1uf_isr;
        EDIS;               // This is needed to disable write to EALLOW protected registers
/* --Initialize all Device Peripherals: (in DSP281x_InitPeripherals.c)-- */
        // InitPeripherals(); // Not required for this example
 /* -------------Initialize ADC,EVA, EVB and SPI------------------------- */
        AdcRegs.ADCTRL1.bit.ACQ_PS = 0x0;      // S/H width in ADC module periods
```

```
        AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;       // 1  Cascaded mode
        AdcRegs.ADCTRL1.bit.CONT_RUN = 0;       // Setup start stop mode
        AdcRegs.ADCTRL3.bit.ADCCLKPS    =0x4;                   // ADC clock =
HSPCLK/(2*ADC_CKPS) =       75MHz/8 = 9.375 MHz
        AdcRegs.ADCMAXCONV.bit.MAX_CONV1 =0xF;   // Setup number of conv's
on SEQ1
        AdcRegs.ADCCHSELSEQ1.all = 0x3210;
        AdcRegs.ADCCHSELSEQ2.all = 0x7654;
        AdcRegs.ADCCHSELSEQ3.all = 0xBA98;
        AdcRegs.ADCCHSELSEQ4.all = 0xFEDB;
        InitAdc();                      // For this example, init the ADC
        init_ev();                       // Initialize Event Manger A and Event Manger B
        //init_evb();                   // Initialize Event Manger B
        spi_init();                      // init SPI
        EvaRegs.CMPR1 = 0;                  // Initialize PWM/compare  registers
        EvaRegs.CMPR2 = Tp;                 // Initialize PWM/compare registers
/* ------------- User defined variable Iitialization.-------------------- */
        for(i=0;i<N;i++)
        {
        sine[i] = _IQ(sin(0.5*pi*i/N));                 // Populate Sine table (0 to 90 deg)
        }
        for (i=0;i<3;i++)                   // Init filter arrays
        {
        pll_flt_ip[i] = _IQ(0.0);
        Vdc_flt_ip[i] = _IQ(0.0);
        Vin_flt_ip[i] = _IQ(0.0);
        Id_flt_ip[i] = _IQ(0.0);
        Iq_flt_ip[i] = _IQ(0.0);
        pll_flt_op_stg1[i] = _IQ(0.0);
        Vdc_flt_op_stg1[i] = _IQ(0.0);
        Vin_flt_op_stg1[i] = _IQ(0.0);
```

```
        Id_flt_op_stg1[i] = _IQ(0.0);
        Iq_flt_op_stg1[i] = _IQ(0.0);
        pll_flt_op[i] = _IQ(0.0);
        Vdc_flt_op[i] = _IQ(0.0);
        Vin_flt_op[i] = _IQ(0.0);
        Id_flt_op[i] = _IQ(0.0);
        Iq_flt_op[i] = _IQ(0.0);
        }
        iop_pll = _IQ(0.0);
        iop_Vdc = _IQ(0.0);
        START_CONT = 0;                         // Init debugging digital o/p
/* ----------Enable interrupts required for this example---------------- */
        PieCtrlRegs.PIECRTL.bit.ENPIE = 1;          // Enable the PIE block
        PieCtrlRegs.PIEIER2.bit.INTx6 = 1;      // Enable PIE Group 2, INT 6 (T1UF)
        IER=0x2;                                    // Enable CPU INT3
        EINT;                                       // Enable Global Interrupts
        ERTM;                                       // Enable Global realtime interrupt DBGM
/* ----------------Just sit and loop forever:---------------------------- */
        Flt_flag = 0;
        Start_flag = 0;
        Spare_op = 0;
        for(;;);      // Triangular Period
}
// ISR's used in this example
// INT 2.6
interrupt void t1uf_isr(void)                // Interrupt from EV-A
{
// EGPIO1=0;
        EvaRegs.T1PR = Tp;                      // Reload for EVA
        EvbRegs.T3PR = Tp_EVB;                  // Reload for EVB
/* ---------------------- Start:  ADC Code-----------------------------
```

```
        1) Clear interrupt
        2) Reset counter
        3) Start conversion
        4) Will till end of conversion
------------------------------------------------------------------- */
        AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;          // clear interrupt
        AdcRegs.ADCTRL2.bit.RST_SEQ1=1;              //Reset counter to CONV00

        AdcRegs.ADCTRL2.bit.SOC_SEQ1=1;      // start of secuence by software
        while( AdcRegs.ADCST.bit.INT_SEQ1 == 0);     // wait till End of conversion
        //temp = (AdcRegs.ADCRESULT0>>4) - 2100;
        Vin = (((long)(AdcRegs.ADCRESULT0))<<9) - _IQ(1.035);
        Vdc = (((long)(AdcRegs.ADCRESULT1))<<9) - _IQ(1.05);
       //Vdc = _IQmpy(Vdc, _IQ(0.5));  // sensor connected across whole dc bus
        Vcap =(((long)(AdcRegs.ADCRESULT2))<<9) - _IQ(1.02
        //Iline = (((long)(AdcRegs.ADCRESULT8))<<9) - _IQ(1.03
        Idiff1 = (((long)(AdcRegs.ADCRESULT9))<<9) - _IQ(1.04);
        //Idiff2 = (((long)(AdcRegs.ADCRESULT10))<<9) - _IQ(1.024
        //Idiff = Idiff1-Idiff2;
        //Idiff = _IQmpy(Idiff, _IQ(0.5));
        Idiff = Idiff1;
        Pwr_Ref  =  (((long)(AdcRegs.ADCRESULT4))<<8);  //  to  convert  3.0V  to
_iq(1.0) (iq 24 by default)
/* ----------------------- End:  ADC Code------------------------------ */
/* ----------------------Start:  Theta increment----------------------
        1) Increment internally generated refernce sine wave
        2) Increment actual theta (PLL o/p)
        3) Find Cos (theta)
         Theta in pu form (1.0 = 360 deg = 1024 array size)
 ------------------------------------------------------------------- */
```

```
        theta_pll += _IQmpy(_IQ(0.006),freq); // Increment theta (PLL o/p) 60*freq
(pu)/Fs
        if(theta_pll  >= _IQ(1))
        {
        theta_pll = theta_pll - _IQ(1.0);
        EGPIO1 = 1;
        }
        // find Sin theta
        theta_index =  (int)(_IQ18int(_IQ18mpyIQX(theta_pll,24,_IQ18(1024),18)));
        if (theta_index >= 1024) theta_index = theta_index - 1024;
        if (theta_index < 256)              {S =  sine[theta_index];}
        else if (theta_index < 512)  {S = sine[511-theta_index];}
        else if (theta_index < 768)  {S = -sine[theta_index - 512];}
        else                        {S = -sine[1023-theta_index];}
        // for slow variation of Phi in cos(wt+Phi) for inv cotrol
if (theta_index < 8)
        {
        if (Pwr_Ref < 0) Pwr_Ref = 0;
        Phi_Ref =  (int)(_IQ18int(_IQ18mpyIQX(Pwr_Ref,24,_IQ18(1024),18)));
        if (Phi_act < Phi_Ref )  Phi_act += 1;
        else if (Phi_act > Phi_Ref )  Phi_act -= 1;
        }
        dac_send(theta_index,0, 1024,1);
        // find Cos theta (add 256 (90 deg) to theta_index)
        theta_index +=  256;
        if (theta_index >= 1024) theta_index = theta_index - 1024;
        if (theta_index < 256)              {C =  sine[theta_index];}
        else if (theta_index < 512)  {C = sine[511-theta_index];}
        else if (theta_index < 768)  {C = -sine[theta_index - 512];}
        else                        {C = -sine[1023-theta_index];}
/* ------------------------ End:  Theta increment---------------------- */
```

```
        ctr1 += 1;                          // used for filtering satges
        if (ctr1>2) ctr1=0;
/* ------------------------- Start:  PLL code ------------------------- */
        Vin = _IQmpy(Vin,pll_gain);
        pll_flt_ip[ctr1] =  _IQmpy(Vin,C);          //multiply with Cos and average
        //pll_flt_ip[ctr1] =  _IQmpy(pll_flt_ip[ctr1],pll_gain);
        filter(pll_flt_ip,pll_flt_op_stg1,pll_flt_op,ctr1);       // call filter
/* ------------------------- PI loop for PLL ---------------------- */
        e_pll    = pll_flt_op[ctr1];
        iop_pll += _IQmpy(e_pll,Ki_pll);
        freq    = _IQ(1.0) + iop_pll + _IQmpy(Kp_pll,e_pll);
        if (iop_pll > _IQ(0.025)) iop_pll = _IQ(0.025);        // Limit the integrator
        else if (iop_pll < _IQ(-0.025)) iop_pll = _IQ(-0.025);
        if (freq > _IQ(1.025))  freq = _IQ(1.025);            // Limit PI output
        else if (freq < _IQ(0.975)) freq = _IQ(0.975);
/* ------------------------- End:  PLL code ---------------------------- */
        //Vin_flt_ip[ctr1] =  _IQabs(Vin);          //get mean value
        //filter(Vin_flt_ip,Vin_flt_op_stg1,Vin_flt_op,ctr1);       // call filter
        Vdc_flt_ip[ctr1] =  Vdc;
        filter(Vdc_flt_ip,Vdc_flt_op_stg1,Vdc_flt_op,ctr1);       // call filter
        if ((Vdc > Vdc_max)||(Vcap > Vdc_max)) Vdc_flt_flag =1 ;
        //else Vdc_flt_count = 0;
        //if (Vdc_flt_count > 1)  Vdc_flt_flag = 1;
EvaRegs.T1CMPR = Tp; // open BR
        EvaRegs.T2CMPR = Tp; // open BR
if ((Conv_Start == 1) && ( FMain == 0) && (Vdc_flt_flag == 0))
        {
        Vdc_temp = Vdc_flt_op[ctr1];
        Sys_Healthy = 1;
        START_CONT = 1;
        //EvaRegs.T1CMPR = 3600; // dc load on
```

```
        //EvaRegs.T2CMPR = 3600; // dc load on
if (Flt_flag == 1)
        {
EvaRegs.ACTRA.all = 0x0000; // 0x00066
        EvbRegs.ACTRB.all = 0x0066;
                }
        Flt_flag = 0;
        if (Start_flag == 0)
        {
        if ((theta_index >= 508) && (theta_index <= 516)) // wait for voltage peak
        {
        EvaRegs.ACTRA.all = 0x0000; // 0x00066
        Start_flag = 1;
          }
        }
/* ------------------------- Start  Vdc loop ---------------------------- */
        // generate id_ref and limit to 0.2
       e_Vdc    = Vdc_Ref-Vdc;
         // ref = mean*1.57*1.2
        iop_Vdc         += _IQmpy(e_Vdc,Ki_Vdc);
        Id_Ref  = iop_Vdc + _IQmpy(Kp_Vdc,e_Vdc);
        if (iop_Vdc > Id_lmt) iop_Vdc = Id_lmt;        // Limit the integrator
        else if (iop_Vdc < -Id_lmt) iop_Vdc = -Id_lmt;
        if (Id_Ref > Id_lmt)  Id_Ref = Id_lmt;             // Limit PI output
        else if (Id_Ref < -Id_lmt) Id_Ref = -Id_lmt;
/* ------------------------- End:  Vdc loop ---------------------------- */
/* ------------------------- Start  Id loop ----------------------------
        // generate Vq_ref and limit to 0.2
        // to increase id increase Vq in negative direction
        Id_flt_ip[ctr1] =  _IQmpy(Idiff,S);
        filter(Id_flt_ip,Id_flt_op_stg1,Id_flt_op,ctr1);       // call filter
```

```
        e_Id     = Id_Ref - Id_flt_op[ctr1];

        iop_Id  += _IQmpy(e_Id,Ki_Id);
        Vq_Ref  = -(iop_Id + _IQmpy(Kp_Id,e_Id));
        if (iop_Id > _IQ(0.2)) iop_Id = _IQ(0.2);       // Limit the integrator
        else if (iop_Id < _IQ(-0.2)) iop_Id = _IQ(-0.2);
        if (Vq_Ref > _IQ(0.2))  Vq_Ref = _IQ(0.2);            // Limit PI output
        else if (Vq_Ref < _IQ(-0.2)) Vq_Ref = _IQ(-0.2);
 ------------------------- End:  Id loop ---------------------------- */
/* ------------------------- Start  Iq loop ----------------------------
        // generate Vd_ref and limit
        // to increase id increase Vd
        Iq_flt_ip[ctr1] =  _IQmpy(Idiff,C);
        filter(Iq_flt_ip,Iq_flt_op_stg1,Iq_flt_op,ctr1);      // call filter
        e_Iq     =  0.0 - Iq_flt_op[ctr1];

        iop_Iq  += _IQmpy(e_Iq,Ki_Iq);
        Vd_Ref  = _IQ(0.8) + iop_Iq + _IQmpy(Kp_Iq,e_Iq);
        if (iop_Iq > _IQ(0.2)) iop_Iq = _IQ(0.2);       // Limit the integrator
        else if (iop_Iq < _IQ(-0.2)) iop_Iq = _IQ(-0.2);
        if (Vd_Ref > _IQ(1.0))  Vd_Ref = _IQ(1.0);            // Limit PI output
        else if (Vd_Ref < _IQ(0.6)) Vd_Ref = _IQ(0.6);
 ------------------------- End:  Id loop ---------------------------- */
/* ------------------------- Start: PWM signal generation -------------- */
        //D_rect = _IQmpy(Vd_Ref,S) + _IQmpy(Vq_Ref, C);
        D_rect = _IQmpy(_IQ(0.94),S) + _IQmpy(_IQ(0.09), C);
// DC bus controlled at 1.2 pu
        D_rect = D_rect - _IQmpy(Id_Ref, C);
        //D_rect = _IQmpy(_IQ(0.4),S);
        D_rect  = _IQ(0.5) + _IQmpy(D_rect,_IQ(0.5));
        if (D_rect > _IQ(0.98)) D_rect = _IQ(0.98);
```

```
        else if (D_rect < _IQ(0.02)) D_rect = _IQ(0.02);
        if (D_rect >= _IQ(0.5))
        {
        D_rect = _IQmpy(_IQ(2.0),D_rect)-_IQ(1.0);
        EvaRegs.CMPR1=Tp -(int)(_IQ18int(_IQ18mpyIQX(D_rect,24,_IQ18(Tp),18)));
        EvaRegs.CMPR2  =  0 ;
        }
        else
        {
        D_rect = _IQmpy(_IQ(2.0),D_rect);
        EvaRegs.CMPR1  =  Tp;
        EvaRegs.CMPR2=Tp- (int)(_IQ18int(_IQ18mpyIQX(D_rect,24,_IQ18(Tp),18)));
        }
        // for calculation of Cos (wt +Phi)
theta_index+=Phi_act ; //+(int)(_IQ20int(_IQ20mpyIQX(theta_pll,24,_IQ20(1024),20)));
        if (theta_index >= 1024) theta_index = theta_index - 1024;
        if (theta_index < 256)              {CS =  sine[theta_index];}
        else if (theta_index < 512)  {CS = sine[511-theta_index];}
        else if (theta_index < 768)  {CS = -sine[theta_index - 512];}
        else                        {CS = -sine[1023-theta_index];}
        if (theta_index < 8)
        {
        if (mi_act < MI) mi_act += _IQ(0.00002);
        }
        D_inv = _IQ(0.5)+ _IQmpy(mi_act,CS);
        dac_send(_IQtoF(D_inv),0.0, 1.0,2);
        if (D_inv >= _IQ(0.5))
        {
        D_inv = _IQmpy(_IQ(2.0),D_inv)-_IQ(1.0);
        EvbRegs.CMPR4=Tp_EVB(int)(_IQ16int(_IQ16mpyIQX(D_inv,24,_IQ16(Tp_E
VB),16)));
```

```
EvbRegs.CMPR5  =  0 ;
//EvaRegs.CMPR3=Tp-(int)(_IQ18int(_IQ18mpyIQX(D_inv,24,_IQ18(Tp),18)));
//EvbRegs.CMPR6  =  0 ;
}
else
{
D_inv = _IQmpy(_IQ(2.0),D_inv);
EvbRegs.CMPR4  =  Tp_EVB;
EvbRegs.CMPR5=(Tp_EVB+1)-
(int)(_IQ16int(_IQ16mpyIQX(D_inv,24,_IQ16(Tp_EVB),16)));
//EvaRegs.CMPR3 =   Tp;
//EvbRegs.CMPR6                    =                    (Tp+1)                -
(int)(_IQ18int(_IQ18mpyIQX(D_inv,24,_IQ18(Tp),18)));
}
}
else
{
Sys_Healthy = 0;
if (FMain == 1)
        {
START_CONT = 0;
Flt_flag = 0;
        EvaRegs.ACTRA.all = 0x0000;
EvbRegs.ACTRB.all = 0x0000;
EvaRegs.T1CMPR = 0; // discharge cap
EvaRegs.T2CMPR = 0; // discharge cap
}
if (Conv_Start == 0)
{
        Start_flag = 0;
        EvaRegs.ACTRA.all = 0x0000; // sw1-sw8 off
```

```
        EvbRegs.CMPR4  =  Tp_EVB;       // sw9/12 off
        EvbRegs.CMPR5  =  0;        // sw10/11 on
        //EvaRegs.CMPR3  =  Tp;       // sw13/16 off
        //EvbRegs.CMPR6  =  0;        // sw14/15 on
        mi_act = _IQ(0.0);
        iop_Vdc = _IQ(0.0);
        }
        if (Vdc_flt_flag == 1)
        {
        START_CONT = 0;
        Flt_flag = 0;
        EvaRegs.ACTRA.all = 0x0000;
        EvbRegs.CMPR4  =  Tp_EVB;       // sw9/12 off
        EvbRegs.CMPR5  =  0;        // sw10/11 on
        //EvaRegs.CMPR3  =  Tp;       // sw13/16 off
        //EvbRegs.CMPR6  =  0;        // sw14/15 on
        if (Vcap >= Vdc_max) EvaRegs.T1CMPR = 0;      // Turn on BR1
        else EvaRegs.T1CMPR = Tp;                // Turn off BR1
          if (Vdc >= Vdc_max) EvaRegs.T2CMPR = 0;      // Turn on BR12
        else EvaRegs.T2CMPR = Tp;                // Turn off BR2
                }
          }
        //START_CONT = 1;                           // START1 for contactor
        //Sys_Healthy = 1;
/* ------------------------ End: PWM signal generation ---------------- */
        //EGPIO1=0;
        // Enable more interrupts from this timer
        EvaRegs.EVAIMRA.bit.T1UFINT = 1;
        // Note: To be safe, use a mask value to write to the entire
        // EVAIFRB register.  Writing to one bit will cause a read-modify-write
        // operation that may have the result of writing 1's to clear
```

```
        // bits other then those intended.
        EvaRegs.EVAIFRA.all = BIT9;
        // Acknowledge interrupt to receive more interrupts from PIE group 2
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}
void filter( _iq *flt_ip, _iq *flt_op_stg1,_iq *flt_op, int ctr1)
{
        int k,i;
/* ---Start: Butterworth 4th order (2 *2) Filter implementation----- */
/* ----------------- Start: Filter Stage1 ---------------------- */
        k = ctr1-1;
        flt_op_stg1[ctr1] = _IQmpy(flt_coeff_b[0],flt_ip[ctr1]);
        for(i=1;i<3;i++)
        {
        if (k < 0) k = 2;
         flt_op_stg1[ctr1] += _IQmpy(flt_coeff_b[i],flt_ip[k])-\
        _IQmpy(flt_coeff_a[i],flt_op_stg1[k]);
        k = k-1;
        }
/* ------------------- End: Filter Stage1 ---------------------- */
/* ----------------- Start: Filter Stage2 ---------------------- */
        k = ctr1-1;
        flt_op[ctr1] = _IQmpy(flt_coeff_b[0],flt_op_stg1[ctr1]);
        for(i=1;i<3;i++)
        {
        if (k < 0) k = 2;
        flt_op[ctr1] += _IQmpy(flt_coeff_b[i],flt_op_stg1[k])-\
         _IQmpy(flt_coeff_a[i],flt_op[k]);
        k = k-1;
        }
/* ------------------- End: Filter Stage1 ---------------------- */
```

```
/* ---End: Butterworth 4th order (2 *2) Filter implementation------- */
}
void init_ev()
{
/* ------------- EVA Configure T1PWM, T2PWM, PWM1-PWM6 ----------------- */
/* -----------------Initalize EVA Timer2 --------------------------
        For synchronization of timer1 and timer2 of EVA:
        1) Set Timer2 to start with TENABLE bit of timer1 and
        2) Set Timer2 to use period reg of Timer1
------------------------------------------------------------------ */
        //EvaRegs.T2PR = Tp;
// Timer2 period, not needed if synchronized with timer1
        EvaRegs.T2CMPR = Tp;            // Initializ Timer2  compare reg
        EvaRegs.T2CNT = 0x0000;             // Timer2 counter
        EvaRegs.T2CON.all = 0x0883;           // TMODE = cont up/down, T2 compare
enable
/* -----------------Initalize EVA Timer1 --------------------------- */
        EvaRegs.T1PR = Tp;                  // Timer1 period
        EvaRegs.T1CMPR = Tp;            // Timer1 compare for chopper
        EvaRegs.T1CNT = 0x0000;             // Timer1 counter
/* -----------------Initalize EVB Timer3 --------------------------- */
        EvbRegs.T3PR = Tp_EVB;                      // Timer3 period
        EvbRegs.T3CNT = 0x0000;             // Timer3 counter
/* ----------------Setup T1/T2 compare outputs (chopper)------------ */
       // Polarity of GP Timer 2 Compare = Active high
        EvaRegs.GPTCONA.bit.T2PIN = 2;     // Timer 2 Compare polarity= Active high
        EvaRegs.GPTCONA.bit.T1PIN = 2;     // Timer 1 Compare polarity= Active high
        EvaRegs.GPTCONA.bit.TCMPOE = 1;        // Enable Timer compare o/p
/* --------- Enable Period interrupt bits for GP timer 1 ----------- */
        EvaRegs.EVAIMRA.bit.T1UFINT = 1;
        EvaRegs.EVAIFRA.bit.T1UFINT = 1;
```

```
/* ------------------ Enable EVA Timers ---------------------------- */
        EvaRegs.T1CON.all = 0x0842;
// TMODE = cont up/down, T1& T2 enable, T1 compare enable

/* ------------------ Enable EVB Timers ---------------------------- */
        EvbRegs.T3CON.all = 0x0842;
// TMODE = cont up/down, T3& T4 enable, T3 compare enable
/*---------------- Initialize Compare registers---------------------- */
        EvaRegs.CMPR1 = Tp;
        EvaRegs.CMPR2 = 0x0000;
        EvaRegs.CMPR3 = Tp;
        EvbRegs.CMPR4 = Tp_EVB;
EvbRegs.CMPR5 = 0x0000;
        EvbRegs.CMPR6 = 0x0000;
/* ----- Compare action control.  Action that takes place ----------
         output pin 1 PWM1, PWM3, PWM5 - active high
        output pin 2 PWM2, PWM4, PWM6 - active low
 ------------------------------------------------------------------- */
        EvaRegs.ACTRA.all = 0x0000; //0x0000-rectifier // 0x00966 -ph staggering
        EvbRegs.ACTRB.all = 0x0066; // 0x00966
/* ------------------- Dead band control --------------------------- */
        EvaRegs.DBTCONA.all = 0x08F0;          // Enable deadband,  150MHz/(16*4)
                                                 // control time with second digit
         EvbRegs.DBTCONB.all = 0x08F0;         // Enable deadband,  150MHz/(16*4)
                                                 // control time with second digit
/* ----------------- Enable PWM/compare operation-------------------
         Compare enable
         Reload condition, CNTR = 0
         Compare o/p enable
------------------------------------------------------------------- */
        EvaRegs.COMCONA.all = 0x8600;
```

```
    EvbRegs.COMCONB.all = 0x8600;
}
void spi_init()
{
    SpiaRegs.SPICCR.all =0x000F;            // Reset on, rising edge, 16-bit char bits
    SpiaRegs.SPICTL.all =0x000E;            // Enable master mode, delay phase,
     // enable talk, and SPI int disabled.
    SpiaRegs.SPIBRR =0x000A;
    SpiaRegs.SPICCR.all =0x009F;            // Relinquish SPI from Reset
    SpiaRegs.SPIPRI.bit.FREE = 1;       // Set so breakpoints don't disturb xmission
}
void dac_send(double x,double xmin, double xmax, int channel)
{
    double Ftest, offset,span;
    Uint16 data,AB;
     if(x<xmin)x=xmin;
     if(x>xmax)x=xmax;
    offset = - xmin;
    span = xmax-xmin;
    Ftest=(x + offset)/span*511.0;
    data = ((int)(Ftest))<<7;
     if (channel == 2) AB= 1024;
    else AB=0;
    SpiaRegs.SPIDAT= AB + 768 + (data>>8);
}
void InitGPIO(void)
{
    EALLOW;
/* ---------- Initialize all GP as inputs ---------------------------- */
    GpioMuxRegs.GPAMUX.all = 0x0000;            // GPIOA registers as I/O
    GpioMuxRegs.GPADIR.all = 0x0000;            // Set pins as inputs
```

```
        GpioMuxRegs.GPBMUX.all = 0x0000;                    // GPIOB registers as
I/O
        GpioMuxRegs.GPBDIR.all = 0x0000;                     // Set pins as inputs
        GpioMuxRegs.GPDMUX.all = 0x0000;                    // GPIOD registers as
I/O
        GpioMuxRegs.GPDDIR.all = 0x0000;                    // Set pins as inputs
        GpioMuxRegs.GPEMUX.all = 0x0000;                    // GPIOE registers as
I/O
        GpioMuxRegs.GPEDIR.all = 0x0000;                    // Set pins as inputs
        GpioMuxRegs.GPFMUX.all = 0x0000;                    // GPIOF registers as
I/O
        GpioMuxRegs.GPFDIR.all = 0x0000;                     // Set pins as inputs
        GpioMuxRegs.GPGMUX.all = 0x0000;                    // GPIOG registers as
I/O
        GpioMuxRegs.GPGDIR.all = 0x0000;                    // Set pins as inputs
/* --------------------- Setting SPI pins ------------------------------- */
        GpioMuxRegs.GPFMUX.bit.SPICLKA_GPIOF2 = 1;
// SPICLKA (CLK,P8-25) register as SPI function
        GpioMuxRegs.GPFMUX.bit.SPISTEA_GPIOF3 = 1;
 // SPISTEA (Enable, P8-26)register as SPI function
        GpioMuxRegs.GPFMUX.bit.SPISIMOA_GPIOF0 = 1;
 // SPISIMOA (Data, P8-23) register as SPI function
/* ------------------------Selecting PWM pins -------------------------- */
        GpioMuxRegs.GPAMUX.bit.PWM1_GPIOA0 = 1;
// Set GPIOA0 (P8-9) as PWM function
        GpioMuxRegs.GPAMUX.bit.PWM2_GPIOA1 = 1;
// Set GPIOA1 (P8-10) as PWM function
        GpioMuxRegs.GPAMUX.bit.PWM3_GPIOA2 = 1;
// Set GPIOA2 (P8-11) as PWM function
        GpioMuxRegs.GPAMUX.bit.PWM4_GPIOA3 = 1;
// Set GPIOA3 (P8-12) as PWM function
```

```
        GpioMuxRegs.GPAMUX.bit.PWM5_GPIOA4 = 1;
// Set GPIOA4 (P8-13) as PWM function
        GpioMuxRegs.GPAMUX.bit.PWM6_GPIOA5 = 1;
 // Set GPIOA5 (P8-14) as PWM function
        GpioMuxRegs.GPAMUX.bit.T1PWM_GPIOA6 = 1;
// T1PWM register (P8-15) as PWM function
        GpioMuxRegs.GPAMUX.bit.T2PWM_GPIOA7 = 1;
// T2PWM register (P8-16) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM7_GPIOB0 = 1;
 // Set GPIOA0 (P8-9) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM8_GPIOB1 = 1;
// Set GPIOA1 (P8-10) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM9_GPIOB2 = 1;
// Set GPIOA2 (P8-11) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM10_GPIOB3 = 1;
 // Set GPIOA3 (P8-12) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM11_GPIOB4 = 1;
// Set GPIOA4 (P8-13) as PWM function
        GpioMuxRegs.GPBMUX.bit.PWM12_GPIOB5 = 1;
// Set GPIOA5 (P8-14) as PWM function
/* ------------------ Selecting XINT pins  ----------------------------- */
GpioMuxRegs.GPEMUX.bit.XINT1_XBIO_GPIOE0 = 1; // P8-5 as XINT1
GpioMuxRegs.GPEMUX.bit.XINT2_ADCSOC_GPIOE1 = 1;    // P4-2 as XINT2
/* ---------------- Setting LEDs pins as DSP outputs -------------------- */
        GpioMuxRegs.GPBDIR.bit.GPIOB13 = 1;         // Set GPIOB13 (P7-5) as output
        GpioMuxRegs.GPBDIR.bit.GPIOB14 = 1;         // Set GPIOB14 (P7-6) as output
        GpioMuxRegs.GPFDIR.bit.GPIOF10 = 1;         // Set GPIOF10 (P4-5) as output
        //GpioMuxRegs.GPDDIR.bit.GPIOD1 = 1;         // Set GPIOD1 (P7-4) as output
/* ----------- Setting Debugging pins as DSP outputs -------------------- */
        //GpioMuxRegs.GPFDIR.bit.GPIOF4 = 1;          // Set GPIOF4 (P8-3) as output
        //GpioMuxRegs.GPFDIR.bit.GPIOF5 = 1;          // Set GPIOF5 (P8-4) as output
```

```
        EDIS;
}
//===========================================================
// No more.
//===========================================================
```

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VITA

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