

Power-scan chain : design for analog testability

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Power-Scan Chain: Design for Analog Testability

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Abstract

This paper reports a Design for Testability technique, which provides necessary diagnostic capability for signature-based testing of analog circuits. To facilitate this kind of testing, it is preferable to observe the current (or voltage) signatures of individual cores instead of observing the current (or voltage) signature of the whole analog SoC. Therefore, our DfT works like a power-scan chain aimed at turning on/off analog cores in an individual manner, providing an observability means at the core's power and output terminals, and at exciting the core under test. The proposed DfT can be used for engineering pre-characterization as well, and can easily be interfaced to standards like I²C and IEEE 1149.1 TAP controllers. In this paper we further provide experimental evidence of our approach as applied to an RF device.

1. Introduction

Modern Systems-on-Chip (SoC) integrate digital, analog and mixed-mode modules, e.g. mixed-signal, or RF analog and digital, etc., on the same chip. This level of integration is further complicated by the use of third-party cores obtained from virtual library descriptions of the final IC block. Furthermore, the variety and number of cores and their nature type, e.g. analog, complicate the testing phase of individual blocks, of combinations of blocks and ultimately of the whole system. The problem in the analog domain is that it is much more difficult to scan signals over long distances in a chip and across its boundary to the outside world, since rapid signal degradation is very likely to occur. The IEEE 1149.4 [1] is a standard mixed-signal test bus that can be used at the device, sub-assembly, and system levels. It aims at improving the controllability and observability of mixed-signal designs and at supporting mixed-signal built-in test structures in order to reduce test development time and costs, and to improve test quality.

There are various known approaches for designing for testability of analog circuits. The most common approach is to partition a system into sub-blocks to have access to internal nodes such that each isolated sub-block receives the

proper stimuli for testing [2]. Soma [3] presented a DfT that is oriented at testing sub-blocks of a filter such that each stage is tested by increasing the bandwidth of the other stages. This is done by adjusting the switching scheme in the case of switched-capacitor filters, or by bypassing the filter capacitors using additional MOS transistor switches. The problem with the latter approach is that MOS transistors are in the direct signal path of the filter degrading the performance. Bratt *et.al.* proposed a switched opamp (sw-opamp) structure to overcome this limitation [4]. This sw-opamp has basically two operational modes, test and normal, depending upon a digital control signal. The opamp is used at the interface between any two sub-blocks. Vazquez *et.al.* presented an enhanced approach similar to [4] that makes use of an opamp with duplicated input stages [5-6]. In this approach every opamp in the initial filter design is replaced by the DfT opamp. Other DfT schemes include ADCs with self-correction capability [7]. Vinnakota *et.al.* reported a DfT scheme suitable to detect parametric faults in switched-capacitor circuits based on a circuit that can compute *all* the capacitor ratios that determine the transfer function of the filter [8].

Unlike previous approaches that test the analog circuit for functionality, we advocate the use of analog structural testing [9-10]. Our approach consists of exciting the circuit under test with a DC or low-frequency stimulus to sample the response at specified times to detect the presence of a fault. The DC-transient waveform can be formed from piecewise-linear segments that excite the circuit's power supply, biasing, and/or inputs. In particular, we have worked on a test methodology that consists of ramping the power supply voltage. To facilitate this kind of testing, it is preferable to observe the current (or voltage) signatures of individual cores instead of observing the current (or voltage) signature of the whole analog SoC. Therefore, our DfT method works like a *power-scan chain* aimed at turning on/off analog cores in an individual manner, at providing observability means at the core's power and output terminals, and at exciting the core under test. Existent DfT techniques do not turn individual blocks on and off, but merely disconnect the observed block from the signal path; neither are they suitable for DC-transient testing such as V_{dd} ramping [9].

In the course of the paper we will present a brief overview of the Vdd ramp test methodology, propose a DfT technique to facilitate this kind of testing, give details on the power-scan chain interface and, at the end, demonstrate the effectiveness of the proposed technique.

2. Vdd Ramp Test Methodology

The supply-current monitoring technique has, so far, found no practical widespread application in analog circuits. This is mainly because analog faulty behaviours are not so pronounced as those in the digital case; special test vectors often have to be applied to increase fault coverage, in a special test mode. To apply the power-supply-current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques. This is because of two factors:

- The method requires more than a simple observation of abnormal currents;
- Unlike digital circuits, bias currents always exist between the power supplies in analog circuits and in most cases abnormal currents cannot be defined.

For analogue circuits and systems, fault diagnosis techniques are more complex when compared to their counterparts in digital circuits for various reasons:

- The requirement of measurements of current and voltage signals at the internal nodes;
- Diagnosis errors caused by soft-faults, which are due to the tolerance of the components.

An advanced methodology for testing analog circuits that overcomes the majority of the obstacles encountered with the supply-current-monitoring technique was proposed in the mid 90s [11]. To obtain signatures rich in information for efficient testing, the transistors in the circuit are forced to operate in all possible regions of operation by applying a ramp signal to the supply terminals instead of the conventional constant DC signal or ground voltage.

The power-supply-ramping technique can potentially detect and diagnose catastrophic [9] as well as parametric faults [10]. The application of a ramp signal to the power supply voltage nodes instead of the conventional step (or DC voltage) can force the majority of the transistors in the circuit to operate in all the regions of operation, and hence, provide bias currents rich in information. The method measures current signatures, not single values. Many faults have unique or near-unique signatures, easing the diagnosis process. Indeed it is independent of the linearity or nonlinearity of the systems, circuit or component.

3. Power-Scan chain DfT

The main feature of the proposed DfT is to selectively turn individual cores on and off such that the core(s) electrical performance can be tested in isolation or together with other cores of an analog SoC. By electrical performance we mean DC, AC, and/or transient characteristics. There are several ways of turning on/off analog cores. Our choice is by placing switches in the biasing network of the analog core, as this does not interfere with signals in the signal path. Another option is to place switches in the power path.

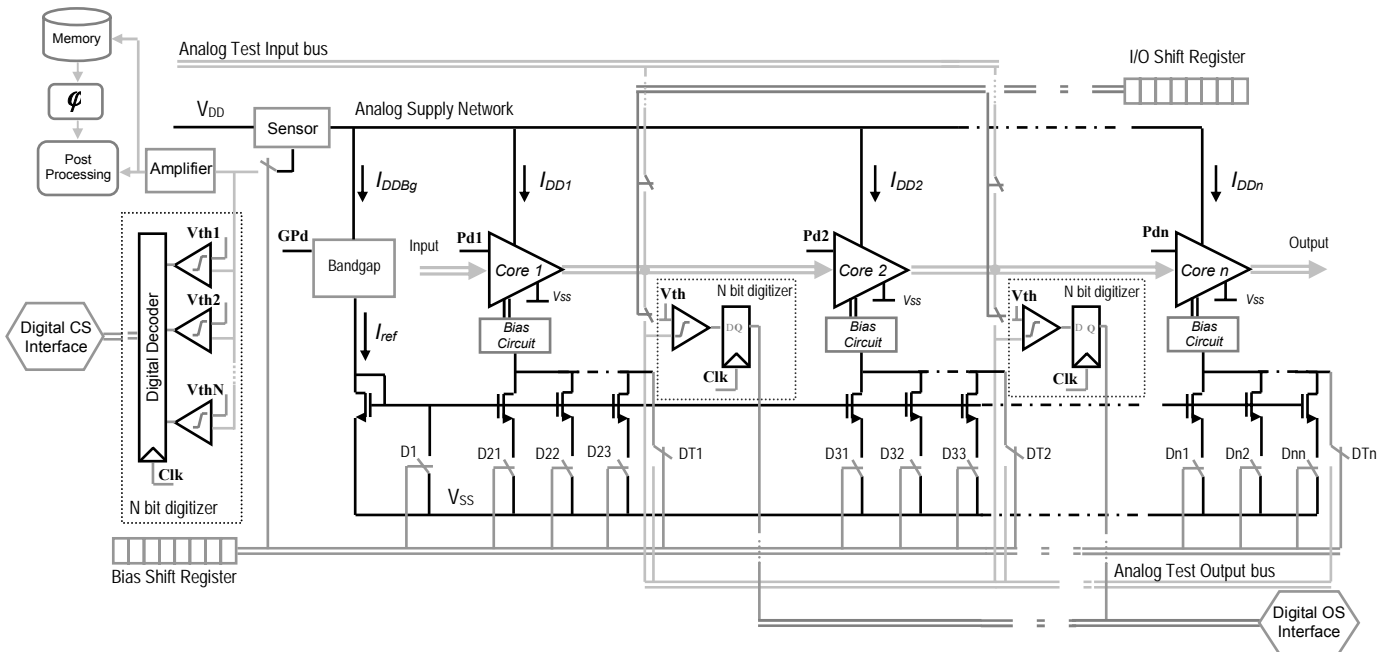


Figure 1: Power-Scan Chain Analog DfT

However, these switches introduce a voltage drop that can have an impact on the core's performance. Additionally, the latter switches may be bulky.

The design of the proposed DfT network shown in Figure 1 has been designed to operate in all possible regions of operation by using a ramp signal at the supply instead of the conventional constant DC signal or ground voltage. The DfT consists of an Analog Test Input Bus to provide input stimuli to the core under test, an Analog Test Output Bus to read out stimuli response, a Digital CS and OS Interface to read out digitized current signatures (CS) and digitized output response stimuli (OS), an Analog Supply Network to read out currents in the power line and two Shift-register controllers to turn on/off individual cores and to select/deselect input/out test busses, respectively.

3.1. Analog Supply Network and Biasing Control

Let us explain first the Analog Supply Network along with the biasing control network. Observe that only one sensor is inserted in the Vdd path. This sensor is basically an amp meter to measure the current flowing through the power supply terminal. Conversely, under the condition that the ratio of the supply current to the background current is not sufficient to differentiate between a fault-free and a faulty circuit, the main limitation would be off-chip sensing. However, with development of built-in current monitor on-chip, these constraints have been largely overcome [12, 13].

To facilitate supply current readings of the individual cores (I_{DDBg} , I_{DD1} , I_{DD2} , ... I_{DDn}), the biasing network of the cores under consideration are turned on/off in an individual manner. The supply currents of the individual cores can be found from the difference between the supply currents found for the different codes, clocked in from left to right out of the bias shift register. The supply current readings are performed at the core's nominal operating conditions. To increase readability and avoid the rounding effects of the low-level power supply current, the quiescent power supply current is sensed across a sensing element and further amplified in a voltage amplifier with automatic-gain-control features to deal with wide dynamic ranges.

After amplification, all individual supply current readings are stored in a memory unit. The ϕ operator allows us to do any type of mathematical operation, such as addition, multiplication, convolutions, etc., for any combination of individual current signatures. Post-processing of the current signature can be done by any post-processing means, such as for instance integration or FFT. In our approach it is possible to observe the analog waveform of the power supply current signature as well as its digitized version.

Figure 1 shows an N-bit digitizer, whose V_{TH} references originate from the Analog Test Input bus. The Digital-Decoder clock signal is related to the system. The biasing network consists of a bandgap circuit providing an I_{ref} current, and of a current mirror with multiple legs, each feeding an analog core. The (bias) shift register controller is a digital circuit with Vdd (logical 1) and Gnd (logical 0) voltage levels. For the NMOS-based biasing network of this example, a bit value 1 in any position of the shift register turns on any of the switches $D_1, D_{21} \dots D_{2N} \dots D_{NN}$. Note that when node D_j is switched on or when the bandgap is powered down by the global power-down signal (GP_d), I_{ref} will no longer flow and all bias currents will become zero irrespective of the $D_{21} \dots D_{2N} \dots D_{NN}$ signals. Switches $D_{21} \dots D_{2N} \dots D_{NN}$ are used to turn off the core-under-test or to adjust the corresponding current biasing. One can regard switch D_{k1} , where $k=2 \dots N$, as the master switch that enables the nominal biasing current to the core under normal operation. The remaining switches are used in test mode to allow the biasing current to be modified for testing purposes. The IC may consume a certain amount of current even if all blocks are off. This is due to the leakage current of the digital circuitry used in mixed-signal circuits. It is important to note that by placing the switches at the ground nodes of the core's biasing circuit and not at the ground nodes of the analog core itself, an impact on the core's bias point due to voltage drop caused by switch on-resistance is limited.

To ensure that a core is totally off, e.g. that it does not have floating nodes, a local power-down signal, P_d , is made available. Keep in mind that the global power-down, GP_d , signal is meant to turn off the complete system, while the local power-down switches off individual cores only. The local power-down signal is active, when switches $D_{21} \dots D_{2N}$ connected to the biasing network of the core 1, $D_{31} \dots D_{3N}$ for core 2, $D_{N1} \dots D_{NN}$ for core N, are disconnected. The implementation for these settings is a logical "nor" port. Switches $D_{T1} \dots D_{TN}$ are used to test the biasing network itself. They connect the bias nodes to the Analog Output Test bus. The core's biasing network is tested by turning on one core at a time and then by reading out the corresponding biasing voltage levels. Sensing of the bias network can be easily adjusted to detect the biasing current as well. As a final test provision is made to test the bandgap power-supply current.

In the Analog Output bus we have illustrated one-bit digitizers, however multi-bit digitizers can also be implemented. The V_{TH} reference comes from the Analog Test Input bus. The FF clock signal is related to the system clock. The Digital CS Interface reads out digitized current signatures. Post-processing of the digitized current signatures can be done by any post-processing means.

3.2. Analog Test Input and Output Bus

The scheme provides an Analog Test Input Bus to control (excite) the cores that are enabled. When using CMOS switches in the signal path of sensitive analog circuits, some possible problems may occur, such as cross-talk and increased noise, distortion and capacitive loading. In our approach we have two switches instead of, conventionally used, four. Observe that there are no switches in the signal path from core to core, and that the Analog test bus is actually shunted with the signal path. This is possible when assuming that the core prior to the core under test is turned off through the I/O register-controlled switch and the local power-down signal.

As an advantage, placing the sensors in individual power supply lines will enable parallel current-sensing operation, which as a consequence, results in significantly reduced test times. A disadvantage is the increased complexity and therefore the increased cost. Compared to the first proposal, the DfT now incorporates an Analog Power Output Bus to read out currents in the power line. The biasing network, Analog Test Input Bus, Analog Test Output Bus, Digital CS and OS Interface and two Shift-register controllers are similar to the ones shown in Figure 1. Note that bandgap sensor alterations can be made, so that the bandgap voltage can be measured and read out on the analog or digital power output bus.

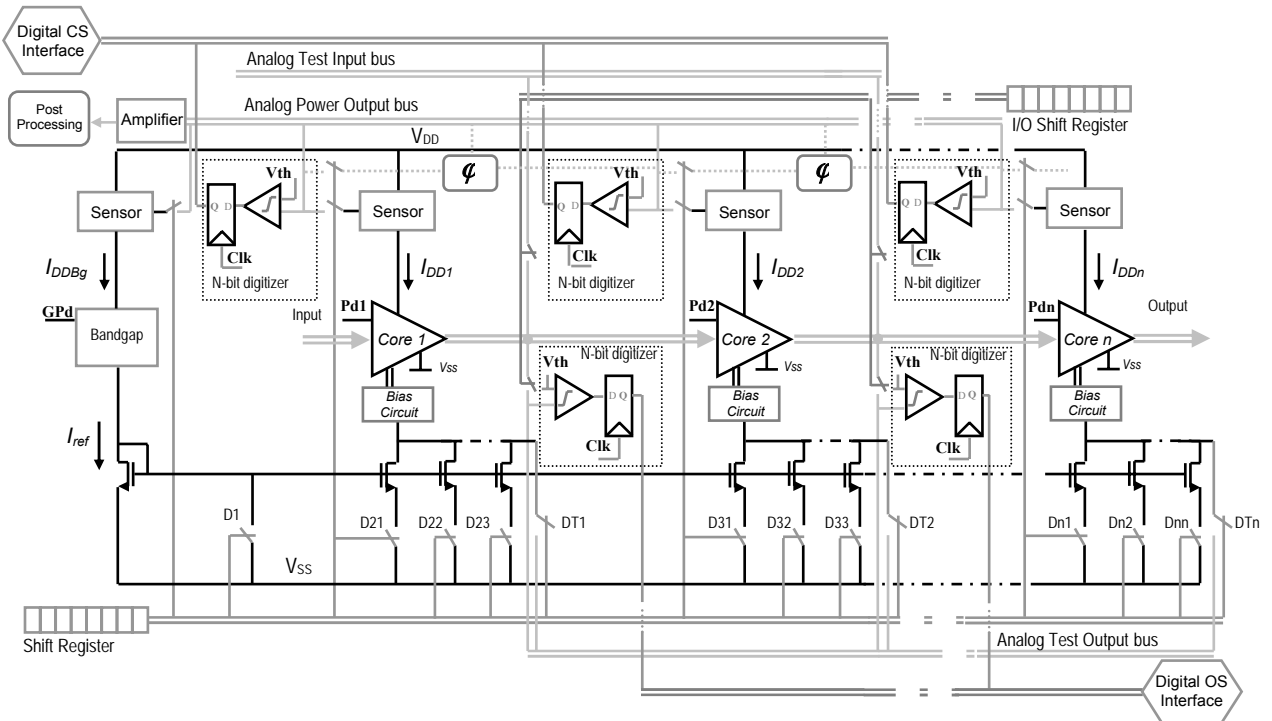


Figure 2: DfT with integrated current sensors

The Analog Test Output Bus provides observability of the core-under-test; associated with this bus is the Digital Output Interface, which basically digitizes the analog signal. The Analog Test Input bus can offer the input signal to the system, and the system output signal can be digitized and offered to the Digital Output Interface as well, to allow voltage read outs in Power-Scan chain mode in the whole system.

3.3. DfT with Integrated Current Sensors

To offer an alternative solution, the current sensors can also be placed between the VDD pad and the core's VDD terminal, as illustrated in Figure 2.

The supply currents of the individual cores can be found by turning on the biasing network of the cores under consideration. All supply current readings are performed at the core's nominal operating conditions. The outputs of the sensors are chained into an amplifier, with automatic-gain-control features to deal with wide dynamic ranges. The amplifier and post-processing units are part of the Automatic Test Equipment (ATE). The measured current(s) of the core(s)-under-test are used for testing purposes. The ϕ operator allows us to do operations on the current signatures of any two consecutively enabled cores. The operations can be any type of mathematical function such as addition, multiplication, convolutions, etc. Post-processing of the current signatures can be done by any post-processing means, such as for instance integration or FFT.

4. Power-Scan Chain Interface

The serial shift register in both proposed DfT architectures provides the control of the various analog switches for bias-current control and connections to the analog test bus. In our implementation this register is a user register controlled by an IEEE Std 1149.1 TAP controller [14], see Figure 3. Using an 1149.1 TAP allows access to the serial register, while the device is in functional mode. Other serial access interfaces, such as I²C or a 3-wire bus can also be used to control the serial shift register, but do not allow accessing the register in functional mode.

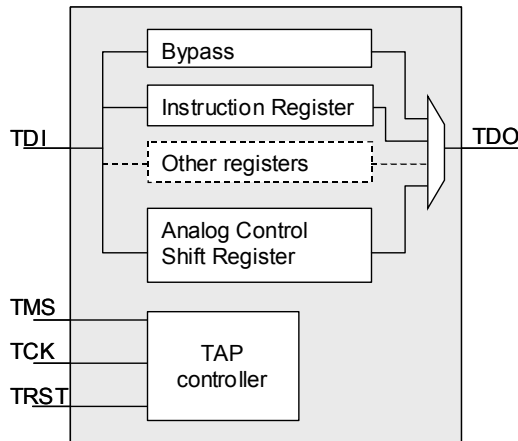


Figure 3: Analog control shift register under 1149.1 TAP architecture

To provide the analog test bus interface we implemented the IEEE 1149.4 analog test bus extension to 1149.1. The 1149.4 internal signals AB1 and AB2 shown in Figure 4 correspond to the analog test input and output bus, respectively, used in Figure 1 to operate in all possible regions of operation by using a ramp signal at the supply instead of the conventional constant DC signal or ground voltage. The fact that one can gain access to the shift registers while the device is in functional mode opens unique opportunities for on-chip silicon debugging.

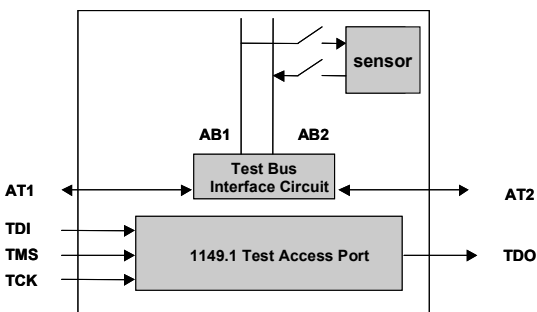


Figure 4: 1149.4 used to provide the analog test bus

We will cite now several examples. For instance, it is possible to debug certain circuit specifications by properly tuning the biasing network of a core in operating mode. Say, the gain of an amplifier, or the bandwidth of an active filter could be debugged by changing their biasing conditions. Another example is to isolate a core and to debug its specs with external input stimuli through the analog test input bus and by adjusting its biasing network. For instance, one can debug the bandwidth and insertion loss of a filter to known input signals, or debug the LSB sections of a data converter. Yet another example is to bypass a core in normal operating mode and to provide its neighboring cores with known input signals, or to analyze a core's output signal through the analog test output bus.

The previous examples are meant to show the capabilities of the proposed DfT for not only test, but also for on-chip silicon debugging.

5. DfT Demonstrator

5.1. Design of GFSK receiver

Our concept has been verified on an IC designed in 0.18- μ m CMOS for applications in the 2.4-GHz ISM band with GFSK-modulated input signals. Specifications have been derived from the Bluetooth standard [15]. A simplified block diagram of the receiver is shown in Figure 5.

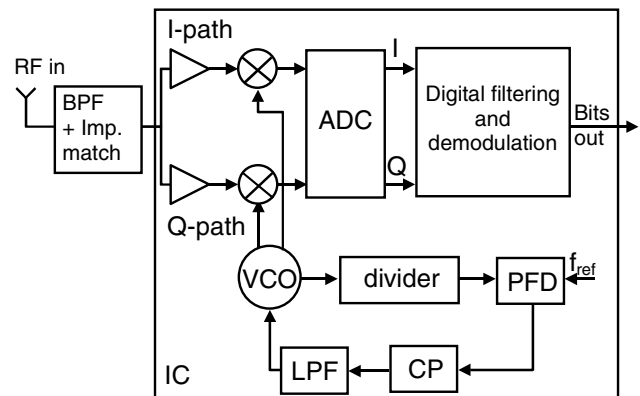


Figure 5: 2.4GHz GFSK receiver

An external band pass filter (BPF) selects the 2.4-GHz band and performs impedance matching. Two LNA's are used in parallel to provide sufficient isolation between the I and Q channels after the mixers. The LNA's have been implemented as V-I converters. The RF output current is downconverted to a low IF of 500 kHz by passive mixers, driven directly by a quadrature VCO in a PLL.

A high-resolution complex ADC converts the quadrature IF currents into noise-shaped I and Q bit streams. The digital block performs channel and decimation filtering as well as demodulation. The receive chain has been realized in a 6-metal-layer 0.18 μ m standard CMOS process on a 10- Ω cm substrate. The die photograph in Figure 6 shows a core area of 3.5 mm².

The IC has been packaged in a 48-pin LQFP plastic package and mounted on an FR-4 board. Apart from supply decoupling capacitances the only external components needed are an antenna filter/impedance matching network and a 64-MHz crystal. The nominal supply voltage of the analog part is 1.8 V, whereas the digital supply voltage is 1.4 V. The total power consumption is 31.7 mW in continuous mode.

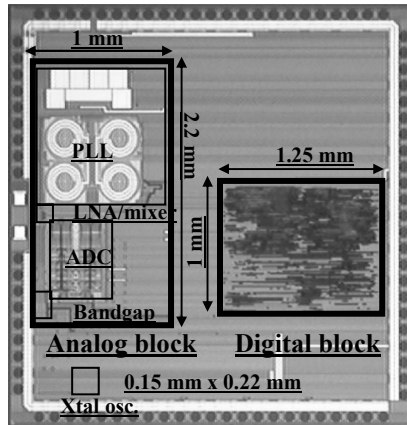


Figure 6: Microphotograph of GFSK receiver

5.2. Functional Testing [15]

The measured power consumptions of the various blocks in the receiver chain are listed in Table I.

TABLE I MEASURED POWER CONSUMPTION OF RECEIVER BLOCKS	
Block Power consumption	
LNA	0.6 mA \times 1.8 V=1.1 mW
PLL	7.6 mA \times 1.8 V=13.7 mW
ADC	2.3 mA \times 1.8 V=4.1 mW
Bandgap	0.1 mA \times 1.8 V=0.2 mW
Crystal oscillator	1.2 mA \times 1.8 V=2.2 mW
Digital filter + demodulator	7.4 mA \times 1.4 V=10.4 mW
Total (analog + digital)	31.17 mW

The SNR at the demodulator input versus the achieved BER based on 10k samples and a modulation index of 0.35 illustrated in Figure 7 reflects the behaviour of the digital demodulator.

The measurements show similar behaviour for Bluetooth channels 0, 48 and 78. The extrapolated input SNR for which BER=0.1% is 17 dB. The linearity of the receiver chain was determined by offering two tones separated 100 kHz apart in the band of interest. The result is shown in Figure 8, revealing an IIP3 value of -11 dBm and a 1-dB compression point of roughly -18 dBm.

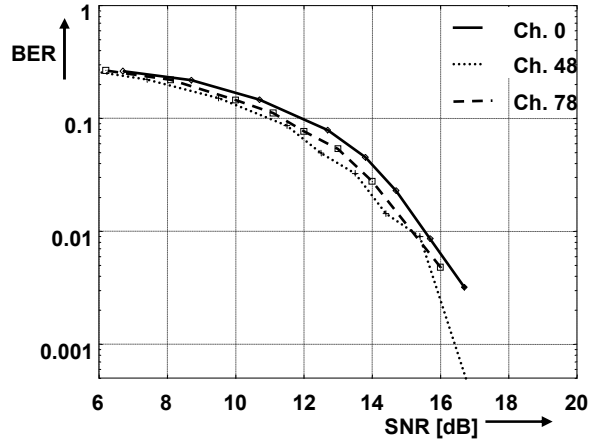


Figure 7: Measured BER curves vs. SNR at the demodulator input for Bluetooth channels 0, 48 and 78.

The interference behaviour was measured according to the Bluetooth specification. For the various interferers at various C/I ratios the BER values were measured to be smaller than 0.1%. It can be concluded that measured specifications comply with the Bluetooth standard.

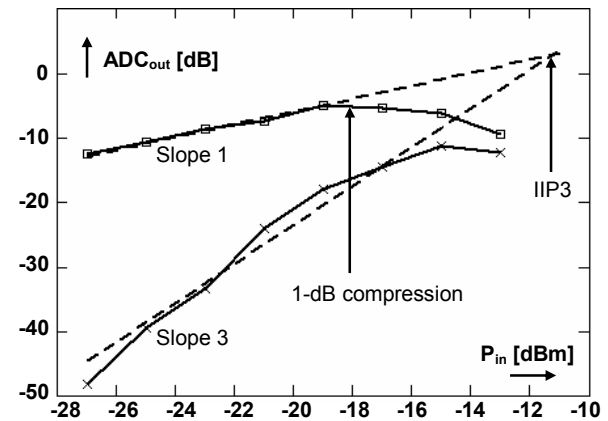


Figure 8: Measured linearity of the receiver chain (channel 0).

5.3. Structural Testing

In addition to the functional tests presented in the previous section, the proposed DfT provides the means for structural testing as well. As an illustration of the concept presented in this paper, current signatures have been measured for the crystal oscillator (XO), LNA, ADC, VCO and divider. The result is shown in Figure 9. Note that the current values at 1.8-V supply voltage in Figure 9 indeed add up to the total value of 11.8 mA shown in Table I, where the VCO and divider current add up yielding the PLL current. Starting from zero current with all blocks switched off, the bandgap and crystal oscillator currents can simply be obtained from individually switching these blocks on. At least the bandgap block should remain switched on to be able to measure sensible current signatures for all other blocks, since without I_{ref} being present, switching blocks on through the bias network is not possible, see Figure 1. Moreover, each block should be tested in its normal operating conditions. For the divider, this implies that the VCO should be switched on as well, since the current consumption of the divider increases when the VCO is on due to the current consumption of the first stages. Similarly, the ADC current signature has been measured with the RF front-end switched on for proper input settings and with the crystal oscillator switched on to ensure a clock input signal to the ADC.

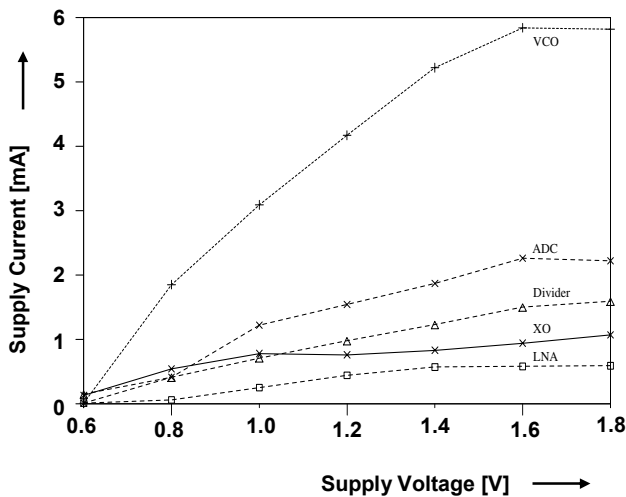


Figure 9: Current signatures of crystal oscillator (XO), LNA, ADC, VCO and divider, obtained by switching blocks on and off and measuring the supply current for various power supply voltages.

The current signatures shown in Figure 9 correspond to correct functional behaviour, since they have been measured on the same IC for which measurement results have been described in section 5.2.

For all current signatures it has been assumed that the circuit can sustain process variations, so the tolerance band can be assumed as well. Any tested signature that falls within $\pm 3\sigma$ spread of the reference value has been assumed to be correct [9]. No current-signature measurements were available for non-functional tests. However, the LNA signature can be compared to current signatures presented earlier in [9], since they refer to the same LNA circuit from a different batch. Note that the current values are twice as high, since two identical LNA's are used on the test IC described in this paper. When divided by two, the LNA current signature of Figure 9 indeed lies within the defined region in [9] implying correct behaviour. As a final remark, the LNA signature in Figure 9 has been measured with the bandgap being switched on. This implies that in the case of Figure 9, the bias current fed to the LNA eventually decreases, because the bandgap no longer functions properly at low supply voltages. This was not the case in [9], where a constant bias current was fed to the LNA, irrespective of the supply voltage value.

The chip performance can be tuned by adjusting the biasing current (switching on/off additional biasing current source to the individual core through the serial interface) without having several metal options.

Conclusions

Our structural test efforts are closely related to signature-based testing and therefore require the appropriate DfT infrastructure to be successful. The proposed DfT intends to facilitate this kind of testing, by providing the means to observe the current (or voltage) signatures of individual cores instead of observing the current (or voltage) signature of the whole analog SoC. Therefore, our DfT method works like a *power-scan chain* aimed at turning on/off analog cores in an individual manner. Existent DfT techniques do not turn individual blocks on and off. Economic considerations are only one of the advantages of providing observability means at the core's power and output terminals. Other advantages include increased fault coverage and improved process control, diagnostic capabilities, reduced IC performance characterization time-cycle, simplified test-program development and easier system-level diagnostics.

The main features of our DfT are: *i)* Power-Scan chain mode to turn individual analog cores on and off, *ii)* current and voltage read outs in Power-Scan chain mode, *iii)* use of switches in biasing path or in supply connections to turn analog cores on and off, *iv)* tuning the chip performance by adjusting the biasing current through the serial interface.

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