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Practical Controller Design of Three-Phase Dual Active Bridge Converter for Low Voltage DC Distribution System

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Abstract: In a low voltage DC (LVDC) distribution system, isolated bi-directional DC-DC converters are key devices to control power flows. A three-phase dual-active-bridge (3P-DAB) converter is one of the suitable candidates due to inherent soft-switching capability, low conduction loss, and high-power density. However, the 3P-DAB converter requires a well-designed controller due to the influence of the equivalent series resistance (ESR) of an output filter capacitor, degrading the performance of the 3P-DAB converter in terms of high-frequency noise. Unfortunately, there is little research that considers the practical design methodology of the 3P-DAB converter's controller because of its complexity. In this paper, the influence of the ESR on the 3P-DAB converter is presented. Additionally, the generalized average small-signal model (SSM) of the 3P-DAB converter including the ESR of the capacitive output filter is presented. Based on this model, an extended small-signal model and appropriate controller design guide, and performance comparison are presented based on the frequency domain analysis. Finally, experimental results verify the validity of the proposed controller using a 25 kW prototype 3P-DAB converter.

Keywords: three-phase dual-active-bridge converter; practical controller design; ESR zero; small-signal mode; output impedance

1. Introduction

Interests in applications for DC grids have recently increased [1–3]. To configure the DC microgrid, which can replace the conventional alternating current (AC) distribution system, the low voltage DC (LVDC) distribution system has been steadily studied and examined [4–6]. As shown in Figure 1, to develop the LVDC system, the IBDC converter is essential, linking the LVDC grid to DC end users. The IBDC converter is required to convert the high voltage level in the distribution system to the low voltage level required by the applications, which is commonly designated as 380 V [7]. Therefore, the suitable candidates for the LVDC converter should treat several hundred DC voltage levels in a smooth bi-directional control manner.

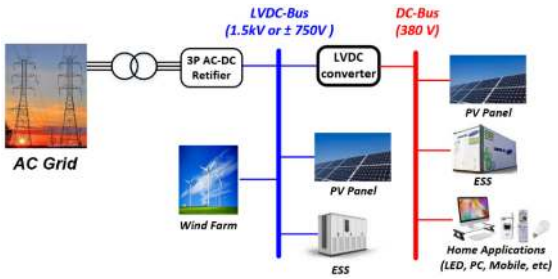

Figure 1. Circuit schematics of a three-phase dual active bridge converter.

One of the appropriate candidates of the IBDC converter for the LVDC system is a three-phase dual-active-bridge (3P-DAB) converter, as shown in Figure 2. The 3P-DAB converter is an extended version of the single-phase DAB (SP-DAB) converter. The 3P-DAB converter is generally considered in bi-directional applications since it has the advantages of the SP-DAB converter such as soft switching capability without additional resonant components and smooth bidirectional power transition under seamless control [8]. In addition, the 3P-DAB converter shows low conduction loss and high-power density because of its interleaved structure [9–12]. The interleaved structure makes the effective switching frequency increase, which can decrease the size of passive components and reduce the peak and root mean square (RMS) current. Therefore, the 3P-DAB converter is suitable for bi-directional high-power applications.

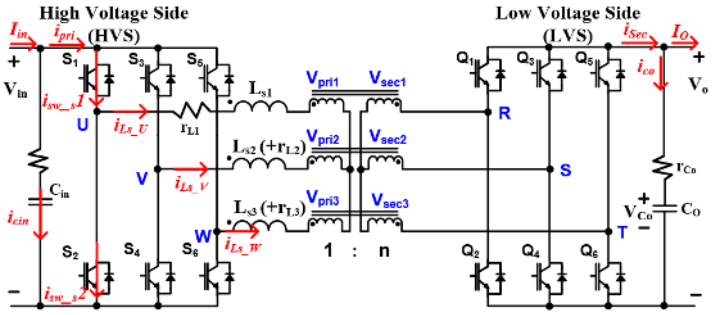

Figure 2. Circuit schematics of a three-phase dual active bridge converter.

One of the performance criteria of the power converter is a stable operation that explains the converter's ability to withstand the external and internal disturbances or transient behaviors in the operational conditions. To design a proper controller and to analyze the reliability and stability of the power converter, a sophisticated design methodology of the control is required [12–20]. The control-to-output transfer function based on the small-signal model (SSM) of the power converter is generally used to design the suitable controller from which the dynamic response of the output voltage is evaluated by perturbations in the control-input [21,22]. Therefore, to improve the stability and the dynamic performance of the power converter, the SSM is one of the significant tools. Since active components, such as power switches and diodes, have nonlinear characteristics, the SSM should be approximated to a linear time invariant (LTI) system, representing the dynamics of the power converter. In general, the dynamics depend on the operating point determined by steady-state variables such as inductor current and capacitor voltage.

Although many research studies have examined the controller design of single-phase DAB (SP-DAB) converters [13–15], there are only a few research studies that have investigated the SSM of the 3P-DAB converter and its theoretical controller design [9,18–20]. This is because they require complex and difficult dedicated design procedures. In terms of the dynamic behaviors of the 3P-DAB converter, the design of the suitable controller is important. In a previous study, the simplified SSM of the 3P-DAB converter has been introduced [18]. Its steady-state operation has been analyzed to describe the dynamic behavior of the 3P-DAB converter, which is based on a generalized average

model [19]. A study of the dynamic control strategy for instantaneous overcurrent control has also been proposed to avoid forced oscillations due to its switching transients [20]. These studies have been based on the simplified SSM; however, the equivalent series resistance (ESR) of capacitors has never been reported to analyze the dynamic behaviors in the SSM because of its high complexity. It is well known that the zero of the transfer-function influences the entire loop response [23,24]. The zero caused by the ESR of the output filter capacitor can degrade the dynamic performance of the 3P-DAB converter and cause the insufficient phase margin since it can decrease the amount of the attenuation of high-frequency noises. In addition, the ESR causes significant ripples to the output voltage, causing the instability of the control-loop [14–16,20–23]. With a capacitor with ESR, the current flowing in the resistance will give an immediate step-change in voltage, which makes a voltage ramp and causes power switches to break. Hence, the ESR zero of the output capacitor should be identified and its influence should be minimized by using a compensator.

In this paper, extended small-signal transfer functions considering the ESR effect of the 3P-DAB converter are introduced to aid the design evaluation of the system's response to disturbances. The design guides of the 3P-DAB converter controller are presented by using the generalized average SSM in the steady-state operation. The organization of this paper is as follows: Section 2 describes the basic operation of the 3P-DAB converter briefly. Section 3 presents the detailed methodology for the effective controller based on the average state-space model. To verify the effectiveness of the proposed controller design, simulation results and output impedance analysis are presented in Section 3. In Section 4, experimental results are presented to verify the performance improvement of the proposed controller design. Finally, in Section 5, the contribution of this research will be summarized.

2. Operation Principles of 3P-DAB Converter

As shown in Figure 2, the 3P-DAB converter consists of two three-phase bridges in both the high voltage side (HVS) and low voltage side (LVS), which are connected to the high-frequency transformer and the coupling inductance. The coupling inductance is defined as the sum of external series inductance and leakage inductance in the transformer. Figure 3 shows the operating waveforms of the 3P-DAB converter in the steady-state when a conventional SPS modulation is applied. The SPS modulation, which adopts a fixed duty cycle of 50%, is generally used to obtain a simple control strategy in the 3P-DAB converter. In this paper, the phase shift difference between two bridges is defined as ϕ_{PS} (=ϕ/π) where ϕ is normalized by π. ϕ_{PS} controls the transmitted power across the coupling inductance of L_S, generating a six-step waveform in each phase voltage of the HVS and LVS [9–12]. A Y-Y connection is adopted by the three-phase transformers to reduce current unbalance in each phase [25].

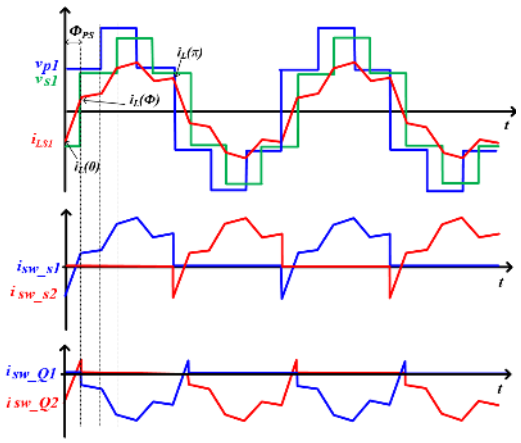

Figure 3. Theoretical waveforms of the three-phase dual-active-bridge (3P-DAB) converter under $0 < \phi_{PS} < 1/3$.

In the 3P-DAB converter, the coupling inductance is a key component since it is utilized to store and to deliver the electric energy. In addition, the coupling inductance determines the shape of the phase current, which is a key factor of power conversion efficiency such as soft switching conditions and RMS phase current. Each phase current passing through the coupling inductance can be expressed as follows:

$$L_{S,x}\frac{di_{Ls,x}(t)}{dt} = v_p(t) - nv_s(t) \tag{1}$$

where v_p is the transformer voltage in HVS, v_s is the transformer voltage in LVS, and n is the turn ratio. Since $i_L(0) = -i_L(\pi)$ is satisfied with the flux balancing law in the steady-state, the initial current of $i_L(0)$ can be derived as follows:

$$i_{L,x}(0) = \frac{V_i}{18f_S L_{S,x}}\left[m\left(\frac{2}{3} - \phi_{ps}\right) - \frac{2}{3}\right] \tag{2}$$

where m is the voltage conversion ratio ($=nV_O/V_{in}$) and f_s is the switching frequency.

Using the initial current, the current passing through the coupling inductor during each switching period can be analyzed. The average output power, P_O, under the SPS control method can be derived by using the phase voltage and the phase current as follows:

$$P_O = \frac{3}{\pi}\int_0^{\pi} V_{Ls,x}(\theta)i_{Ls,x}(\theta)d\phi = \begin{cases} \frac{V_i^2}{2f_S L_{S,x}} m\left(\frac{2}{3} - \frac{\phi_{PS}}{2}\right)\phi_{PS}, 0 \le \phi_{PS} \le \frac{1}{3} & (3a) \\ \frac{V_i^2}{2f_S L_{S,x}} m\left[\phi_{PS}\left(1 - \frac{\phi_{PS}}{2}\right) - \frac{1}{18}\right], \frac{1}{3} \le \phi_{PS} \le \frac{1}{2} & (3b) \end{cases} \tag{3}$$

As shown in (3a) and (3b), the output power of the 3P-DAB converter differs depending on the range of ϕ_{PS} since the waveform of the phase current has changed. Theoretically, the maximum output power can be achieved when ϕ_{PS} is ±1/2 in the 3P-DAB converter. However, as shown in Figure 4, when ϕ_{PS} approaches ±1/2, the nonlinearity of the output power becomes more significant than the lower ϕ_{PS} since the trajectory of the output power according to ϕ_{PS} is parabolic. Therefore, in this paper, ϕ_{PS} is limited to ±1/3.

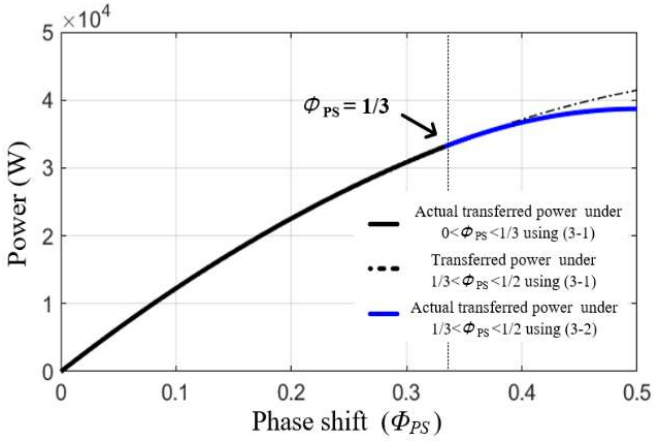

Figure 4. Transmitted power according to normalized phase shift degree.

3. Design Procedure of Improved Controller

To reduce the error between the theoretical model behavior and the practical operation of the real converter, a full-order model is generally used in the converter analysis. The higher-order coefficient of the full-order model can make the converter model more accurate; however, its complexity and difficulty are increased with a higher computation burden. There is a trade-off relation between the complexity of the model computation and the accuracy of the converter model. In the case of the 3P-DAB converter, a simplified SSM, which does not include the dynamics affected by the phase inductor, is often adopted in the frequency-domain analysis since the model accuracy is not significantly degraded with lower complexity and difficulty compared to the conventional full-order SSM [14,15].

In [18], the simplified SSM of the 3P-DAB converter has been presented for the first time. Based on the generalized average model, the performance of the 3P-DAB converter has been analyzed under the steady-state operation [19,20]. However, in the previous research, the ESR zero of the output filter capacitor has not been considered in the control-to-output transfer function and the considerations of the controller according to the size of the output capacitor are not shown. In this paper, an extension of the simplified SSM considering the ESR zero is derived. In addition, an enhanced controller design methodology is presented including the ESR zero effect and the output filter capacitance. Since the 3P-DAB converter has a symmetrical feature, it is assumed that the phase voltage and current are balanced, and the power flow is considered as the forward direction in the proposed analysis.

3.1. Extended Small-Signal Model

The conventional state-space average (SSA) technique widely used for modeling power converters ignores the current ripple [12]; however, it cannot be employed to the controller design in terms of the 3P-DAB converter. This is because the phase current is a quasi AC waveform, which makes the average value of the phase current zero as shown in Figure 3. In this paper, instead of the conventional SSA, the generalized average model based on the Fourier series of state variables is employed to derive the SSM of the 3P-DAB converter. To obtain the control-to-output transfer function, the average state-space model is shown in Appendix A of (A1) and (A2). To obtain the simplified SSM, the voltage across the output filter capacitor is used as a state variable as shown in (A3). From (A2) to (A6), the state variable considering the ESR of the output capacitor filter can be expressed as follows:

$$\frac{dV_{Cof}}{dt} = \frac{i_{s,DC}}{C_{of}\left(1+\frac{r_{Cof}}{R_L}\right)} - \frac{v_{Cof}}{R_L C_{of}\left(1+\frac{r_{Cof}}{R_L}\right)} \tag{4}$$

where C_{of} is the output filter capacitance, v_{Cof} is the voltage across the output filter capacitor, r_{Cof} is the ESR of the output filter capacitor, R_L (= *Vo*/*Io*) is the load resistor, and $i_{S,DC}$ is the current of the LVS.

From (A7) to (A22), the average state-space model of the 3P-DAB converter with the design specification in Table 1 can be obtained. Here, several assumptions are carried out. The output voltage is the same as the voltage across the output capacitor and the magnetizing inductance of the transformer can be ignored since the voltage across the ESR and the current passing through magnetizing inductance are too small to be considered, respectively. Finally, the control-to-output small-signal transfer function, including the ESR zero, is expressed as (5).

$$\frac{\hat{V}_o(s)}{\hat{\phi}(s)} = k_{v\phi}\frac{\left(\frac{s}{\omega_{v\phi,zero}}+1\right)}{\left(\frac{s}{\omega_{v\phi,pole}}+1\right)}, k_{v\phi} = \frac{R_L v_i\left(\frac{2}{3}-\phi_{PS}\right)}{2f_s L_{S,x}}, \omega_{v\phi,pole} = \frac{1}{\left(R_L + r_{Cof}\right)C_{of}}, \omega_{v\phi,zero} = \frac{1}{r_{Cof}C_{of}} \tag{5}$$

where S is the Laplace operator, $k_{v\phi}$ is the DC gain of the transfer function, $\omega_{v\phi,\,pole}$ and $\omega_{v\phi,zero}$ are the angular frequency of the single-pole and the single-zero, respectively. The comparison of the control-to-output transfer function between the theoretical model from (5) and the empirical simulation model obtained by PSIM simulation software is shown in Figure 5. In Figure 5, the blue line represents the theoretical Bode plot, and the red line represents the empirical Bode plot under the same conditions. The pole and zero of the small-signal transfer function are 58.25 Hz and 3.66 kHz, respectively. As shown in Table 2, to reduce the output voltage ripple, the output filter capacitance of 1.4 mF is adopted where the ESR is 138 mΩ. The location of the ESR zero can be estimated in the high-frequency region since the phase angle is boosted towards zero degrees as shown in Figure 5.

Table 1. Converter specification for experiments.

Symbol	Quantity	Value
V_{in}	Input Voltage	550 V
V_{out}	Output Voltage	278 V
m	Voltage gain	0.986
f_{SW}	Switching frequency	8 kHz
$P_{o,max}$	Rated Power	25 kW
$L_{s,e}$	Effective Coupling inductance	43.7 µH (CH740060)
N_L	Turns	13
-	Transformer Material	Nano-crystalline
n_P:n_S	Turn ratio	39:20
$R_{S,HVS\backslash}$	Parasitic resistor on LVS	850 mΩ
$R_{S,LVS}$	Parasitic resistor on HVS	380 mΩ
Cof	Output filter capacitance	1.4 mF
ESR	Equivalent series resistance	138 mΩ
t_d	Dead time	1.25 µSec
-	Controller	TMS320F28335

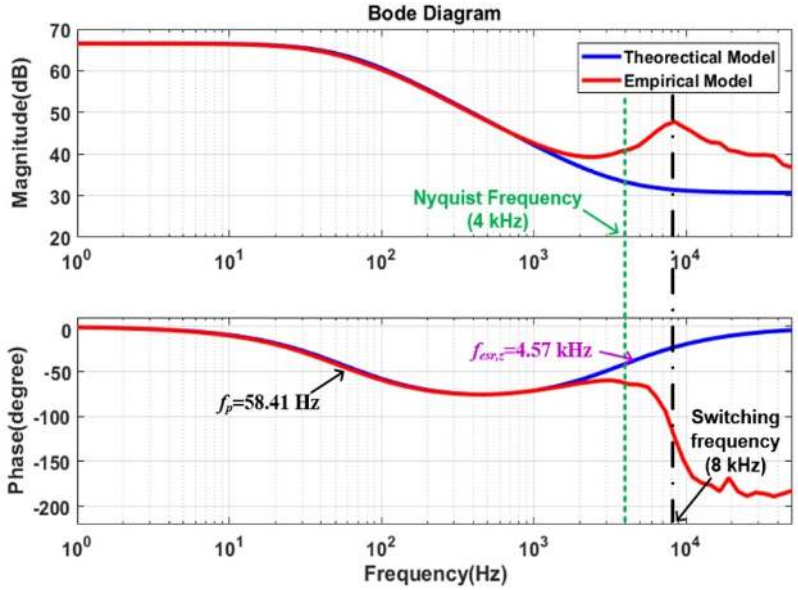

Figure 5. Bode plots of control-to-output transfer function of the 3P-DAB converter including the equivalent series resistance (ESR).

Table 2. Type of controller.

	P (Proportional)	I (Integration)	PI	PD	PID
Target	Reduce the transient error	Reduce the steady state error	Fast response with eliminating steady state error	Improved transient response characteristics	Improve both steady-state error and transient time
Control parameter number	1	1	2	2	3
Complexity	Low	Low	mid	Mid	high
Regulation	Rough	Rough	tight	tight	Very tight

The errors of the control-to-output transfer function between the empirical model and the simplified model are in high-frequency regions. This is because the simplified SSM does not consider the dynamics of the phase inductor and the nonlinearity of the pulse width modulation (PWM) generator. As shown in Figure 5, the control-to-output transfer function of the 3P-DAB converter's empirical model has a

phase-drop because of a double pole at the switching frequency. However, since the converter dynamics are effective under the Nyquist frequency, the model errors in the high-frequency region are not serious in the design of the controller [21,22]. The proposed extended SSM model can accurately represent the effect of the ESR zero of the output filter capacitor under the Nyquist frequency, which is indicated by the dashed line in Figure 5. Under the Nyquist frequency, the 3P-DAB converter seems to have a single-pole located in the low-frequency region, and the ESR zero is located in the high-frequency region, which is expressed in (5).

If the ESR zero of the output filter capacitor is not compensated, the magnitude of the control-to-output voltage transfer function of the 3P-DAB converter has a 0 dB/decade slope after the ESR zero, which affects less damping in the high-frequency region. It can make the system have poor relative stability against disturbances and it degrades the attenuation performance of external and internal noises. Figure 6 shows the control-to-output transfer function before Nyquist frequency with the effect of the ESR zero and the output capacitance. As shown in Figure 6a, even if the magnitude of the Bode plot does not much change, the corresponding phase changes are relatively large. Therefore, the desired controller design requires the obtention of the magnitude of the Bode plot of the loop gain, which has a slope of −20dB/decade in all the frequency ranges, i.e., the compensation of the ESR zero caused by the output filter capacitor is required in the design of the linear controller for the 3P-DAB converter.

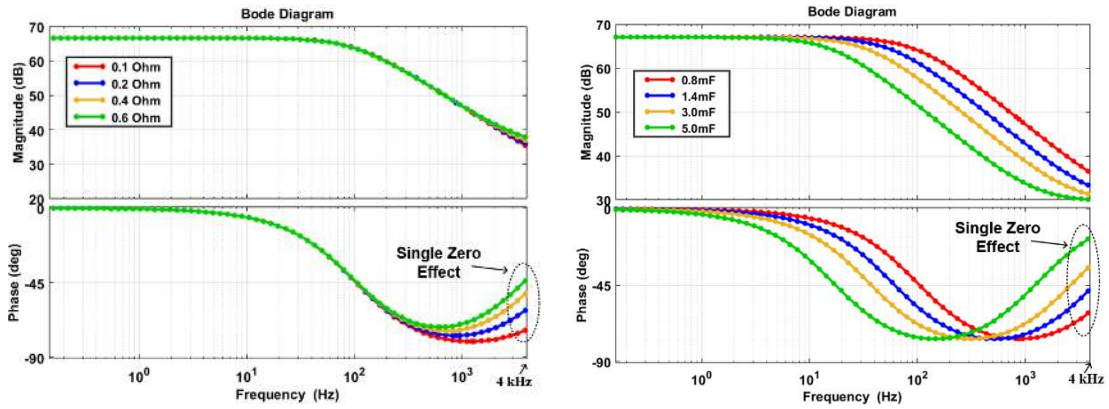

Figure 6. Bode diagram of control-to-output transfer function of 3P-DAB converter within Nyquist frequency in the theoretical model: (**a**) effect of ESR zero according to equivalent series resistance; (**b**) effect of ESR zero according to output capacitance variation.

Figure 6b shows the magnitude and phase of the control-to-output transfer function of the 3P-DAB converter according to the output filter capacitance. For high-power applications such as LVDC power systems, the output capacitors are usually parallelly connected to obtain enough capacitance to stabilize the DC bus voltage, to reduce the output voltage ripple under limited power fluctuation, and to reduce the equivalent ESR. However, as shown in Figure 6b, the position of the single-zero of the 3P-DAB converter depends on the output filter capacitance. For example, the capacitance increments of the output filter result in a single zero that is relatively located at low frequency and is close to the crossover frequency, which induces more phase boost. In other words, the influence of the ESR zero of high output filter capacitance becomes more significant than in the case of the lower output filter capacitor to the phase response of Bode plot. It can cause the dynamics of the converter to become slow. Therefore, a proper controller design is required to compensate for the effect of the output filter capacitor in the design of the linear controller.

3.2. Design Strategy of Improved Controller

To suppress the ESR zero effect, a proper controller design can be one of the great methods. The ESR zero can be reduced through practical hardware design methods and parallel/series connection; however, it cannot be vulnerable to high power density applications and this method has low cost-efficiency. By using the appropriate designed controller, the impact of ESR zero can be attenuated without increasing cost. As shown in Table 2, there are a lot of useful controllers that operate the converter. The most used control variables are proportional (P), integration (I), and differential (D), which allow the converter to be controlled by combining the three control variables. P controller is a control method that reduces the difference between the target's current location and the target's goal, but it has the disadvantage that normal error can occur. I controller is used to eliminate steady-state errors, but depending on the coefficient, the system can become unstable and the transient response can slow. PI controller improves steady-state errors but is disadvantageous for transient responses such as a delay in rising time. PD controllers improve transient response by increasing the braking rate of the system, but they are not effective in improving steady-state responses. PID controller is used to overcoming the steady-state error and has a fast-transient response. However, this method requires many computations and is vulnerable to external noise for the differentiation terms.

Even though the PI controller is dependent on the gain coefficient, it is widely used in industrial fields as a representative linear controller since a PI controller can eliminate the steady-state errors and operate under noisy conditions with its very simple structure. For that reason, in this paper, as the reference of the proposed controller, the PI controller is chosen. The PI controller consists of a pole at origin and a zero, expressed as follows:

$$G_{pi}(s) = K_{pi}\frac{\left(1+\frac{s}{\omega_{pi,z}}\right)}{s} \tag{6}$$

where k_{pi} is the DC gain, $\omega_{pi,z}$ is the angular frequencies of the single zero. The controller can be designed by using a k-factor approach [21,26,27].

To design the controller, the crossover frequency of f_C should be set first to obtain suitable dynamics of the power converter. The high f_C can effectively attenuate the disturbance in the low-frequency region. However, too high f_C can make the converter unstable due to insufficient PM. In addition, too low f_C can show slow dynamics with high overshoots and undershoots in the transient response. By using the k-factor approach, f_C is selected at 800 Hz and ϕ_{boost} is determined to be around 84°. By using f_C and ϕ_{boost}, the place of PI controller zero can be calculated as shown in (7).

$$f_{pi,z} = f_c \tan\left(\frac{\pi}{2} - \phi_{boost}{}^{\circ}\right) \tag{7}$$

Figure 7a shows the Bode plot of the PI controller designed by considering the transfer function derived in (6) where the pole is at 0 Hz and the zero is at 61.8 Hz. Figure 7b shows the closed-loop gain with the PI controller shown in 7a employed to the 3P-DAB converter. Even if the PM is obtained as 95.8° under the high-frequency region just before Nyquist frequency, the magnitude is almost 0 dB/decade and the phase reaches 0°. Although the PI controller is widely used in the industrial field, it cannot compensate for the ESR zero in the control-to-output voltage transfer function of the 3P-DAB converter.

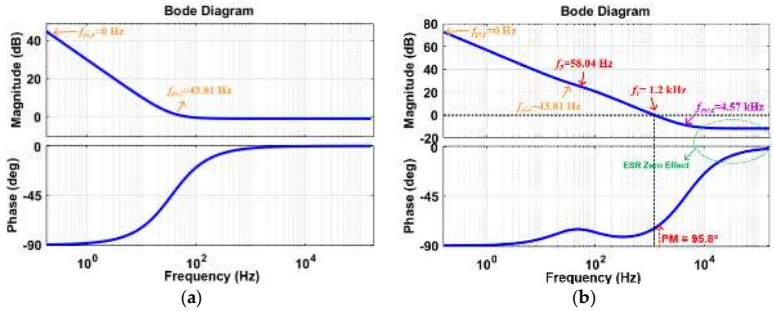

Figure 7. Bode plots of the 3P-DAB converter employing the conventional proportional integration (PI) controller in the theoretical model: (**a**) Bode plot of PI controller; (**b**) closed-loop gain of the entire converter.

Instead of the conventional PI controller, a two-pole one-zero (2P1Z) controller is proposed in this paper to compensate for the effect of the ESR zero. To increase the gain in the low-frequency region and to eliminate the steady-state error, a single-pole should be located at the origin. To compensate for the effect of the low-frequency pole in the 3P-DAB converter, a zero can be placed at low frequency. Finally, another pole can be located to compensate for the effect of the ESR zero caused by the capacitive output filter, i.e., the ESR zero can directly be compensated by the pole placement method using the proposed 2P1Z controller. Its transfer function can be expressed in S-domain as follows:

$$G_{2p1z}(s) = K_{2p1z}\frac{1+\frac{s}{\omega_{2p1z,z}}}{s\left(1+\frac{s}{\omega_{2p1z,p}}\right)} \tag{8}$$

where k_{2p1z} is the DC gain, $\omega_{2p1z,z}$ and $\omega_{2p1z,p}$ are the angular frequency of the single zero and the pole, respectively. The 2P1Z controller derived in (8) is designed by the k-factor approach, the same as the PI controller.

The Bode plot of the 2P1Z controller is plotted in Figure 8a. Figure 8b shows the Bode plot of the entire closed-loop gain of the 3P-DAB converter where f_C is selected at 800 Hz, which is the same as that of the PI controller. ϕ_{boost} is set to 76.8°. Using the k-factor approach, the pole and the zero are located at 4.25 kHz and 58.8 Hz in the frequency domain, respectively. The PM is obtained as 89.9°. The slope of the Bode plot shows almost −20 dB/decade formulated by the compensation of the ESR zero by using the proposed 2P1Z controller. Compared with Figure 8b, Figure 7b shows the magnitude of the control-to-output voltage transfer function, which has 0 dB/decade slope in the higher frequency region. It is vulnerable to high-frequency noises and disturbances. As described above, the controller is designed by using the theoretical 3P-DAB model shown in the blue line of Figure 5. The influences of the double poles at the switching frequency illustrated in the empirical model of Figure 5 are ignored. In other words, neither Figure 7b nor Figure 8b shows the phase-drop in the closed-loop gain.

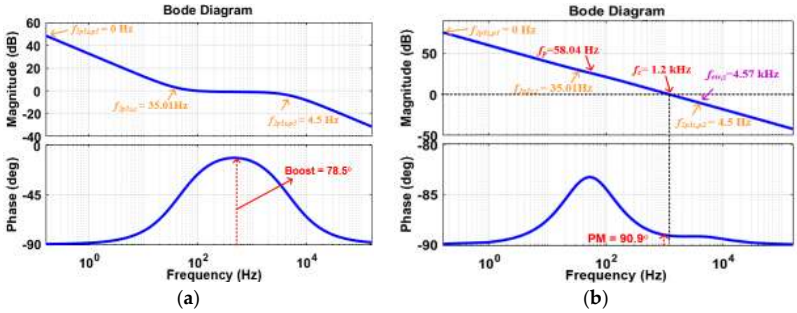

Figure 8. Bode plots of the 3P-DAB converter employing the proposed two-pole one-zero (2P1Z) controller in the theoretical model: (**a**) Bode plot of 2P1Z controller; (**b**) closed-loop gain of the entire converter.

3.3. Analysis of Output Impedance

The dynamic performance of the power converter according to input variations or load fluctuations employing the feedback controller can be expected based on the analysis of the output impedance. The open-loop load current-to-output voltage transfer function can be derived as (9), and the output impedance can be calculated using (9) as (10):

$$Z_p(s) = \frac{\hat{V}_o(s)}{\hat{i}_o(s)} = k_p \frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}\right)}$$
$$k_p = R_L \| r_{Ls},\ \omega_{z1} = \frac{r_{Ls}}{L_s},\ \omega_{esr} = \frac{1}{r_{Cof}C_{of}},\ \omega_o = \frac{1}{\sqrt{L_s C_{of}}}\sqrt{\frac{R_L+r_{Ls}}{R_L+r_{Cof}}},\ Q = \frac{1}{\omega_o}\frac{R_L+r_{Ls}}{L_s+C_{of}(r_{Ls}r_{Cof}+R_L r_{Cof}+R_L r_{Ls})} \quad (9)$$

$$Z_{o,x}(s) \equiv \left.\frac{\hat{V}_o(s)}{\hat{i}_o(s)}\right|_{closed} = \frac{Z_p(s)}{1+T_{m,x}(s)} \quad (10)$$

where k_p is the DC gain of the load current-to-output voltage transfer function, ω_o is the angular frequency of the double pole, Q is the damping ratio, and r_{Ls} is the effective series resistance of L_S, $Z_{o,x}$ is the closed-loop output impedance, and $T_{m,x}$ is the loop gain of the 3P-DAB converter.

The Bode plot of the output impedance in the frequency-domain is shown in Figure 9. The blue line and the red line show the loop gain employing the conventional PI controller and the proposed 2P1Z controller, respectively. In the case of Zo, x, the loop gain should be minimized in the operating frequency range for the converter to operate as an ideal voltage source with low noise sensitivity. Since the peaking in |Zo| under the low-frequency region indicates less attenuation according to the load variation, the under-damped term produces a poor dynamic response in the time-domain when the PI controller is employed. Therefore, due to the disturbance suppressing capability, the proposed 2P1Z controller is expected to show better dynamic performance than the conventional PI controller.

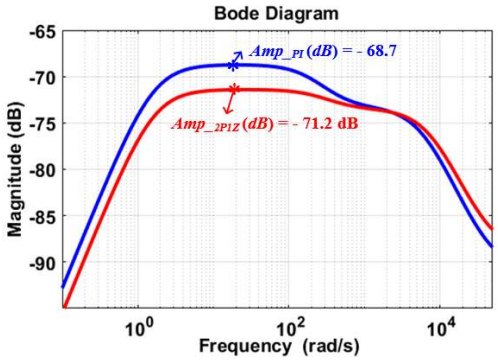

Figure 9. Plots of output impedance with closed-loop control of the 3P-DAB converter in the theoretical model.

The step load response of the output voltage of each controller in the time-domain can be investigated using the inverse Laplace transform with the step input. The peak value of the output voltage is determined by the size of the step load change and the peaking in |Zo|. Figure 10 shows simulated transient responses when the output power changes in a step from 25 kW (100%) to 2.5 kW (10%). The step load current of I_{step} is set to 81 A. In the case of the 2P1Z controller, the peaking of |Zo| is smaller than in the case of the PI controller. In addition, the settling time of the 2P1Z controller also decreases compared to the PI controller, even though the crossover frequency is not different. Therefore, by employing the proposed controller, the improvement of the dynamic performance of the 3P-DAB converter can be achieved.

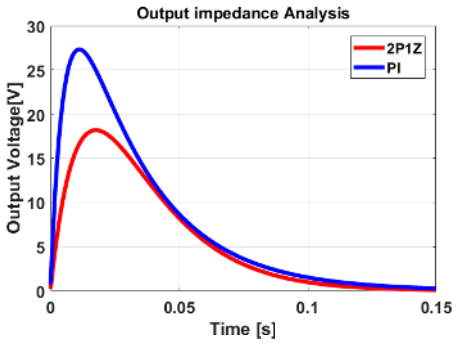

Figure 10. Simulated transient responses of the 3P-DAB converter using the theoretical model in the time-domain.

4. Experimental Results

As shown in Figure 11, a 25 kW 3P-DAB converter prototype for experimental verification is developed by using IGBT modules of CM600DX-24S1 manufactured by MITSUBISHI, three phase-inductors, and input/output filter capacitors with three Y-Y connected transformers. To improve efficiency, a high-flux core of CH740060 is used as the material of the coupling inductance of 43.7 μH [5]. Due to the facility limitation, the input voltage is limited to 550 V, but the ratio of the input and output voltage is the same as the ratio of 750 V to 380 V, which is the common voltage of the DC grid system. To reduce ESR, even if the filter size is bigger than that of the electrolytic capacitor, a film capacitor of K3490070106K0L155 manufactured by KENDEIL is employed in the prototype converter. To reduce the core loss, to prevent saturation, and to obtain better temperature performance than that of ferrite cores below the operating frequency of 20 kHz, a nano-crystalline core of TC-1308040-1 manufactured by AVERTEC [28] is used as the material for the transformer core [29–31]. The TMS320F28335 is used as a digital controller.

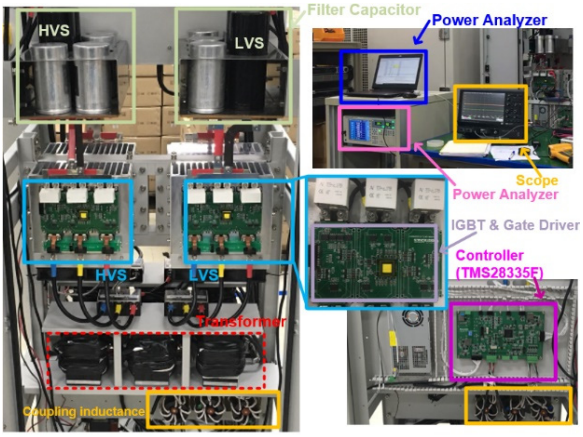

Figure 11. Photograph of the 25 kW prototype 3P-DAB converter and its test bench.

Experimental results in the steady-state operation using the 2P1Z controller are shown in Figure 12. The output power and the amount of the phase shift are shown above in each figure. According to the load variation, the phase shift angle has changed. As the output power increases, the phase-shift angle increases to transfer the power to the secondary side as shown in (3). In all the load ranges, the output voltage is well regulated to the target of 278 V. The peak and RMS current at the rated load is measured as 54.5 A and 36.03 A, respectively. In the rated power, the output voltage ripple is measured as 49.32 V.

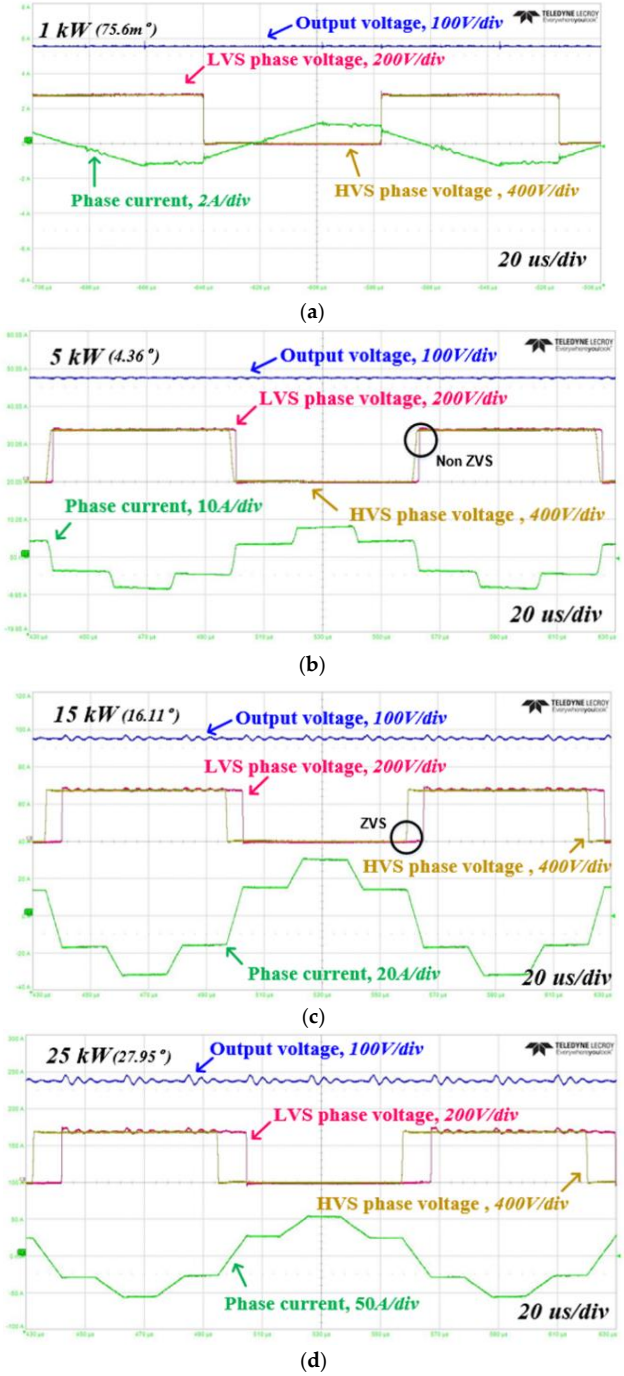

Figure 12. Experimental waveforms of the 3P-DAB converter in steady-state operation using the proposed controller: (**a**) 1 kW; (**b**) 3 kW; (**c**) 15 kW; and (**d**) 25 kW.

Figures 13 and 14 show the experimental comparison waveforms between the conventional PI controller and the proposed 2P1Z controller according to the step load responses from 25 kW to 2.5 kW and from 2.5 kW to 25 kW. As shown in Figure 13a,b, the settling time of the PI controller is measured to be 114 ms and that of the 2P1Z controller is measured to be 93 ms. This means that the dynamics of the proposed 2P1Z controller are relatively faster than that of the PI controller. In addition, the overshoots are measured as 27.8 V and 21.3 V, respectively, where the overshoot of the PI controller is higher than that of the 2P1Z controller. From the output impedance analysis, the overshoots of the PI controller and 2P1Z controller are expected to be 27.2V and 18.7 V, respectively, which are closely matched to experimental measurements. The errors between the theoretical analysis and the

experimental measurement can be expected due to the converter model errors that ignore the dynamics of L_S and unexpected impedances from the power source, electric load, PCB layouts, etc. In Figure 14, the undershoots of the PI controller and the 2P1Z controller are measured to be 29.8 V and 19.2 V, respectively. Their tendency is similar to the results shown in Figure 13. As a result, the proposed 2P1Z controller shows a better dynamic performance than that of the PI controller for the 3P-DAB converter. The efficiency curves of the converters, which employ the conventional PI controller and the proposed 2P1Z controller, are shown in Figure 15. The highest efficiency is measured to be 97.2% at 8.5 kW. The efficiency values of the 2P1Z controller and the conventional PI controller are very close to each other. From Figure 15, it is noted that there is no difference in efficiency according to the controllers.

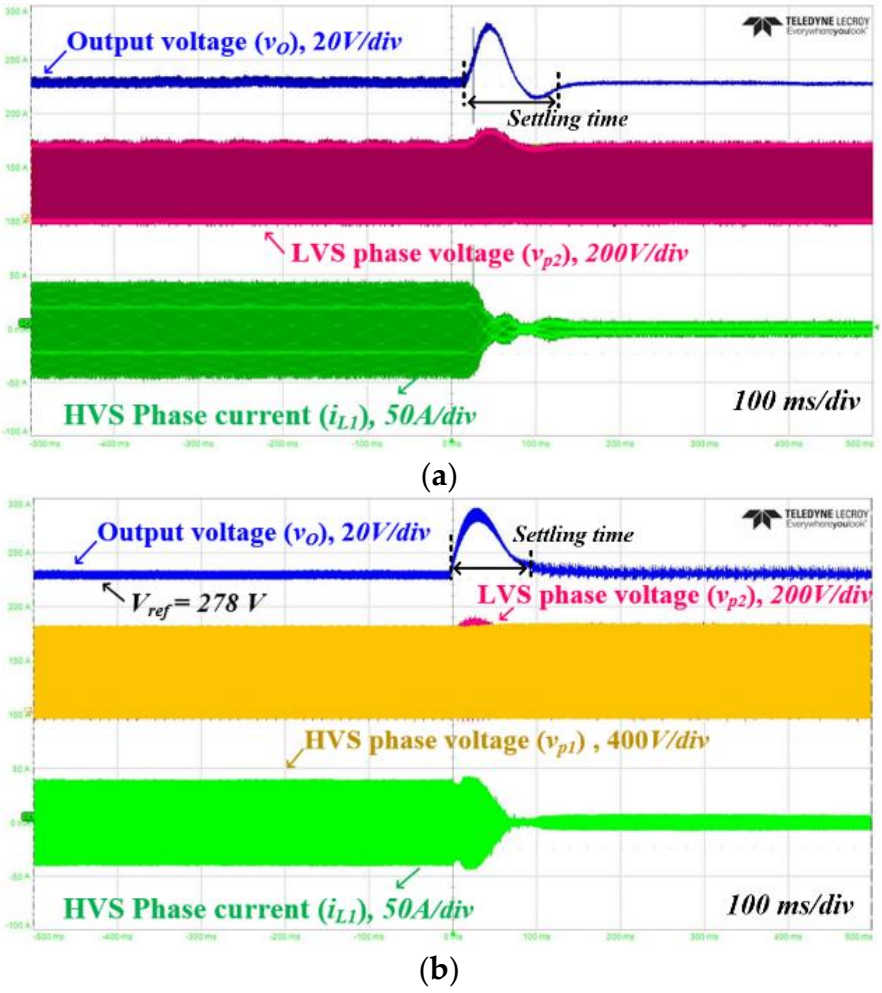

Figure 13. Experimental waveforms of the step-down load response according to load variation from 25 kW to 2.5 kW: (**a**) PI controller; (**b**) 2P1Z controller.

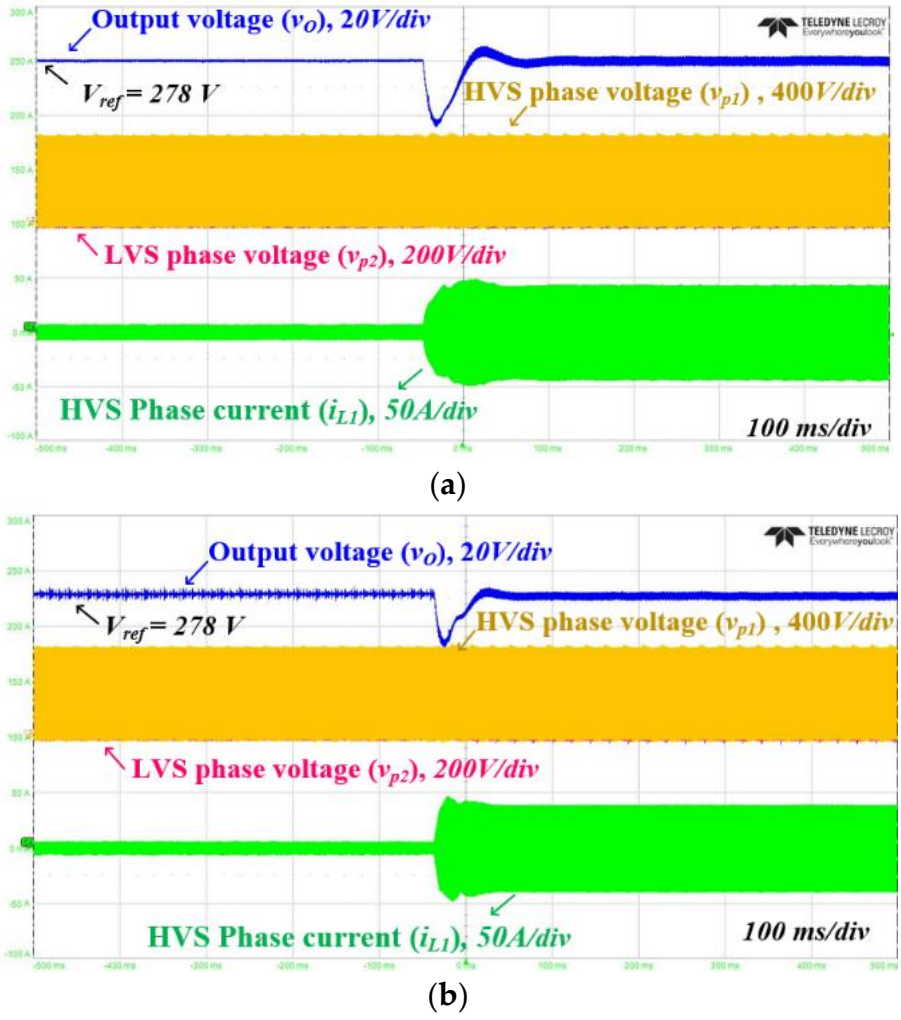

Figure 14. Experimental waveforms of the step-up load response according to load variation from 2.5 kW to 25 kW: (**a**) PI controller; (**b**) 2P1Z controller.

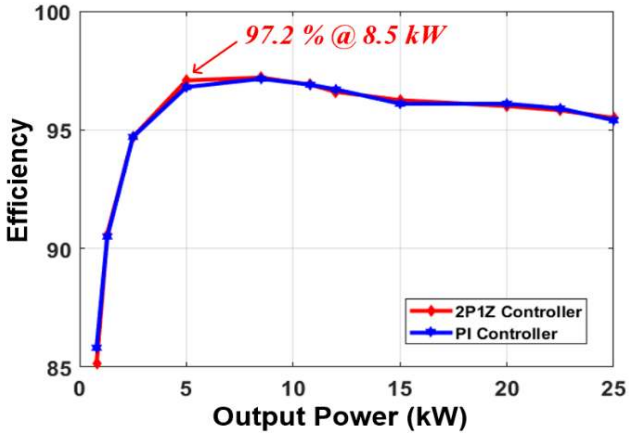

Figure 15. Experimental waveforms of the step-up load response according to load variation from 2.5 kW to 25 kW: (Blue) PI controller; (**Red**) 2P1Z controller.

5. Conclusions

In this paper, the design methodology of the enhanced 2P1Z controller is proposed to eliminate the effect of the ESR zero of the output filter capacitor in the 3P-DAB converter. The converter,

which employs the prevalent PI controller, could be unstable due to noises and disturbances from the effect of the ESR in the capacitive output filter and its high capacitance. The suitable design procedure of the linear controller for the 3P-DAB converter is presented by using the generalized average SSM including the ESR zero of the output capacitor. To demonstrate the performance of the proposed controller, the output-impendence analysis is carried out. Using the 25 kW prototype 3P-DAB converter, the dynamic performance of the proposed 2P1Z controller as well as its steady-state operation are verified. The step-up and step-down load responses, and the settling time of the 3P-DAB converter employing the 2P1Z controller, are measured as 21.3 V, 19.2 V, and 93 ms, respectively. The step-up and step-down load responses and the settling time of the 3P-DAB using the PI controller are 27.8 V, 29.8 V, and 114 ms, respectively. The step load response of the 2P1Z controller is improved to 23% and 35%, and the settling time of the 2P1Z controller is improved 18.4% more than the PI controller. The 2P1Z controller has the characteristics of lower overshoot, undershoot and faster settling time compared to the conventional PI controller.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

DC MG	direct current microgrid.
AC	alternating current
LVDC	low voltage direct current
IBDC	isolated bi-directional DC-DC converter
SP-DAB	single phase dual active bridge
3P-DAB	three phase dual active bridge
SSM	small-signal model
LTI	linear time invariant
SPSM	single phase shift modulation
HVS	high voltage side
LVS	low voltage side
ZVS	zero voltage switching
ϕ_{PS} (=ϕ/π)	the amount of the phase shift between HVS and LVS
ESR	equivalent series resistance
SSA	state-space average
2P1Z	two-pole one-zero
GM	gain margin
SPS	single phase shift
PM	phase margin

Appendix A

The appendix is an optional section that can contain details and data supplemental to the main text. For example, explanations of experimental details that would disrupt the flow of the main text, but remain crucial to the understanding and reproducing of the research shown; figures of replicates for experiments of which representative data are shown in the main text can be added here if brief, or as supplementary data. Mathematical proofs of results not central to the paper can be added as an appendix. This appendix presents the process of deriving the small-signal model of the 3P-DAB converter including the ESR zero of the capacitive output filter. This is not covered in the paper as it is too heavy and complex.

Through (A1) to (A7), the state variable of the 3P-DAB converter is defined. The average state-space model can be expressed as (A1) and can be reorganized as (A2) based on the 3P-DAB converter.

$$\dot{\vec{x}} = A\vec{u} + B\vec{x} \tag{A1}$$

$$\frac{dv_{cof}}{dt} = Av_i + Bv_{cof} \tag{A2}$$

The voltage differential equation can be expressed as (A3) and (A4)

$$v_o = v_{Cof} + r_{Cof}i_C = v_{Cof} + r_{Cof}C_{of}\frac{dv_{Cof}}{dt} \tag{A3}$$

$$i_c = C_{of}\frac{dV_{Cof}}{dt} = i_{s,DC} - I_{out} \tag{A4}$$

Using the (A3) and (A4), the (A5) can be derived as follows:

$$\frac{dV_{Cof}}{dt} = \frac{i_{s,DC}}{C_of} - \frac{v_o}{R_LC_of} = \frac{i_{s,DC}}{C_of} - \frac{v_{Cof} + r_{Cof}C_{of}\frac{dv_{Cof}}{dt}}{R_LC_of} \tag{A5}$$

$$\left(1 + \frac{r_{Cof}}{R_L}\right)\frac{dV_{Cof}}{dt} = \frac{i_{s,DC}}{C_of} - \frac{v_{Cof}}{R_LC_of} \tag{A6}$$

Meanwhile, depending on the upper and lower switches on-state in the LVS, the secondary current $i_{s.DC}$ will be divided into two equations according to the phase angle as shown in (A7).

$$\begin{cases} \overline{i_{s,DC\_I}} = \frac{1}{9wL}\left\{(3\phi - \pi)v_{Cof} + \left(\frac{3\phi}{2} + \pi\right)v_i\right\} & 0 \le \theta < \phi \\ \overline{i_{s,DC\_II}} = \frac{1}{9wL}\left\{3\phi\left(v_{Cof} + v_i\right)\right\} & \phi \le \theta \le \frac{\pi}{3} \end{cases} \tag{A7}$$

When (A7) is substituted to (A6), matrix A and B in (A2) can be derived, depending on the phase shift range.

$$\left(\frac{r_{Cof} + R_L}{R_L}\right)\frac{dV_{Cof}}{dt} = \frac{3\phi - \pi}{9\omega LC_{of}}v_{Cof} + \frac{\frac{3}{2}\phi + \pi}{9\omega LC_{of}}v_i - \frac{v_{Cof}}{R_LC_{of}} \tag{A8}$$

$$+\left(\frac{1}{r_{Cof} + R_L}\right)\frac{\left\{R_L(3\phi - \pi) - 9\omega L\right\}}{9\omega LC_{of}}v_{Cof} \tag{A9}$$

Finally, A_1 and B_1 can be derived as follows:

$$A_1 = \frac{R_L}{9\omega LC_{of}\left(r_{Cof} + R_L\right)}\left(\frac{3}{2}\phi + \pi\right) \tag{A10}$$

$$B_1 = \frac{\left\{R_L(3\phi - \pi) - 9\omega L\right\}}{9\omega LC_{of}\left(r_{Cof} + R_L\right)} \tag{A11}$$

In the same way, A_2 and B_2 have relationships as follows:

$$\left(1 + \frac{r_{Cof}}{R_L}\right)\frac{dv_{Cof}}{dt} = \frac{1}{9\omega LC_{of}}3\phi\left(v_{Cof} + v_i\right) - \frac{v_{Cof}}{C_{of}R_L} \tag{A12}$$

$$\frac{dv_{Cof}}{dt} = \left(\frac{1}{r_{Cof} + R_L}\right)\frac{3(\phi R_L - 3\omega L)}{9\omega LC_{of}}v_{Cof} + \frac{R_L}{r_{Cof} + R_L}\frac{3\phi}{9\omega LC_{of}}v_i \tag{A13}$$

Finally, A_2 and B_2 can be derived by using (A12) and (A13).

$$A_2 = \frac{3\phi R_L}{\left(r_{Cof} + R_L\right)9\omega LC_{of}} \tag{A14}$$

$$B_2 = \frac{3(\phi R_L - 3\omega L)}{\left(r_{Cof} + R_L\right)9\omega L C_{of}} \tag{A15}$$

Based on (A10), (A11), (A14), and (A15), matrix A and B in (A1) can be derived.

$$\begin{aligned} A &= \frac{3}{\pi}\left\{\frac{R_L}{\left(r_{Cof}+R_L\right)9\omega L C_{of}}\left(\frac{3}{2}\phi + \pi\right)\phi + \frac{3\phi R_L}{\left(r_{Cof}+R_L\right)9\omega L C_{of}}\left(\frac{\pi}{3} - \phi\right)\right\} \\ &= \frac{R_L\phi}{\left(r_{Cof}+R_L\right)\omega L C_{of}}\left(\frac{2}{3} - \frac{\phi}{2\pi}\right) \end{aligned} \tag{A16}$$

$$B = \frac{3}{\pi}\left\{\frac{\left\{R_L(3\phi - \pi) - 9\omega L\right\}}{\left(r_{Cof} + R_L\right)9\omega L C_{of}}\phi + \frac{3(\phi R_L - 3\omega L)}{\left(r_{Cof} + R_L\right)9\omega L C_{of}}\left(\frac{\pi}{3} - \phi\right)\right\} = -\frac{1}{\left(r_{Cof} + R_L\right)C_{of}} \tag{A17}$$

Therefore, (A2) can be reorganized as (A18), and the average state-space model of the 3P-DAB converter can be obtained.

$$\frac{dv_{cof}}{dt} = \frac{R_L\phi}{\left(r_{Cof} + R_L\right)\omega L C_{of}}\left(\frac{2}{3} - \frac{\phi}{2\pi}\right)v_i + \frac{-1}{\left(r_{Cof} + R_L\right)C_{of}}v_{cof} \tag{A18}$$

To derive the small-signal model, (A3) is modified to S-domain using the small-signal technique.

$$\Delta v_o = \Delta v_{Cof} + r_{Cof}C_{of}S\Delta v_{Cof} = \Delta v_{Cof}\left(1 + r_{Cof}C_{of}S\right) \tag{A19}$$

When (A19) is applied to (A3), finally, (A20) can be derived.

$$\Delta\frac{dv_{cof}}{dt} = \frac{R_L}{\left(r_{Cof} + R_L\right)\omega L C_{of}}\left\{\left(\frac{2}{3} - \frac{\phi}{\pi}\right)v_i\Delta\phi + \left(\frac{2}{3} - \frac{\phi}{2\pi}\right)\phi\Delta v_i\right\} + \frac{-1}{\left(r_{Cof} + R_L\right)C_{of}}\Delta v_{cof} \tag{A20}$$

To neglect the effect of the input voltage, $\Delta v_i = 0$ is applied to (A20), and it is expressed as (A21).

$$\left(S + \frac{1}{\left(r_{Cof} + R_L\right)C_{of}}\right)\Delta v_{cof} = \frac{R_L}{\left(r_{Cof} + R_L\right)\omega L C_{of}}\left\{\left(\frac{2}{3} - \frac{\phi}{\pi}\right)v_i\Delta\phi\right\} \tag{A21}$$

Finally, the control to output transfer function of the 3P-DAB converter can be derived as (A22).

$$\frac{\Delta v_{cof}}{\Delta\phi} = \frac{v_i R_L\left(r_{Cof}C_{of}S + 1\right)}{\left\{\left(r_{Cof} + R_L\right)C_{of}S + 1\right\}\omega L}\left(\frac{2}{3} - \frac{\phi}{\pi}\right) \tag{A22}$$

The 3P-DAB converter's small-signal transfer function from control to output gives the response of the output voltage due to the changes in the load angle ϕ.

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