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Practical Evaluation of Loss Reduction in Isolated Series Resonant Converter with Fixed Frequency Modulation

Danish Khan ¹, Pengfei Hu ^{1,*}, Muhammad Waseem ¹, Muhammad Yasir Ali Khan ², Mustafa Tahir ¹ and Andres Annuk ³

¹ College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China

² College of Energy and Electrical Engineering, Hohai University, Nanjing 211100, China

³ Institute of Forestry and Engineering, Estonian University of Life Sciences, 51006 Tartu, Estonia

* Correspondence: hpf@zju.edu.cn

Abstract: Nowadays, power converters with reduced cost, compact size and high efficiency are evolving to overcome the emergent challenges of renewable energy integrations. In this context, there is an increased demand for well-designed power converters in renewable energy applications to reduce energy utilization and handle a variety of loads. This paper proposes a center-tapped bridge cascaded series-resonant LC dual active bridge (DAB) converter for DC-DC conversion. The low part count of the proposed converter enables a high-power density design with reduced cost. The proposed converter offers reduced conduction losses as the reverse current is eliminated by adopting current blocking characteristics. Reverse current blocking also enables zero voltage switching (ZVS) and zero current switching (ZCS) over a wide operating range. Therefore, using a simple fixed frequency modulation (FFM) scheme offers a wide operating range compared to a conventional DAB converter. A thorough comparison of the proposed converter and a conventional DAB converter is provided based on conduction losses and switching losses to illustrate the performance improvement. Lastly, the effectiveness of the proposed converter is validated through simulation and experimental results.

Keywords: LC tank circuit; center-tapped (CT) bridge; zero current switching (ZCS); series resonant converter (SRC); discontinuous conduction mode (DCM); zero voltage switching (ZVS)



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1. Introduction

Demand for electric power keeps on increasing nowadays. Therefore, the world is switching over to the field of renewable energy sources as it is pollution free, free of cost, and easy to access in remote areas [1,2]. Researchers are mainly focusing on solar PV generation renewable energy sources since it is more reliable and easier to install. The output voltage of a photovoltaic system is variable due to the uncertainty of environmental conditions. However, to provide a constant and regulated output voltage, power electronic DC-DC converters are employed [3–5]. A dual-active-bridge (DAB) DC-DC converter was initially proposed in [6]. It has gained increasing attention for its use in high-power applications such as energy storage systems, electric vehicles, and solid-state transformers [7]. Due to the recent advancements in semiconductor devices, digital signal processors, and magnetic components, DAB converters have shown many advantages over their counterpart topologies (i.e., buck and boost converters) in terms of galvanic isolation, soft-switching capability, bidirectional power transfer, ease of control, high power conversion efficiency and high-power density [8–11].

DC-DC converters are classified into two types: isolated DC-DC converters and non-isolated DC-DC converters. In an isolated DC-DC converter, the input and output of the converter are isolated by an electrical barrier using a high-frequency transformer. The main advantage of the isolated DC-DC converter is that it protects the sensitive load from source disturbances, the output of the converter can be configured in either positive or negative

polarity, and it has a high noise interference elimination capability. Numbers of isolated DC-DC converters are presented in the literature. Different DC-DC converter topologies are developed concerning higher efficiencies, reliable control switching strategies, fault-tolerant configurations, and mostly on renewable energy-based applications [12,13].

A conventional DAB converter is made up of two H-bridges connected via a high-frequency transformer (HFT). In contrast to the DC-DC topologies with unidirectional switches, the DAB topology employs current bidirectional switches that enable bidirectional power flow [14]. Inspired by DAB performance, DAB-based novel topologies are being investigated with the aim of improving performance with a reduced number of devices [6]. Authors in [15] used a center-tapped bridge topology that reduced conduction losses by eliminating reverse current and employed fewer devices. However, the power density and performance deteriorated due to the linearly increasing nature of the inductor current. Resonant tanks such as L, LC, LLC, and CLLC are introduced in traditional DAB topology to improve the overall performance [16,17]. L-tank is explored for single-phase and three-phase converters in [18], reducing energy losses. Other researchers in [19] proposed the LLC and CLLC resonant tanks for DAB topology that feature extended input voltage range along with reduced energy losses. The advantages of an LLC resonant converter include its simple structure and soft switching. It can facilitate the transmission of power in both directions, but it is challenging to achieve a normalized gain greater than one in the backward mode (backward step-up mode) [19,20]. Among different studies addressed, the DAB converter with LC tank offers high-power density with a reduced number of devices, since at the resonance frequency it can accomplish zero impedance [21]. In addition, the employed capacitor in the resonant tank assists in avoiding the saturation condition of the transformer and the inductor as it can block the DC current. Though the DAB with LC resonant tank has advantages, it requires several passive components, which increase the size, weight, and cost of the converter. To reduce the size of the passive components, switching frequency is typically increased, which enables high-power density design but reduces the efficiency since the switching losses increase at a higher frequency [22].

The control strategy has been one of the key research challenges in this field. For voltage-source series-resonant converters, many control strategies have been analyzed and investigated [23–25], which has turned this into a mature technology nowadays. A control scheme based on variable frequency phase-shifting is proposed in [24] that features a wider input voltage range and extended ZVS range; however, the output voltage range is still limited. Studies in [26] indicate that energy losses and limited load voltage range are two main challenges in such bidirectional DC-DC converters. To overcome these issues, a new modulation strategy, fixed frequency modulation (FFM), is presented in [27] that enables improved efficiency design along with reduced passive components by adopting fixed frequency to realize soft switching. In addition to a substantial reduction in switching losses, FFM features robustness, and the size of the heat sink can be reduced. Besides, it is relatively simple as it reduces the control complexity and design effort [28]. To realize soft switching under large loads and to achieve effective output voltage tracking under load variation, a duty ratio control method is presented in [26]. However, maximum efficiency can only be realized under peak voltage due to the limited soft-switching range offered by the duty ratio control method. Researchers in [29] studied the resonant characteristics of the LC-DAB topology by using the transient current to extend the zero voltage switching (ZVS) range and to handle the large load variation. The integrated gate-commutated thyristor's (IGCT's) very low conduction losses make it an appealing candidate for use in soft-switched topologies that operate under favorable ZVS or ZCS conditions [30]. However, these have turn-off currents in the range of several kA, for which the device needs to be optimized with resonant converter topologies. Time-domain analysis was carried out that assists in the optimum selection of modulation method and design parameters. These issues can be addressed by exploring new modulation schemes for the converters.

In this paper, a new DAB converter with an LC resonant tank is studied. The proposed converter employed the FFM-based novel modulation. The modulation scheme enables

soft switching for the switches at the primary and secondary sides of the HFT without using any auxiliary circuits. Therefore, the overall power losses are minimized by using the least number of components for a wide range of load by employing the proposed modulation scheme. The proposed LC resonant based converter has the following advantages over the traditional counterparts:

1. Soft switching capability from zero to full load range of the proposed converter leads to low primary switch turn off currents and switching loss.
2. With high input voltage, high efficiency can be achieved.
3. It enables zero impedance at resonant frequency, which is highly desirable.
4. Compared with other resonant DAB topologies, it employs a smaller number of passive components in the resonant tank and hence facilitates the size reduction, and higher power density can be achieved.
5. Saturation of the inductor and transformer, which is one of the main issues, can be avoided with the help of the capacitor employed in the resonant tank of the proposed converter.
6. Moreover, the performance of topology is further boosted by employing an advance modulation technique.

The key points of this research are summarized as follows:

- A DAB converter is proposed in this paper, which fulfills the galvanic isolation requirement by employing a high-frequency center-tapped transformer between the primary and secondary sides. The primary side consists of a full bridge topology and a resonant tank for soft switching and at the secondary side pairs of anti-series MOSFETs are employed at both ends of the center-tapped transformer, which blocks the reverse current.
- A novel modulation scheme that is based on the FFM is employed and verified. With the implementation of the proposed modulation scheme in discontinuous conduction mode (DCM), the performance of the converter is considerably improved due to reduced power losses, as the switching losses are minimized with the help of soft switching, and the conduction losses are reduced by blocking the reverse current.
- The proposed modulation method extends the voltage gain of the converter without compromising the soft switching or adding any complexity to the modulation method. Therefore, improved reliability and voltage gain are achieved in this research without employing any auxiliary components.

The remaining organization of this paper includes the following sections: In Section 2, the background of the suggested topology is explained in detail along with the suggested modulation scheme. In Section 3, operational modes of the proposed topology are described. Section 4 contains the explanation of the control approach employed by the suggested converter. The power losses curves and efficiencies of existing and suggested converters are compared in Section 5. The simulation and experimental results are given in Sections 6 and 7, respectively. Finally, in Section 8, decisive comments for the suggested converter are specified.

2. Background of the Suggested Converter

2.1. Proposed Converter

The schematic illustration of the suggested series resonant converter (SRC) is presented in Figure 1. Here it is considered that the PV module generates the maximum power with constant DC. The full bridge on the primary end is comprises four MOSFETs (Q_1 to Q_4) switches alongside their body diodes (D_1 to D_4) in an antiparallel manner. The center-tapped (CT) bridge on the secondary side is composed of two limbs, where each limb has two MOSFETs (Q_5 , Q_6 , and Q_7 , Q_8) with their body diodes (D_5 to D_8) in an anti-parallel fashion. The resonant LC tank is cascaded with CT-HFT, and this combination is positioned in between the two bridges. The diodes of the primary end facilitate the backflow of current and hence allow the power to flow in reverse mode. In comparison, the CT bridge does not

permit the backflow of current and blocks the reverse current. When both the switches of a limb (Q_5, Q_6 or Q_7, Q_8) in the CT bridge are turned off then no current will flow in that limb and vice versa. Similarly, a limb with one conducting switch (i.e., Q_5) will only allow the stream of positive current via that limb and the non-conducting switch of the limb will block the flow of negative current (i.e., Q_6). The stream of current depends upon the input signal and the direction of power flow can be switched by adjusting the input signals of the MOSFETs.

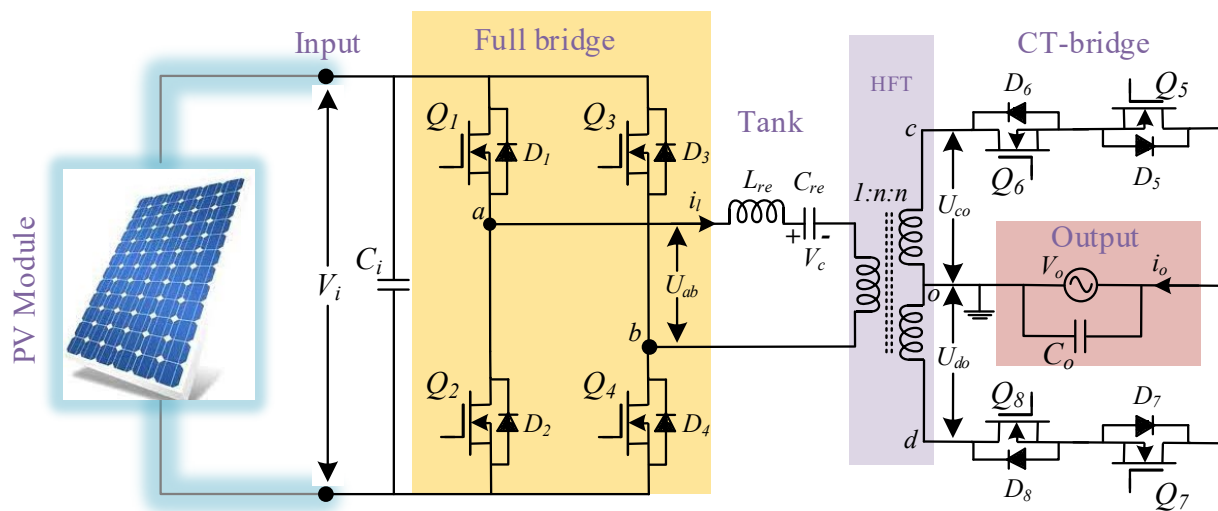


Figure 1. Schematic illustration of the suggested converter topology.

To improve the flow of current and power density, the inductor L_{re} and capacitor C_{re} of the resonant tank are connected in series with the CT-bridge and the high-frequency transformer (HFT). The input voltage to the resonant tank is the output of the input side full bridge, which is denoted by U_{ab} , while U_{co} and U_{do} represent the output side CT bridge voltages. The two CT-bridge voltages are employed to define the magnitude and phase of the system. If U_{do} is positive, then the lower limb of the CT bridge will conduct and vice versa. Moreover, bipolar-voltage generation leads to complexity in the control of switches, which becomes very hard and needs suitable modulation techniques to adopt soft switching and ensure high effectiveness.

The conduction and switching features of existing DAB converters and the proposed converter are compared in Table 1. The conventional DAB equipped LC-tank topologies control the power by regulating the duty ratio of the used square wave. Nevertheless, due to the hard switching strategy, these topologies are threatened by higher switching losses [16]. The comparison chart of the proposed topology with other methods is given in Table 2.

Table 1. Assessment of existing and proposed converters.

| Converter Types | Backflow of Current | Switching Features |
|--------------------------------|---------------------|--------------------|
| L-Tank Topology [6] | Allow | soft-switching |
| LC-Tank Existing Topology [13] | Block | hard-switching |
| LC-Tank Proposed Topology | Block | soft-switching |

Table 2. Comparison Table of Proposed Topology with other Methods.

| Parameters | Conventional LLC [31] | Hybrid Control Strategy [32] | Dual Full Bridge LLC [33] | Proposed |
|---------------------------|-----------------------|------------------------------|---------------------------|-----------|
| Control stability | Simple | Complex | Complex | Simple |
| Control complexity | High | High | High | Low |
| Accuracy of analysis | Poor | High | High | High |
| Components design | Complicated | Medium | Medium | Simple |
| Design method | Simple | complex | complex | Simple |
| Soft switching capability | Narrow | medium | medium | Full Load |

2.2. Fixed Frequency Modulation (FFM)

The working procedure and effective outcomes of the proposed series resonant converter (SRC) under the proposed modulation are presented in Figure 2. Where the modulation frequency (f_M) is similar to the resonance frequency of the LC circuit and is given in Equation (1).

$$f_M = \frac{\omega_{re}}{2\pi} = \frac{1}{2\pi\sqrt{L_{re}C_{re}}} \tag{1}$$

$$T_M = \frac{1}{f_M} \tag{2}$$

where L_{re} and C_{re} correspond to the inductance and capacitance values of the LC-tank circuit.

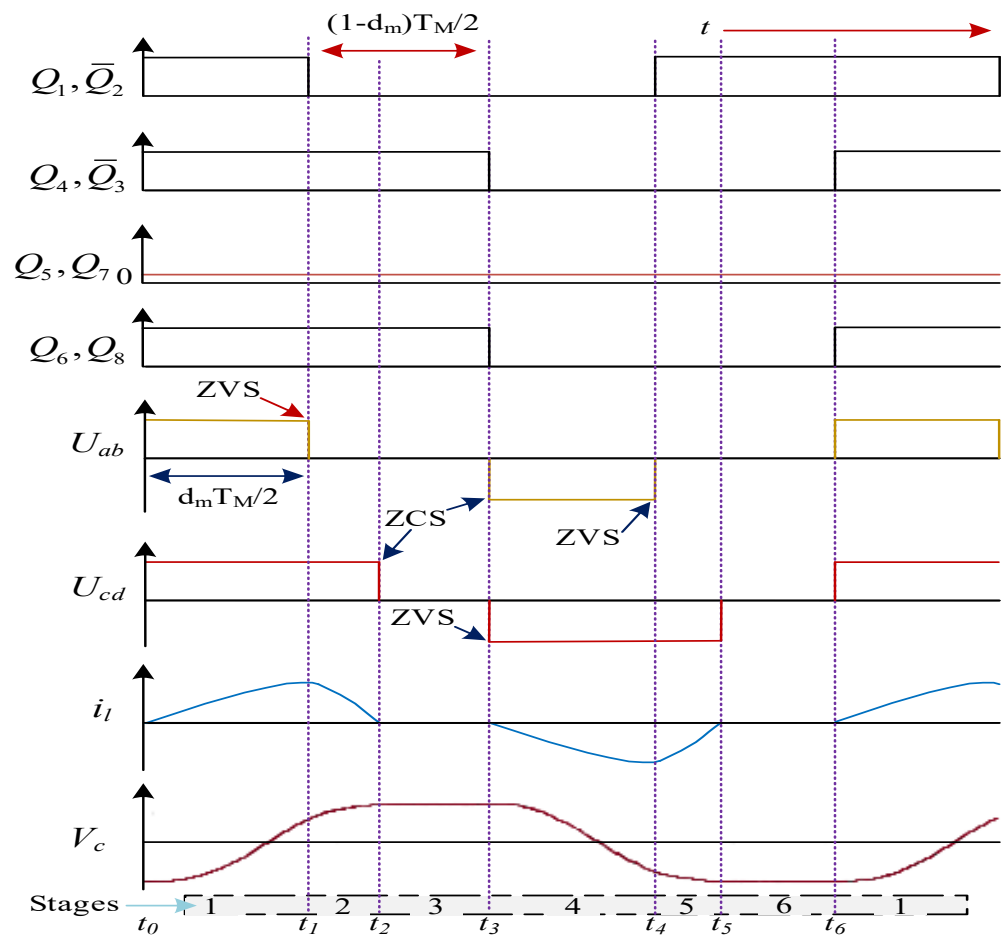


Figure 2. Suggested converter waveforms under FFM.

The amplitude of the output current is controlled by the phase shift at the input side of the converter. The MOSFETs of the full bridge will always work in a complementary manner. In Figure 2, the term $1 - d_m$ represents the phase shift ratio between any two complementary switches working at the same instant, where d_m is the duty ratio of the output voltage U_{ab} of the input side full bridge. The proposed SRC works into six stages, where stages three and six are named $t_3 = T_M/2$ and $t_6 = T_M$. These two stages make up half of the operational waveform. Furthermore, stage one and stage four shared similar time interludes and were given as $t_4 = t_1 + T_M/2$. Likewise, the time breaks of stage two and stage five are equal and are represented as $t_5 = t_2 + T_M/2$.

The current i_l of the tank circuit in stage one and stage two is above zero due to which the tank voltage V_c starts raising. In contrast, the i_l in stage four and stage five is below zero, and therefore the voltage V_c starts falling. Moreover, the tank voltage will remain unchanged in stage three and stage six as the i_l stays at zero in these two stages. For ease, the secondary side voltage (V_o) is transformed into the primary side voltage (V'_o) by dividing it by the turns ratio (n) of the HFT as given in Equation (3).

$$V'_o = \frac{V_o}{n} \tag{3}$$

There will be no energy transfer from input to output ends of the converter if ($V_i > V'_o$) is not followed. Additionally, the switches Q_5 and Q_7 will block the backflow of current, and therefore no power will conduct until V_i becomes greater than V'_o . Here, it is presumed that the DC-link capacitances at input and output ends are sufficient enough, hence the voltages V_i and V_o are considered constant during the working of converter. The operational waveforms of the respective stages are given in Figure 2.

3. Operation Modes of the Proposed Converter

The working stages of the suggested LC-DAB series resonant converter are explained in detail in Figure 3. It operates in six stages. Originally, there is no path for current to stream, therefore no inductor current i_l will flow as expressed in Equation (4).

$$i_l(t_0) = 0 \tag{4}$$

Similarly, the voltage V_c remains at the lowermost position as given in Equation (5).

$$V_c(t_0) = -\Delta V_c \tag{5}$$

The primary and secondary sides are detached. Therefore, no power will be transformed between the full bridge and CT-bridge.

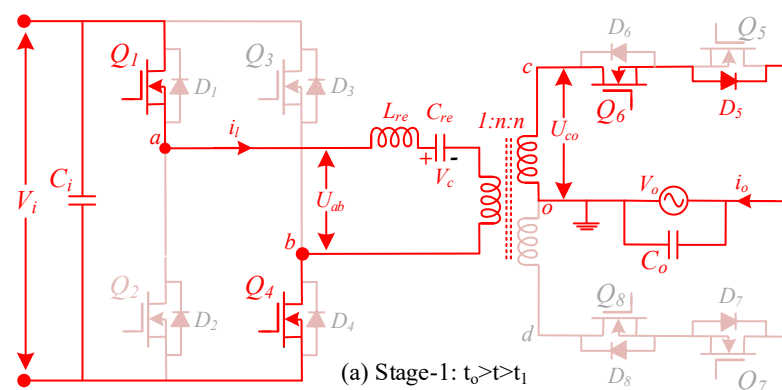


Figure 3. Cont.

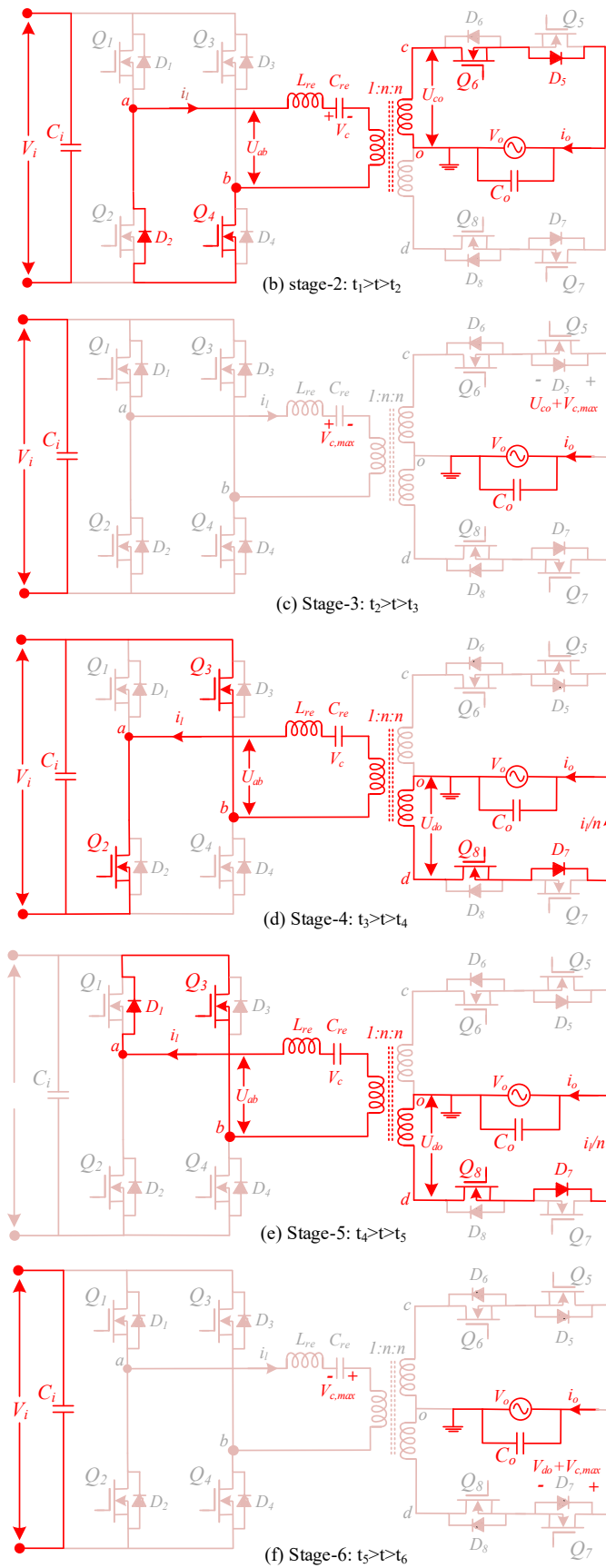


Figure 3. Working stages of proposed converter ($V_o > 0$).

3.1. Stage 1

The switches Q_1, Q_4 of the input side and Q_6 of the CT-bridge with antiparallel diode D_5 start conducting on ZCS in this stage [$t_0 < t < t_1$], as shown in Figure 3a. The total voltage in the resonant circuit at this point is equal to $V_i - V'_o$. The i_l begins to grow up gradually and reaches its highest point as given in Equation (6).

$$L_{re} \frac{di_l}{dt} = V_i(t) + V_c(t) - V_o(t) \tag{6}$$

Moreover, within the limits of [$0 \leq t \leq t_1$], the voltage V_c is discharged to zero, as stated in Equation (7). In this stage, the output end MOSFET Q_6 is successively conducting at the line frequency.

$$C_{re} \cdot V_c(t) = \int_0^t i_l(t) + V_c(t) \tag{7}$$

3.2. Stage 2

In this mode [$t_1 < t < t_2$], Q_1 is turned off and the switch Q_2 is turned on at ZVS, as shown in Figure 3b. At the output end, the switch Q_6 and the diode D_5 remain in working mode just as in stage 1. Moreover, at time t_2 , the negative tank current i_l will reach zero level and the tank voltage will touch its highest point. The switch Q_3 will not conduct until and unless switch Q_2 releases all its energy via D_2 . The tank current i_{l1} at t_1 is achieved by using Equation (8).

$$i_{l1} = (H + V_c) \sqrt{\frac{L_{re}}{C_{re}}} \sin(\omega_{re} t_1) \tag{8}$$

where, $H = V_0 - V_i$; the reductions of i_l to zero level is given by Equation (9).

$$i_{l2} = i_{l1} \cos(\omega_{re} t_2) + (H_1 - V_c(t_2)) \sqrt{\frac{C_{re}}{L_{re}}} \sin(\omega_{re} t_2) \tag{9}$$

where, $H_1 = -V_0$; furthermore, the resonant capacitor of the tank C_{re} reaches it maximum voltage and is shown in Equation (10).

$$V_c(t_2) = V_c(t_1) + \frac{w - x - y + z}{\omega_{re} C_{re}} \tag{10}$$

where, $w = i_{l1} \sin(\omega_{re} t_1)$, $x = i_{l1} \sin(\omega_{re} t_2)$, $y = (H_1 - V_c(t_1)) \sqrt{\frac{C_{re}}{L_{re}}} \cos(\omega_{re} t_2)$, and $z = (H_1 - V_c(t_1)) \sqrt{\frac{C_{re}}{L_{re}}}$.

The term t_2 can be calculated by employing Equation (11).

$$t_2 = \frac{\frac{\pi}{2} - \cos^{-1}(\sin \omega_{re} t_1)}{\omega_{re}} + t_1 \tag{11}$$

The duty ratio of input side H-bridge is stated in Equation (12).

$$d_m = \frac{2t_1}{T_M} \tag{12}$$

3.3. Stage 3

In this interval, the current i_l stays at zero level in the tank circuit and hence the diode D_5 stops conducting. The time interval of this stage is [$t_2 < t < t_3$], as shown in Figure 3c. The switch Q_5 at the output end will prevent the current from flowing in the reverse direction. Here, the voltage across Q_5 is equal to [$V_{cmax} + V_o$]. This stage is called zero current stage because it guarantees the moment of current in one direction (i.e., towards the secondary

end) and consequently the next stage starts with the current level at zero. Furthermore, no change in the tank voltage and current is recognized and this explains why both stay at the same level in this stage.

3.4. Stage 4

During this mode [$t_3 < t < t_4$], the other switches Q_2 , Q_3 and Q_8 start working with D_7 at ZCS, as shown in Figure 3d. This sequence generates a negative U_{ab} at the output of the full bridge. At this point, the tank voltage V_c starts decreasing from its highest level, which is equal to $(V'_o - V_i)$, and the tank current i_l moves towards the negative plane. Both the parameters of the LC tank are opposite to each other, as discussed in stage 1.

3.5. Stage 5

In this stage [$t_4 < t < t_5$], due to the backflow of current the switch Q_1 begins to conduct (i.e., at ZVS), as shown in Figure 3e. Moreover, at time t_4 , Q_2 is turned off and the capacitor voltage V_c in the tank is equal to V'_o . The tank current i_l is increased again to zero and the tank voltage is increased back to its highest point, V_{cmax} .

3.6. Stage 6

This interval [$t_5 < t < t_6$] is the same as stage 3, as shown in Figure 3f. In this stage, due to the zero level of tank current, the diode D_8 stops conducting naturally. The current in the LC circuit stays at zero until the next mode starts. Moreover, the negative voltage [$nV_{cmax} + V_o$] is blocked by the switch Q_7 . This mode remains until the new cycle begins at $1/f_M$.

4. Design of the Closed Loop Current Control

This part implements a closed loop current control for the suggested SRC, as shown in Figure 4. Through the utilization of the closed loop, the current reference i_{rf} has been successfully tracked. The transfer function of the controller is denoted by the symbol $G_p(s)$ in Figure 4, and the transfer function of the converter is shown by the symbol $G_i(s)$. The value of the i_{rf} is decided upon in accordance with the power rating of the converter during the process of forming the control loop. The output of the converter is used as feedback at a reference point, and a proportional-integral (PI) regulator is utilized in order to achieve the desired level of compensation.

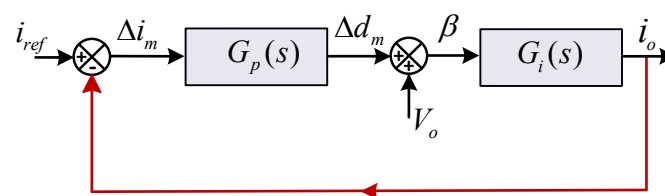


Figure 4. Diagram of closed loop current control for proposed converter.

The PI controller eliminates the error from the signal and produces a measured current signal. The measured signal is added to the feed-forward loop to produce a firing angle β , which is specified in Equation (13). A modulated input for the switches is produced, which is transformed in the form of β and individual gating PWM signals are produced. These gating signals are applied to the input and output side switches accordingly.

$$\beta = \cos^{-1}\left(\frac{V_o}{V_i}\right) \quad (13)$$

The voltage gain k of the open loop varies with the firing angle under a resistive load. The value of k is calculated by using Equation (14). In contrast, the total time-constant (τ) is estimated with the central time-constant as the modulation frequency has a very small time

period compared to the central time-constant. Furthermore, the capacitor at the output end has a more significant impact on the central time constant, as specified in Equation (15).

$$k = \frac{\Delta i_m}{\Delta d_m} = \frac{\frac{2\pi}{n} V_i i'_o (V_i - V'_o + i'_o / 8\pi C_{re} \sqrt{L_{re} C_{re}})}{V'_o (2V'_o - V_i - V_i \cos \omega_{re} t_{re})} \tag{14}$$

$$\tau = \frac{n^2 V'_o C_o}{i'_o} \tag{15}$$

The values of the PI regulators parameters are selected according to the highest attainable gain, so that the proposed SRC can provide sensible performance and remain in a stable state. Hence, the appropriate transfer function for the PI controller can be stated as:

$$G_p(s) = k_i \frac{1 + T_i}{s T_i} \tag{16}$$

with the limits, $k_i = \frac{1}{k_{max}}, T_i = \tau$.

5. Converter Power Losses

In converters, conduction and switching losses contribute the most losses in the network. In this portion, the proposed SRC is compared with the traditional converters [15,16,22]. The parameters of MOSFETs for calculating switching losses are listed in its datasheet [34].

5.1. Conduction Losses Calculation

The resistance and RMS value of the current describe the conduction losses. The output waveform of the system is symmetrical and therefore, in the steady state the RMS value can be considered as the RMS value of the current in the half cycle. By employing the equations of stage 2 (i.e., Equations (7), (11) and (12)) for the initial half cycle, the RMS current for the proposed SRC under FFM can be achieved, as indicated in Equation (17).

$$I_{RMS,M} = \sqrt{\frac{2}{T_M} \left(\int_0^{t_{1,M}} i_{re}^2 dt + \int_{t_{1,M}}^{t_{2,M}} i_{re}^2 dt + 0 \right)} \tag{17}$$

There are three terms in the RMS current shown in Equation (17), in which the first term is from stage 1, the second term is from stage 2 and the third term is from stage 3. The conduction losses in the proposed SRC based on FFM is nearly the same as the conventional LC-DAB topology, as shown in Figure 5. The losses in the proposed topology mostly occurred when the current reached DCM. In the same way, Figure 5 demonstrates that the conduction losses for existing topology rise marginally with a rise in output voltage.

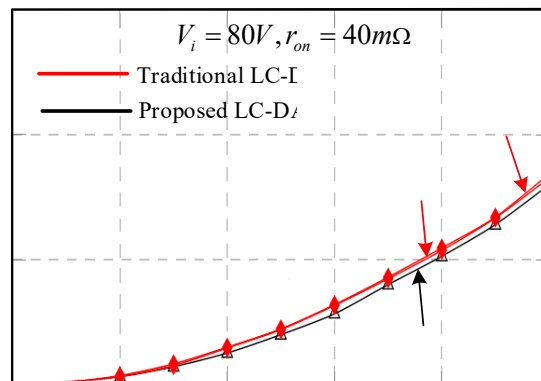


Figure 5. Conduction losses waveforms of two LC-DAB converters.

5.2. Switching Losses Calculation

The other losses, which affect the system efficiency, are switching losses. The conventional converter contains two modes of hard switching and two ZVS stages in each sequence, which leads to a high extent of switching losses. On the other hand, the proposed topology under the FFM technique provides soft switching on the entire load range. The leading limb (Q_1 and Q_2) in the full bridge operates under ZVS or ZCS and therefore the snubber circuit is only used for the rated operation current. In contrast, the lagging limbs in the full bridge (Q_3 and Q_4) are frequently turned on and off at zero current and therefore required no snubber circuitry [29]. Moreover, the CT-bridge switches achieve ZCS in every cycle and hence do not require a snubber circuit. Although the switching losses are greatly reduced by using the soft-switching technique, some losses still occurred in the switching process of the converter. These losses are measured approximately by employing the current and voltage equations given in [28]. The current at the switching time I_{sp} is shown in Equation (18).

$$I_{sp,M} = i(t_{1,M}) = (E + V_C) \sqrt{\frac{L_{re}}{C_{re}}} (\sin(\omega_{re} t_{1,M})) \quad (18)$$

The total losses produced by the switching pattern under the proposed modulation are specified in Equation (19), where t_{ri} denotes the rising time.

$$P_{sp,M} = V_i I_{sp,M} t_{ri} \frac{2}{T_M} \quad (19)$$

The diagram for switching losses is presented in Figure 6, in which the losses for the proposed converter under FFM are lower than those of the traditional LC-DAB converter. The curves shown in the figure for the proposed converter at two different output voltage values are close to each other with a small gap at higher current values. Whereas in the existing LC-DAB topology, the switching losses increased intensely for lower output values due to a hard switching pattern. In addition, the gap between the two curves is significantly wider at higher current values for the existing LC-DAB converter.

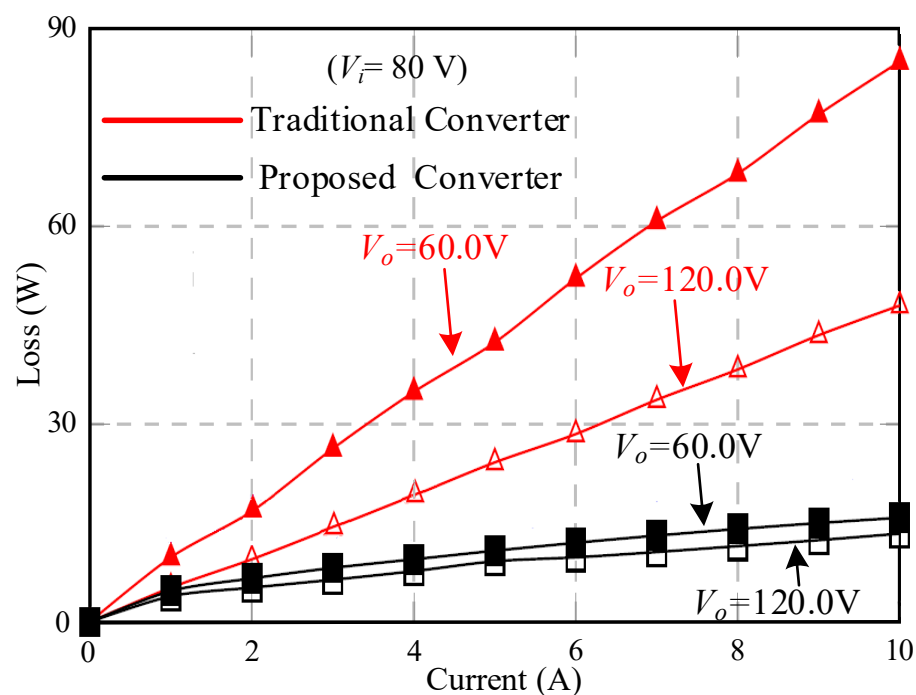


Figure 6. Switching losses waveforms of two LC-DAB converters.

5.3. Efficiency

The total losses for the ideal inductor and transformer are equivalent to the amount of conduction and switching losses present in a system, as illustrated in the efficiency curves in Figure 7. The switching losses added generally in lighter loads, while the conduction losses control the total losses in heavier loads. The proposed topology under the FFM scheme displays improved performance in the case of both heavier and lighter loads. Moreover, the efficiency of the system shows that with a rise in the output voltage, the operative region of the proposed converter is also prolonged. In contrast, the operative range of the existing LC-DAB is tightened due to high extent of switching losses, which leads to decreasing efficiency. The distribution of the power increases with a rise in output voltage and therefore the efficiency of both the topologies increases. For 60 V (output voltage), the proposed topology gives over 91% efficiency, whereas the existing topology offers less than 85% efficiency. Moreover, for 120 V (output voltage), both topologies offer above 95% efficiency in most of the current ratings.

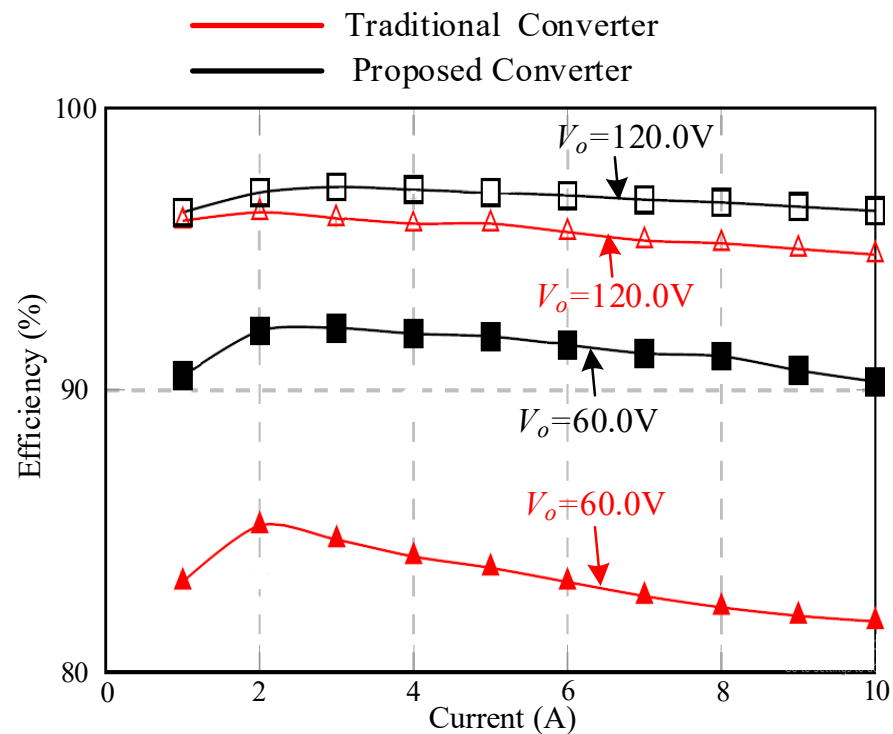


Figure 7. Efficiency waveforms of the two LC-DAB Converters.

6. Simulation Results

In this part, a Simulink model of the suggested converter was constructed in a MATLAB environment. The model is supposed to be an ideal, where the parasitic resistance is ignored. The results obtained from simulation determine the correctness of the theoretical idea, including blocking of reverse current, calculation of duty cycle and pattern of the gate signal. The tank inductor current i_l and voltage across the capacitor V_c waveforms at 98% duty ratio are shown in Figure 8. The zoom-in plots of the i_l having three levels are presented in Figure 9b, where the harmonics content is mitigated in i_l and this is achieved by using the capacitor in the tank circuit, as shown in Figure 9a. In Figure 9b, the charging and discharging of i_l can be observed, which happens according to the boundary conditions discussed in Section 2.

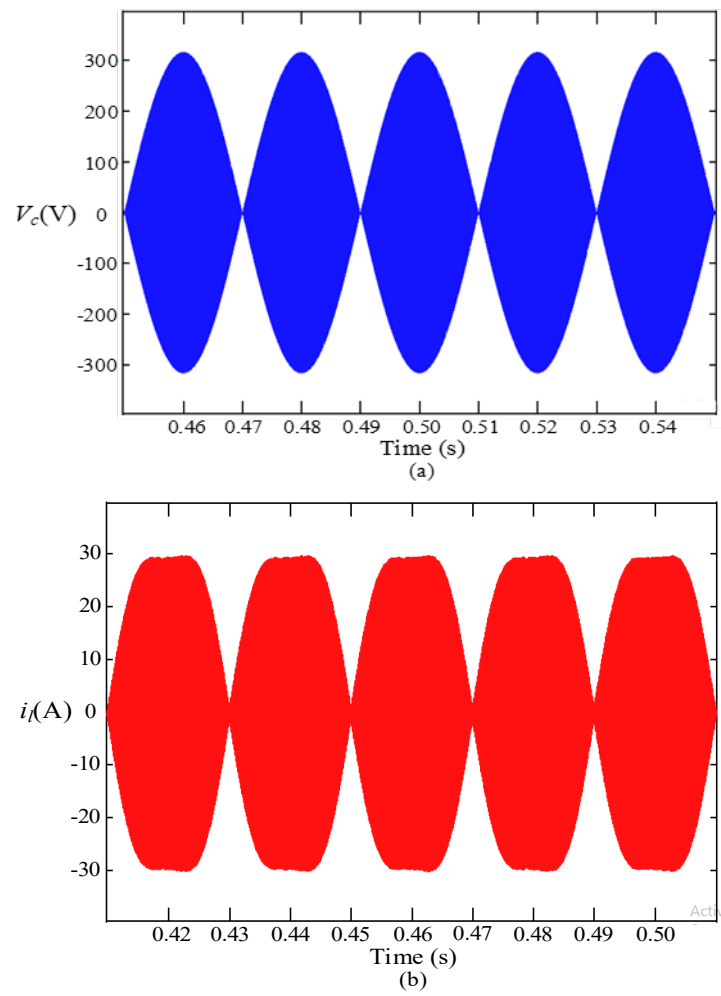


Figure 8. Simulation results (a) Resonant capacitor voltage V_c and (b) Resonant inductor current i_l .

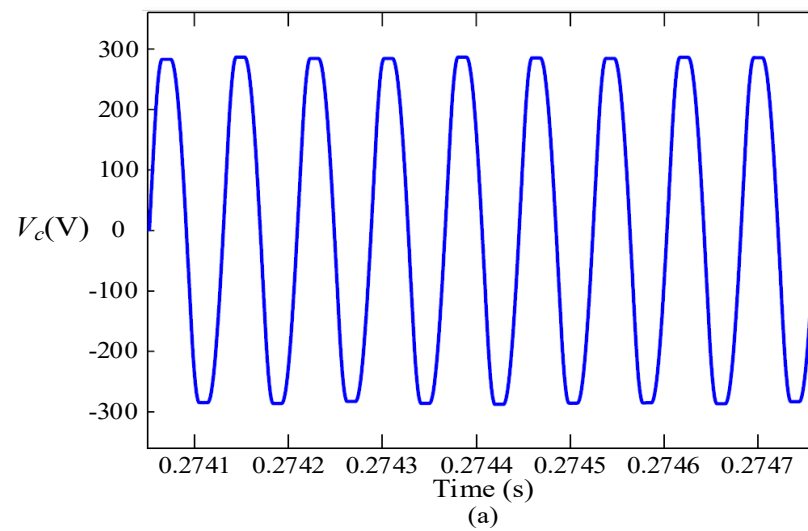


Figure 9. Cont.

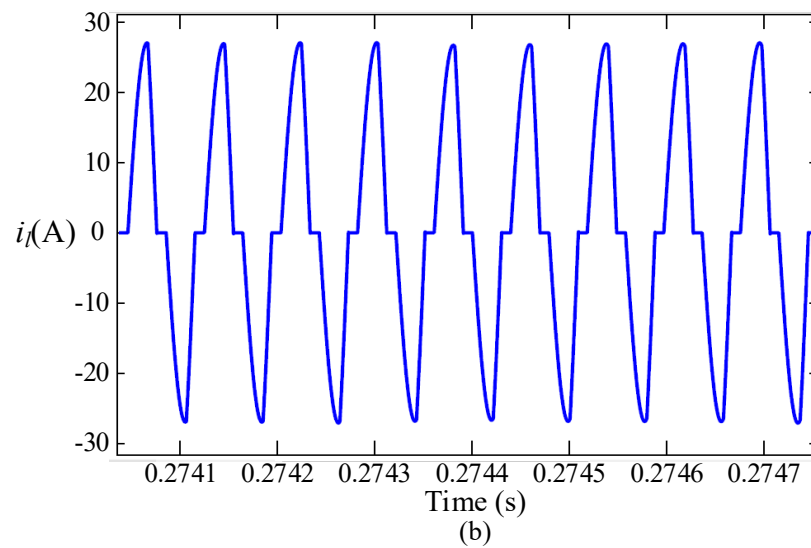


Figure 9. Zoom-in waveforms of (a) resonant capacitor voltage V_c and (b) resonant inductor current i_l .

The waveforms of the output voltage of the full bridge U_{ab} , inductor current i_l , and capacitor voltage V_c across the tank are presented at 0.15 duty cycle ($V_i = 80$ V and $V_o = 50$ V) in Figure 10. The duty cycle is raised to 0.7 ($V_o = 160$ V) in Figure 11. In both figures, the current returns and stays at zero until the beginning of a new switching mode, which operates in discontinuous conduction mode (DCM). The results support the precise anticipation of current and voltage in Sections 2 and 3, whereas the boundary conditions are achieved at the derived turns ratio and the resonance frequency. In both cases, the output current i_o is fixed at Figure 9a.

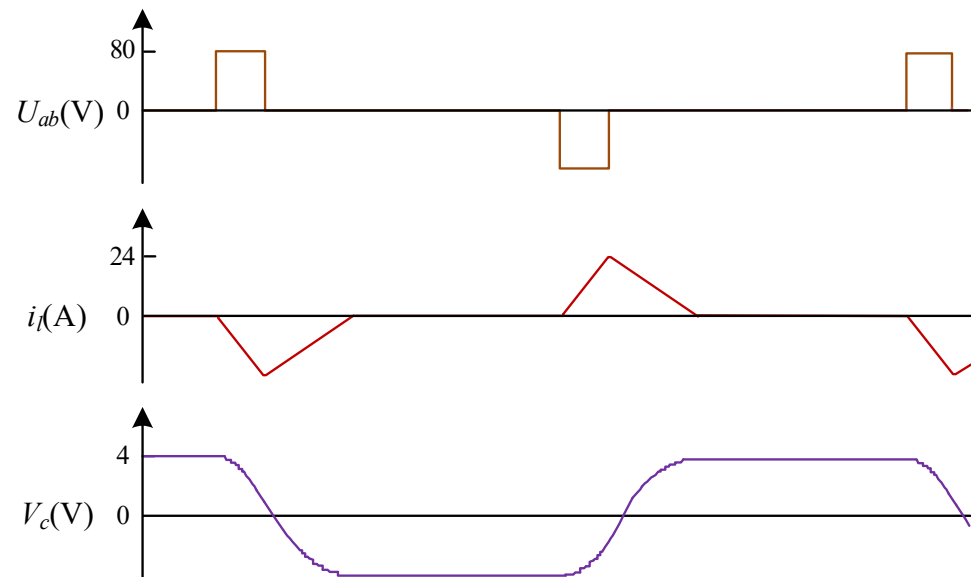


Figure 10. Simulation results at 15% duty ratio.

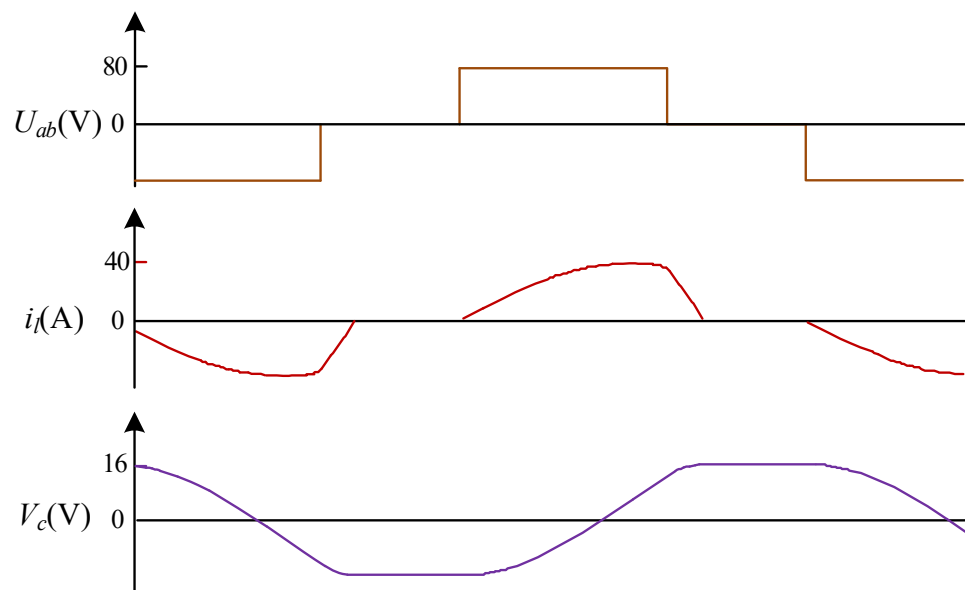


Figure 11. Simulation results at 60% duty ratio.

7. Experimental Results

In this part, a 1.5 kW laboratory prototype was designed and tested to determine the feasibility and efficacy of the proposed converter and modulation technique. Generally, the prototype is printed on PCB, which includes MOSFET (IRPF4668, 200 V) on the primary side and MOSFET (IPW60R045CPA, 600 V) on the secondary side, opt coupler IC (HCPL2232), DC/DC converter (24 V–15 V), IC (tpsw2812), IC (UCC27712-Q1) and electronic components consist of diodes, resistor, and capacitor, and their values are presented in Table 3. Moreover, a ferrite core inductor (EE70/68/19) and a ferrite core CTT (PC40 EE70) were used. The experimental setup diagram of the proposed converter is shown in Figure 12. Besides, Figure 12a shows the initial setup of the converter in the lab and Figure 12b presents the final setup of the proposed converter.

Table 3. Parameter of the Proposed Converter.

| Parameters | Representation | Values (Unit) |
|------------------------------|----------------|-------------------------|
| Input side voltage | V_i | 80.0 (V) |
| Tank inductor | L_{re} | 160.0 (μH) |
| Maximum Output voltage | $V_{o,max}$ | 160.0 (V) |
| Tank capacitor | C_{re} | 1.0 (μF) |
| Output side filter capacitor | C_o | 20.0 (μF) |
| Turn ratios | n | 1:2.2:2.2 |
| Regulator Parameters | k | 0.800 |
| (PI-controller) | t | 0.000250 |

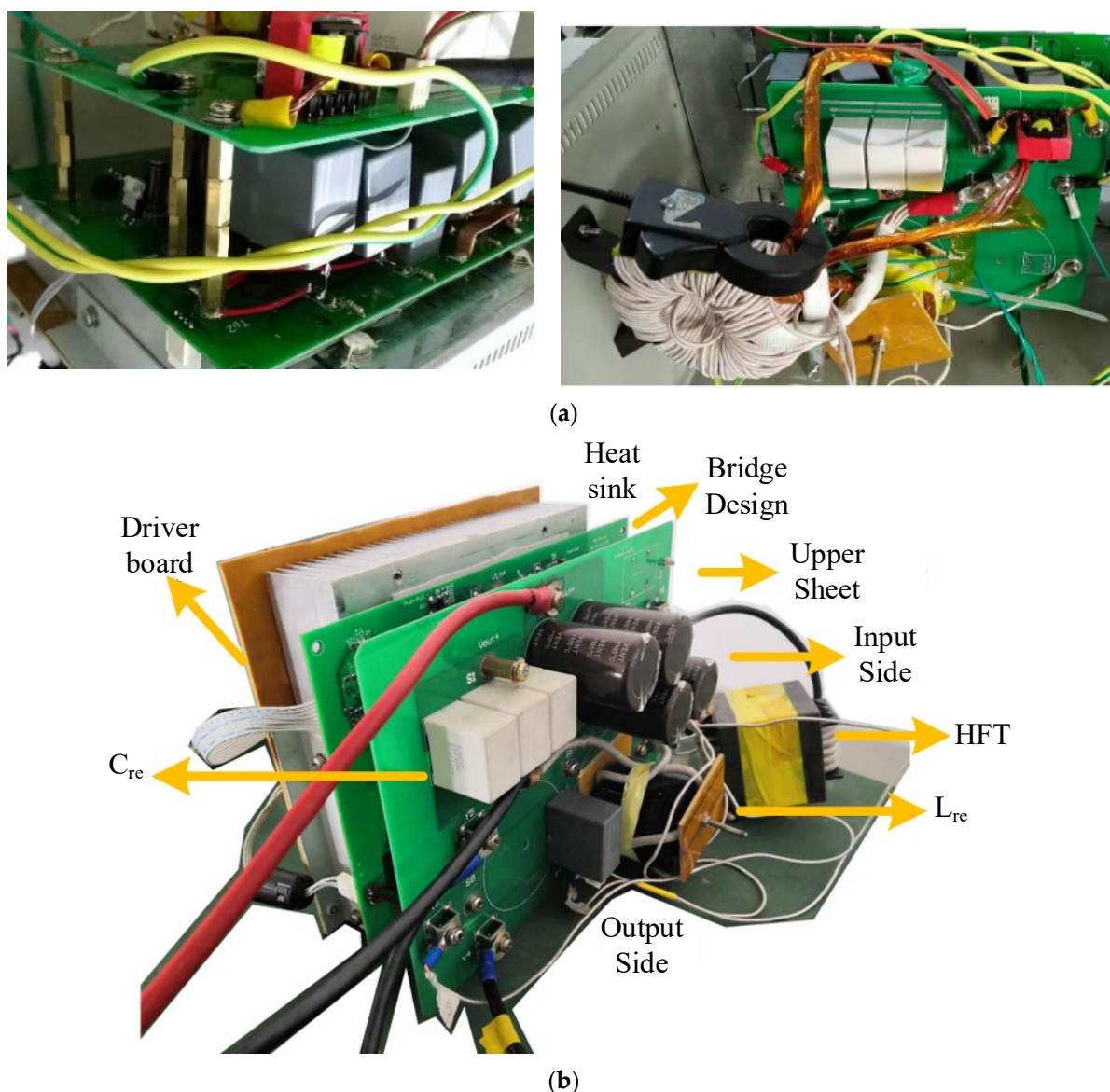


Figure 12. Experimental setup up of the proposed converter (a) Initial designs for the proposed converter in the lab and (b) Laboratory setup of proposed converter.

Each switch pair was set to a dead time of $2 \mu\text{s}$. The DSP kit was used for controller coding and the FPGA kit was employed to produce modulation signals. The control board was mounted on the opposite end of the heatsink to reduce the effect of electromagnetic waves. The ADC on DSP calculates the input voltage, output current, and output voltage. Figure 13 displays the operation of the proposed topology for various duty ratios. Initially, the duty cycle was set to 0.1 in Figure 13a, where the tank circuit acts more as an L tank due to small current and less contribution of capacitor voltage. In the prototype, the LC tank behavior depicted when the tank voltage reached 0.6 of the input side voltage. With increasing tank voltage, the dipping time of the waveform also reduces. The duty ratios in Figure 13b,c, are beyond 0.6. In these two cases, the resonance time never surpasses 0.5 of the total duration. Furthermore, a pair of ZVS and ZCS for turned-on condition of the switch in each cycle for the proposed converter under the proposed modulation scheme can be noticed in Figure 13.

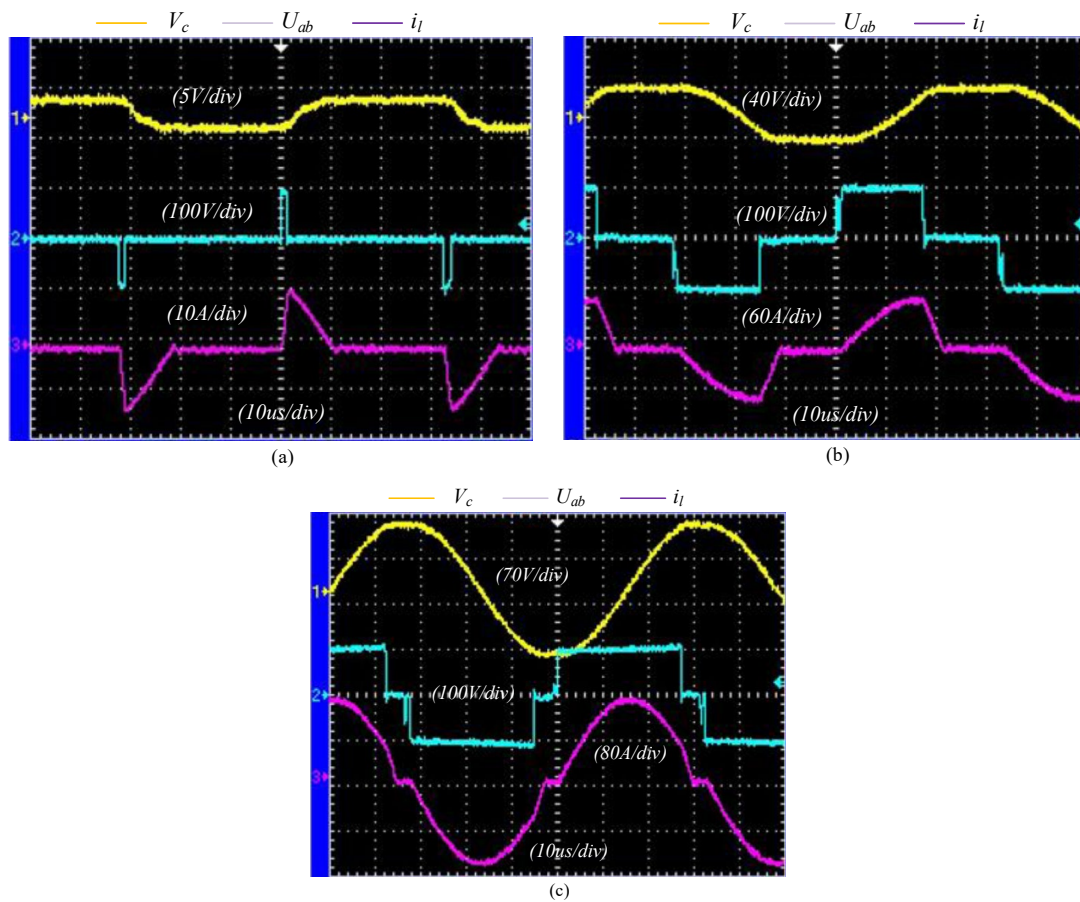


Figure 13. Experimental outcomes at duty ratios (a) 0.10 (b) 0.70 and (c) 0.9.

The power was measured at the input and output ends by employing a DC meter. The efficiency curve achieved from the experiment is compared with the theoretical curve, as presented in Figure 14. The curves are close to each other at heavier loads, however a small gap can be noticed at smaller and medium powers. This gap may occur due to the aging of MOSFETs and inner resistance of passive components, which were excluded in the theoretical scheme. However, the gap between the output curves is not significant enough and therefore confirms the exactness of the suggested topology.

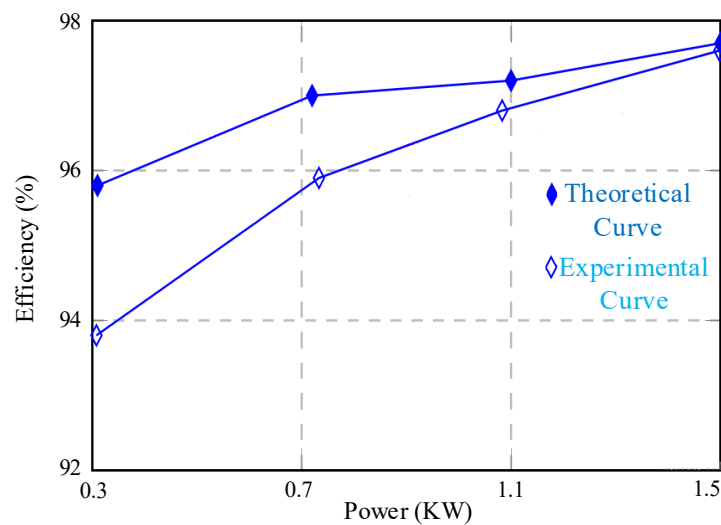


Figure 14. Comparison of Power Efficiencies ($V_{in} = 60\text{ V}$, $V_s = 120\text{ V}$).

8. Conclusions

In this paper, an FFM modulation-based soft-switched isolated SRC has been proposed. The proposed converter has the capability to prevent reverse power flow in order to decrease conduction losses and enhance converter efficiency. Moreover, with the implementation of the FFM in DCM, the performance of the converter is considerably improved due to reduced power losses, as the switching losses are minimized with the help of soft switching, and the conduction losses are reduced by blocking the reverse current. The proposed converter has fewer passive components in the resonant tank than other resonant DAB topologies, making it easier to reduce size and obtain higher power densities. Capacitor use in the resonant tank of the proposed converter can assist in minimizing inductor and transformer saturation, which is one of the key concerns for converter topologies. Further, with this topology, zero impedance at resonance frequency is made possible, which is very desirable. Moreover, the performance of topology is further boosted by employing an advanced modulation technique. Besides, the experimental prototype has attained a high operational efficiency of about 97.6% by employing the proposed modulation scheme. Furthermore, the soft-switching method is identified and switching devices' protection is improved. The suggested control method and structure were simulated and verified using an experimental prototype of 1.5 kW.

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