Predicting SiC MOSFET Behaviour Under Hard-Switching, Soft-Switching and False Turn-On Conditions

Md Rishad Ahmed, Rebecca Todd, *Senior Member, IEEE*,
and Andrew J. Forsyth, *Senior Member, IEEE*

***Abstract*— Circuit level analytical models for hard-switching, soft-switching and dv/dt-induced false turn on of SiC MOSFETs and their experimental validation are described. The models include the high frequency parasitic components in the circuit and enable fast, accurate simulation of the switching behaviour using only datasheet parameters. To increase the accuracy of models, nonlinearities in the junction capacitances of the devices are incorporated by fitting their nonlinear curves to a simple equation. The numerical solutions of the analytical models provide more accurate prediction than a LTspice simulation with a threefold reduction in the simulation time. The analytical models are evaluated at 25°C and 125°C. The effect of snubber capacitors on the soft-switching waveforms is explained analytically and validated experimentally, which enables the techniques to be used to evaluate future soft-switching solutions. Finally, the dv/dt- induced false turn on conditions are predicted analytically and validated experimentally. It was observed that consideration of nonlinearities in the junction capacitances ensures accurate prediction of false turn on, and that the small shoot through current due to false turn on can increase the switching loss by 8% for an off state gate bias of -2V.**

***Index Terms*— SiC MOSFET switching analysis; switching losses; parasitic effect; soft-switching; dv/dt-induced false turn on, shoot-through current.**

I. INTRODUCTION

TRANSFORMING the device level advances of SiC technology (lower on-state losses, lower parasitic capacitances and potentially higher switching frequencies) into smaller and more efficient converters present numerous challenges. One of the challenges is understanding and optimising the more rapid switching waveforms, including predicting and managing parasitic oscillations, switching losses and electromagnetic interference (EMI).

To understand the SiC MOSFET static and dynamic behaviour, several modelling approaches have been proposed, including semiconductor physics models [1] and behavioural models [2-4]. Most of the models are complex or poorly incorporate the circuit parasitic components, and so produce inaccurate circuit waveforms. Although the behavioural Spice model of [2] has a detailed model of the nonlinear Miller capacitor, C_{gd}, it did not consider any parasitic inductance at the source or drain terminal. The model was extended in [3] considering the nonlinearity in all the device capacitances, however the approximation of drain to source capacitance, C_{ds}, during the switching transients was complex as it was considered to fall exponentially for gate-source voltages around the threshold level. Recently, another PSpice based behavioural model of a SiC MOSFET module was reported in [4] which included a model for the nonlinear Miller capacitor, C_{gd} dependent on the physical parameters of the MOSFET such as doping concentrations of the drift and JFET regions and the active chip area. The model also requires an estimation of the transition voltage near the knee point of the C_{gd}-V_{ds} curve to model C_{gd} accurately.

Analytical modelling of the switching transients can be a good approach to understand the switching behaviour of SiC MOSFETs [5]. The models can then be extended to incorporate circuit parasitics, soft-switching of the power devices and also false turn on conditions. One of the key objectives of this work is to develop an analytical model to evaluate the SiC MOSFET's full switching behaviour.

Although the analysis of dv/dt-induced false turn on has been widely examined for low voltage Si MOSFETs [6-8], very little has been published [9] for the SiC MOSFET. Opposing views are apparent in the published literature on Si MOSFETs with regard to the impact of common source inductance on the false turn on. [6, 7] suggest common source inductance reduces the chance of false turn on, whereas [8] suggests the opposite. [8] gives the most detailed analysis of a 80V Si MOSFET's false turn on by including almost all the parasitic components. However, the model did not consider the nonlinear characteristics of the device capacitances which are shown in this work to be critical for determining the dv/dt-induced false turn on of SiC MOSFETs. An experimental

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The authors are with the Power Conversion Group, School of Electrical and Electronic Engineering, The University of Manchester, Manchester M13 9PL, UK (e-mail: mdrishad.ahmed@manchester.ac.uk; rebecca.todd@manchester.ac.uk; andrew.forsyth@manchester.ac.uk)

analysis of temperature dependent losses associated with SiC MOSFET's false turn on was presented in [9] and compared with a Si IGBT. An analytical model was also introduced to predict only the gate to source voltage of the MOSFET and IGBT during false turn on, again considering only fixed device capacitances. However, the losses associated with the output capacitance of the devices were not quantified; these losses can be determined from the modelling approach presented in this paper.

In this paper, Section II presents a theoretical overview of three different SiC MOSFET switching circuits. The associated waveforms establish the basis of the analytical models explained in Sections III and IV, which also show how the models can be implemented in MATLAB. Section V verifies the modelling approach for hard-switching, soft-switching and dv/dt-induced false turn on conditions. Finally, Section VI draws conclusions.

II. Overview of SiC MOSFET switching

A. Hard-switching

To investigate hard-switching the double-pulse test (DPT) circuit is used, Fig. 1 (a). The diagram includes the main circuit parasitics such as the MOSFET common source inductance, L_s, drain inductance, L_d, gate lead inductance, L_g, parasitic capacitances of the MOSFET, C_{gs}, C_{gd} and C_{ds}, diode and load inductor lumped parasitic capacitance, C_{ak}, and the equivalent series resistance of the power loop, R_s. Fig. 1 (b) shows simplified turn on waveforms for the MOSFET, including drain to source voltage, V_{ds}, drain current, I_d, gate to source voltage, V_{gs}, Schottky diode voltage, V_{ak}, and the diode current, I_f.

V_{gs} increases during t_0-t_1 in an exponential manner as the gate current charges the MOSFET input capacitances, C_{gs} and C_{gd}. V_{gs} reaches the threshold level, V_{th} at t_1 and I_d starts to increase. At the same time, diode current, I_f also starts to fall from the load current level, I_{dd} and at time t_2, the current commutation between the diode and MOSFET finishes. During this sub-period, t_1-t_2, due to the voltage drop, V_{ls}, across L_d and L_s, V_{ds} reduces from the input DC voltage, V_{dd}.

At time t_2, V_{ds} starts to fall as the voltage starts to increase across the diode parasitic capacitor, C_{ak}. The MOSFET current I_d increases beyond the load current level due to the charging current of C_{ak} until V_{ak} reaches the level $V_{dd}-V_{ls}$ at time t_3. At this point, V_{ds} reaches its on-state voltage level, $V_{ds(on)}$.

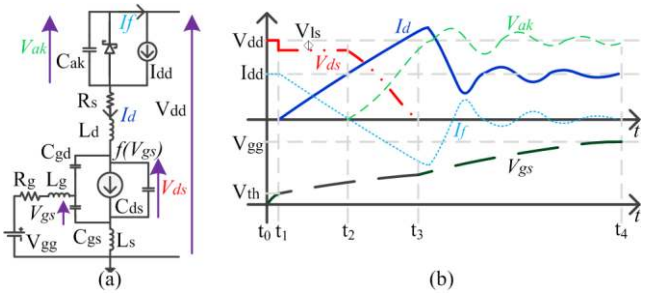


Fig. 1. (a) Equivalent circuit of DPT circuit during the active region of SiC MOSFET, (b) DPT circuit waveforms during turn on

After t_3, I_d rises slightly then starts to reduce as the energy in the stray inductances transfers to C_{ak} in a resonant manner. This resonance continues until all the resonating energy is dissipated by the stray resistance, R_s, of the circuit. Finally, the drain current is equal to the load current, I_{dd}, the diode voltage, V_{ak} becomes equal to the DC voltage, V_{dd}, and V_{gs} is equal to the gate supply voltage, V_{gg}. The switching transient at turn off follows a reverse process to that seen at turn on. The sub-intervals for turn off are the same as those at turn on but occur in the reverse order.

B. Soft-switching

To facilitate the soft-switching test, a different arrangement of the DPT circuit, shown in Fig. 2(a), was used where C1 and C2 are large voltage dividing capacitors. Two snubber capacitors, C_{s1} and C_{s2} are added across Q1 and Q2 to reduce the MOSFET turn off losses and control the dv/dt. The total capacitance across the devices is therefore the sum of the snubber capacitor and the device output capacitances. The capacitances are charged and discharged in a lossless manner as Q1 and Q2 turn off (Fig. 2(b)). During the turn off instant of the device under test (DUT), Q2, C_{s1} and C_{s2} slow down the voltage transient to reduce the turn off losses. Energy is stored in C_{s2} whilst C_{s1} is discharged. The energy stored by C_{s2} is recovered into the conversion process when Q1 turns off.

Fig. 3(a) shows the soft-switching circuit during the turn off of the DUT, Q2. Here I_{c1} and I_{c2} are the currents flowing through the snubber capacitors C_{s1} and C_{s2}, respectively. The turn off waveforms are shown in Fig 3 (b).

The gate to source voltage, V_{gs} decreases during t_0'-t_1' in an exponential manner as the gate current discharges the MOSFET input capacitances, C_{gs} and C_{gd}. V_{gs} reaches the Miller level, V_{mil} at t_1', V_{ds} starts to increase and I_d starts to decrease. Due to the snubber capacitors, V_{ds} increases gradually while I_d falls, reaching zero at t_2' as V_{gs} reaches its threshold level, V_{th}. In this sub-period I_{dd} commutates to the snubber capacitors.

During the sub-period t_2'-t_3' I_{dd} is shared equally by the two snubber branches. Due to the parasitic inductance in the current paths, both I_{c1} and I_{c2} will be oscillatory. Towards the end of the t_2'-t_3' sub-period V_{ds} will reach V_{dd} and the upper device will start to conduct (I_{d1}) terminating the snubber branch currents. After t_3', the circuit capacitances and inductances will continue to resonate until a steady state is reached when the upper device current, I_{d1} equals the load current, I_{dd}, I_{c1} and I_{c2} become zero, and V_{gs} equals the negative bias level of V_{ggl}.

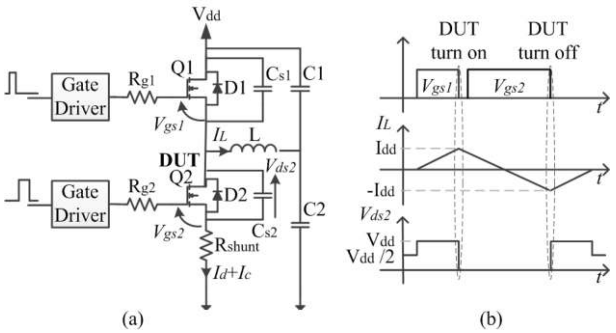


Fig. 2. (a) Test circuit for soft-switching (b) Ideal circuit waveforms

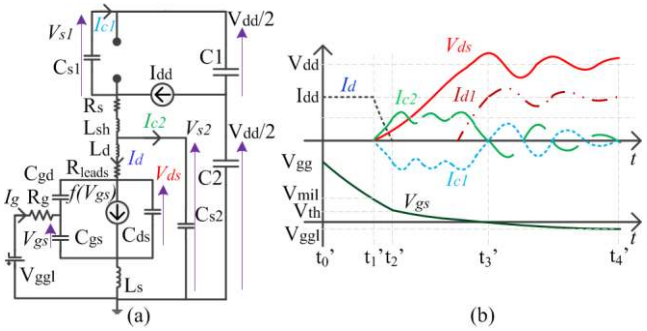


Fig. 3. (a) Soft-switching circuit during the active region of SiC MOSFET Q2, (b) circuit waveforms during turn off

C. dv/dt-induced false turn on

To investigate the dv/dt-induced false turn on, the DPT circuit in Section II.B was used with some minor modifications. In Fig. 2, the inductor, L, was connected to the ground, the snubber capacitors were removed and the DUT was held off by setting a negative gate bias on Q2. A single pulse was applied to the gate of Q1 and as the device turned on a high dv/dt was imposed across Q2 which created a displacement current through the output capacitors of Q2. Depending on the speed at which Q1 turns on, the gate resistance of Q2, R_{g2}, the negative gate bias, V_{ggl}, and the stray inductances associated with Q2, a false turn on of Q2 could happen if the induced gate to source voltage, V_{gs2}, exceeds the threshold level. The presence of the load inductor ensures that the initial voltage across Q2 is zero, however the inductor current remains virtually zero due to its large inductance (460 µH) and the component is neglected in the analysis. It was assumed that the effect of inductor current on the dv/dt is negligible compared with the effect of gate resistances and device capacitances and the validity of this assumption was confirmed by the experimental measurements in Section V. Also the current sensed at the source of Q2 by the shunt resistance, R_{shunt}, will include the displacement current through the output capacitor of Q2 and its channel current if false turn on happens.

The false turn on process is explained in Fig. 4 using the equivalent circuit in Fig. 4 (a). During t_0''-t_1'', Q1 remains turned off as $V_{gs} < V_{th}$. At t_1'', the current starts to flow in the channel of Q1 as well as in the drain of Q2 (I_d) while the output capacitance of Q1 discharges and the output capacitance of Q2 is charged. The induced voltage across L_{s2} initially reduces V_{gs2}, but V_{gs2} then increases due to the Miller current flowing through R_{g2}. If V_{gs2} crosses the threshold level, Q2 turns on and I_d increases. At t_2'', Q1 becomes fully on and V_{ds2} reaches the DC voltage, V_{dd}, and the dv/dt across Q2 starts to decrease. During the rest of sub-period t_2''-t_3'' V_{gs2} gradually decreases to V_{ggl} while the oscillations in V_{ds2} and I_d are damped by the resistance of the circuit, R_s.

III. Modelling of SiC MOSFET Hard-Switching Transients

Modelling the SiC MOSFET turn on and turn off transients requires the solution of four equivalent circuits corresponding to the four distinct stages of each transient. The modelling

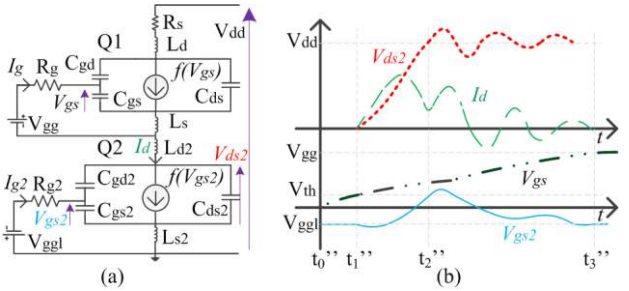


Fig. 4. (a) Equivalent circuit of the DPT during false turn on of Q2 while Q1 turns on, (b) DPT waveforms

approach is similar to the published Si-MOSFET analytical models [10, 11], but the difference is the incorporation of the major circuit parasitic components in all of the transient stages. Also no assumptions are used in the model to predict the voltage transitions between the equivalent circuits. The 'ode45' differential equation solver was used in MATLAB to solve the state equations for each sub-period. The final values from one sub-period form the initial conditions for the next sub-period.

The equivalent circuits for the turn on and turn off transient states are shown in Fig. 5. Here, L_d is the sum of the inductances of the MOSFET drain lead, L_{drain}, PCB current paths, L_{pcb}, diode leads, L_{lead}, and current shunt resistor, L_{shunt}. Four state variables, V_{gs}, V_{ds}, I_d and $\dot{I}_d$ (rate of change of drain current), were considered and were solved using four state space equations. A step gate pulse from V_{ggl} to V_{gg} was used to initiate the turn on transient. The other two inputs were the supply voltage, V_{dd} and load current, I_{dd}. The four sub-periods during the turn on transient correspond to (i) turn on delay, (ii) drain current rise, (iii) drain to source voltage fall and (iv) ringing stages. The gate inductance, L_g was neglected because it is small (around one fourth) compared with the power loop inductance, L_d+L_s, and the validity of this assumption was confirmed by the experimental measurements in Section V.

A. Turn on model

A step gate pulse from V_{ggl} to V_{gg} initiates turn on which drives the solution of the turn on transient model ($V_{ggl} < 0$).

Sub-period 1: (t_0- t_1) (turn on delay)

After the gate pulse is applied, the gate current charges the MOSFET input capacitors C_{gs} and C_{gd}. The MOSFET stays off until V_{gs} reaches V_{th} and the load current, I_{dd} circulates through the Schottky diode. The drain current is zero and the drain to source voltage is equal to the DC link voltage, V_{dd} in this sub-period. From equations (1)-(3) the state equations (4)-(5) for this sub-period can be found where, $I_d = 0$ and $C_{iss} = C_{gs} + C_{gd}$. After solving state equations (4)-(5) in MATLAB using $V_{g\_in}=V_{gg}$ and the initial conditions, $V_{gs}(0) = V_{ggl}$ and $I_g(0) = 0$, V_{gs} and I_g for this sub-period can be found. The turn on delay, t_1–t_0, is the time required for V_{gs} to reach V_{th} from V_{ggl}.

$$R_g I_g = V_{g\_in} - V_{gs} - L_s \frac{dI_d}{dt} - L_s \frac{dI_g}{dt} \quad (1)$$

$$I_g = C_{gs} \frac{dV_{gs}}{dt} + C_{gd} \frac{dV_{gd}}{dt} \quad (2)$$

$$V_{gs} = V_{gd} + V_{ds} \tag{3}$$

$$\frac{dV_{gs}}{dt} = \frac{I_g}{\mathrm{C_{iss}}} \tag{4}$$

$$\frac{dI_g}{dt} = -\frac{V_{gs}}{\mathrm{L_s}} - \frac{\mathrm{R_g}\, I_g}{\mathrm{L_s}} + \frac{\mathrm{V_{g\_in}}}{\mathrm{L_s}} \tag{5}$$

Sub-period 2: (t_1- t_2) (current rise time)

The current commutation between the diode and MOSFET happens in this stage. As the MOSFET is in the saturation region its channel current will be directly proportional to (V_{gs} − $\mathrm{V_{th}}$). V_{ds} decreases in this stage because of the *di/dt* induced voltages across $\mathrm{L_s}$ and $\mathrm{L_d}$ as shown in (6).

$$V_{ds} = \mathrm{V_{dd}} - (\mathrm{L_s} + \mathrm{L_d})\frac{dI_d}{dt} - \mathrm{R_s} I_d \tag{6}$$

The drain current can be found by combining the channel current with the MOSFET output capacitance current as shown in (7) where $\mathrm{C_{oss}} = \mathrm{C_{ds}} + \mathrm{C_{gd}}$.

$$I_d = \mathrm{g_m}(V_{gs} - \mathrm{V_{th}}) + \mathrm{C_{oss}}\frac{dV_{ds}}{dt} \tag{7}$$

To simplify the model the impact of the gate current, I_g, on the common source inductance, $\mathrm{L_s}$ was neglected assuming I_g is much smaller than the drain current, I_d.

$$\mathrm{R_g} I_g = \mathrm{V_{g\_in}} - V_{gs} - \mathrm{L_s}\frac{dI_d}{dt} \tag{8}$$

The state equations (A1) for this sub-period are derived using (2)-(3) and (6)-(8) and are shown in the Appendix. The current rise time, $t_2 - t_1$ is the time required for V_{gs} to reach $\mathrm{V_{mil}}$ from $\mathrm{V_{th}}$, where, $\mathrm{V_{mil}} = \mathrm{I_{dd}}/\mathrm{g_m} + \mathrm{V_{th}}$ and $\mathrm{g_m}$ is the transconductance of the MOSFET. The drain current will reach the load current level at the end of this sub-period.

Sub-period 3: (t_2-t_3) (Voltage fall time)

The voltage V_{ak} across the Schottky diode capacitance $\mathrm{C_{ak}}$ is expressed as (9) and V_{ds} can be expressed as (10) for this sub-period. The state equations (A2) for this sub-period are derived using (2)-(3) and (7)-(10) and are shown in the Appendix. The voltage fall time, $t_3 - t_2$ is the time required for V_{ds} to reach $\mathrm{V_{ds(on)}}$ from V_{ds} (t_2).

$$\frac{dV_{ak}}{dt} = \frac{1}{\mathrm{C_{ak}}}(I_d - \mathrm{I_{dd}}) \tag{9}$$

$$V_{ds} = \mathrm{V_{dd}} - (\mathrm{L_s} + \mathrm{L_d})\frac{dI_d}{dt} - V_{ak} - \mathrm{R_s} I_d \tag{10}$$

Sub-period 4: (t_3-t_4) (Ringing period)

As the MOSFET is now in the ohmic region, the drain current can be expressed as (11). The state equations (A3) for this sub-period, derived using (2)-(3) and (8)-(11), are shown in the Appendix. High frequency parasitic inductances are considered in this sub-period as well as shown in (10). The time for this sub-period, $t_4 - t_3$ is approximated by the time required for V_{gs} to reach $\mathrm{V_{gg}}$ from V_{gs} (t_3).

$$I_d = \frac{V_{ds}}{\mathrm{R_{ds}}} + \mathrm{C_{oss}}\frac{dV_{ds}}{dt} \tag{11}$$

B. Model implementation

Fig. 6 shows a summary of the turn on solution process in MATLAB. The state equations are solved using the parameters and parasitic values shown in Table I (Section IV.C). When solving (A2) for sub-period 3, the nonlinearities in junction capacitances were considered. These voltage dependent parasitic capacitances of the MOSFET ($\mathrm{C_{gd}}$, $\mathrm{C_{iss}}$ and $\mathrm{C_{oss}}$) and the Schottky diode ($\mathrm{C_{ak}}$) were modelled by fitting their datasheet curves to (12) which is based on the equation typically used for low voltage silicon MOSFETs [10]. $\mathrm{C_{0v}}$ and $\mathrm{C_{hv}}$ are the low voltage and high voltage capacitance values used to calculate the curve fitting coefficients x and $\mathrm{C_j}$. The $\mathrm{C_{hv}}$ term was included in (12) to achieve acceptable fitting of the variable capacitance curve over the wide voltage range of the 1200V SiC MOSFETs.

$$C = \frac{1}{\dfrac{1}{\mathrm{C_{0v}}} + \dfrac{V^{\mathrm{x}}}{\mathrm{C_j}}} + \mathrm{C_{hv}} \tag{12}$$

The linear state equations (A2) were solved in a loop with the junction capacitance values being updated after every ten time steps until V_{ds} reached $\mathrm{V_{ds(on)}}$. Then, (A3) was solved for sub-period 4, using the low voltage junction capacitance values, until V_{gs} reached $\mathrm{V_{gg}}$ when the simulation finally ends.

Datasheet values of the devices' capacitances [12-14] were compared with the fitted model, equation (12) in Fig. 7 for a SiC MOSFET, C2M0080120D and two SiC Schottky diodes, Cree C4D10120D and ROHM SCS230KE2. Fig. 7 shows that the variation of the devices' capacitances is well captured. The program updates the capacitor values around 100 times during a 600V, 20A switching transient which was judged to provide a good balance between accuracy and speed of simulation.

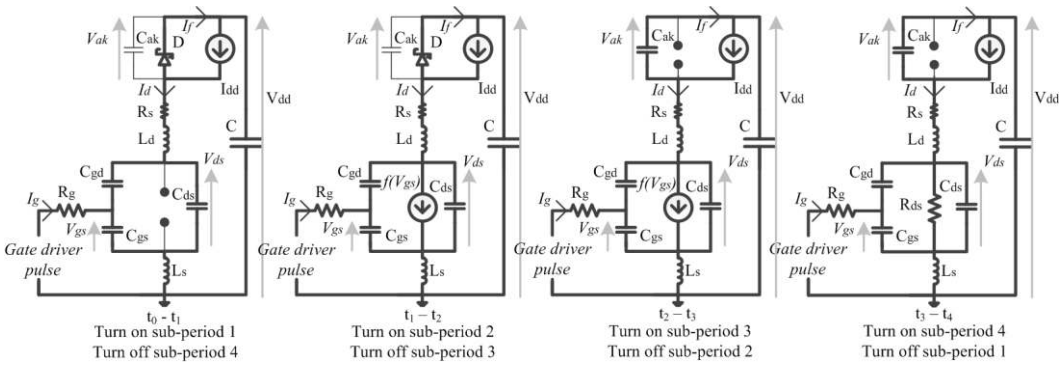


Fig. 5. Equivalent circuits for turn on and turn off sub-periods corresponding to the hard-switching DPT circuit

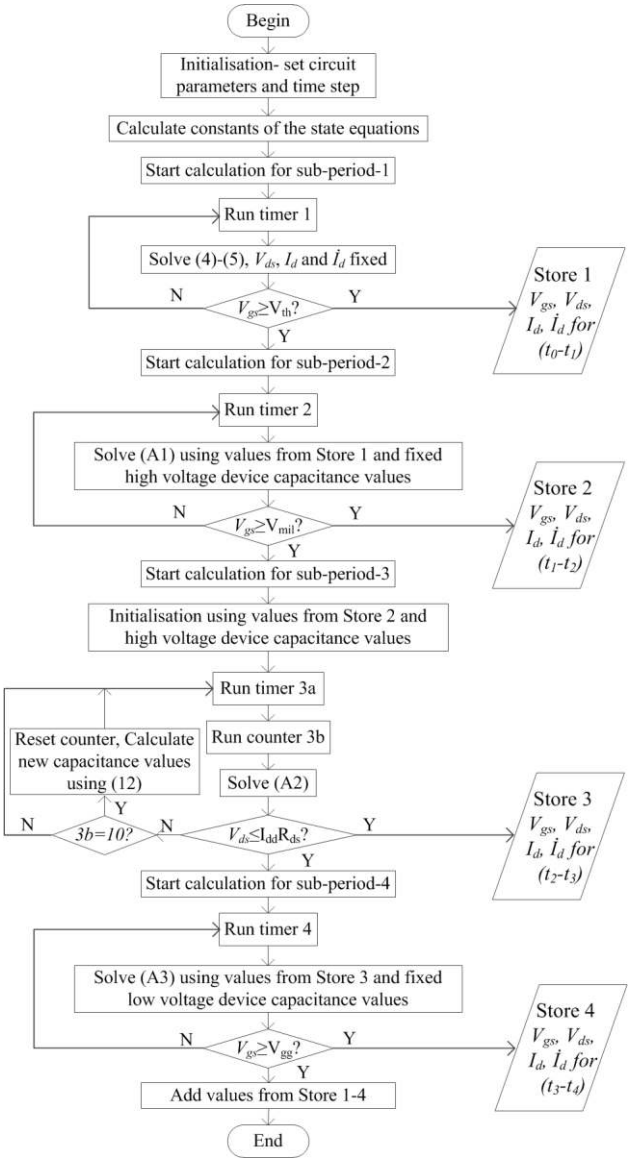


Fig. 6. Flow chart of turn on solution process

C. Turn off model

A gate voltage transition from V_{gg} to V_{ggl} initiates the turn off sequence. The four turn-off sub-periods, Fig. 5, are identical to the turn-on sub-periods but occur in reverse order. The state equations can be derived in a similar manner. After the negative gate pulse is applied, the MOSFET input capacitors C_{gs} and C_{gd} begin to discharge. (4) and (5) are the state equations for the sub-period 1 (turn off delay) and the state variables can be solved using $V_{g\_in} = V_{ggl}$ and the initial conditions, $V_{gs}(0) = V_{gg}$ and $I_g(0)=0$. The state equations for sub-periods 2 and 3 will be exactly the same as the corresponding turn on equations, (A2) and (A1), respectively. In sub-period 4, the MOSFET is in the cut-off region and the MOSFET output capacitor, C_{oss} resonates with the stray inductances of the circuit. The drain current can be expressed as (13). The state equations (A4) for this sub-period are derived using (2)-(3), (6), (8) and (13) and are shown in the Appendix.

$$I_d = C_{oss}\frac{dV_{ds}}{dt} \tag{13}$$

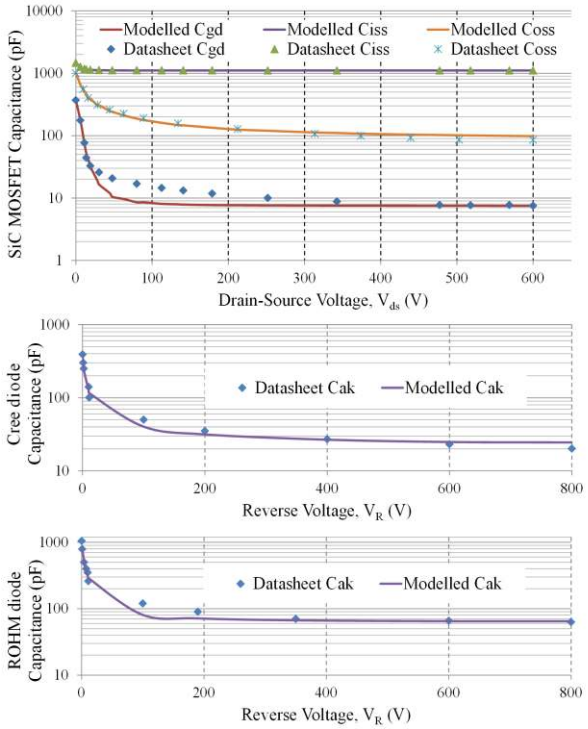


Fig. 7. Datasheet capacitances of the C2M0080120D MOSFET and Schottky diodes and the nonlinear model

IV. Modelling of SiC MOSFET Soft-Switching and dv/dt-Induced False Turn On

A. Soft-switching

To model the soft-switching transient only the turn off transient of the lower device (DUT) in Fig. 2(a) was analysed because this transient also corresponds to turn on of the upper device. The equations modelling soft-switching can be derived from Fig. 3. Similar to hard-switching, the soft-switching model is based on the solution of four distinct stages of the transient, (i) turn off delay, (ii) drain current fall, (iii) drain to source voltage rise and (iv) ringing periods. Two additional state variables, snubber capacitor current, I_{c2} and its rate of change, $\dot{I}_{c2}$ were used in addition to the other four state variables, V_{gs}, V_{ds}, I_d and $\dot{I}_d$. The resulting state space equations were solved sequentially.

Sub-period 1': (t_0'- t_1') (turn off delay)

This is exactly the same as the turn off delay sub-period of the hard-switching model.

Sub-period 2': (t_1'- t_2') (Current fall period)

The system of state equations (A5) for this sub-period can be formed from (2)-(3), (7)-(8), and (14)-(17). Here, V_{s1} and V_{s2} are the voltages across the snubber capacitors. t_2'–t_1' is the time required for V_{gs} to reach V_{th} from V_{mil}.

$$V_{ds} = V_{dd} - V_{s1} - (R_s + R_{leads})I_d - R_s I_{c2} - (L_s + L_d)\frac{dI_d}{dt} - L_{sh}\frac{d}{dt}(I_d + I_{c2}) \tag{14}$$

$$\frac{dV_{s1}}{dt} = \frac{1}{C_{s1}}(I_d + I_{c2} - I_{dd}) \tag{15}$$

$$\frac{dV_{s2}}{dt} = \frac{I_{c2}}{C_{s2}} \quad (16)$$

$$V_{s1} + V_{s2} = V_{dd} - R_s(I_d + I_{c2}) - L_{sh}\frac{d}{dt}(I_d + I_{c2}) \quad (17)$$

Sub-period 3': (t_2'- t_3') (Voltage rise period)

The state equations (A6) for this sub-period are derived using (2)-(3), (8), (13), and (14)-(17). $t_3' - t_2'$ is the time required for V_{s1} to reach zero from V_{s1} (t_2').

Sub-period 4': (t_3'- t_4') (Ringing period)

Because the diode on state resistance, R_d was considered, one additional state variable V_{s1} has to be solved in this sub-period. The state equations (A7) are derived using (2)-(3), (8), (13)-(14), and (16)-(18). $t_4' - t_3'$ is approximated by the time required for V_{gs} to reach V_{ggl} from $V_{gs}(t_3')$.

$$\frac{dV_{s1}}{dt} = \frac{1}{C_{s1}}\left(I_d + I_{c2} - \frac{V_{s1} + V_F}{R_d} - I_{dd}\right) \quad (18)$$

B. dv/dt-induced false turn on

The equations modelling the dv/dt induced false turn on can be derived from Fig. 4. In this case there are three sub-periods; (i) turn on delay, (ii) voltage and current transitions, and (iii) ringing period. The upper MOSFET Q1 is modelled in the same way as in the turn on transient in Section III.A except now the voltage and current transitions happen simultaneously and the load current, I_{dd} = 0. Apart from the four state variables, V_{gs}, V_{ds}, I_d and $\dot{I}_d$ associated with Q1 another additional state variable, the gate to source voltage of Q2, V_{gs2}, is added to the model to determine the false turn on of Q2. The state equations for sub-period t_0''- t_1'' are exactly same as those for sub-period t_0- t_1 of the hard-switching model with V_{gs2} fixed at V_{ggl}. For the second and third sub-periods the state equations (A8, A9) are derived from Fig. 4 (a) assuming Q2 remains in the off state. Circuit equations (2)-(3) and (7)-(11) of the previously described hard-switching model in Section III.A are used to derive (A8) and (A9). When solving (A8) all the device parasitic capacitances are modelled by fitting their nonlinear curves to equation (12) as explained in Section III.B.

C. Numerical solution of analytical model

The analytical models were solved in MATLAB using datasheet information for R_{ds}, g_m, R_d, V_F, package inductances and device capacitances [12-14], and measured values from the PCB layout, Table I. The power circuit parasitic values were measured using a precision impedance analyser, Agilent 4294A. The resistance of the power loop, R_s is the sum of the AC resistances of current shunt resistor, R_{shunt}, PCB current paths, R_{PCB}, MOSFET and diode resistances (R_{ds}, R_d and R_{leads}). The inter-winding parasitic capacitance of the load inductor, C_L and its high frequency AC resistance, R_L were included in the model in the ringing sub-periods.

V. Simulation and Experimental Results

A 600V, 20A double-pulse test (DPT) circuit shown in Fig. 8 was considered. A Cree SiC MOSFET gate driver circuit, CRD-001 was used. T&M Research's high-bandwidth (2 GHz) current shunt resistor, SDN-414-01 was used to measure the source current. LeCroy high-voltage-high-bandwidth passive probes, PPE2KV (400 MHz) and PP008 (500 MHz) were used to measure V_{ds} and V_{gs} respectively. A de-skew calibration test was performed in the Teledyne LeCroy 400 MHz Wave Runner 44Xi-A oscilloscope to compensate the different propagation delays between V_{ds} and I_d. The connection of the load inductor can be changed to enable hard-switching, soft-switching and false turn on tests to be performed using the same circuit for fair comparison.

TABLE I
PARAMETERS AND PARASITIC VALUES

Section	Parameter	Value	Parameter	Value
Power circuit	V_{dd}	600 V	I_{dd}	8A-20A
	R_{shunt}(DC)	10 mΩ	L_{pcb}	20 nH
	R_{shunt} (100 MHz)	53 mΩ	C_L (100 MHz)	6.5 pF
	R_{pcb} (100 MHz)	100 mΩ	R_L (100 MHz)	16.8 Ω
	R_{leads} (100 MHz)	70 mΩ	L_{shunt}	8 nH
Gate drive circuit	V_{gg}	20 V	V_{ggl}	-4 V
	R_g	11.27 Ω (including R_{gint} = 4.6 Ω)		
SiC MOSFET C2M0080120D	R_{ds} (25°C)	80 mΩ	g_m (25°C)	8.1 S
	L_s	10.5 nH	L_{drain}	7.5 nH
	R_{ds} (125°C)	130 mΩ	g_m (125°C)	7.9 S
Snubber circuit	C_{s1}, C_{s2}	1 nF		
Cree Diode, C4D10120D	L_{lead}	12.5 nH	V_F	0.93 V
	R_d (25°C)	10 mΩ		
ROHM Diode, SCS230KE2	L_{lead}	12.5 nH	V_F	0.95 V
	R_d (25°C)	15 mΩ		

The DPT circuits were also simulated in LTspice using the manufacturers' Spice models of the SiC MOSFET (C2M0080120D library beta version) and Schottky diodes (C4D10120D-11/2014 version and SCS230KE2-02/2013 version). A time step of 0.01ns was selected for both the numerical calculation of the model and the LTspice simulation as the SiC MOSFET switching transient times are around tens of ns.

A. Hard-switching

Experimental, calculated and LTspice simulation transients for hard switching operation at 600V 20A are shown in Fig. 9 and 10 for two different Schottky diodes when the junction temperature of the MOSFET (T_j) was around 25°C. The V_{ds} and V_{gs} waveforms include the voltages across the device package inductances and resistances. The experimental dV_{ds}/dt was 31 kV/µs at turn on and 46 kV/µs at turn off. The experimental di/dt was 1.5 kA/µs at turn on and 1.1 kA/µs at turn off. In both figures, the calculated and LTspice simulated voltage and current transients showed a good match with the experimental results. The V_{ds} and I_{ds} waveforms are first multiplied to get P_{on} and P_{off} and then integrated to calculate the switching energy losses. The losses from the experiments are summarised in Table II. It is evident that compared to the LTspice models the analytical models gave a better switching loss estimation (less than 10% error in most cases). The maximum errors from the analytical models were around 13% for individual losses and around 3% for the total switching losses. Whereas, the maximum errors from the LTspice simulations were around 47% for individual losses and around

26% for the total switching losses (with the ROHM diode). The maximum errors from the LTspice simulations with the Cree diode were around 11% for both the individual losses and the total switching losses. The DPT circuit was also tested using higher and lower gate resistances and lower supply voltages; the percentage errors in the predicted switching losses were found to be similar to those in Fig. 9 and 10.

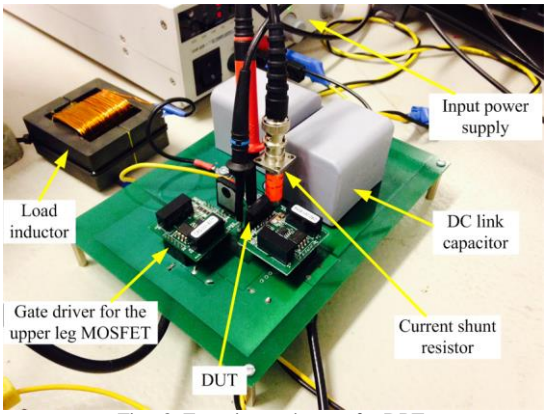


Fig. 8. Experimental setup for DPT tests

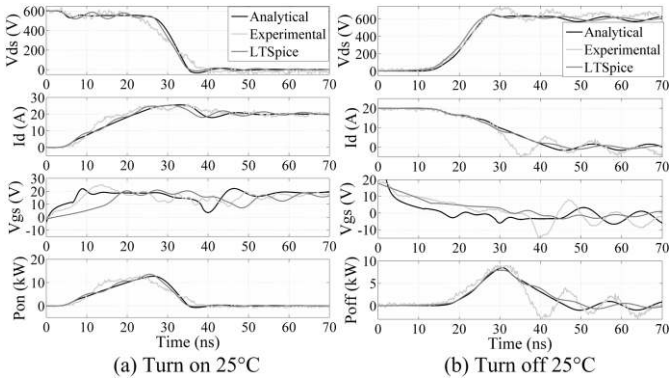


Fig. 9. Measured, predicted and Spice simulation results with Cree C4D10120D diode 600V, 20A at T_j=25°C

Both experimental and LTspice turn off losses include the energy stored in the device output capacitance and other circuit stray capacitances, which eventually is dissipated during the turn on transient. Ideally this loss should be part of the turn on loss, however due to practical limitations it is almost impossible to measure the MOSFET channel current. Therefore, this loss is normally considered to be a part of the turn off loss. The analytical model enables the actual turn on and turn off losses to be calculated from the modelled channel current of the MOSFET and V_{ds}.

The analytical modelling results considering constant device capacitances as assumed for Si MOSFETs in [10, 11] have a very poor correlation with the experimental results. Using the SiC MOSFET datasheet, [12], C_{gd} was calculated from the Miller charge, Q_{gd} assuming linear drain to source voltage transitions and C_{oss} was calculated from the C_{oss} stored energy. Diode capacitances C_{ak} were calculated using the total capacitive charge from their respective datasheets [13, 14]. The results are omitted in Fig. 9 and 10 for clarity, but the switching losses are listed in Table II which showed as high as 154% error in estimating the individual losses and 69% error in the total switching losses.

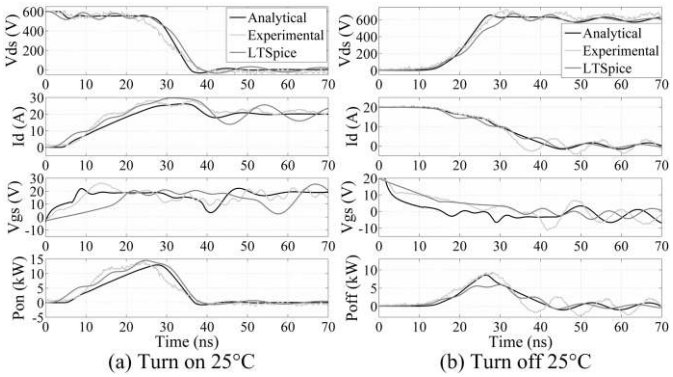


Fig. 10. Measured, predicted and Spice simulation results with ROHM SCS230KE2 diode 600V, 20A at T_j=25°C

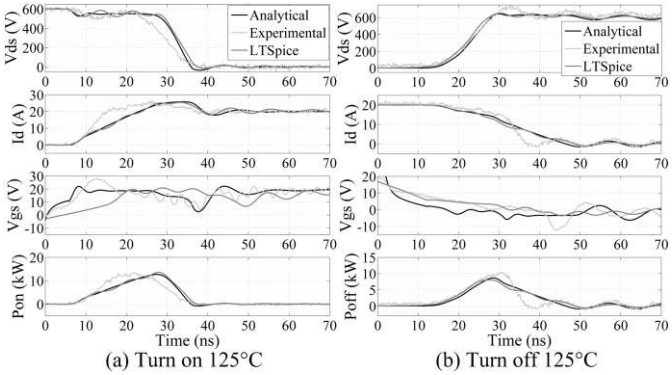
The advantage of the proposed analytical model over the LTspice model is a three times reduction in calculation time, a single turn on transient takes 0.6s to complete on an Intel Core i7 3.4 GHz computer. Therefore, the model has the potential to be used in a design optimization program where increasing the speed of the simulation is one of the key challenges because of the numerous iterations within the program. Also the effect of temperature on the switching transients can be evaluated easily by changing the temperature dependent parameters in Table I. However, the modelling of ringing in the different waveforms is still limited in both the analytical and LTspice models as it can be seen that the measured results are more oscillatory than the predictions (Fig. 9 and 10). Additional parasitic elements such as drain to gate external parasitic capacitance and accurate approximation of the high frequency AC inductance of the power loop may need to be considered for better modelling of the ringing.

Experimental, calculated and LTspice simulation transients and switching energy losses for hard switching operation with the Cree diode at higher MOSFET junction temperature, Tj=125°C are shown in Fig. 11 and Fig. 12. Fig. 11 compares the calculated and LTspice simulation transients with the experiment transients for high-temperature DPT operation at 600V, 20A. The temperature dependent parameters V_{th}, g_m and R_{ds} were updated in the analytical model and the manufacturers' high temperature Spice model of the SiC MOSFET was used in LTspice. Fig. 12 compares the calculated and LTspice simulated switching energy losses with the experimental losses for a wide range of load currents (8A to 20A) at both T_j= 25°C and 125°C with V_{dd} fixed at 600V.

From both Fig. 11 and 12 it is clear that the calculated and LTspice simulated transients and switching energy losses show an excellent match with the experimental results. As expected, the turn on losses are reduced and the turn off losses are increased with the higher junction temperature (consistent with the MOSFET datasheet [12]). In most cases errors from the analytical models were less than 10% and from the LTspice models were less than 13% (similar to the 25°C results). However, the modelling of the ringing becomes more challenging at higher temperature. Comparing the I_d waveforms at turn off between Fig.11(b) and Fig. 9(b) it is clear that the turn off oscillation is more heavily damped, which was attributed to the increased MOSFET-lead resistances at higher temperature.

TABLE II
SWITCHING LOSS COMPARISON 25°C OPERATION

Conditions	State	Loss (µJ)			
		Experiment	Analytical	LTspice	Fixed Cap
600V 20A	Turn on	236	225	228	265
with Cree	Turn off	117	120	130	251
C4D10120D	*Total*	*353*	*345*	*358*	*516*
600V 20A	Turn on	234	232	302	263
with ROHM	Turn off	126	116	104	252
SCS230KE2	*Total*	*360*	*348*	*406*	*515*
600V 13A	Turn on	115	123	128	145
with Cree	Turn off	54	49	59	137
C4D10120D	*Total*	*169*	*172*	*187*	*282*
600V 13A	Turn on	125	128	184	143
with ROHM	Turn off	55	48	43	140
SCS230KE2	*Total*	*180*	*176*	*227*	*283*



(a) Turn on 125°C (b) Turn off 125°C

Fig. 11. Measured, predicted and Spice simulation results with the Cree C4D10120D diode 600V, 20A at T_j=125°C

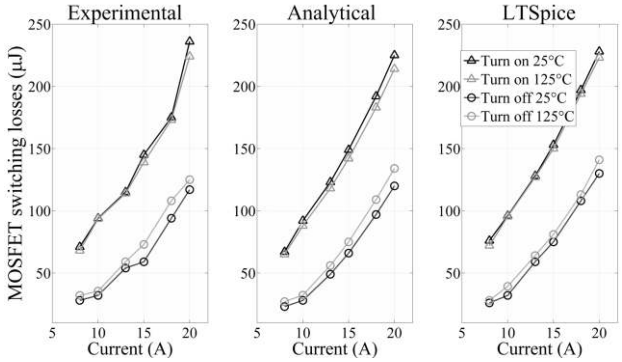
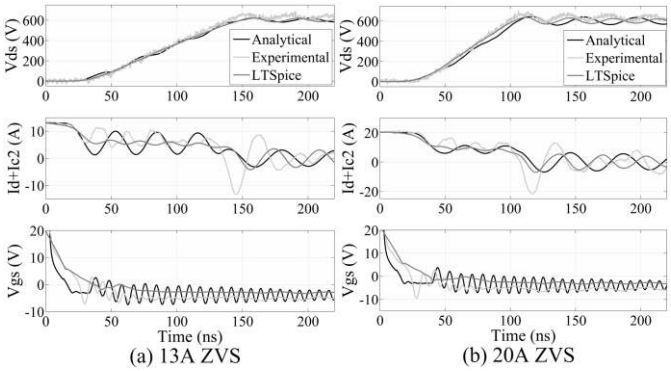


Fig. 12. Measured, predicted and Spice simulation of turn on and turn off energy loss for different currents at T_j=25°C and 125°C, V_{dd}= 600V

B. Soft-switching

The DPT circuit was tested in the soft-switching configuration using identical SiC MOSFETs as used in the hard-switching tests as the upper and lower leg devices. Fig. 13 shows experimental, analytical and simulation results of soft-switching at 600V, 13A and 20A. Comparing Fig. 13(b) with Fig. 9, the snubber circuit has reduced both the dv/dt by a factor of seven and the frequency of oscillations by a factor of three. Here, the analytical model predicts much more ringing in the V_{gs} waveforms which is attributed to the high frequency AC resistance of the upper MOSFET-connections (Q1) which needs to be predicted more accurately to enable a better match.



(a) 13A ZVS (b) 20A ZVS

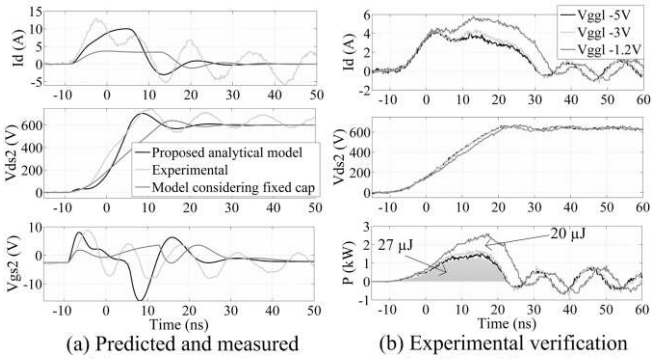
Fig. 13. Measured, predicted and Spice simulation results for soft-switching turn off 600V at T_j= 25°C

The analytical model also enables the calculation of the small turn off loss of 4 µJ and 10 µJ for 13A and 20A operations respectively by separating the MOSFET drain current, I_d, from the shunt resistor current, I_d+I_{c2}. The turn on losses will be approximately zero as the MOSFET turns on with zero voltage across it because of its body diode conduction. Therefore, for 20A soft-switching operation around 92% of the hard-switching energy was saved during turn off making the total soft-switching loss reduction 97% compared to the hard-switching conditions.

C. dv/dt-induced false turn on

The test circuit was operated with two Cree SiC MOSFETs in the phase-leg to investigate false turn on at different conditions by changing the gate resistances and negative gate-bias voltages. The analytical model accurately predicted the false turn on conditions by calculating the voltage across the gate to source capacitance (C_{gs2}) of the lower MOSFET during the turn-on transient of the upper device. Fig. 14 (a) shows the experimental and analytical results for the lower MOSFET (Q2) while the upper MOSFET (Q1) turns on at 600V with a speed of 40 kV/µs causing false turn on of the bottom device. The experimental V_{gs2} does not give an accurate indication of false turn on as it consists of voltages across the internal gate resistance (R_{gint}) of the MOSFET, common source inductance (L_{s2}) and C_{gs2}.

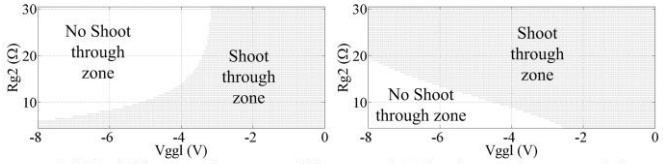
Fig. 14 (a) also shows that analytical results considering constant device capacitances, as assumed in [8, 9], have a poor correlation with the experimental results. This again confirms the importance of including the nonlinearity in the device capacitances. To check the efficacy of the modelling approach two specific gate resistances were selected for the upper and lower MOSFET, 34.6Ω and 24.6Ω, respectively. Now the negative gate bias, V_{ggl} was changed gradually to find a voltage where V_{gs2}, the gate-source voltage of the lower MOSFET crosses the threshold level. It was found that for a negative gate bias of 1.2V false turn on happens for the lower MOSFET (Fig. 14(b)). Analytical modelling also predicts a similar value for V_{ggl} during the false turn on of the lower MOSFET.



(a) Predicted and measured false turn on transients (b) Experimental verification varying V_{ggl} and loss calculation

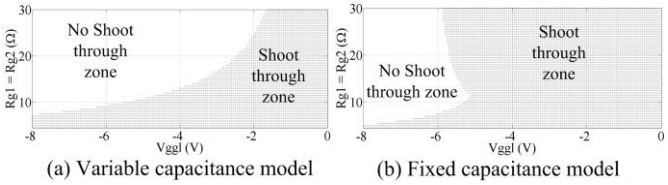
Fig.14. (a) Q2's false turn on, 11.27Ω gate resistance for both MOSFETs (V_{ggl}= -2V) and (b) False turn on by reducing V_{ggl} (R_{g1}= 34.6Ω and R_{g2}= 24.6Ω)

The analytical modelling results considering non-linear and constant device capacitances are again compared in Fig. 15 and Fig. 16. Considering the upper MOSFET turning on at 600V with a gate resistance (R_{g1}) of 11.27Ω, Fig. 15 shows the combinations of lower MOSFET gate resistance, R_{g2} (varied from 4.6Ω to 30Ω) and V_{ggl} (varied from 0V to -8V) which cause false turn on of the lower MOSFET. In one analytical model the MOSFET device capacitances were non-linear (Fig. 15(a)) and in the other model the MOSFET device capacitances were taken as average values (Fig. 15(b)). It is clear that when V_{ggl} is between -2.5V to -8V, the fixed capacitance based model gives inaccurate prediction of false turn on. Also in the non-linear capacitance based model the chance of shoot through reduces with the increased R_{g2} because the high common source inductance, L_{s2} is dominating the shoot through mechanism [8]. Fig. 16 shows a similar analysis when both of the gate resistances are equal, R_{g1}= R_{g2}. Comparing Fig. 16 (a) with the Fig. 16 (b), when V_{ggl} is between -1.7V to -8V, the fixed capacitance based model gives inaccurate prediction of false turn on.



(a) Variable capacitance model (b) Fixed capacitance model

Fig. 15. Predicted false turn on zones from the model (R_{g1}= 11.27Ω)



(a) Variable capacitance model (b) Fixed capacitance model

Fig. 16. Predicted false turn on zones from the model (R_{g1}= R_{g2})

The shoot through current due to false turn on increases the switching loss of the bottom and top devices by around 20 µJ and 7 µJ, respectively, because of the increased device current. However, 27 µJ of energy is stored in the bottom device and the circuit parasitic capacitances (Fig. 14 (b)). Ideally this energy should not be considered as dv/dt-induced loss as it is part of total stored capacitive energy in the device and circuit parasitic capacitances. The total dv/dt-induced loss was the same (27 µJ) as for the experiment in Fig. 14 (a) which makes the additional loss 8% of the total switching loss of the MOSFET (considering 600V, 20A operation with the Cree diode and assuming false turn on loss is independent of the load current).

VI. CONCLUSIONS

The analytical model presented in the paper, and validated experimentally can be used to enable rapid and accurate evaluation of circuit waveforms, device switching losses and dv/dt-induced false turn on events. The analytical model uses only datasheet parameters, so the impact on circuit operation and switching losses of SiC MOSFETs or diodes at different temperatures with different snubber capacitor values and circuit parasitics can be evaluated. In comparison with established Si-MOSFET analytical models, this paper shows how those models must be enhanced and refined in order to represent accurately the behaviour of SiC MOSFETs.

The paper also describes the analytical and experimental evaluation of the impact of soft-switching on the MOSFET switching loss, dv/dt and parasitic ringing, which provides an understanding of the benefits of soft-switching in very high speed SiC circuits. The switching loss was reduced by 97% with soft-switching along with an 86% reduction in dv/dt during the switching transients, which is likely to reduce significantly the EMI signature and unwanted parasitic events such as dv/dt-induced false turn on. These improvements suggest that the use of soft-switching techniques in high speed SiC MOSFET based converters could offer significant performance benefits.

It has been shown that false turn on can increase switching energy loss of the MOSFET but not as significantly as reported in some recent papers. For example in the results reported here almost half of the switching energy losses associated with the false turn on of the devices is actually the stored capacitive energy in the device and circuit parasitic capacitances - conventionally it was included in the total false turn on related losses.

Finally, it has been shown that to predict the SiC MOSFET's switching behaviour accurately it is important to model the non-linear device capacitances. If these capacitances are assumed fixed, inaccurate circuit waveforms will result and there will be serious errors in the estimation of losses, and shoot through events. Therefore, it is recommended that the Spice model of a SiC MOSFET or Schottky diode should include a good model of device capacitances for better prediction of its behaviour.

APPENDIX

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\end{bmatrix}=\begin{bmatrix}-(a1+a2) & a3 & a4 & 0\\ -b1 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ d1 & 0 & -d2 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1+u2+u3\\ v1\\ 0\\ -w1\end{bmatrix} \quad \text{(A1)}$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\end{bmatrix}=\begin{bmatrix}-(a1+a2) & 0 & a4 & -a5\\ -b1 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ d1 & 0 & -d4 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1+u2\\ v1\\ 0\\ w2-w1\end{bmatrix} \quad \text{(A2)}$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\end{bmatrix}=\begin{bmatrix}-a1 & -a4/R_{ds} & a4 & -a5\\ -b2/R_{ds} & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ 0 & d2/R_{ds} & -(d2+d5) & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ w2\end{bmatrix} \quad (A3)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5\\ 0 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ 0 & 0 & -d2 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ 0\end{bmatrix} \quad (A4)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\\ \dot{I}_{c2}\\ \ddot{I}_{c2}\end{bmatrix}=\begin{bmatrix}-(a1+a2) & 0 & a4 & -a5 & 0 & 0\\ -b1 & 0 & b2 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0\\ d1 & 0 & -d2 & -d6 & d7 & 0\\ 0 & 0 & 0 & 0 & 0 & 1\\ -d1 & 0 & f1 & f2 & -f3 & -f4\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\end{bmatrix}+\begin{bmatrix}u1+u2\\ v1\\ 0\\ -w1\\ 0\\ w1+y1\end{bmatrix} \quad (A5)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\\ \dot{I}_{c2}\\ \ddot{I}_{c2}\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5 & 0 & 0\\ 0 & 0 & b2 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0\\ 0 & 0 & -d2 & d6 & -d7 & 0\\ 0 & 0 & 0 & 0 & 0 & 1\\ 0 & 0 & f1 & f2 & -f3 & -f4\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ 0\\ 0\\ y1\end{bmatrix} \quad (A6)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\\ \dot{I}_{c2}\\ \ddot{I}_{c2}\\ \dot{V}_{s1}\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5 & 0 & 0 & 0\\ 0 & 0 & b2 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0 & 0\\ 0 & 0 & -d2 & d6 & -d7 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 1 & 0\\ 0 & 0 & f1 & f2 & -f3 & -f4 & f5\\ 0 & 0 & g1 & 0 & g1 & 0 & -g2\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\\ V_{s1}\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ 0\\ 0\\ y1+y2\\ -z1\end{bmatrix} \quad (A7)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\\ \dot{V}_{gs2}\end{bmatrix}=\begin{bmatrix}-(a1+a2) & 0 & a4 & -a5 & 0\\ -b1 & 0 & b2 & 0 & 0\\ 0 & 0 & 0 & 1 & 0\\ d1/2 & 0 & -(d2+d8)/2 & -d3/2 & 0\\ -a6 & 0 & a7 & -a8 & 0\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ V_{gs2}\end{bmatrix}+\begin{bmatrix}u1+u2\\ v1\\ 0\\ -w1/2\\ u4\end{bmatrix} \quad (A8)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \ddot{I}_d\\ \dot{V}_{gs2}\end{bmatrix}=\begin{bmatrix}-a1 & -a4/R_{ds} & a4 & -a5 & 0\\ -b2/R_{ds} & 0 & b2 & 0 & 0\\ 0 & 0 & 0 & 1 & 0\\ 0 & d2/(2R_{ds}) & -(d2+d8)/2 & -d3/2 & 0\\ -a6 & a7 & -a8 & 0 & 0\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ V_{gs2}\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ 0\\ u4\end{bmatrix} \quad (A9)$$

where, $a1=1/(R_gC_{iss})$, $a2=g_mC_{gd}/(C_{iss}C_{oss})$, $a3=L_s/(R_gC_{iss}L_{sd})$,

$a4=C_{gd}/(C_{iss}C_{oss})$, $a5=L_s/(R_gC_{iss})$, $a6=1/(R_{g2}C_{iss2})$,

$a7=C_{gd2}/(C_{iss2}C_{oss2})$, $a8=L_{s2}/(R_{g2}C_{iss2})$, $b1=g_m/C_{oss}$, $b2=1/C_{oss}$,

$d1=g_m/(C_{oss}L_{sd})$, $d2=1/(C_{oss}L_{sd})$, $d3=R_s/L_{sd}$,

$d4=(C_{ak}+C_{oss})/(C_{ak}C_{oss}L_{sd})$, $d5=1/(C_{ak}L_{sd})$, $d6=R_{leads}/L_{sd}$,

$d7=1/(C_{s2}L_{sd})$, $d8=1/(C_{oss2}L_{sd})$, $f1=1/(C_{oss}L_{sd})-1/(L_{sh}C_{s1})$,

$f2=R_{leads}/L_{sd}-R_s/L_{sh}$, $f3=L_{e1}/C_{s2}+1/(L_{sh}C_{s1})$, $f4=R_s/L_{sh}$,

$f5=1/(R_dL_{sh}C_{s1})$, $g1=1/C_{s1}$, $g2=1/(C_{s1}R_d)$

$L_{sd}=L_s+L_d$, $L_{sh}=L_{shunt}+L_{pcb}+L_{lead}$, $L_{e1}=(L_{sh}+L_{sd})/(L_{sh}L_{sd})$,

$u1=V_{g\_in}/(R_gC_{iss})$, $u2=g_mV_{th}C_{gd}/(C_{iss}C_{oss})$,

$u3=(R_sL_s-V_{dd}L_s)/(R_gC_{iss}L_{sd})$, $u4=V_{gg}/(R_{g2}C_{iss2})$, $v1=g_mV_{th}/C_{oss}$,

$w1=g_mV_{th}/(C_{oss}L_{sd})$, $w2=I_{dd}/(C_{ak}L_{sd})$, $y1=I_{dd}/(C_{s1}L_{sh})$,

$y2=V_F/(R_dC_{s1}L_{sh})$, $z1=I_{dd}/C_{s1}+V_F/(R_dC_{s1})$

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Md Rishad Ahmed received the B.Sc. degree from the Bangladesh University of Engineering and Technology (BUET) in 2011 and the M.Sc. degree (with distinction) from the University of Manchester, Manchester, U.K., in 2013. Since 2014, he has been working toward the Ph.D. degree at the University of Manchester.

His research interests include wideband-gap devices and high-frequency DC-DC converters.

Rebecca Todd (M'08–SM'12) received the M.Eng. degree from The University of Manchester Institute of Science and Technology, Manchester, U.K., in 2001 and the Eng.D. degree from The University of Manchester, Manchester, in 2006. Since 2010, she has been a Lecturer with The University of Manchester.

Her research interests include advanced control methods and converter design for energy storage systems.

Andrew J. Forsyth (M'98–SM'07) received the B.Sc. (Eng.) degree in electrical engineering from Imperial College, London, U.K., in 1981 and the Ph.D. degree in power electronics from the University of Cambridge, Cambridge, U.K., in 1987. Since 2004, he has been a Professor of power electronics with the School of Electrical and Electronic Engineering, The University of Manchester, Manchester, U.K.

His research interests include high-frequency converters, magnetic components, aerospace and electric-vehicle applications.