Prediction and Mitigation of Vertical Cracking in High-Temperature Transient Liquid Phase Sintered Joints by Thermomechanical Simulation

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Transient liquid phase sintering (TLPS) is a novel high-temperature attach technology. It is of particular interest for application as die attach in power electronic systems because of its high-melting temperature and high thermal conductivity. TLPS joints formed from sinter pastes consist of metallic particles embedded in matrices of intermetallic compounds (IMCs). Compared to conventional solder attach, TLPS joints consist to a considerably higher percentage of brittle IMCs. This raises the concern that TLPS joints are susceptible to brittle failure. In this paper, we describe and analyze the cooling-induced formation of vertical cracks as a newly detected failure mechanism unique to TLPS joints. In a power module structure with a TLPS joint as interconnect between a power device and a direct bond copper (DBC) substrate, cracks can form between the interface of the DBC and the TLPS joint when large voids are located in the proximity of the DBC. These cracks do not appear in regions with smaller voids. A method has been developed for the three-dimensional (3D) modeling of paste-based TLPS sinter joints, which possess complex microstructures with heterogeneous distributions of metal particles and voids in IMC matrices. Thermomechanical simulations of the postsintering cooling process have been performed and the influence of microstructure on the stress-response within the joint and at the joint interfaces have been characterized for three different material systems ($Cu + Cu_6Sn_5$, $Cu + Cu_3Sn$, $Ni + Ni_3Sn_4$). The maximum principal stress within the assembly was found to be a poor indicator for prediction of vertical crack formation. In contrast, stress levels at the interface between the TLPS joint and the power substrate metallization are good indicators for this failure mechanism. Small voids lead to higher joint maximum principal stresses, but large voids induce higher interfacial stresses, which explain why the vertical cracking failure was only observed in joints with large voids. [DOI: 10.1115/1.4039265]

1 Introduction

Power electronic devices are subject to continuously increasing heat dissipation levels because of growing current densities and voltage levels. Simultaneously, power electronic systems are becoming more miniaturized, further increasing dissipation heat flux densities. Additionally, electronic systems are increasingly used in high-temperature environments, such as automotive under-the-hood, deep well drilling, military, and energy harvesting. The combination of higher intrinsically generated heat flux densities and increased extrinsic environmental loads leads to high temperatures and thermomechanical stresses in devices and packages. Devices based on wide band-gap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) have been introduced and have become commercially available. These devices have application temperatures up to 450 °C [1], much higher than the operation limit of silicon (Si) based devices of 175 °C.

Conventional packaging technologies have been developed for the lower application temperatures of Si-based devices and are not able to function reliably under these intensified thermal conditions. Traditional high-temperature die attaches were solder alloys with high Pb-content of 85 at % and higher and melting temperatures of approximately 300 °C. Yet, because of the toxicity of Pb, legislative initiatives such as the Restrictions of Hazardous Substances Directive (RoHS) ban the use of Pb in electronic applications. Exemptions for Pb-alloys for high temperature die attaches exist in RoHS, but are currently under review. The exemption will be eliminated when a commercially competitive, reliable, high-temperature attach alternative exists.

Potential substitute materials for high Pb-content attaches include Sn-, Bi-, Au-, and Zn-alloys as well as solid state and liquid state sintering technologies. The melting temperatures of Sn-alloys are below 232 °C and lower than the anticipated wide band-gap device application temperature regimes. Bi-alloys have relatively low-melting temperatures of 262 °C. Furthermore, their low thermal conductivity, brittleness, and low ductility reduce their applicability. Au-alloys possess high strength and stiffness. Their melting temperatures exceed 280 °C, depending on the alloying element. The high cost of Au renders its application as

electronic attach technology commercially unfeasible for most applications. Zn-alloys have high-melting temperatures, but their processing is complicated by their bad wetting capabilities and their susceptibility to oxidation and corrosion. Solid-state sintering of silver particles can be used to form joints with excellent thermal, electrical, and mechanical properties, and high-melting temperatures of 961 °C. Yet, application of considerable levels of pressure is required during processing to densify the particles and form joints with low levels of porosity. Additionally, noble metallization is required for good adhesion of the silver sinter joint to the bonding surfaces. The high cost of silver makes the use of silver sinter technology as a commercially competitive substitute technology very challenging.

Transient liquid phase sintering (TLPS) is a novel attach technology that combines low processing temperature, high application temperatures, good thermal and electrical properties, and low cost. It is a liquid-assisted sintering process during which a low-melting temperature constituent melts, surrounds, and mutually diffuses with a high-melting temperature constituent. Intermetallic compounds (IMCs) with a melting temperature between that of the original constituents and significantly higher than that of the low-melting temperature constituent are formed. The original constituents are partially consumed during the process as IMCs grow simultaneously. The process is completed when the low-melting temperature constituent has been consumed completely. At this point, the joint consists of IMCs and residual high-melting temperature constituents, and the joint temperature has shifted toward the higher melting temperature of the IMC.

The copper–tin (Cu–Sn) and nickel–tin (Ni–Sn) material systems are of high interest as TLPS attach solutions because of their advantageous properties. The Cu–Sn system consists of constituents with high thermal conductivity and has high diffusion rates for rapid process completion. TLPS joints formed from the Ni–Sn system have a stable microstructure that converges rapidly and consists of phases with high-melting temperatures. Both, the Cu–Sn and Ni–Sn system, are compatible with metallization types commonly used in electronic assemblies. They are nontoxic and not subject to regulation, and the constituents are of low cost.

Two different TLPS approaches for Cu–Sn and Ni–Sn systems have been introduced: A layer-based approach with a layer of low-melting temperature constituent sandwiched between layers of high-melting temperature constituents, and a paste-based approach which utilizes sinter pastes that consists of particles of high and low-melting temperature constituents. Considerable research on layer-based TLPS approaches has been published for Cu–Sn [2–7] and Ni–Sn [8–12]. Detrimental to this approach is that bondline thicknesses are limited to thin joints: IMC growth is a diffusion-driven process, and the layer thickness is proportional to the square root of time. In consequence, conventional joint thicknesses (∼50 μm) require extensive process durations [7]. It has been demonstrated that thin TLPS bondlines have limited capability to compensate for surface roughness differences between joint surfaces [13].

The paste-based TLPS approach does not suffer from the bondline thickness limitations of the layer-based approach and enables unproblematic compensation of joint surface roughness. Because sinter pastes consist of a mix of particles in a binder system and are stencil printed, particles can rearrange and compensate for surface roughness. Furthermore, IMC growth not only occurs from the joint surfaces toward the joint center. In addition, IMCs are growing from all particle surfaces simultaneously. This decouples the process completion time from the joint thickness, because the required IMC thickness is equal to the short distance between high-melting temperature particles. Because of these advantages, considerable research has been pursued on the Cu–Sn [14–22] and Ni–Sn [18,23–27] material systems in the last years.

In the prior work, we have introduced flux-based Cu–Sn and Ni–Sn TLPS sinter pastes that do not require the application of a vacuum, inert, or reducing atmosphere and possess high-melting temperatures [22]. A two-step process was developed that reduced

joint voiding and improved process capability [26,27]. The joints have high strength and low susceptibility to creep [21] even though the microstructure of joints continues to evolve during high temperature aging [14]. Furthermore, we predicted that the thermal conductivity of TLPS joints formed from these pastes is high [18]. Additionally, we demonstrated that they have good reliability under cyclic drop loads [25] but are susceptible to crack formation in the brittle IMC regions under power cycling conditions [19].

In this paper, we describe and analyze the postprocess cooling-induced formation of vertical cracks as a newly detected failure mechanism in Cu–Sn and Ni–Sn TLPS joints. TLPS joints between power diodes and direct bond copper (DBC) substrates can show formation of vertical cracks between the DBC substrate and voids within the TLPS joint close to the DBC side. A modeling and simulation approach for three-dimensional (3D) joint geometries with microstructural details such as IMC regions, voids, and metal particles was developed. Thermomechanical simulations of the postsintering cooling process were performed, and the influence of microstructure on the stress-response of the joint and interface were characterized for three material systems (Cu + Cu_6Sn_5, Cu + Cu_3Sn, Ni + Ni_3Sn_4).

2 Sample Preparation and Failure Analysis

Samples were manufactured by sintering Si power diodes to DBC substrates with TLPS sinter pastes. The side length and thickness of the diodes were 6.35 mm and 0.35 mm, respectively. The diode backside metallization consisted of Al/Ti/Ni/Ag layers with a combined thickness of 1.2 μm. A two-step sintering process was used. Initially, a layer of sinter paste with a size of 6.5 mm × 6.5 mm × 0.2 mm was stencil printed on the DBC surface. Subsequently, a diode die was placed on the stencil-printed sinter paste layer. Afterward, a ring of solder paste with a width of 1 mm was dispensed around the stencil printed layer of sinter paste. Si diode dies were used because no SiC power diode dies of similarly large areas were available at the time of the studies. It is expected that the use of large devices increases the risk of crack formation in the joints because of increased thermal mismatch between the low coefficient of thermal expansion (CTE) of the diode and the high CTE of the interconnect layer. The stiffness and CTE of Si and SiC are similar, which should lead to similar joint failure modes. In fact, as will be shown later, the failure modes determined experimentally in this failure analysis can be predicted by simulations for structures with SiC diodes.

Two types of Cu–Sn sinter pastes were used: (1) a Cu–Sn sinter paste consisting of small Cu–particles with diameters <45 μm and spherical Sn-particles with diameters between 20 μm and 38 μm and (2) a Cu–Sn sinter paste consisting of large spherical Cu-particles with diameters between 37 μm and 88 μm and spherical Sn-particles with diameters between 20 μm and 38 μm. One type of Ni–Sn sinter paste was used that consisted of spherical Ni-particles with diameters in the range between 44 μm and 88 μm and spherical Sn-particles with diameters between 20 μm and 38 μm. Sinter pastes were prepared by mixing 66 weight-percent (wt %) Cu-particles (or Ni-particles, respectively), 17 wt % Sn-particles, and 17 wt % low-postreflow solid residue resin-free flux (flux type R0L0). The solder paste consisted of 85 wt % Sn-particles with particle diameters between 20 μm and 38 μm mixed with 15 wt % resin-based flux with high activity. The purity of the Sn-particles was 99.9%. No intentional alloying elements were present in the Sn-solder. The DBC substrates for Ni–Sn sinter pastes had a Ni top metallization layer. The DBC substrates for Cu–Sn substrates did not have a plating layer other than the base Cu.

The samples were placed on a combined hot-/coldplate. A pressure of 0.30 MPa was applied to the top of the diode die. The sintering temperature profile consisted of a ramp from a room temperature to 300 °C within 5 min followed by a dwell at 300 °C for 30 min and final cooling from 300 °C to room temperature

within 5 min. Sintering was performed in ambient atmosphere. No vacuum, inert gas, or reducing gas was applied. When the temperature exceeds 232 °C, the Sn particles of the solder paste melt. Because of the high purity of the Sn in the solder paste, potential impurities of the solder paste metals do not significantly influence the joint composition. In the joint region, Sn wets the Cu- and Ni-particles. Interparticle spaces are bridged by the liquid and particles rearrange. Remaining voids are filled by influx of liquid Sn from the solder ring. After sintering, pressure was relieved from the diode dies.

More than ten samples for each joint type were manufactured, and a few representative samples chose for figures in this paper. The samples were mounted and cross sectioned at the centerline of the diodes parallel to the diode side. The samples were ground with SiC grinding papers with grit sizes 240–1200 until the joint center was reached and subsequently polished with 1 μm diamond particle suspension. In prior studies, diamond particle suspension was found to be an excellent polishing slurry for these samples. No cracks are induced by the polishing step, microstructural details are revealed, and the sample surface has minimal residual scratches. The final cross-sectional areas were located at the center of the die in a plane parallel to the die side. Scanning electron microscopy images of the joints were taken at these locations. The joint regions consistently consisted of IMCs and embedded metal particles at both the edges and centers of the cross section.

Figure 1 shows a cross section of a TLPS joint manufactured by sintering of Cu–Sn sinter pastes with small particles. The joint microstructure consists predominately of a matrix of Cu_3Sn IMCs with small regions of dispersed Cu_6Sn_5 and Ag_3Sn phases. Because Ag is not part of either the sinter paste or the solder paste, the source of the Ag_3Sn IMCs must be the backside metallization of the diode die. During sintering, Ag dissolves into the liquid Sn. As Cu–Sn IMCs grow, Sn is consumed, and the concentration of Ag in the liquid increases, until Ag_3Sn IMCs nucleate. No significant quantities of residual pure Cu are present in the joint region as almost all of the Cu-particles have been converted to Cu–Sn IMCs.

Excellent wetting of the DBC and diode die surfaces occurred. Voids of varying sizes are dispersed throughout the joint. Multiple cracks were found in the joint. The cracks have formed vertically between the surfaces of the DBC and the diode. All cracks contacted the surface of the DBC, but not all cracks propagated completely toward the die surface. This indicates that the crack initiation site might be the interface between the top surface of the DBC and the intermetallic joint matrix.

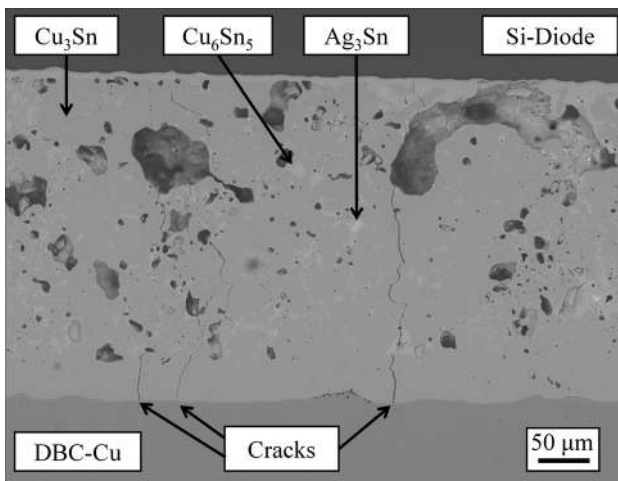The CTE mismatch between the joint and the DBC is smaller than between the die and the joint. Yet, cracks are initiated at the interface between the joint and the DBC. This indicates that CTE mismatch is not the sole driver of crack formation and that the high plasticity of the Cu-layer might further increase the susceptibility of crack initiation near the interface between the joint and the DBC. In contrast to the findings in Ref. [19], the cracks did not propagate into the die at any location. Cracks were predominately concentrated in regions with large voids. Cracks in other vertical planes existed, but the density of cracks was highest at the chosen cross section, which intersect the joint center. The number and length of the cracks were not quantified in this study. As can be seen in Fig. 1, most of the cracks formed between the DBC surface and large voids. The cracks showed intergranular propagation behavior, developing through regions with different IMC types. Rows of smaller voids were utilized as crack propagation paths between the DBC surface and the impediment locations.

Figure 2 shows a cross section of a TLPS joint manufactured by sintering of Cu–Sn sinter paste with large Cu-particles. The joint consists predominately of residual Cu-particles embedded in a matrix of Cu_6Sn_5 IMCs, see Fig. 2. The size of the Cu-particles has decreased from 37 μm to 88 μm before sintering to approximately 10 μm to 50 μm after sintering due to the reaction of some of the Cu to form Cu_6Sn_5 and Cu_3Sn. The quantity of Cu_3Sn IMCs generated in a given time for the large particle sinter pastes (Fig. 2) is considerably smaller compared to that generated in the same time for the small particle sinter pastes (Fig. 1) due to the slower rate of reaction given the smaller surface area to volume ratio in the larger particles. Furthermore, the Cu_3Sn IMCs in the larger particle materials are concentrated in layers with a thickness <10 μm. In contrast, the joints formed from small Cu-particles consist almost completely of Cu_3Sn IMCs, with an effective IMC thickness >200 μm, compare Fig. 1, again due to the faster transformation of Cu to Cu–Sn IMCs during the sintering process of the smaller particles. This influences the resulting microstructure and fracture behavior as will be discussed later. Few regions with Ag_3Sn IMCs are present. The size of the Ag_3Sn IMC regions is considerably larger than that of joints formed from sinter pastes with small particles.

Voids of similar sizes as those shown in Fig. 1 are present throughout the joint. Yet, no cracks have formed between the DBC substrate and the diode die or the DBC substrate and the
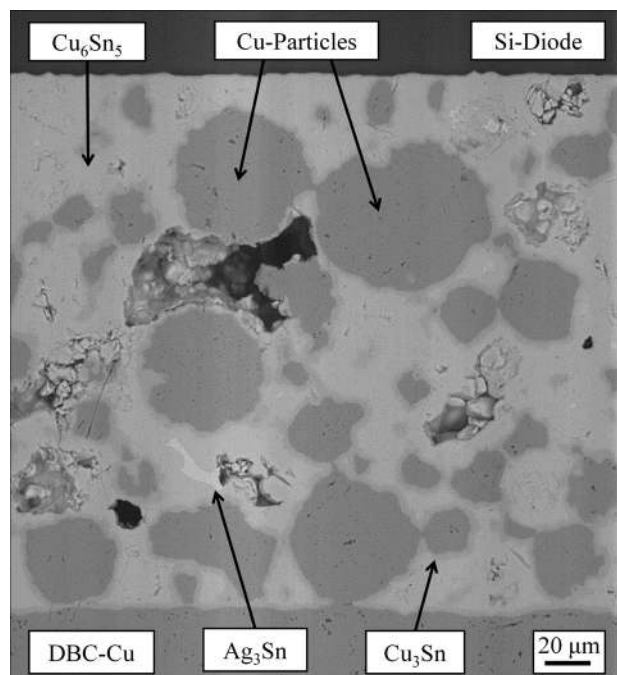

Fig. 1 Cross section of a TLPS joint formed from Cu–Sn sinter pastes with small Cu-particles

Fig. 2 Cross section of a TLPS joint formed from Cu–Sn sinter pastes with large Cu-particles
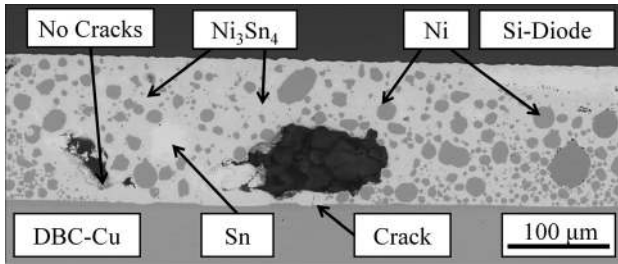
Fig. 3 Cross section of a Ni–Sn TLPS joint

voids. This indicates that the fracture toughness of joints formed from larger Cu-particles is higher than that of joints formed from smaller particles. This cannot be explained by the properties of the IMC matrix material. In fact, the fracture toughness of Cu_6Sn_5 is smaller than that of Cu_3Sn [28]. Furthermore, it cannot be explained by voiding, because the voiding behavior of both types of joints is similar. This leaves the residual Cu for the joints formed from large Cu-particles as explanation for the increased joint toughness. In contrast to Cu–Sn IMCs, Cu is a highly ductile material which undergoes considerable plastic deformation before fracture. During plastic deformation, Cu absorbs energy which would otherwise be absorbed by brittle crack formation in the IMC matrix. The ductility of residual Cu increases the effective fracture toughness of the TLPS joint formed from Cu–Sn sinter pastes with large particles.

Figure 3 shows a cross section of a Ni–Sn TLPS joint formed between a diode and a Ni-plated DBC. The microstructure consists predominantly of residual Ni-particles embedded in a matrix of Ni_3Sn_4 IMCs. Few regions of residual Sn are dispersed throughout the joint. Excellent wetting of the DBC and die surfaces occurred during processing. Voids of various sizes were found throughout the joint.

Multiple cracks were found in the Ni–Sn TLPS joints. Figure 4 provides high magnification examples of some of these cracks. All cracks were located at the DBC surface and propagated
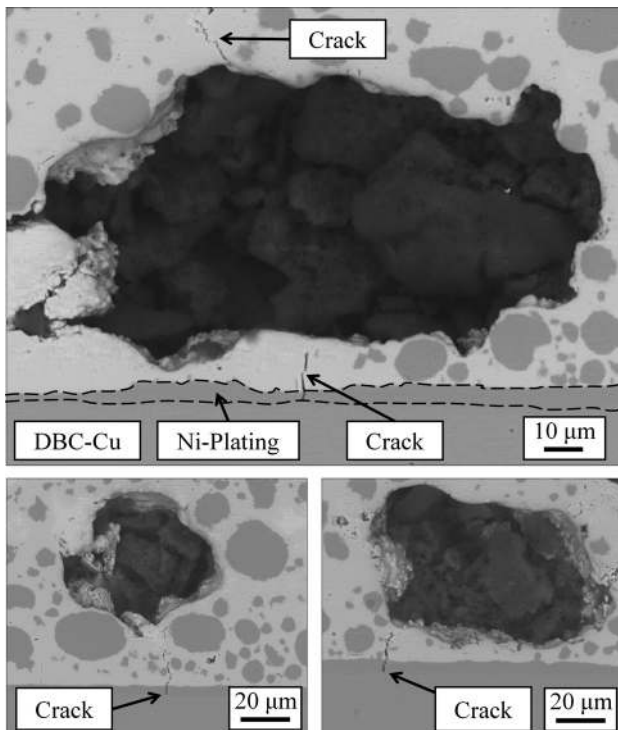

Fig. 4 Examples of crack formation in Ni–Sn TLPS joints

toward large voids (>20 μm) close to the DBC. No cracks were found to develop in the proximity of small voids, compare Fig. 3, left. The cracks initiated at the interface between the Cu-layer and the Ni-metallization layer of the DBC substrate and propagated toward the voids. Yet, not all cracks merged with the voids, compare Fig. 4. In one example, Fig. 4 (top), the cracks were impeded shortly before merging with the void, but a second crack formed at the top of the void. In another example, Fig. 4 (bottom right), the crack did not form beneath the center of the void, but rather at its edge. The cracks formed preferentially in regions with low density of residual Ni-particles, and no inter-Ni-particle crack propagation was found. On the DBC-side, cracks did not propagate into the Cu-layer.

No such cracks have appeared in Cu–Sn TLPS joints between Cu-substrates [18,19,21,22] or Ni–Sn joints between Ni-substrates [25–27] under identical process conditions. This indicates that thermomechanical loads induced by CTE mismatch between the TLPS joint, the diode, and the substrate, in combination with temperature gradients between sintering and ambient, are the source of the crack formation. Simulations of the structural response of diode-TLPS-DBC packages to thermomechanical loads during the cooling process have been performed to verify this hypothesis.

The tendency to form voids is related to the size of particles used and the size of the voids in the joint area after processing. Unfortunately, because of the complexity of the TLPS process, it is practically impossible to adjust these parameters independently. When small particles are used, the tendency to form large voids is reduced considerably. Yet, because IMCs are very brittle, cracks form easily in joints without residual metal particles. The goal of the simulation study is to gain an understanding if a critical void size exists, below which crack formation tendency is reduced. That way an optimized sinter paste can be designed that contains metal particles for ductility and voids below the critical crack initiation size. A joint formed from such a sinter paste should possess high toughness.

3 Simulation Approach

Paste-based TLPS sinter joints possess a highly complex microstructure, see above, that consists of residual metal particles and voids with multiple sizes distributed randomly within an intermetallic matrix. Assessing the structural response to thermomechanical loads for these types of interconnect requires a realistic geometric representation of the joint microstructure in the simulation environment. A simulation approach that enables this assessment has been developed. A similar approach has been used to assess the thermal conductivity of TLPS joints in Ref. [18], and will be described below briefly.

Figure 5 provides an overview of the process flow of the simulation approach. Initially, the type, size, and number of objects in the sinter joint are specified. Object types can be voids or metal particles. The size information specifies the radius of the spherical objects, and the number of objects in combination with the size of
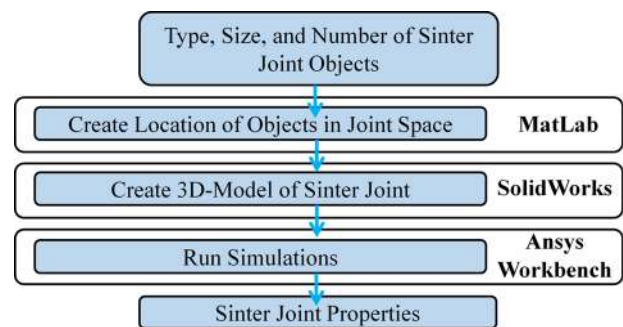

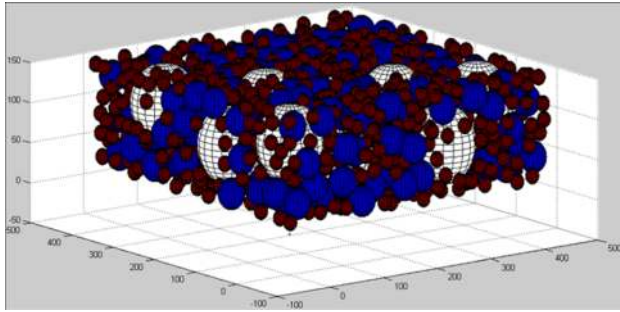**Fig. 5 Process flow of the simulation approach for TLPS joint simulations**

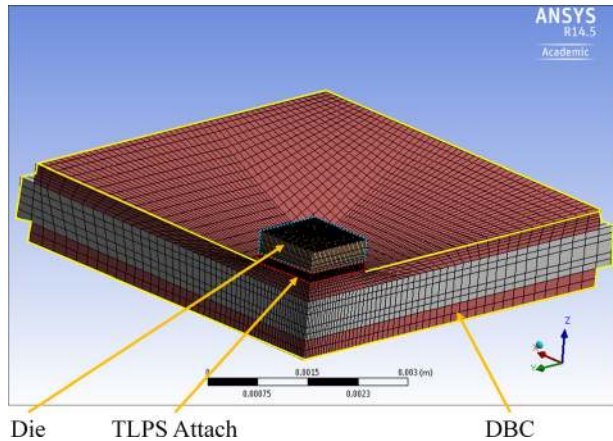**Fig. 6 Example structure of a sinter joint with objects of three different sizes**

Fig. 7 Side view on the meshed quarter-model

Fig. 8 Horizontal cross section through the TLPS joint of the quarter-model with large voids

Table 1 Properties of materials applied in the simulation study

Material	AlN	Cu	Cu_3Sn	Cu_6Sn_5	Ni	Ni_3Sn_4	SiC
E-Modulus (GPa)	330	119	133	117	250	144	410
CTE (ppm/K)	4.5	17	19	19	13.4	13.7	4

Fig. 9 Stress versus plastic strain for Cu and Ni at 20 °C, compare [29,30]

the joint region defines the final volume percentage of voids and particles in the joint. Afterward, a MATLAB script computes random locations of nonintersecting spherical objects according to the specified object properties. Subsequently, data files are created that are imported into SOLIDWORKS via a macro and are used to create a three-dimensional model of the sinter joint. This model includes spherical metal particles and/or spherical voids embedded in an intermetallic matrix. A .step file is created and imported into the ANSYS WORKBENCH simulation environment.

Figure 6 shows a side view of a geometry generated by the MATLAB script. Three object types with radii of 10, 20, and 50 μm were used to generate the geometry (white, blue, and red for radii of 50, 20, and 10 μm, respectively). The total joint space for this case spanned $500 \times 500 \times 150 \, \mu m^3$.

Figure 7 shows a side view of a quarter-model used for simulation. The model consists of three subelements: a diode die attached to a DBC with a TLPS interconnect indicated by the dashed blue, solid yellow, and dashed red lines, respectively. Two geometries were used. One with large voids and one with small voids with radii of 30 μm and 12 μm distributed throughout the joint, respectively.

Figure 8 shows a horizontal cross section through the center plane of the TLPS joint model with large voids. The display of the top part of the TLPS joint and of the diode have been disabled in this view. IMCs are shown in gray, metal particles in blue, and voids as empty spherical space.

The TLPS joint model included a total of 641 metal particles with a radius of 20 μm, which corresponds to 20 vol % of residual metal in the TLPS interconnect. For each type of void, the total volume added up to 10 vol % of interconnect volume. Voids of two different sizes with radii of 12 μm and 30 μm were included in the interconnect model. These are from here on referred to as sm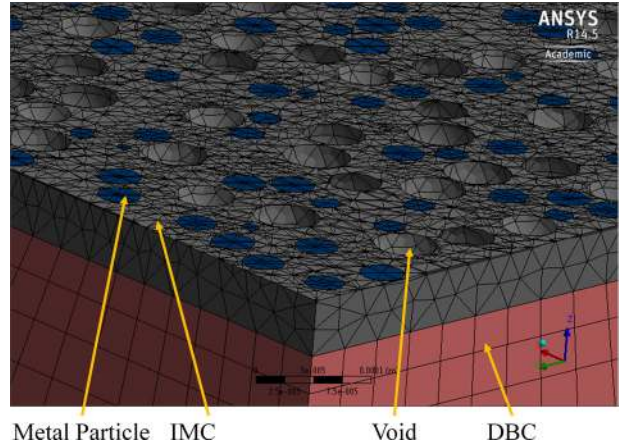all and large voids, respectively. The size of the voids was chosen to correspond with the small and large voids of experimental joints, compare Figs. 2–4. The thermal boundary conditions for the simulations were a homogeneous cooling of the system from a sintering temperature of 300 °C to the ambient temperature of 25 °C. The structural boundary conditions were symmetry conditions applied to the x- and y-direction at the center sections of the quarter-model as well as a no-displacement condition at the bottom of the DBC substrate. Table 1 summarizes the elastic modulus and CTE of the materials used in the simulations. Figures 9 and 10 show the plastic stress–strain models at room temperature and at elevated temperature levels for Cu and Ni.

A total of six simulation cases was performed for three material systems and two void sizes. The material systems were (1) Cu metal particles with Cu_6Sn_5 IMCs ($Cu + Cu_6Sn_5$), (2) Cu-particles with Cu_3Sn IMCs ($Cu + Cu_3Sn$), and (3) Ni-particles with Ni_3Sn_4 IMCs ($Ni + Ni_3Sn_4$). The geometries for joints with a specific void size type were identical for the different material systems.

Mesh convergence studies were performed to assess grid independence for the two joint geometries. The varied mesh parameter was the maximum size of mesh elements in the IMC layer, from here on referred to as body size. Five different body sizes from a
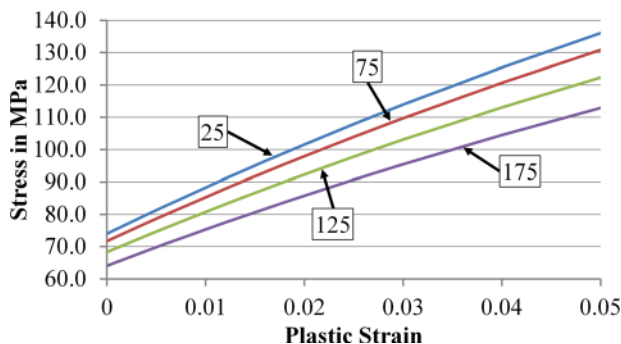
Fig. 10 Temperature dependence of the stress versus plastic strain for Cu, compare [30]
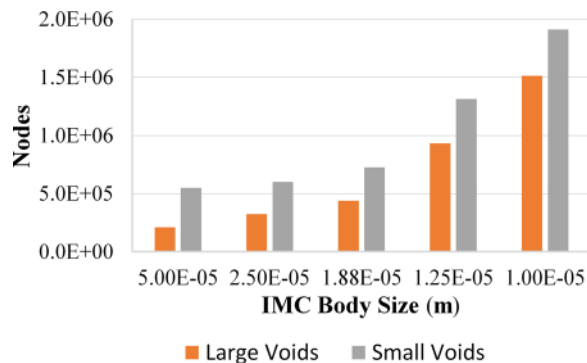

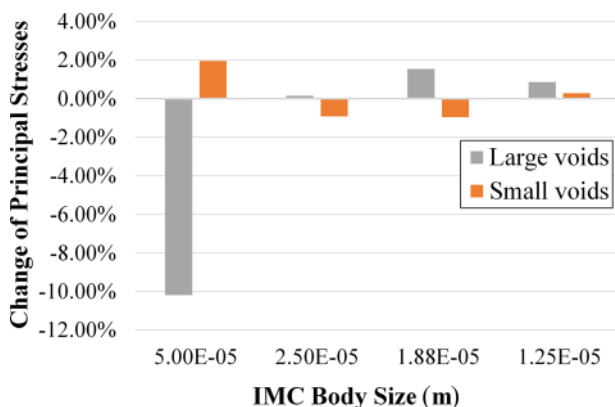**Fig. 11 Dependence of the number of nodes in the simulation model on the maximum mesh size in the IMC layer**

Fig. 12 Difference of the principal stresses at the interface between the IMC and the DBC substrate compared to the finest body size (1.00 × 10⁻⁵ m)

coarse mesh to a fine mesh with body sizes of 5×10^{-5} and 1×10^{-5} m, respectively, were assessed. The meshing algorithm automatically refines meshes where required, which results in local mesh element sizes significantly smaller than the body sizes.

The mesh convergence study was performed for the $Cu + Cu_6Sn_5$ material system.

Figure 11 shows the dependence of the total number of nodes in the simulation model on the body size of the IMC. For both, the large and the small voids, the number of nodes increases exponentially as the body size decreases. Small voids lead to higher mesh refinement levels for coarse meshes compared to large voids. As the body size decreases, the number of nodes increases rapidly for small and large voids. For fine meshes, the relative difference in the number of nodes between small and large voids decreases.

As will be shown later, the most important parameter for the prediction of the vertical cracking are the principal stress levels at the interface between the IMC and the DBC substrate. Figure 12 shows the dependence of the principal stress levels of the Cu_6Sn_5 IMCs on the body size. The results were acquired by determining the locations of the three highest stress concentration regions and their respective highest principal stress levels for the coarsest mesh. Subsequently, models with finer meshes were created, and the respective stresses with these models were determined in the identical stress concentration regions. This was performed for all meshes.

The relative differences of the stress levels compared to the finest mesh setting were computed for each region. Finally, the average differences between the mesh sizes and the finest mesh settings were computed. Figure 12 summarizes these results. A large initial variation exists for the coarse mesh with a body size of 5×10^{-5} m. For the large voids, the stress levels were -10.2% lower with the coarsest mesh compared to the finest mesh. In contrast, the difference for the small voids was $+1.9\%$. With smaller mesh sizes, the maximum differences were less than $\pm 2.0\%$ and $\pm 1.0\%$ for the large and small voids, respectively. This shows that for IMC body sizes smaller than 2.5×10^{-5} m, the results are independent of the mesh size. The change of principal stress swings between positive and negative percentage values. The reasons behind this phenomenon are unclear. Yet because of the small variation of amplitude for small mesh sizes, the results can be used to compare the simulation results with experimental results. Because the computation effort increases considerably with the number of nodes in the simulation model, 2.5×10^{-5} m was chosen as body size for the thermomechanical simulations of the other material systems.

4 Simulation Results

Table 2 summarizes the maximum stresses in the assembly after cooling from 300 °C to 25 °C. The void size has a small influence on the von Mises stress in the metal particles. The metal particle stresses for samples with large voids are 1.6%, 1.7%, and 2.8% higher for the $Cu + Cu_6Sn_5$, $Cu + Cu_3Sn$, and $Ni + Ni_3Sn_4$ system compared to the samples with small voids, respectively. Similarly, the principal stresses in the die are only slightly influenced by the size of the voids. The die stresses for the samples with large voids are 1.0% higher for $Cu + Cu_6Sn_5$, 3.4% smaller for $Cu + Cu_3Sn$, and 3.0% smaller for the $Ni + Ni_3Sn_4$ system than those for the samples with small voids.

In contrast, the maximum principal stresses of the IMCs show a considerable dependence on the size of the voids, see Fig. 13. The stresses for the samples with large voids are 14.9%, 11.4%, and 11.4% smaller for the $Cu + Cu_6Sn_5$, $Cu + Cu_3Sn$, and $Ni + Ni_3Sn_4$

Table 2 Maximum stresses in the assembly after cooling for large and small voids (30 μm and 12 μm, respectively)

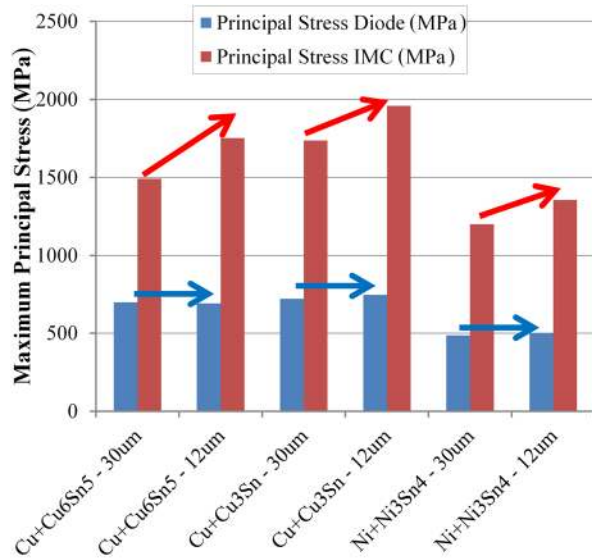|	$Cu + Cu_6Sn_5$		$Cu + Cu_3Sn$		$Ni + Ni_3Sn_4$	
Void radius (μm)	30	12	30	12	30	12
von Mises stress, particle (MPa)	87.4	86.0	87.4	85.9	143.9	139.9
Principal stress die (MPa)	698	691	721	746	485	500
Principal stress IMC (MPa)	1491	1752	1736	1959	1201	1355

Fig. 13 Dependence of the maximum principal stress of the diode and the IMCs on the void size
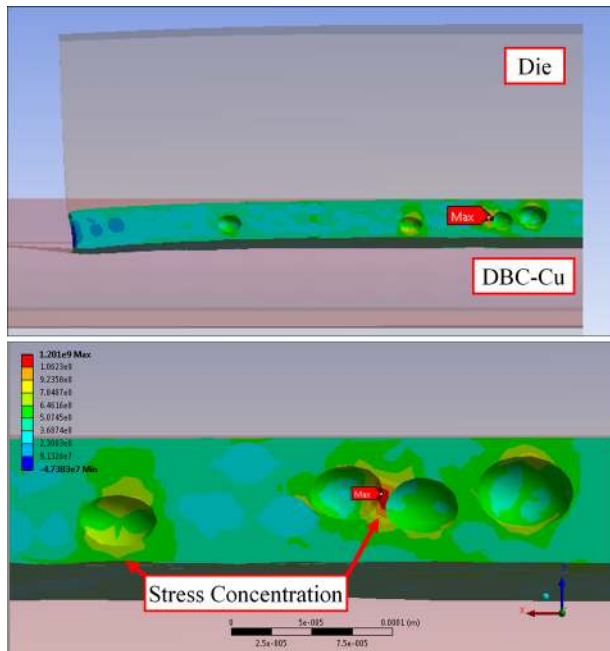

Fig. 14: Cross section through a TLPS joint with large (30 μm radius) voids. Two distinct types of stress concentrations exist: (1) between voids and Cu or the die and (2) between adjacent voids in close proximity.

Fig. 15 Cross section through a TLPS joint with small (12 μm radius) voids. The higher number of voids in the joint increases the probability of voids in close proximity.

system, respectively, compared to samples with small voids. This is counter-intuitive to conventional engineering judgment (i.e., larger voids should lead to locally more concentrated stress fields and higher stress levels). Additionally, the constant stress levels in the die indicate that the influence of void size is confined to the TLPS joint region.

Figure 14 shows a cross section through an assembly with a TLPS joint with large (30 μm) voids after cooling from 300 °C to 25 °C. Figure 15 shows an analogous cross section of a TLPS joint with small (12 μm) voids. The cross section views were chosen to show the maximum principal stress locations in the IMC. Two distinct types of stress concentration regions exist: The first are (type I) stress concentrations between voids located at the edge of
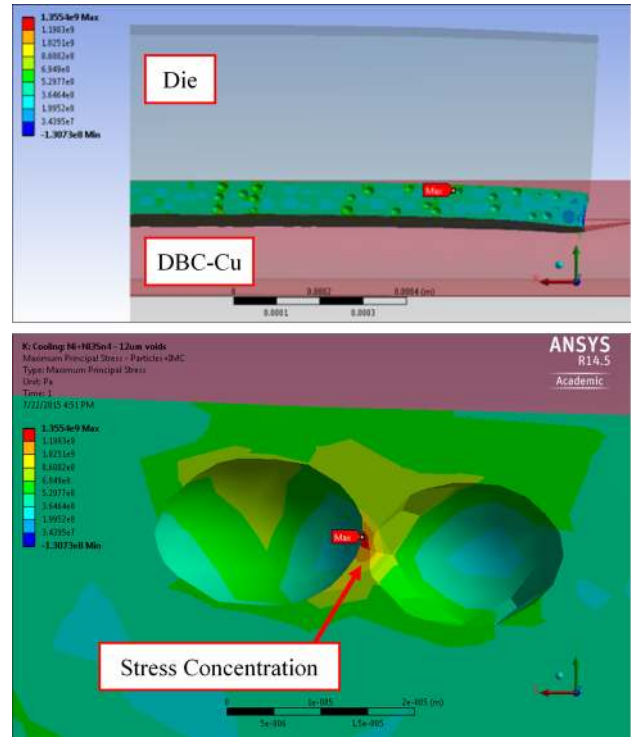
the joint close to the DBC Cu or the Si die. The second (type II) are stress concentrations located at regions between adjacent voids in close proximity. The CTE of the DBC and the die are small compared to the TLPS joint. During cooling, the joint contracts faster than the DBC and the die. This induces tensile stresses within the joint, which can result in the initiation of cracks and fracture during the cooling process.

The maximum principal stresses in the TLPS joints are located between voids in close proximity (type II). No voids of considerable size were found in such close proximities in actual joints. Two or more voids in very close proximity have a low likelihood of persisting after process completion. During processing, many small voids may form temporarily. Yet, these voids typically coalesce to few or an individual single large void. Because of this void coalescence phenomenon, the thin bridges connecting these voids in the simulations typically do not exist in real joints. If they should exist briefly after processing, the type II stress regions will crack and effectively form areas characterized by the presence of large voids. Yet, no such cracks were found in the cross section, compare Figs. 1–4.

The failure mode found in real joints, as shown in Figs. 1 and 4, is of type I stress concentrations. Figures 16 and 17 show stress distributions at the DBC_Cu-to-TLPS joint interfaces for samples with large (30 μm radius) and small (12 μm radius) voids, respectively. Local stress maxima (yellow regions) are distributed along the interface. The density of these regions increases in proximity to the joint center. The maxima correlate to regions with voids close to the Cu-to-TLPS joint interface (type I). The average stress level at this interface is higher at the joint center than at the joint edges (upper right corner and lower right corner in the quarter-model in the left images of Figs. 16 and 17, respectively). This is in good agreement with the experimental results that showed higher susceptibility to cracking at the joint center.

For example, for the Ni + Ni$_3$Sn$_4$ system, the highest principal stresses at this interface are 860 MPa and 720 MPa for the large and small voids, respectively. Additionally, the influence zone is larger for large voids than for small voids. When choosing, for
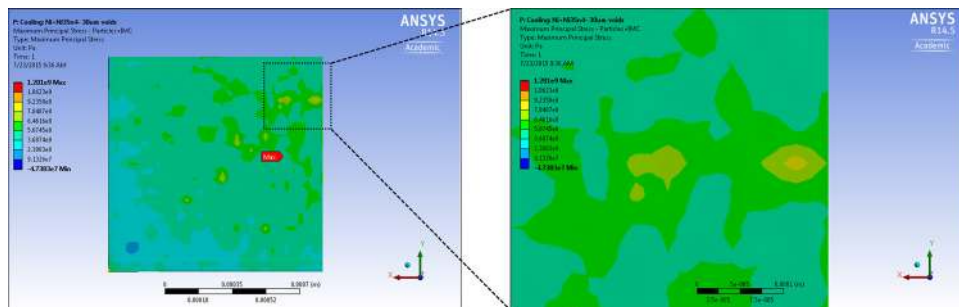
Fig. 16 Maximum principal stress distribution at the DBC_Cu-to-TLPS joint interfaces for large (30 μm radius) voids
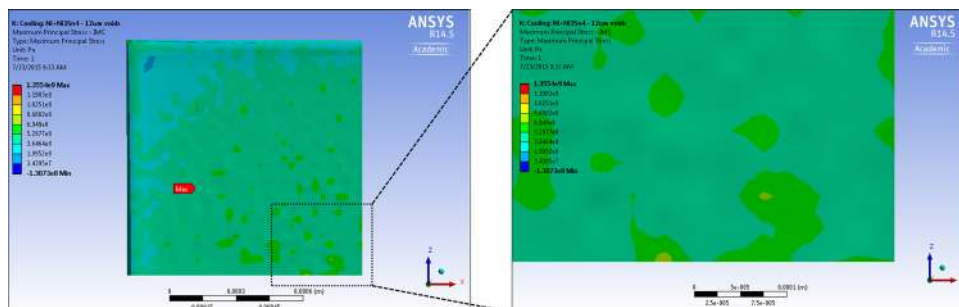

Fig. 17 Maximum principal stress distribution at the DBC_Cu-to-TLPS joint interfaces for small (12 μm radius) voids
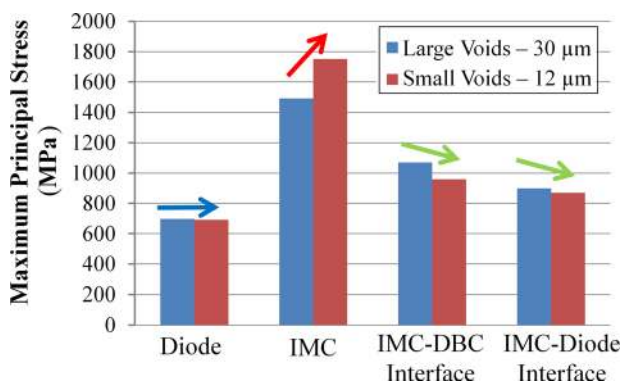

Fig. 18 Maximum principal stresses in the IMC, diode, IMC-to-Diode and IMC-to-DBC_Cu interfaces for the Cu + Cu$_6$Sn$_5$ system with large and small voids

example, a threshold criterion of 640 MPa, the zone of influence with stresses above this level has a radius of approximately 25 μm for the joint with large voids in contrast to an influence zone radius of approximately 7.5 μm for small voids.

Because the maximum mesh element stresses converged for small mesh sizes for both, models with large and small voids, compare Fig. 11, the maximum stresses of fine meshes for large and small voids can be compared quantitatively. Figure 18 shows the element maximum principal stresses in the assembly for the Cu + Cu$_6$Sn$_5$ system for the TLPS joints with large (30 μm radius) and small (12 μm radius) voids. The maximum principal stress in the diode is almost independent of the void size (indicated by the blue arrow). The maximum principal stress in the IMC is increasing considerably with decreasing void size (red arrow). This increase corresponds to type II stress regions. The maximum principal stresses at the IMC-to-DBC Cu and IMC-to-Diode interfaces decreases with void size. These stress locations correspond to type

I stress regions and the associated vertical cracking failure modes described earlier.

Very limited data are available in the literature on the ultimate tensile strength of the IMCs found in these systems. The fracture stress of Cu$_6$Sn$_5$ IMCs under compressive load has been analyzed by micropillar testing in Ref. [31]. The stress–strain curves of pillars until first strain burst show that fracture begins at stress levels of approximately 1200 MPa. Considering that Cu$_6$Sn$_5$ is a brittle material, the fracture stress for compression will be significantly higher than the fracture stress under tension. In consequence, the required stress levels for fracture would then be exceeded by the results yielded in the above simulations. Yet by reducing the void size the maximum principal stress levels can be reduced below the noncritical threshold, which mitigates the crack formation and propagation.

5 Summary and Conclusion

The cooling-induced formation of vertical cracks in paste-based TLPS joints has been documented as a novel failure mode and thermomechanical simulations have been performed to assess the underlying failure mechanism. Vertical cracks can form after cooling from processing temperature to ambient temperature if the joint is located between two layers of materials with low CTE. For the Cu–Sn TLPS system, cracks form only if no or limited residual Cu is present within the joint. Vertical cracks initiate at the interface between the TLPS joint and the Cu-metallization of the DBC substrate and propagate toward large voids within the joint. The presence of residual Cu-particles in the TLPS joint mitigates the growth of cracks. For the Ni–Sn TLPS system, cracks also form when residual Ni-particles are present in the joint. Here, cracks initiate in the Ni-metallization layer of the DBC substrate and propagate toward large voids in the TLPS joint. Small voids on the other hand do not increase the likelihood of crack formation.

A method for the three-dimensional modeling of paste-based TLPS sinter joints with high complexity and high degree of

similarity to real interconnects has been developed. Thermomechanical simulations of the postsintering cooling process have been performed for both, the Cu–Sn and Ni–Sn material systems. The influence of the size of voids on the stress-response of $Cu + Cu_6Sn_5$, $Cu + Cu_3Sn$, and $Ni + Ni_3Sn_4$ TLPS joints has been assessed. The maximum principal stress within the assembly was found to be a bad indicator for the prediction of vertical crack formation. In contrast, stress levels at the interface between the TLPS joint and the DBC substrate metallization are good indicators to predict the vertical cracking failure mechanism. Small voids lead to higher maximum principal stresses, which are located within the TLPS joint. Yet, the failure analyses showed that small voids are less susceptible to contribute to vertical cracking than large voids. Large voids induce higher principal stresses at the TLPS-to-DBC interface and the regions with high stress levels are larger compared to small voids. This explains why the vertical cracking failure mode was predominately observed in joints with large voids.

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