Predictive digital control of Power Factor Preregulators using disturbance observer for input voltage estimation

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***Abstract* – The paper presents a fully digital control of single-phase boost Power Factor Preregulators (PFPs) based on inductor (or switch) current and output voltage measurements. Input voltage sensing is avoided using a disturbance observer, which provides a waveform proportional to the rectified input voltage. The proposed solution is based on a multi-loop structure for PFP with an internal deadbeat current control and an outer voltage control with fast dynamic response. The resulting control algorithm is simple, accurate and robust respect to parameter mismatch. The digital control has been implemented both in a Field Programmable Gate Array (FPGA) and in a DSP (TMS320F2812), so as to test the proposed algorithm with different control delays. Experimental results on a single-phase 500W boost PFP show the effectiveness of the proposed solution.**

I. INTRODUCTION

Digital controllers for switch-mode power supplies have some interesting advantages compared to their analog counterparts, i.e. low quiescent power, immunity to analog component variations, ability to implement sophisticated control schemes and system diagnostics. While the application of digital control in high-frequency switching converters was almost unpractical up to now due to the cost, performance, and availability of DSP and microcontroller systems, the feasibility of low cost dedicated digital ICs [1,2] is somehow changing the future roadmaps of digital controller applications for switched-mode power supplies.

The investigation of digital control for Power Factor Preregulators (PFPs) is relatively new and a few works are available up to now [3-10]. The control structure described in previous paper is defined according to what is normally done in conventional analog controllers and widely discussed in literature; thus, the control algorithm is essentially based on a multi-loop control where the outer voltage loop determines the amplitude of the current reference, while its waveform is given by the rectified input voltage. Moreover, in [3-5,8-9] some potentialities of the digital implementation have been exploited and, more specifically, digital techniques aimed to remove the output voltage ripple at twice the line frequency have been used in order to increase voltage loop bandwidth. Finally, a recent implementation with FPGA has been proposed [3], which exploits the potentiality of simultaneous executions of control procedures. To the authors' knowledge, while three-phase PFC control without input voltage sensing has been widely investigated in the past, single-phase digitally controlled PFC proposed up to now requires the measurement of the input voltage.

This paper presents a fully digital control of boost PFP, where line input voltage sensing is avoided and a disturbance observer is used for its estimation. More specifically, the proposed solution is based on a multi-loop structure for PFP with an internal deadbeat current control, which highlights a simple algorithm for input voltage estimation, and an outer voltage control with fast dynamic response. Stability analysis of the proposed scheme shows that the system is stable even in presence of a relatively large parameter mismatch. The control algorithm has been firstly implemented in a FPGA board with fast A/D converters, where the overall control delay is quite small respect to the sampling period and, thus, negligible for the control law derivation. The proposed solution has been also implemented in a DSP (TMS320F2812), where the conventional one-sampling-period delay has been taken into account in the control algorithm. In both cases, experimental results confirm the effectiveness of the proposed approach.

II. CONTROL METHOD

Fig. 1 shows the basic scheme of the proposed method applied to a boost PFP. The PFP current controller operates the switch so as to draw from the grid a current $i_g(t)$ whose waveform is proportional to the line voltage $v_g(t)$ by a factor determined by the voltage control loop. Being the line voltage $v_g(t)$ estimated, the proposed control requires the sampling of two variables: output voltage and average input current. An advantage of the digital approach is that the average value of the sensed current is obtained, without low-pass filters in the loop, by synchronizing sampling and modulation so that the current is always sampled in the middle of the switch on period. This allows precise regulation of the average current, at least in the Continuous Conduction Mode (CCM), which is assumed hereafter.

In section II.A-C, we derive the control technique taking into account the one-sampling-period delay usually required due to computational time in microcontrollers and DSPs. In section II.D, we extend the technique in the case where digital processing time is negligible.

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A. Digital deadbeat current control

As far as the current control is concerned, the discrete-time model of inductor dynamics in CCM can be expressed as:

$$i_L(k+1) = i_L(k) + \frac{T_{sw}}{L}\left(v_r(k) - \delta'(k)\cdot v_o(k) \right) \qquad (1)$$

where $i_L(k)$ is the average inductor current, $v_r(k)$ the rectified input voltage, $v_o(k)$ the output voltage and $\delta'(k)$ the complement of the duty-cycle $\delta(k)$, all of them evaluated at the sampling instant $k\cdot T_{sw}$. The inductor current control is performed by means of the dead-beat control technique [12], which ensures fast dynamic response and simple implementation. In a dead-beat controller, the control algorithm calculates the duty-cycle so as to ensure that the current reaches its reference by the end of the following modulation period, taking into account one period delay in the digital implementation. By imposing that the current $i_L(k+2)$ is equal to the current reference $i_L^{ref}(k)$ at instant k+2, the following control algorithm is obtained:

$$\delta'(k+1) = -\delta'(k) + 2\frac{v_r(k)}{V_o^{ref}} + \frac{L}{T_{sw}\cdot V_o^{ref}}\left(i_L(k) - i_L^{ref}(k) \right) \qquad (2)$$

where we have assumed that $v_o(k) \cong V_o^{ref}$ and $v_r(k+1) \cong v_r(k)$. If the rectified line voltage $v_r(k)$ is sensed, control algorithm (2) ensures that the line current $i_L(k)$ is able to follow the reference current $i_L^{ref}(k)$ with two-cycle delay.

B. Disturbance Observer

Assuming that the rectified line voltage $v_r(k)$ is not sensed, we propose to put this term to zero in (2), obtaining the following control law:

$$\delta'(k+1) = -\delta'(k) + \frac{L}{T_{sw}\cdot V_o^{ref}}\left(i_L(k) - i_L^{ref}(k) \right) \qquad (3)$$

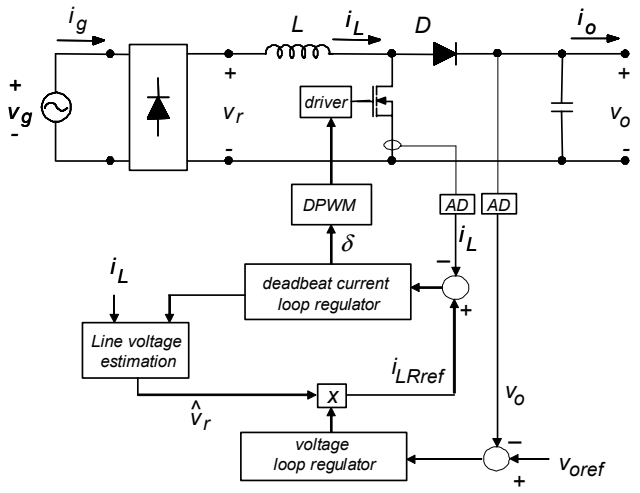

Fig. 1 – Digital control of Boost PFC with line voltage estimation.

Using (3), the current is now able to follow the reference with a two cycle delay besides an uncompensated disturbance given by the rectified input voltage. In order to evaluate the expression of this uncompensated term, let us combine (1) and (3) using the Z-transform; thus, the inductor current $i_L(z)$ can be written as:

$$i_L(z) = z^{-2} i_L^{ref}(z) + \frac{T_{sw}}{L}\left[z^{-1} + z^{-2} \right] v_r(z) , \qquad (4)$$

where the first term is the two-cycle delay inherently present in the deadbeat control and the second term represents the uncompensated disturbance, which is, indeed, *proportional to* a combination of delays of *the rectified input voltage*. Assuming that the input voltage is slowly varying, so that its variation is negligible between two samples (i.e. $v_r(k+1) \cong v_r(k)$), (4) can be written in the following form [13]:

$$\begin{aligned} i_L(k) &\cong i_L^{ref}(k-2) + \frac{2T_{sw}}{L} v_r(k-1) \\ &\cong i_L^{ref}(k-2) + i_D(k-1) \end{aligned} \qquad (5)$$

where $i_D(k)=(2\,T_{sw}/L)\cdot v_r(k)$. Thus, the proposed current control can be represented as the block diagram reported in Fig 2a, where $i_D(k)$ is the unknown disturbance which includes the uncompensated rectified input voltage and $i_r(k) = i_L^{ref}(k-1)$.

In order to provide a precise current control, disturbance $i_D(k)$ is now estimated and then compensated by a feedforward action, subtracting the estimated disturbance term $\hat{i}_D(k)$ to actual current reference $i_{LR}^{ref}(k)$, as shown in Fig. 2b. Moreover, signal $\hat{i}_D(k)$ gives an estimation of the rectified input voltage waveform.

The estimation of the disturbance $i_D(k)$ is obtained following Fig. 2a and assuming $i_D(k) = i_D(k-1)$; thus, the following state equations can be written:

$$x(k) = \begin{bmatrix} i_r(k) \\ i_D(k) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}}_{A_S} x(k-1) + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{B_S} i_L^{ref}(k-1) \qquad (6)$$

The observer for disturbance $i_D(k)$ is then evaluated using the following estimator:

$$\hat{x}(k) = A_S\,\hat{x}(k-1) + B_S\,i_L^{ref}(k-1) + C\left(i_L(k) - \hat{i}_L(k)\right) \qquad (7)$$

where $\hat{i}_L(k) = \hat{i}_D(k-1) + \hat{i}_r(k-1)$ and $C^T = \begin{bmatrix} c_1 & c_2 \end{bmatrix}$, being c_1 and c_2 the estimator gains. The result obtained solving (7) for $\hat{i}_D(k)$ is

$$\hat{i}_D(z) = \frac{c_2\left[z^2\, i_L(z) - i_L^{ref}(z) \right]}{z^2 + (c_1 + c_2 - 1)\,z - c_1} \qquad (8)$$

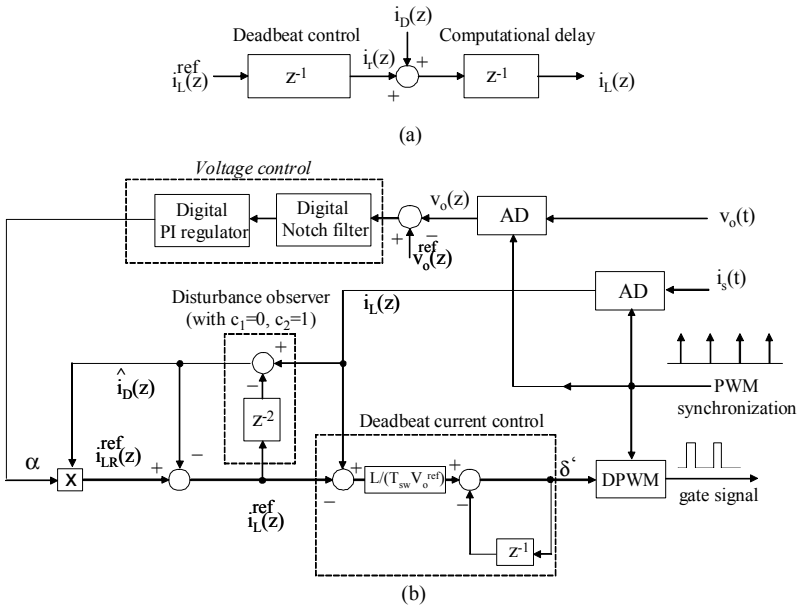

Fig. 2– (a) Equivalent block diagram of the current control; (b) proposed control with deadbeat disturbance estimation.

where coefficients c_1 and c_2 determine the speed of response of the estimator. In the case of deadbeat estimation, $c_1=0$ and $c_2=1$ and the final estimation law is

$$\hat{i}_D(z) = i_L(z) - i_L^{ref}(z) \cdot z^{-2} \qquad (9)$$

and it is reported in Fig. 2b. Note that the control algorithm is very simple and requires only a delay line and a subtraction. The feedforward compensation of disturbance term $i_D(k)$ shown in Fig. 2b realizes an additional loop in the proposed control. However, it is easy to verify that, without accounting for parameter or model mismatches, the closed loop poles of the resulting scheme shown in Fig. 2b, are still in the origin, thus ensuring the deadbeat response of the overall system.

C. PFC control with line voltage estimation

One of the main properties of the proposed approach is that signal $i_D(k)$, estimated using (8-9), is theoretically proportional to the rectified input voltage $v_r(k)$. Even in the practical case, we expect this term to be dominant respect to second order effects, such as delays in the gate pulse, inductor saturation, etc. . Thus, the estimated disturbance $\hat{i}_D(z)$ can be used for the determination of the waveform of the actual inductor current reference $i_{LR}^{ref}(z)$, as reported in Fig. 2b, where the proposed digital control algorithm, including a possible implementation for the voltage loop, is shown. Indeed, the use of the estimated disturbance $\hat{i}_D(z)$ in order to determine the reference current $i_{LR}^{ref}(z)$, introduces an additional loop in the proposed scheme, which must be analysed in order to validate the proposed approach, as performed in section III.B.

D. Control algorithm in case of negligible delay in the digital implementation

If A/D conversion time and control algorithm execution are just a small fraction of the sampling period, which may be the case in FPGA implementation with fast A/D converters or in dedicated digital ICs, the duty cycle can be updated just after the sampling of inductor current $i_L(k)$; thus, there is no delay in the digital implementation and the predictive algorithm needs to be modified accordingly. It is easy to verify that the control algorithm (3) becomes:

$$\delta'(k) = \frac{L}{T_{sw} \cdot V_o^{ref}} \left(i_L(k) - i_L^{ref}(k) \right) \qquad (10)$$

and the line current $i_L(k)$ is able to follow the reference current $i_L^{ref}(k)$ with only one-cycle delay. Moreover, the estimation process (9) simplifies as:

$$\hat{i}_D(z) = i_L(z) - i_L^{ref}(z) \cdot z^{-1} \qquad (11)$$

and this term can again be used for the estimation of the input voltage waveform. Note that the resulting control algorithm is even simpler, requiring only a proportional gain (10), a delay line and a few additions/subtractions.

III. STABILITY ANALYSIS

In order to highlight some properties of the proposed scheme, the robustness against parameter variations, the effect of the reference current generation, and the behaviour in DCM mode are analysed. For such purpose, let us define the inductor current reference $i_{LR}^{ref}(k)$ as:

$$i_{LR}^{ref}(k) = \alpha \hat{i}_D(k) \qquad (12)$$

where α is determined by the voltage loop control (see Fig. 2). Moreover, we define L_m the modeled inductor value, which is assumed in the control gain derivation, and β a factor which accounts for parameter mismatch, being $\beta=L_m/L$.

A. Effects of parameter variations

In this section, we focus on the current control, neglecting the interaction with the reference current generation and, thus, we assume coefficient α equal to zero. In this simplified case, the stability analysis of the closed loop system can be performed by applying the Z-transform to (1) and (3), where L has been substitute by L_m, by deriving the characteristic polynomial of the closed loop system, and by mapping the closed loop poles. If the magnitude of the closed loop poles is equal or greater that one, the resulting system is, of course, unstable.

Following this procedure, we found that the characteristic polynomial is given by:

$$\lambda(z) = z^4 + 2z^2(\beta-1) - (\beta-1) = 0 \qquad (13)$$

if the control delay is included, which we refer as Case A. In the case this delay is negligible, which we refer as Case B, the characteristic polynomial has the same structure as (13), as long as term z^2 is substituted with z and z^4 with z^2, as it is easy to verify using (1), (10) and (11). Inspection of (13) shows that the system is stable as long as parameter β is below a factor of around 1.33, showing that underestimation of the inductor value L do not cause stability problem. Clearly, severe underestimation also decreases the current control bandwidth so that a trade-off between robustness and speed of response determines the control gain. As an example, Figs. 3-4 report the closed loop poles of Case A and B, respectively, when β parameter is varied between 0.1 and 1.3. In both cases, system stability is verified.

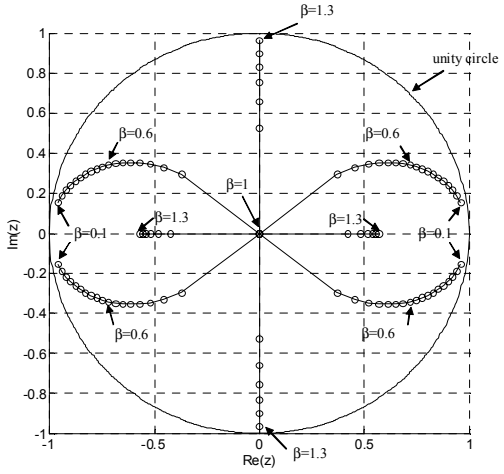

Fig. 3 - Real and imaginary part of the closed loop poles with: Case A, α=0, β varied between 0.1 and 1.3.

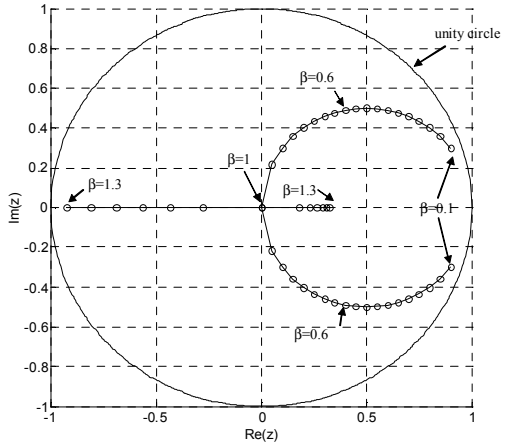

Fig. 4 - Real and imaginary part of the closed loop poles with: Case B, α=0, β varied between 0.1 and 1.3.

B. Effects of reference current proportional to estimated input voltage

Including (12) in the stability analysis, (13) modifies as:

$$\lambda(z) = z^4 + 2z^2(\beta-1)(2-\alpha) - (\beta-1)(1-\alpha) = 0 \qquad (14)$$

Let us firstly estimate the value of parameter α. A steady-state analysis on the PFP boost converter in CCM shows that:

$$\alpha = \frac{\hat{I}_g}{8\Delta i_{max}} \frac{V_o}{\hat{V}_g} \qquad (15)$$

where Δi_{max} is the maximum peak-to-peak ripple current occurring at δ=0.5, $\hat{I}_g$ the peak of the sinusoidal input current, $\hat{V}_g$ the peak input voltage. Analysis of (15) shows that, respect to the case of the previous section (α=0), there is always an increase of the system phase margin as long as α<2, which is very likely to happen in a standard CCM design (see (15)). As an example, Fig. 5 reports the closed loop poles of Case A, when α is varied between 0 and 0.8 and β=0.6.

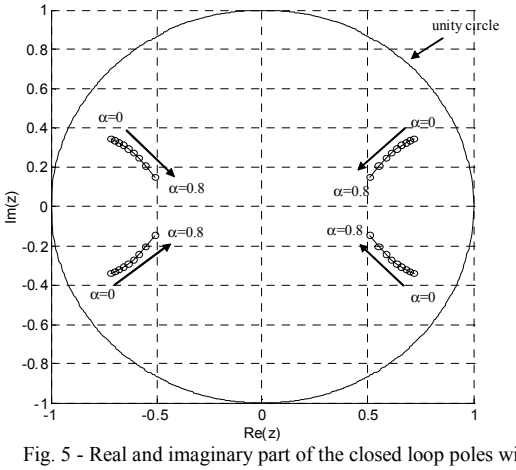

Fig. 5 - Real and imaginary part of the closed loop poles with: Case A, α=0÷0.8, β=0.6.

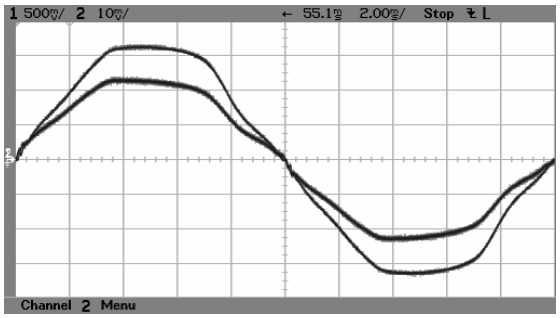

Fig. 6 – Line input voltage v_g (100V/div) and input current i_g (1A/div).

C. *Issues in DCM mode*

In order to understand how the closed-loop poles move when the converter operate in DCM, we have substituted the discrete time dynamic model (1) with the dynamic equation corresponding to DCM and, then, applied the procedure presented in previous sections. As a result, we have seen that the stability of the system is ensured in both cases A and B, even for parameter variations of α and β greater than what founded in CCM. The main issue in DCM is that the loop gain is much lower, as typically reported also in analog implementation, and thus current tracking is somehow compromised.

IV. EXPERIMENTAL RESULTS

The proposed solution has been tested both using numerical simulations and experimental prototypes. Simulation results, which have confirmed the analysis presented in the previous sections, are not reported due to space constrains. From the experimental point of view, a boost PFP prototype has been realized with the following parameters: $L = 2$ mH, $C = 330$ μF, $V_g = 220\ V_{RMS}$, $f_{sw} = 50$ kHz, $V_o = 400$ V and $P_{oNOMINAL} = 500$W. The digital controller has been firstly implemented using a Field Programmable Gate Array (FPGA) by Altera (specifically the EPF10K20 device, a member of FLEX 10K family) and the control algorithm has been developed using a hardware description language (VHDL), providing great flexibility and technology independence. Fast A/D converters have been used so that the overall control algorithm takes less than 1 μs, which can be considered a negligible delay compared to the switching period. Some results are reported in Fig. 6 (for $V_g = 220V_{RMS}$, $P_o = 370$W), which shows that the filtered input current waveform reproduces the highly distorted voltage waveform, thus achieving an almost unity power factor.

The control algorithm has been intensively tested also in a newly developed DSP by Texas Instruments (TMS320F2812), which we found a powerful and flexible hardware support for rapid prototyping. In this case, the control delay is assumed to be equal to the PWM period. Indeed, all experimental results reported, besides Fig. 6, are related to the DSP implementation mainly because this experimental setup was developed in a laboratory where a low distorted sinusoidal power supply was available.

Fig. 7 shows the input voltage $v_g(t)$ and unfiltered input current $i_g(t)$ at full load and nominal input voltage of 220 V_{RMS}. Note that the distortion on the current waveform is quite small, even during zero crossing of the input current. This is also verified by the input current spectrum, reported in Fig. 8, where all harmonics are below 40 dB the fundamental one, besides the 3rd harmonic component. The input current THD is around 1.8%.

We have also tested our system in DCM, as reported in Fig. 9. In this case the current waveform distortion is much higher due to the lower control gain in DCM. The current THD is now 8%.

Finally, we have tested the dynamics of the voltage control imposing step load changes from 25% to 100% of the nominal load (Fig. 10) and viceversa (Fig. 11). One important advantage of the digital implementation is the possibility to obtain quite easily a fast dynamic response. Among the solutions proposed in the past, we have implemented a voltage notch tuned at twice the line frequency. Figs 10 and 11 report the load transients and confirm the possibility to realize a high control loop bandwidth, which is not easy to achieve by analog means.

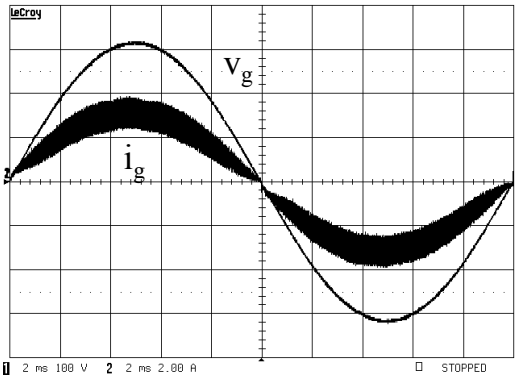

Fig. 7 – Line input voltage v_g (100V/div) and input current i_g (2A/div).

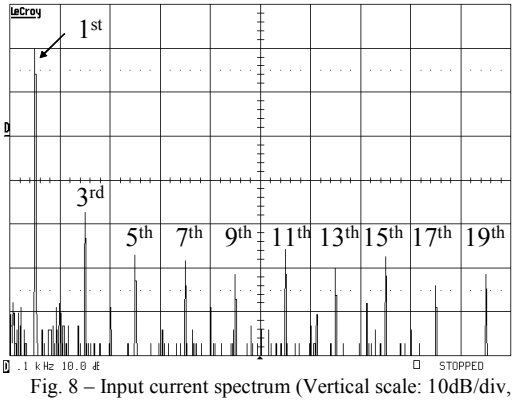

Fig. 8 – Input current spectrum (Vertical scale: 10dB/div, horizontal scale: 100Hz/div).

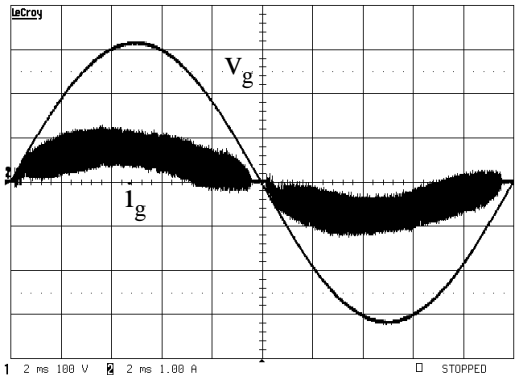

Fig. 9 – Line input voltage v_g (100V/div), input current i_g (1A/div) at reduced output power, where the converter operates in DCM for a fraction of the line period.

IV. CONCLUSIONS

This paper has proposed a fully digital control of boost Power Factor Preregulators, where the line input voltage sensing is avoided and a disturbance observer is used for its estimation. A predictive-type current control has been adopted since it features simple implementation, fast dynamic response and a direct algorithm for input voltage estimation. As shown in the stability analysis, the proposed solution is robust against parameter variations, especially if the inductor value is underestimated. The proposed algorithms have been verified by experimental tests on a boost PFP, basically confirming the theoretical analysis.

V. ACKNOWLEDGMENT

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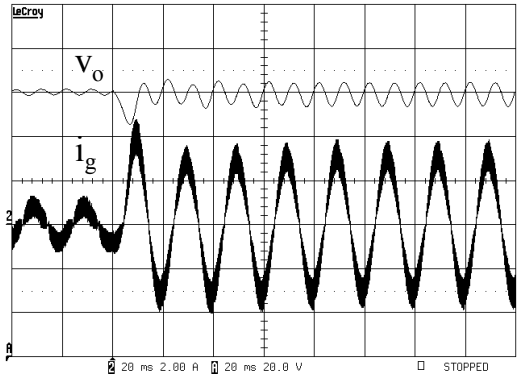

Fig. 10 – Load transient from 25% to 100% of nominal load: ouput voltage v_o (20V/div) and input current i_g (2A/div).

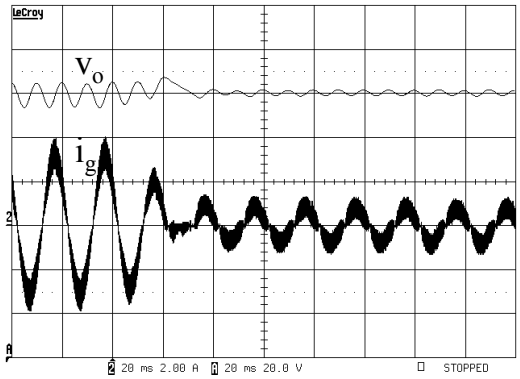

Fig. 11 – Load transient from 100% to 25% of nominal load: ouput voltage v_o (20V/div) and input current i_g (2A/div).